LMH6611/LMH6612 Single Supply 345 MHz Rail-to-Rail Output Amplifiers

Check for Samples: LMH6611, LMH6612

FEATURES

- **V_S = 5V, R_L = 1 kΩ, T_A = 25°C and A_V = +1, Unless Otherwise Specified.**
- **Operating Voltage Range 2.7V to 11V**
- **Supply Current Per Channel 3.2 mA**
- **Small Signal Bandwidth 345 MHz**
- **Open Loop Gain 103 dB**
- **Input Offset Voltage (Limit at 25°C) ±1.5 mV**
- **Slew Rate 460 V/µs**
- **0.1 dB Bandwidth 45 MHz**
- **Settling Time to 0.1% 67 ns**
- **Settling Time to 0.01% 100 ns**
- **SFDR (f = 100 kHz, A_V = 2, V_{OUT} = 2 V_{PP}) 102 dBc**
- **Low Voltage Noise 10 nV/$\sqrt{Hz}$**
- **Output current ±100 mA**
- **CMVR −0.2V to 3.8V**
- **Rail-to-Rail Output**
- **−40°C to +125°C Temperature Range**

APPLICATIONS

- **ADC Driver**
- **DAC Buffer**
- **Active Filters**
- **High Speed Sensor Amplifier**
- **Current Sense Amplifier**
- **1080i and 720p Analog Video Amplifier**
- **STB, TV Video Amplifier**
- **Video Switching and Muxing**

DESCRIPTION

The LMH6611 (single, with shutdown) and LMH6612 (dual) are 345 MHz rail-to-rail output amplifiers consuming just 3.2 mA of quiescent current per channel and designed to deliver high performance in power conscious single supply systems. The LMH6611 and LMH6612 have precision trimmed input offset voltages with low noise and low distortion performance as required for high accuracy video, test and measurement, and communication applications. The LMH6611 and LMH6612 are members of the PowerWise family and have an exceptional power-to-performance ratio.

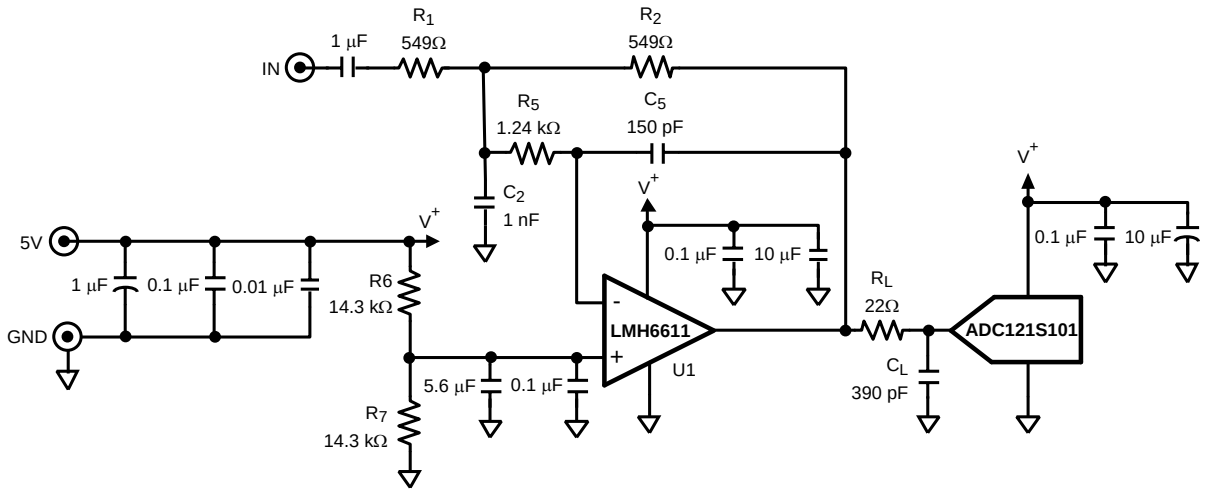
With a trimmed input offset voltage of 0.022 mV and a high open loop gain of 103 dB the LMH6611 and LMH6612 meet the requirements of DC sensitive high speed applications such as low pass filtering in baseband I and Q radio channels. These specifications combined with a 0.01% settling time of 100 ns, a low noise of 10 nV/$\sqrt{Hz}$ and better than 102 dBc SFDR at 100 kHz make these amplifiers particularly suited to driving 10, 12 and 14-bit high speed ADCs. The 45 MHz 0.1 dB bandwidth (A_V = 2) driving 2 V_{PP} into 150Ω allows the amplifiers to be used as output drivers in 1080i and 720p HDTV applications.

The input common mode range extends from 200 mV below the negative supply rail up to 1.2V from the positive rail. On a single 5V supply with a ground terminated 150Ω load the output swings to within 49 mV of the ground, while a mid-rail terminated 1 kΩ load will swing to 77 mV of either rail.

DESCRIPTION (CONTINUED)

The amplifiers will operate on a 2.7V to 11V single supply or ±1.35V to ±5.5V split supply. The LMH6611 single is available in 6-Pin SOT and has an independent active low disable pin which reduces the supply current to 120 µA. The LMH6612 is available in 8-Pin SOIC. Both the LMH6611 and LMH6612 are available in −40°C to +125°C extended industrial temperature grade.

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	For input pins only	2000V
		For all other pins	2000V
	Machine Model		200V
	Charge Device Model		1000V
Supply Voltage ($V_S = V^+ – V^-$)			12V
Junction Temperature(4)			150°C max

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}) – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings(1)

Supply Voltage ($V_S = V^+ – V^-$)		2.7V to 11V
Ambient Temperature Range(2)		−40°C to +125°C
Package Thermal Resistance (θ_{JA})	6-Pin SOT	231°C/W
	8-Pin SOIC	160°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}) – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

+3V Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = +25°C, V^+ = 3V, V^- = 0V, $V_S = V^+ - V^-$, $\overline{DISABLE}$ = 3V, $V_{CM} = V_O = V^+/2$, A_V = +1, R_F = 0Ω, when $A_V \neq +1$ then R_F = 560Ω, R_L = 1 kΩ. **Boldface** limits apply at temperature extremes.(1)

Symbol	Parameter	Condition	Min(2)	Typ(3)	Max(2)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		305		MHz
		A_V = 2, −1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		115		
GBW	Gain Bandwidth (LMH6611)	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}	115	135		MHz
	Gain Bandwidth (LMH6612)	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		130		
LSBW	−3 dB Bandwidth Large Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 1.5 V_{PP}		90		MHz
		A_V = −1, R_L = 150Ω, V_{OUT} = 2 V_{PP}		85		
Peak	Peaking	A_V = 1		1.0		dB
0.1 dBBW	0.1 dB Bandwidth	A_V = 1, V_{OUT} = 0.5 V_{PP}, R_L = 1 kΩ		33		MHz
		A_V = 2, V_{OUT} = 0.5 V_{PP}, R_L = 1 kΩ $R_F = R_G$ = 560Ω		65		
		A_V = 2, V_{OUT} = 1.5 V_{PP}, R_L = 150Ω, $R_F = R_G$ = 510Ω		47		
DG	Differential Gain	A_V = 2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.03		%
DP	Differential Phase	A_V = 2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.06		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	1.5V Step, A_V = 1		2.8		ns
SR	Slew Rate	2V Step, A_V = 1		330		V/µs
$t_{s\_0.1}$	0.1% Settling Time	2V Step, A_V = −1		74		ns
$t_{s\_0.01}$	0.01% Settling Time	2V Step, A_V = −1		116		
Noise and Distortion Performance						
SFDR	Spurious Free Dynamic Range	f_C = 100 kHz, A_V = −1, V_{OUT}= 2 V_{PP}		109		dBc
		f_C = 1 MHz, A_V = −1, V_{OUT} = 2 V_{PP}		97		
		f_C = 5 MHz, A_V = −1, V_{OUT} = 2 V_{PP}		80		
e_n	Input Voltage Noise	f = 100 kHz		10		nV/√Hz
i_n	Input Current Noise	f = 100 kHz		2		pA/√Hz
CT	Crosstalk (LMH6612)	f = 5 MHz, V_{IN} = 2 V_{PP}		71		dB
Input, DC Performance						
V_{OS}	Input Offset Voltage (LMH6611)	V_{CM} = 0.5V		0.022	±1.5 **±2**	mV
	Input Offset Voltage (LMH6612)	V_{CM} = 0.5V		−0.015	±1.5 **±2**	
TCV_{OS}	Input Offset Voltage Average Drift	See(4)		4		µV/°C
I_B	Input Bias Current	V_{CM} = 0.5V		−5.9	−10.1 **−11.1**	µA
I_O	Input Offset Current			0.01	±0.5 **±0.7**	µA
C_{IN}	Input Capacitance			2.5		pF
R_{IN}	Input Resistance			6		MΩ
CMVR	Input Voltage Range	DC, CMRR ≥ 76 dB	−0.2		1.8	V

(1) Boldface limits apply to temperature range of −40°C to 125°C
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Voltage average drift is determined by dividing the change in V_{OS} by temperature change.

+3V Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_J = +25°C, V^+ = 3V, V^- = 0V, $V_S = V^+ - V^-$, $\overline{DISABLE}$ = 3V, $V_{CM} = V_O = V^+/2$, A_V = +1, R_F = 0Ω, when $A_V \neq +1$ then R_F = 560Ω, R_L = 1 kΩ. **Boldface** limits apply at temperature extremes.(1)

Symbol	Parameter	Condition	Min(2)	Typ(3)	Max(2)	Units
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −0.1V to 1.7V	79	98		dB
A_{OL}	Open Loop Gain	R_L = 1 kΩ, V_{OUT} = 2.7V to 0.3V	89	101		dB
		R_L = 150Ω, V_{OUT} = 2.5V to 0.5V	78	85		
Output DC Characteristics						
V_O	Output Swing High (LMH6611) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to $V^+/2$		59	72 **76**	mV
		R_L = 150Ω to $V^+/2$		133	169 **182**	
	Output Swing Low (LMH6611) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to $V^+/2$		59	74 **80**	
		R_L = 150Ω to $V^+/2$		133	171 **188**	
		R_L = 150Ω to V^-		42	52 **56**	
	Output Swing High (LMH6612) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to $V^+/2$		58	68 **73**	
		R_L = 150Ω to $V^+/2$		131	157 **172**	
	Output Swing Low (LMH6612) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to $V^+/2$		61	71 **79**	
		R_L = 150Ω to $V^+/2$		139	168 **187**	
		R_L = 150Ω to V^-		43	51 **56**	
I_{OUT}	Linear Output Current	$V_{OUT} = V^+/2$(5)		±70		mA
R_O	Output Resistance	f = 1 MHz		0.07		Ω
Enable Pin Operation						
	Enable High Voltage Threshold	Enabled(6)	2.0			V
	Enable Pin High Current	$V_{\overline{DISABLE}}$ = 3V		0.001		µA
	Enable Low Voltage Threshold	Disabled(6)			1.0	V
	Enable Pin Low Current	$V_{\overline{DISABLE}}$ = 0V		0.8		µA
t_{on}	Turn-On Time			18		ns
t_{off}	Turn-Off Time			50		ns
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, V_{CM} = 0.5V, V_S = 2.7V to 11V	81	96		dB
I_S	Supply Current (LMH6611)	$R_L = \infty$		3.0	3.4 **3.8**	mA
	Supply Current (LMH6612) (per channel)	$R_L = \infty$		2.95	3.45 **3.9**	
I_{SD}	Disable Shutdown Current (LMH6611)	$\overline{DISABLE}$ = 0V		101	132	µA

(5) Do not short circuit the output. Continuous source or sink currents larger than the I_{OUT} typical are not recommended as they may damage the part.

(6) This parameter is ensured by design and/or characterization and is not tested in production.

+5V Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = +25°C, V^+ = 5V, V^- = 0V, $V_S = V^+ - V^-$, $\overline{DISABLE}$ = 5V, $V_{CM} = V_O = V^+/2$, A_V = +1, R_F = 0Ω, when $A_V \neq +1$ then R_F = 560Ω, R_L = 1 kΩ. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		345		MHz
		A_V = 2, −1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		112		
GBW	Gain Bandwidth (LMH6611)	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}	115	135		MHz
	Gain Bandwidth (LMH6612)	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		130		
LSBW	−3 dB Bandwidth Large Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}		77		MHz
		A_V = 2, R_L = 150Ω, V_{OUT} = 2 V_{PP}		85		
Peak	Peaking	A_V = 1		0.3		dB
0.1 dBBW	0.1 dB Bandwidth	A_V = 1, V_{OUT} = 0.5 V_{PP}, R_L = 1 kΩ		45		MHz
		A_V = 2, V_{OUT} = 0.5 V_{PP}, R_L = 1 kΩ $R_F = R_G$ = 680Ω		68		
		A_V = 2, V_{OUT} = 2 V_{PP}, R_L = 150Ω, $R_F = R_G$ = 665Ω		45		
DG	Differential Gain	A_V = 2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.05		%
DP	Differential Phase	A_V = 2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.06		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, A_V = 1		3.6		ns
SR	Slew Rate	2V Step, A_V = 1		460		V/µs
$t_{s\_0.1}$	0.1% Settling Time	2V Step, A_V = −1		67		ns
$t_{s\_0.01}$	0.01% Settling Time	2V Step, A_V = −1		100		
Distortion and Noise Performance						
SFDR	Spurious Free Dynamic Range	f_C = 100 kHz, A_V = 2, V_{OUT} = 2 V_{PP}		102		dBc
		f_C = 1 MHz, A_V = 2, V_{OUT} = 2 V_{PP}		96		
		f_C = 5 MHz, A_V = 2, V_O = 2 V_{PP}		82		
e_n	Input Voltage Noise	f = 100 kHz		10		nV/√Hz
i_n	Input Current Noise	f = 100 kHz		2		pA/√Hz
CT	Crosstalk (LMH6612)	f = 5 MHz, V_{IN} = 2 V_{PP}		71		dB
Input, DC Performance						
V_{OS}	Input Offset Voltage (LMH6611)	V_{CM} = 0.5V		0.013	±1.5 **±2**	mV
	Input Offset Voltage (LMH6612)	V_{CM} = 0.5V		0.022	±1.5 **±2**	
TCV_{OS}	Input Offset Voltage Average Drift	See (3)		4		µV/°C
I_B	Input Bias Current	V_{CM} = 0.5V		−6.3	−10.1 **−11.1**	µA
I_O	Input Offset Current			0.01	±0.5 **±0.7**	µA
C_{IN}	Input Capacitance			2.5		pF
R_{IN}	Input Resistance			6		MΩ
CMVR	Input Voltage Range	DC, CMRR ≥ 78 dB	−0.2		3.8	V

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Voltage average drift is determined by dividing the change in V_{OS} by temperature change.

+5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_J = +25°C, V^+ = 5V, V^- = 0V, $V_S = V^+ - V^-$, $\overline{DISABLE}$ = 5V, $V_{CM} = V_O = V^+/2$, A_V = +1, R_F = 0Ω, when $A_V \neq +1$ then R_F = 560Ω, R_L = 1 kΩ. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −0.1V to 3.7V	81	98		dB
A_{OL}	Open Loop Gain	R_L = 1 kΩ, V_{OUT} = 4.6V to 0.4V	92	103		dB
		R_L = 150Ω, V_{OUT} = 4.4V to 0.6V	80	86		
Output DC Characteristics						
V_O	Output Swing High (LMH6611) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to $V^+/2$		76	90 **93**	mV
		R_L =150Ω to $V^+/2$		195	239 **256**	
	Output Swing Low (LMH6611) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to $V^+/2$		74	92 **98**	
		R_L =150Ω to $V^+/2$		193	243 **265**	
		R_L = 150Ω to V^-		48	60 **64**	
	Output Swing High (LMH6612) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to $V^+/2$		75	86 **91**	
		R_L =150Ω to $V^+/2$		195	223 **241**	
	Output Swing Low (LMH6612) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to $V^+/2$		77	88 **98**	
		R_L =150Ω to $V^+/2$		202	234 **261**	
		R_L = 150Ω to V^-		49	58 **64**	
I_{OUT}	Linear Output Current	$V_{OUT} = V^+/2$ (4)		±100		mA
R_O	Output Resistance	f = 1 MHz		0.07		Ω
Enable Pin Operation						
	Enable High Voltage Threshold	Enabled (5)	3.0			V
	Enable Pin High Current	$V_{\overline{DISABLE}}$ = 5V		1.2		µA
	Enable Low Voltage Threshold	Disabled (5)			2.0	V
	Enable Pin Low Current	$V_{\overline{DISABLE}}$ = 0V		2.8		µA
t_{on}	Turn-On Time			20		ns
t_{off}	Turn-Off Time			60		ns
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, V_{CM} = 0.5V, V_S = 2.7V to 11V	81	96		dB
I_S	Supply Current (LMH6611)	R_L = ∞		3.2	3.6 **4.0**	mA
	Supply Current (LMH6612) (per channel)	R_L = ∞		3.2	3.7 **4.25**	
I_{SD}	Disable Shutdown Current (LMH6611)	$\overline{DISABLE}$ = 0V		120	162	µA

(4) Do not short circuit the output. Continuous source or sink currents larger than the I_{OUT} typical are not recommended as they may damage the part.

(5) This parameter is ensured by design and/or characterization and is not tested in production.

±5V Electrical Characteristics

Unless otherwise specified, all limits are specified for T_J = +25°C, V^+ = 5V, V^- = −5V, $V_S = V^+ - V^-$, $\overline{DISABLE}$ = 5V, $V_{CM} = V_O$ = 0V, A_V = +1, R_F = 0Ω, when $A_V \neq +1$ then R_F = 560Ω, R_L = 1 kΩ. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
Frequency Domain Response						
SSBW	–3 dB Bandwidth Small Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		365		MHz
		A_V = 2, −1, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		110		
GBW	Gain Bandwidth (LMH6611)	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}	115	135		MHz
	Gain Bandwidth (LMH6612)	A_V = 10, R_F = 2 kΩ, R_G = 221Ω, R_L = 1 kΩ, V_{OUT} = 0.2 V_{PP}		130		
LSBW	−3 dB Bandwidth Large Signal	A_V = 1, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}		85		MHz
		A_V = 2, R_L = 150Ω, V_{OUT} = 2 V_{PP}		87		
Peak	Peaking	A_V = 1		0.01		dB
0.1 dBBW	0.1 dB Bandwidth	A_V = 1, V_{OUT} = 0.5 V_{PP}, R_L = 1 kΩ		92		MHz
		A_V = 2, V_{OUT} = 0.5 V_{PP}, R_L = 1 kΩ $R_F = R_G$ = 750Ω		65		
		A_V = 2, V_{OUT} = 2 V_{PP}, R_L = 150Ω, $R_F = R_G$ = 680Ω		45		
DG	Differential Gain	A_V = 2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.05		%
DP	Differential Phase	A_V = 2, 4.43 MHz, 0.6V < V_{OUT} < 2V, R_L = 150Ω to $V^+/2$		0.05		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, A_V = 1		3.5		ns
SR	Slew Rate	2V Step, A_V = 1		460		V/µs
$t_{s\_0.1}$	0.1% Settling Time	2V Step, A_V = −1		60		ns
$t_{s\_0.01}$	0.01% Settling Time	2V Step, A_V = −1		100		
Noise and Distortion Performance						
SFDR	Spurious Free Dynamic Range	f_C = 100 kHz, A_V = 2, V_{OUT} = 2 V_{PP}		102		dBc
		f_C = 1 MHz, A_V = 2, V_{OUT} = 2 V_{PP}		100		
		f_C = 5 MHz, A_V = 2, V_{OUT} = 2 V_{PP}		81		
e_n	Input Voltage Noise	f = 100 kHz		10		nV/√Hz
i_n	Input Current Noise	f = 100 kHz		2		pA/√Hz
CT	Crosstalk (LMH6612)	f = 5 MHz, V_{IN} = 2 V_{PP}		71		dB
Input DC Performance						
V_{OS}	Input Offset Voltage (LMH6611)	V_{CM} = −4.5V		0.074	±1.5 **±2**	mV
	Input Offset Voltage (LMH6612)	V_{CM} = −4.5V		0.095	±1.5 **±2**	
TCV_{OS}	Input Offset Voltage Average Drift	See (3)		4		µV/°C
I_B	Input Bias Current	V_{CM} = −4.5V		−6.5	−10.1 **−11.1**	µA
I_O	Input Offset Current			0.01	±0.5 **±0.7**	µA
C_{IN}	Input Capacitance			2.5		pF
R_{IN}	Input Resistance			6		MΩ
CMVR	Input Voltage Range	DC, CMRR ≥ 81 dB	−5.2		3.8	V

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Voltage average drift is determined by dividing the change in V_{OS} by temperature change.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are specified for T_J = +25°C, V^+ = 5V, V^- = −5V, V_S = V^+ – V^-, $\overline{DISABLE}$ = 5V, V_{CM} = V_O = 0V, A_V = +1, R_F = 0Ω, when $A_V \neq +1$ then R_F = 560Ω, R_L = 1 kΩ. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −5.1V to 3.7V	81	98		dB
A_{OL}	Open Loop Gain	R_L = 1 kΩ, V_{OUT} = +4.6V to −4.6V	96	103		dB
		R_L = 150Ω, V_{OUT} = +4.3V to −4.3V	80	87		
Output DC Characteristics						
V_O	Output Swing High (LMH6611) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to GND		107	125 **130**	mV
		R_L = 150Ω to GND		339	402 **433**	
	Output Swing Low (LMH6611) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to GND		103	123 **132**	
		R_L = 150Ω to GND		332	404 **445**	
		R_L = 150Ω to V^-		54	70 **74**	
	Output Swing High (LMH6612) (Voltage from V^+ Supply Rail)	R_L = 1 kΩ to GND		107	118 **125**	
		R_L = 150Ω to GND		340	375 **407**	
	Output Swing Low (LMH6612) (Voltage from V^- Supply Rail)	R_L = 1 kΩ to GND		108	120 **135**	
		R_L = 150Ω to GND		348	389 **434**	
		R_L = 150Ω to V^-		56	66 **74**	
I_{OUT}	Linear Output Current	V_{OUT} = GND (4)		±120		mA
R_O	Output Resistance	f = 1 MHz		0.07		Ω
Enable Pin Operation						
	Enable High Voltage Threshold	Enabled (5)	0.5			V
	Enable Pin High Current	$V_{\overline{DISABLE}}$ = +5V		17.0		µA
	Enable Low Voltage Threshold	Disabled (5)			−0.5	V
	Enable Pin Low Current	$V_{\overline{DISABLE}}$ = −5V		18.6		µA
t_{on}	Turn-On Time			19		ns
t_{off}	Turn-Off Time			60		ns
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, V_{CM} = −4.5V, V_S = 2.7V to 11V	81	96		dB
I_S	Supply Current (LMH6611)	R_L = ∞		3.3	3.8 **4.4**	mA
	Supply Current (LMH6612) (per channel)	R_L = ∞		3.45	4.05 **4.85**	
I_{SD}	Disable Shutdown Current (LMH6611)	$\overline{DISABLE}$ = −5V		160	212	µA

(4) Do not short circuit the output. Continuous source or sink currents larger than the I_{OUT} typical are not recommended as they may damage the part.

(5) This parameter is ensured by design and/or characterization and is not tested in production.

Connection Diagram

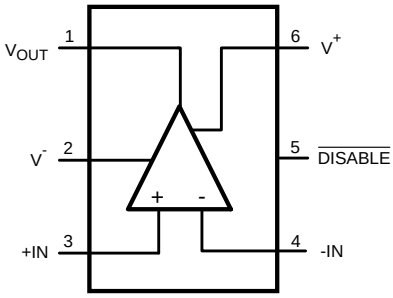


Figure 1. 6-Pin SOT
Top View

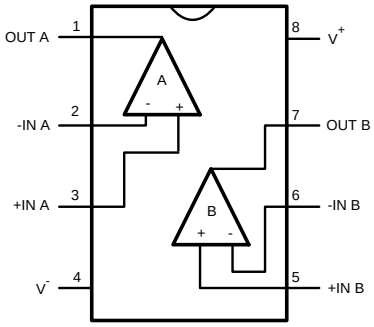


Figure 2. 8-Pin SOIC
Top View

Typical Performance Characteristics

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

Closed Loop Frequency Response for Various Supplies

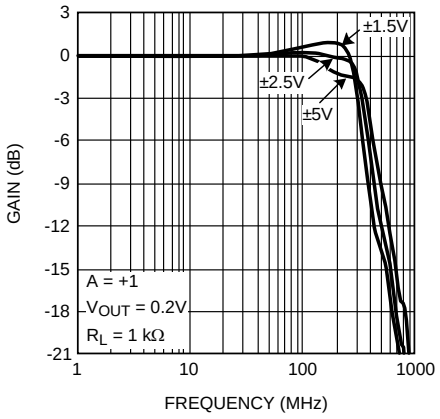


Figure 3.

Closed Loop Frequency Response for Various Supplies

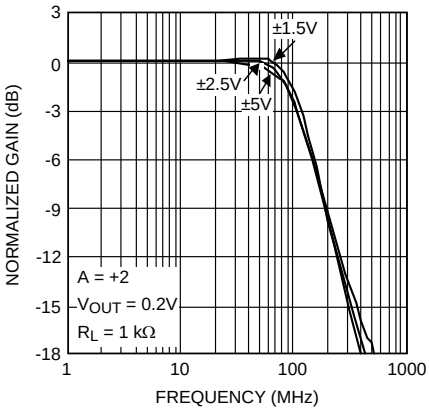


Figure 4.

Closed Loop Frequency Response for Various Supplies

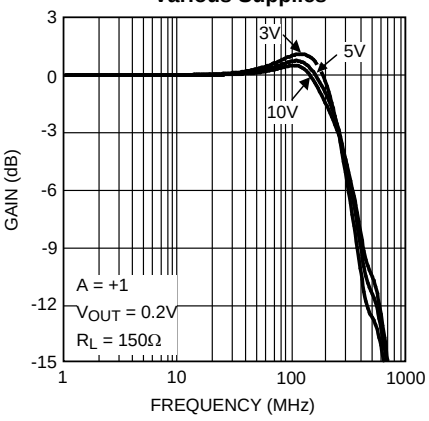


Figure 5.

Closed Loop Frequency Response for Various Supplies (Gain = +2)

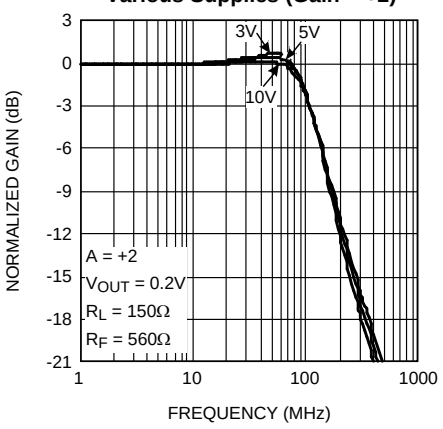


Figure 6.

Closed Loop Gain vs. Frequency for Various Temperatures

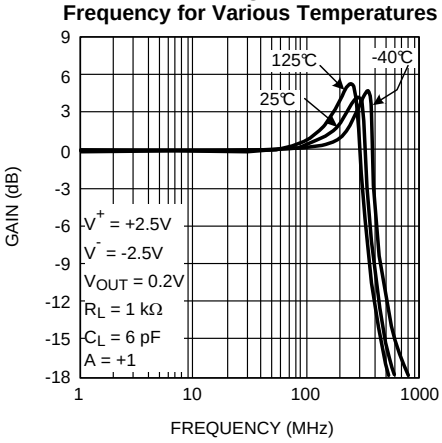


Figure 7.

Closed Loop Gain vs. Frequency for Various Temperatures

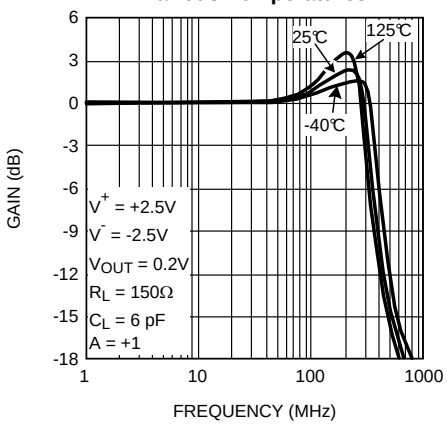


Figure 8.

Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

Closed Loop Gain vs. Frequency for Various Gains

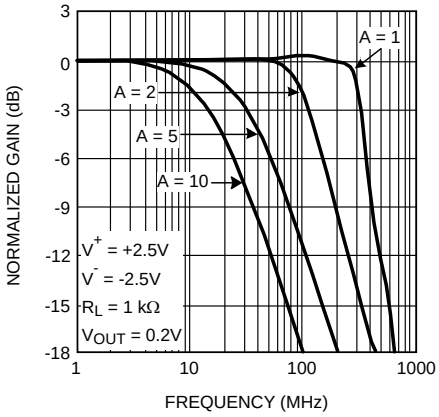


Figure 9.

Large Signal Frequency Response

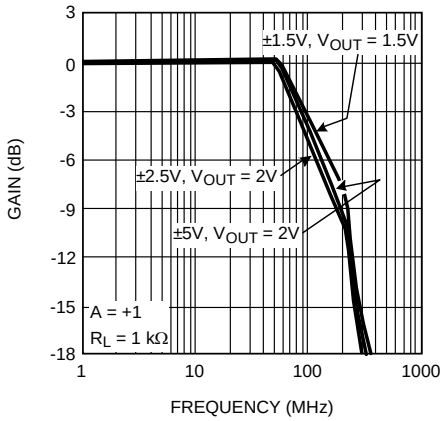


Figure 10.

Large Signal Frequency Response

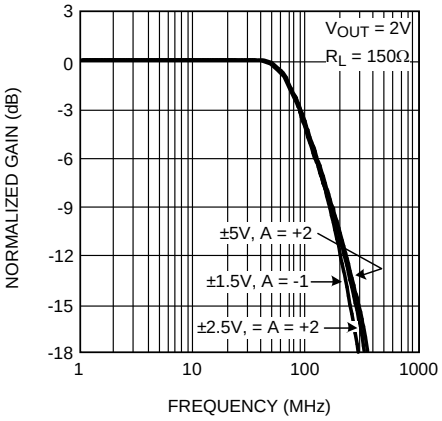


Figure 11.

±0.1 dB Gain Flatness for Various Supplies

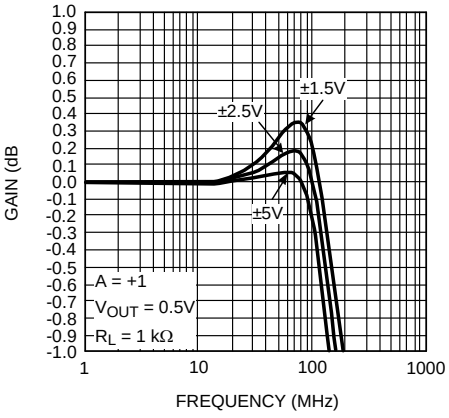


Figure 12.

±0.1 dB Gain Flatness for Various Supplies

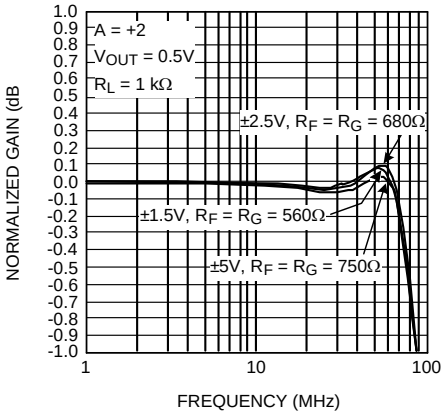


Figure 13.

±0.1 dB Gain Flatness for Various Supplies

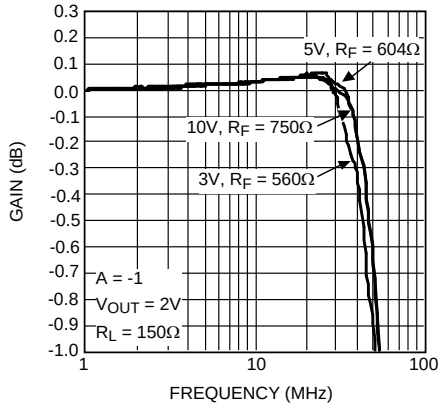


Figure 14.

Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

±0.1 dB Gain Flatness for Various Supplies

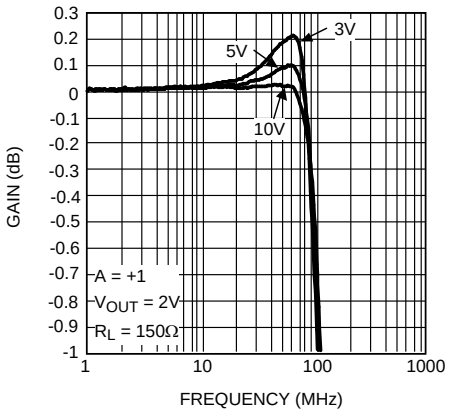


Figure 15.

±0.1 dB Gain Flatness for Various Supplies (Gain = +2)

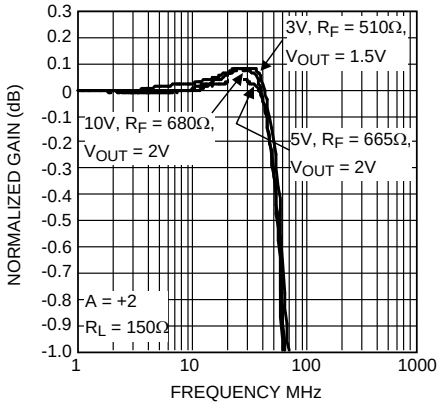


Figure 16.

Small Signal Frequency Response with Various Capacitive Load

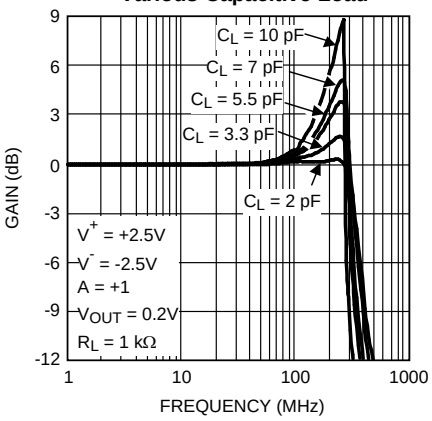


Figure 17.

Small Signal Frequency Response with Capacitive Load and Various R_{ISO}

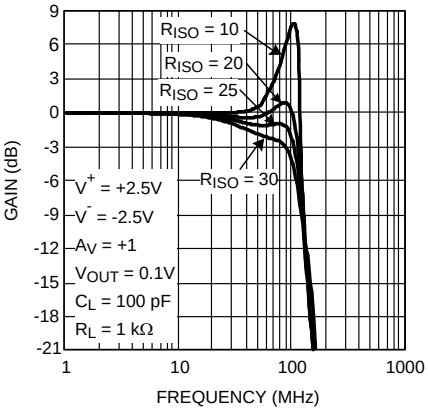


Figure 18.

HD2 and HD3 vs. Frequency and Supply Voltage

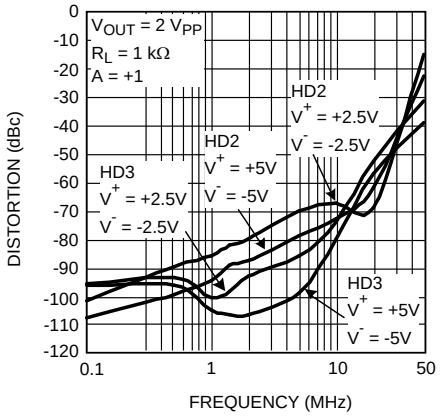


Figure 19.

HD2 and HD3 vs. Frequency and Load

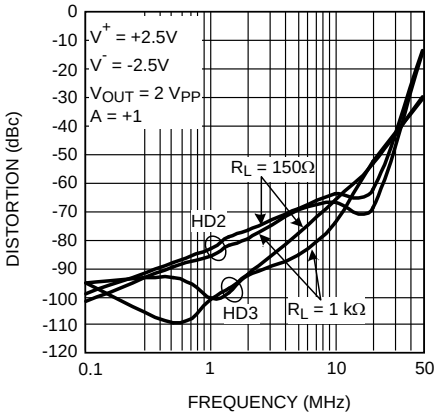


Figure 20.

Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

HD2 and HD3 vs. Common Mode Voltage

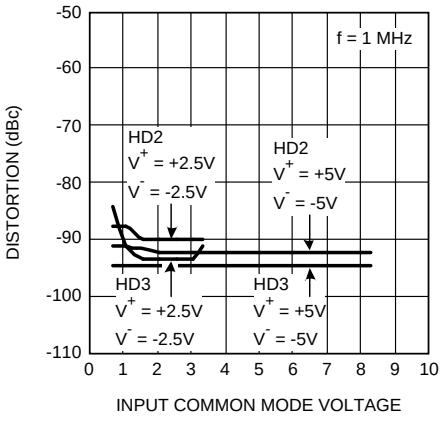


Figure 21.

HD2 and HD3 vs. Common Mode Voltage

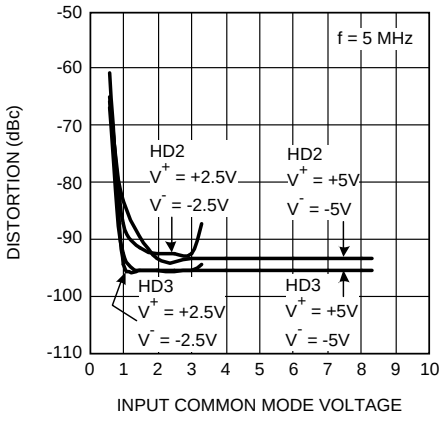


Figure 22.

HD2 vs. Frequency and Gain

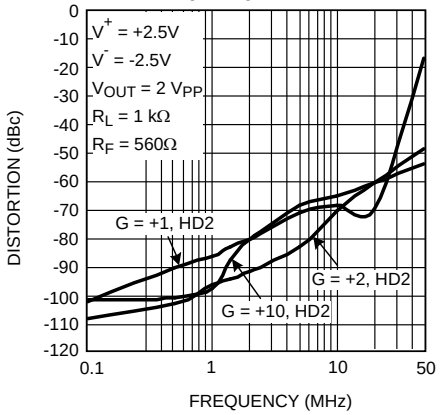


Figure 23.

HD3 vs. Frequency and Gain

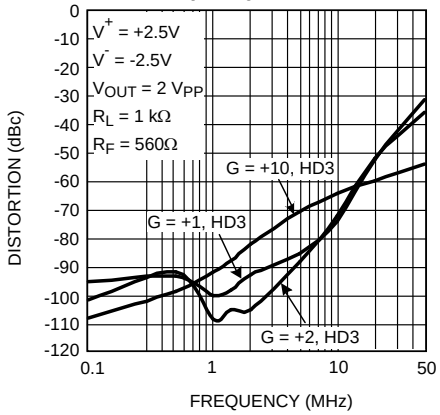


Figure 24.

Open Loop Gain and Phase

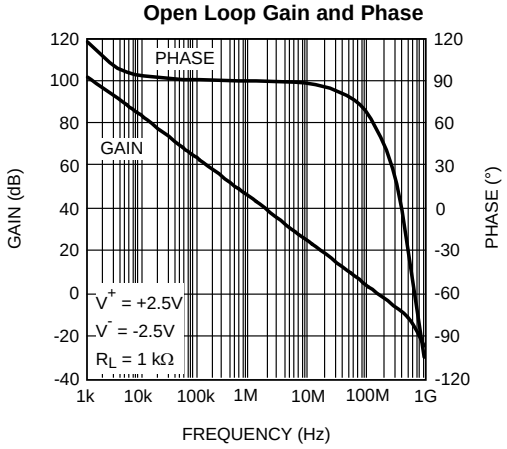


Figure 25.

HD2 vs. Output Swing

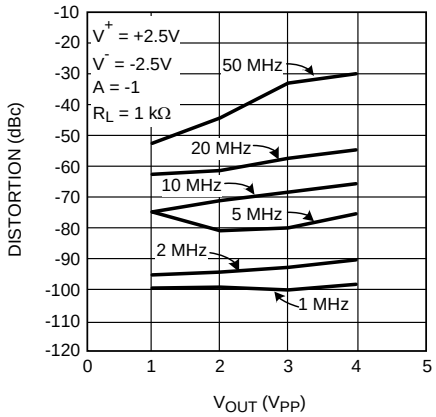


Figure 26.

Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

HD3 vs. Output Swing

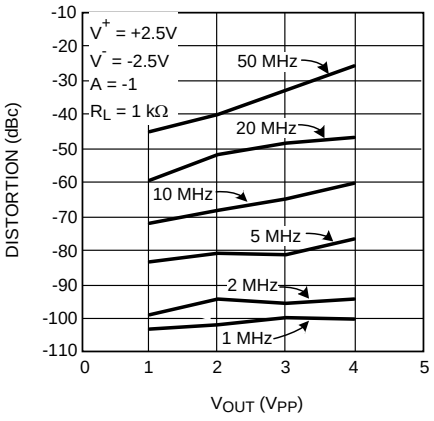


Figure 27.

HD2 vs. Output Swing

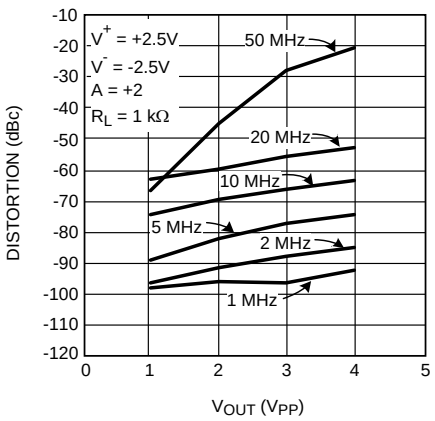


Figure 28.

HD2 vs. Output Swing

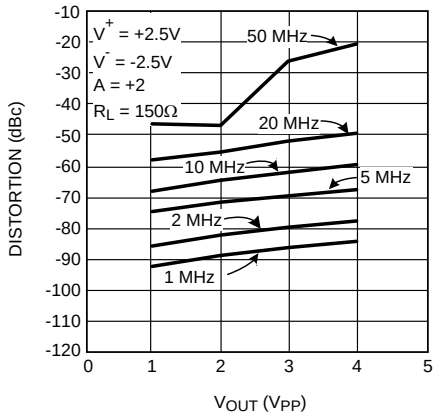


Figure 29.

HD3 vs. Output Swing

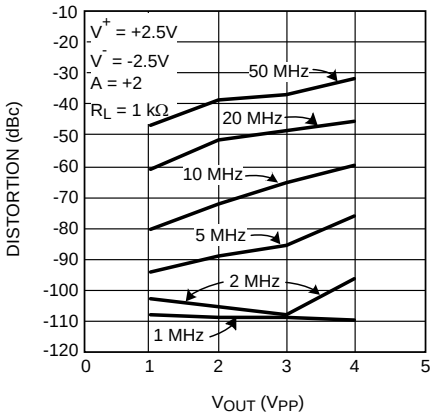


Figure 30.

HD3 vs. Output Swing

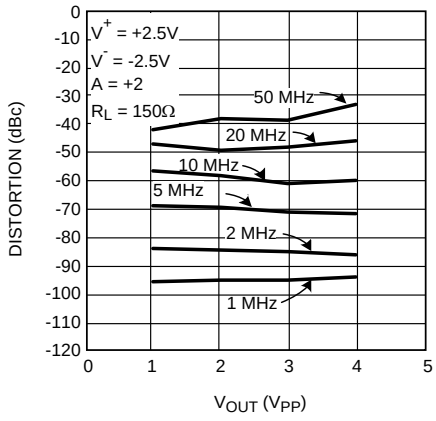


Figure 31.

Settling Time vs. Input Step Amplitude

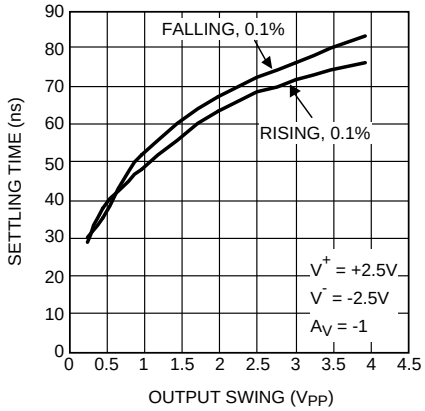


Figure 32.

Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

Settling Time vs. Input Step Amplitude

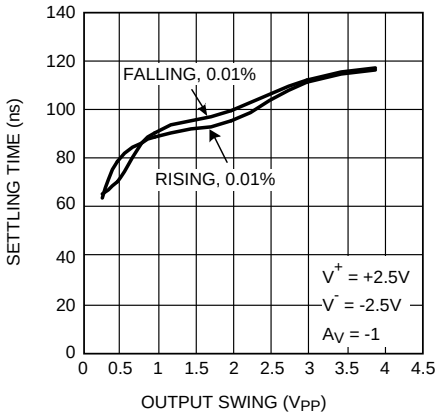


Figure 33.

Input Noise vs. Frequency

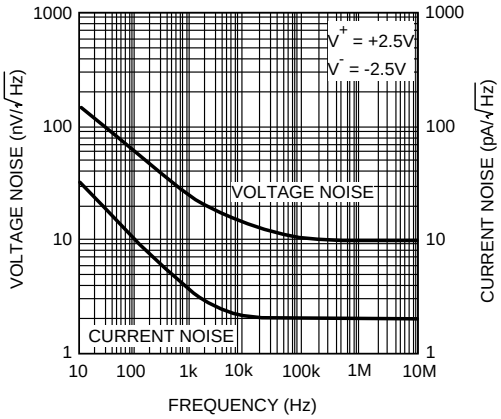


Figure 34.

V_{OS} vs. V_{OUT}

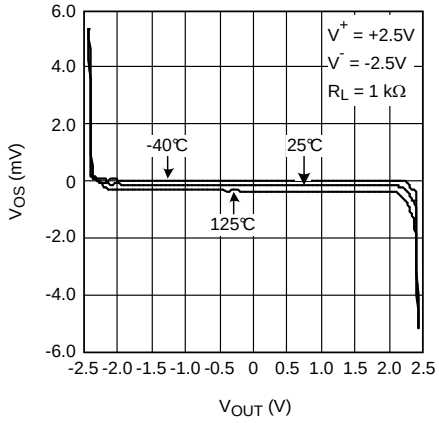


Figure 35.

V_{OS} vs. V_{OUT}

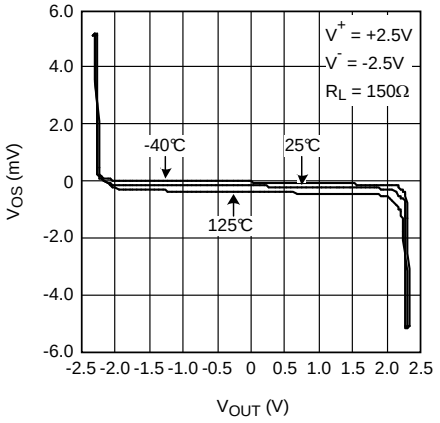


Figure 36.

V_{OS} vs. V_{CM}

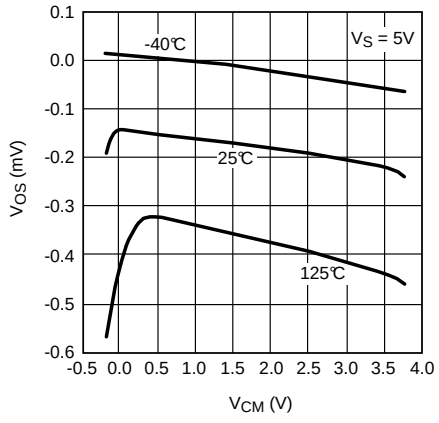


Figure 37.

V_{OS} vs. V_S

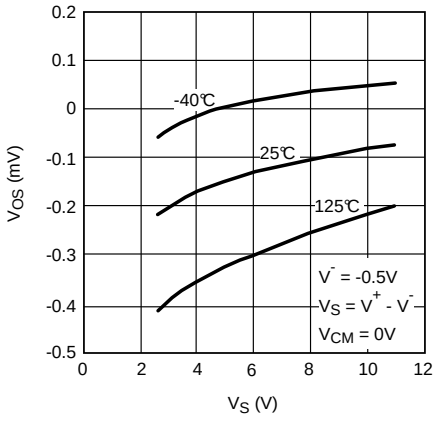


Figure 38.

Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

V_{OS} vs. I_{OUT}

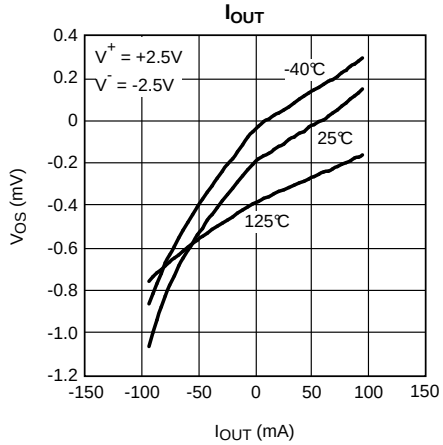


Figure 39.

V_{OS} Distribution

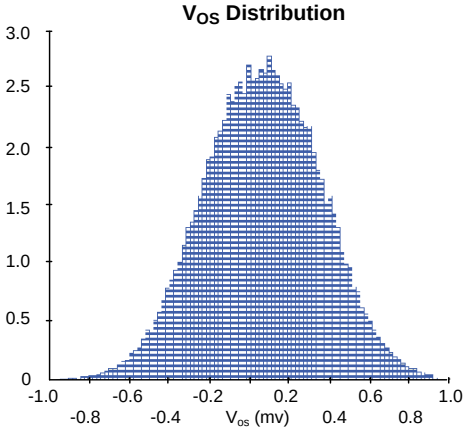


Figure 40.

I_B vs. V_S

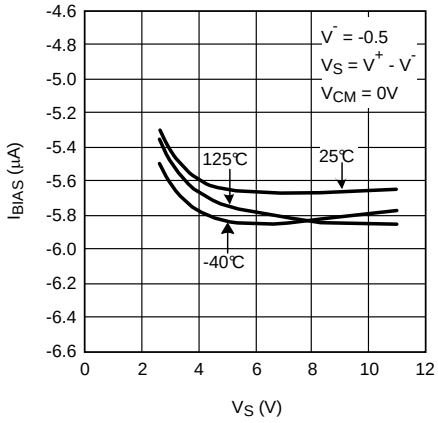


Figure 41.

I_S vs. V_S

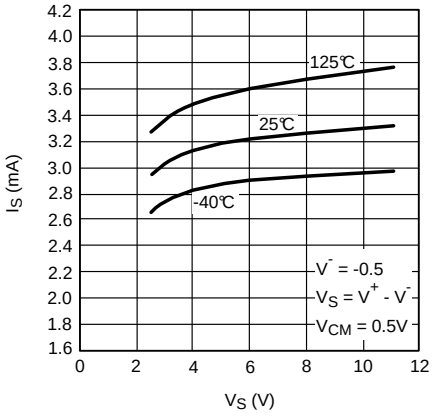


Figure 42.

V_{OUT} vs. V_S

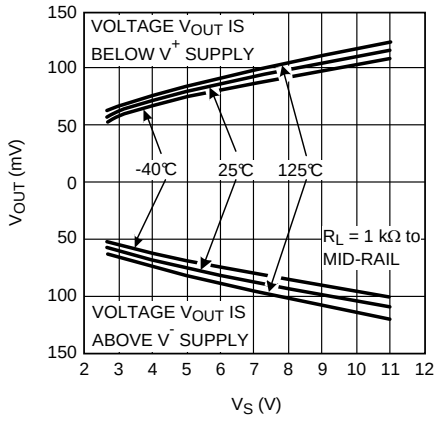


Figure 43.

V_{OUT} vs. V_S

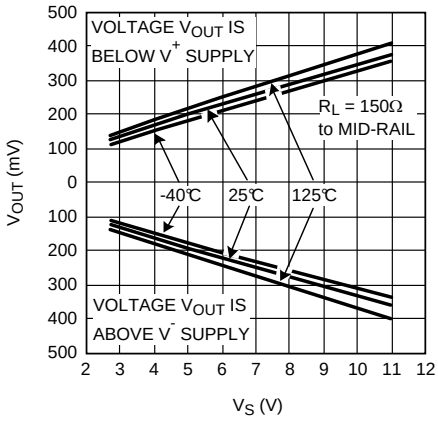


Figure 44.

Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

V_{OUT} vs. V_S

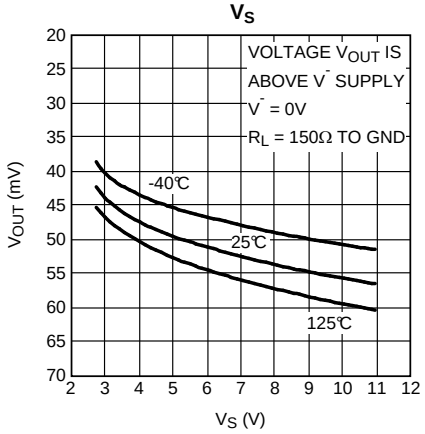


Figure 45.

Closed Loop Output Impedance vs. Frequency A_V = +1

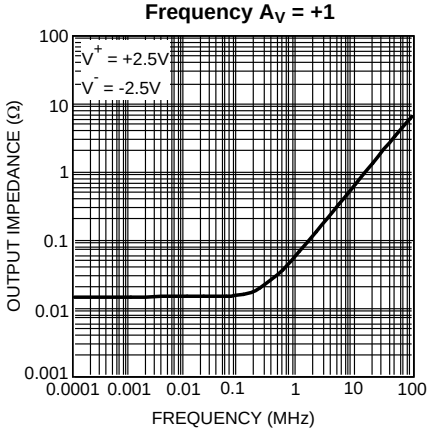


Figure 46.

Circuit for Positive (+) PSRR Measurement

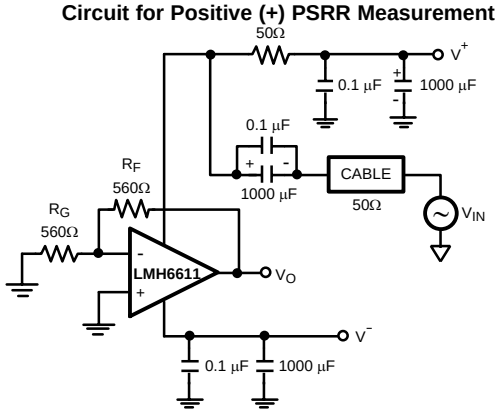


Figure 47.

+PSRR vs. Frequency

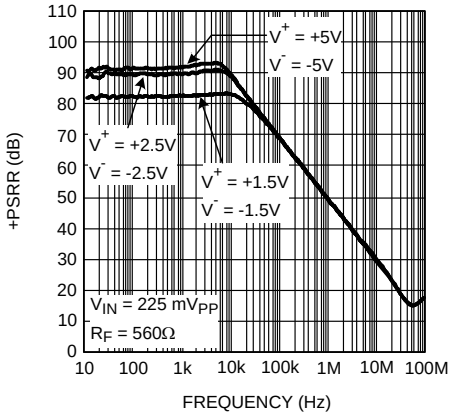


Figure 48.

Circuit for Negative (−) PSRR Measurement

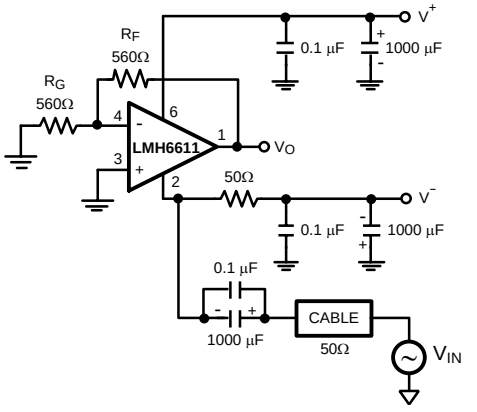


Figure 49.

−PSRR vs. Frequency

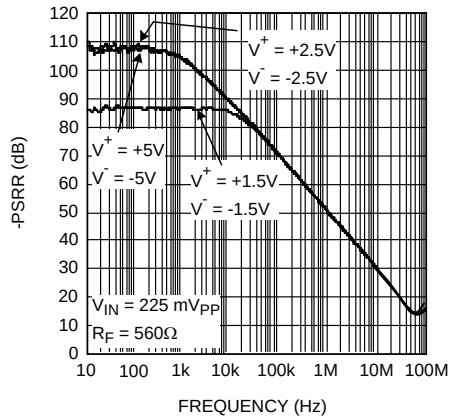


Figure 50.

Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

CMRR vs. Frequency

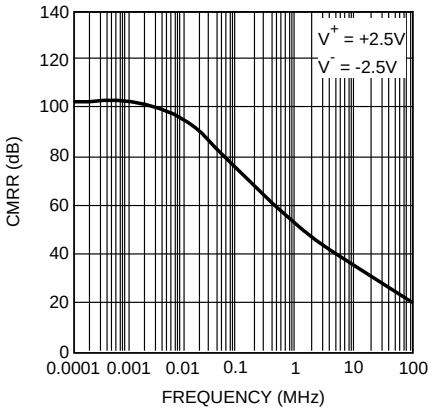


Figure 51.

Crosstalk vs. Frequency

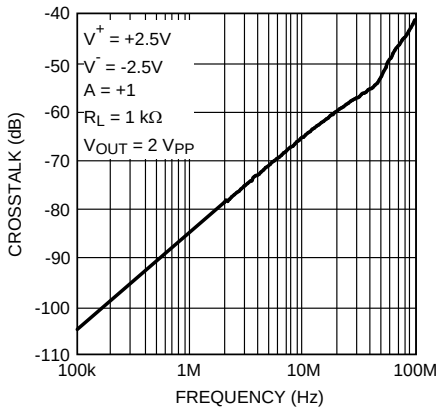


Figure 52.

Small Signal Step Response

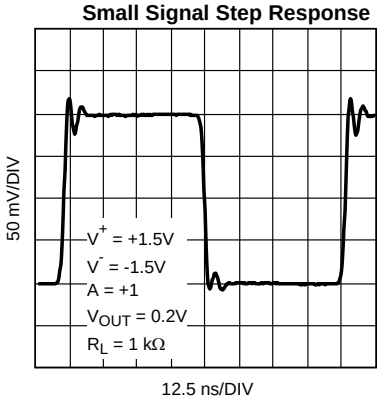


Figure 53.

Small Signal Step Response

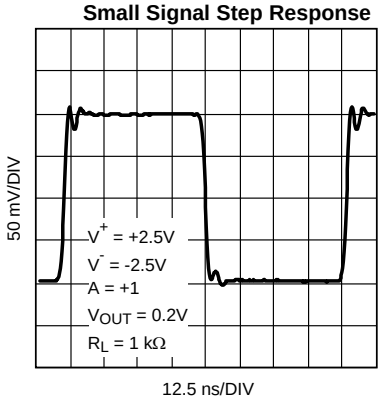


Figure 54.

Small Signal Step Response

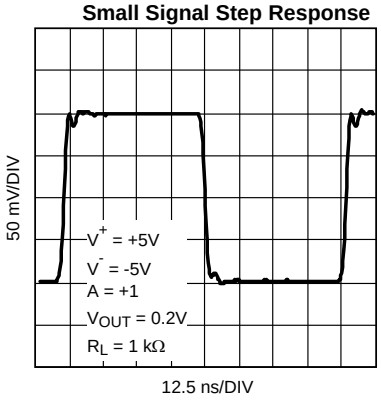


Figure 55.

Small Signal Step Response

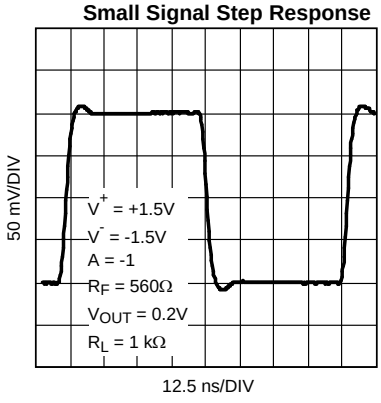


Figure 56.

Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

Small Signal Step Response

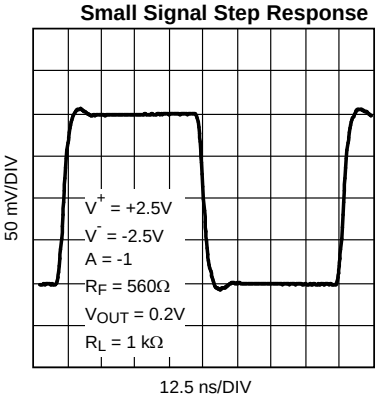


Figure 57.

Small Signal Step Response

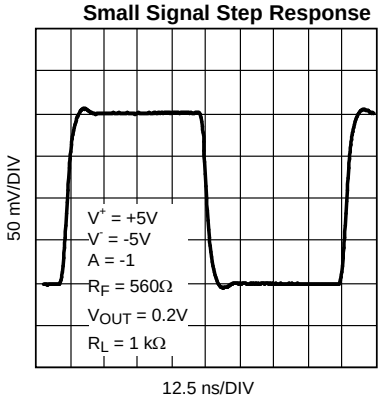


Figure 58.

Small Signal Step Response

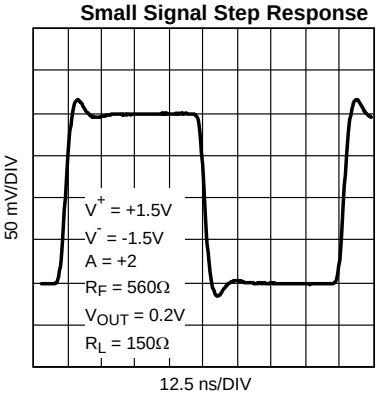


Figure 59.

Small Signal Step Response

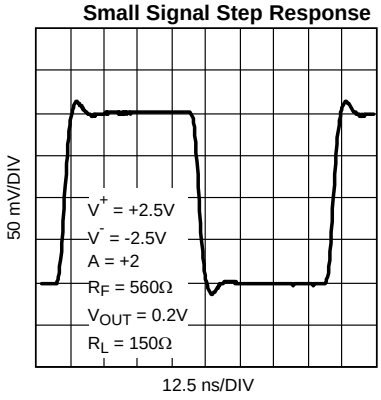


Figure 60.

Small Signal Step Response

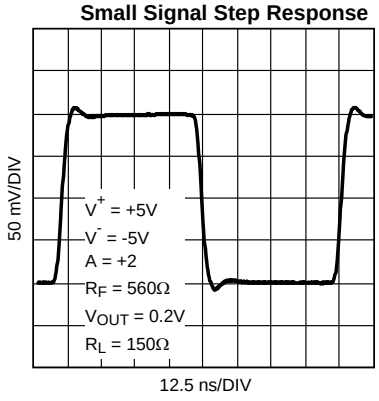


Figure 61.

Large Signal Step Response

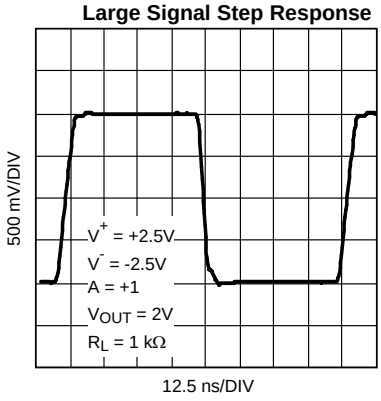


Figure 62.

Typical Performance Characteristics (continued)

At T_J = 25°C, A_V = +1 (R_F = 0Ω), otherwise R_F = 560Ω for $A_V \neq +1$, unless otherwise specified.

Large Signal Step Response

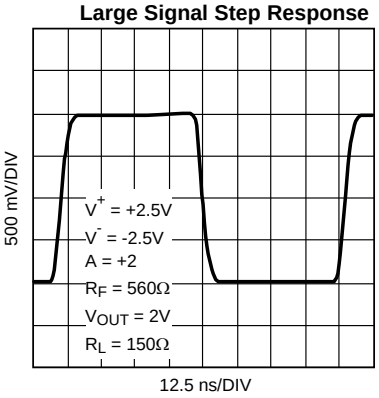


Figure 63.

Overload Recovery Response

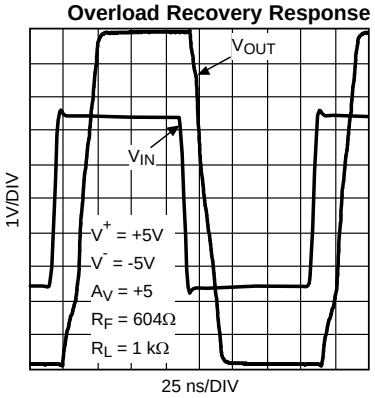


Figure 64.

I_S vs. $V_{DISABLE}$

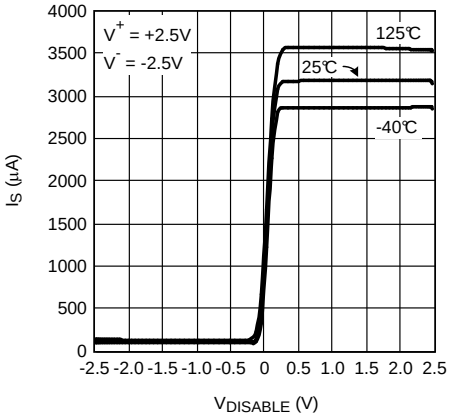


Figure 65.

APPLICATION INFORMATION

The LMH6611 and LMH6612 are based on proprietary VIP10 dielectrically isolated bipolar process. This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8 GHz) even under low supply voltage (2.7V) and low bias current.
- Common emitter push-push output stage. This architecture allows the output to reach within millivolts of either supply rail.
- Consistent performance with little variation from any supply voltage (2.7V - 11V) for the most important specifications (BW, SR, I_{OUT}, for example.)
- Significant power saving compared to competitive devices on the market with similar performance.

With 3V supplies and a common mode input voltage range that extends beyond either supply rail, the LMH6611 is well suited to many low voltage/low power applications. Even with 3V supplies, the −3 dB BW (at A_V = +1) is typically 305 MHz.

The LMH6611 and LMH6612 are designed to avoid output phase reversal. With input overdrive, the output is kept near the supply rail (or as close to it as mandated by the closed loop gain setting and the input voltage). Figure 66 shows the input and output voltage when the input voltage significantly exceeds the supply voltages.

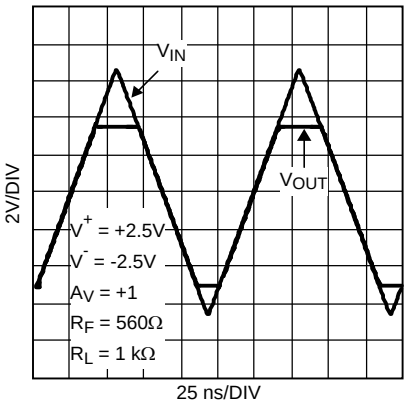


Figure 66. Input and Output Shown with CMVR Exceeded

If the input voltage range is exceeded by more than a diode drop beyond either rail, the internal ESD protection diodes will start to conduct. The current flow in these ESD diodes should be externally limited.

SHUTDOWN CAPABILITY AND TURN ON/OFF BEHAVIOR

The LMH6611 can be shutdown by connecting the $\overline{\text{DISABLE}}$ pin to a voltage 0.5V below the supply midpoint which will reduce the supply current to typically 120 µA. The $\overline{\text{DISABLE}}$ pin is “active low” and can be connected through a resistor to V^+ or left floating for normal operation. Shutdown is specified when the $\overline{\text{DISABLE}}$ pin is 0.5V below the supply midpoint at any operating supply voltage and temperature. Typical turn on time is 20 ns and the turn off time is 60 ns.

In the shutdown mode, essentially all internal device biasing is turned off in order to minimize supply current flow and the output goes into high impedance mode. During shutdown, the input stage has an equivalent circuit as shown in Figure 67.

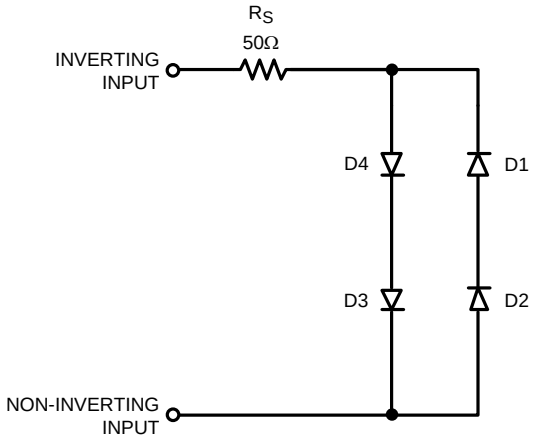


Figure 67. Input Equivalent Circuit During Shutdown

When the LMH6611 is shutdown, there may be current flow through the internal diodes shown, caused by input potential, if present. This current may flow through the external feedback resistor and result in an apparent output signal. In most shutdown applications the presence of this output is inconsequential. However, if the output is "forced" by another device, the other device will need to conduct the current described in order to maintain the output potential.

To keep the output at or near ground during shutdown when there is no other device to hold the output low, a switch using a transistor can be used to shunt the output to ground.

SELECTION OF R_F AND EFFECT ON STABILITY AND PEAKING

The peaking of the LMH6611 depends on the value of the R_F. From the graph shown in Figure 68, as the R_F value increases, the peaking increases.

For A_V = 2, at R_F = 1 kΩ, the −3 dB bandwidth is 113 MHz and peaking is about 0.6 dB whereas at R_F = 665Ω, the −3 dB bandwidth is about 110 MHz and peaking is 0 dB. R_F and the input capacitance form a pole in the amplifier's response. If the time constant is too big, it will cause peaking and ringing.

Except for A_V = 1 when R_F should be 0Ω, across all other gain settings it is recommended that R_F remain between 500Ω and 1 kΩ to ensure optimum performance.

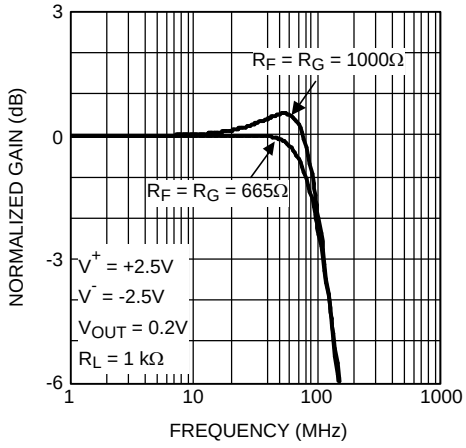


Figure 68. Closed Loop Gain vs. Frequency and $R_F = R_G$

$R_F = R_G$	f −3 dB (MHz)	Peaking (dB)
665	110	0
1000	113	0.6

MINIMIZING NOISE

With a low input voltage noise of 10 nV/√Hz and an input current noise of 2 pA√Hz the LMH6611 and LMH6612 are suitable for high accuracy applications. Still being able to reduce the frequency band of operation of the various noise sources (that is, op amp noise voltage, resistor thermal noise, input noise current) can further improve the noise performance of a system. In a non-inverting amplifier configuration inserting a capacitor, C_G, in series with the gain setting resistor, R_G, will reduce the gain of the circuit below frequency, $f = 1/2\pi R_G C_G$. This can be set to reduce the contribution of noise from the 1/f region. Alternatively applying a feedback capacitor, C_F, in parallel with the feedback resistor, R_F, will introduce a pole into your system at $f = 1/2\pi R_F C_F$ and create a low pass filter. This filter can be set to reduce high frequency noise and harmonics. Finally remember to keep resistor values as small as possible for a given application in order to reduce resistor thermal noise.

POWER SUPPLY BYPASS

Since the LMH6611 and LMH6612 are wide bandwidth amplifiers, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing or oscillation. 0.1 µF capacitors should be connected from the supply pins, V^+ and V^-, to ground, as close to the device as is practical. Additionally, a 10 µF electrolytic capacitor should be connected from both supply pins to ground reasonably close to the device. Finally, near the device a 0.1 µF ceramic capacitor between the supplies will provide the best harmonic distortion performance.

INTERFACING HIGH PERFORMANCE OP AMPS WITH ADCs

These amplifiers are designed for ease of use in a wide range of applications requiring high speed, low supply current, low noise, and the ability to drive complex ADC and video loads.

The source that drives the modern high resolution analog-to-digital converters (ADCs) sees a high frequency AC load and a DC load of a few hundred ohms or more. Thus, a high performance op amp with high input impedance of a few mega ohms and low output impedance would be an ideal choice as an input ADC driver. The LMH6611/LMH6612 have the low output impedance of 0.07Ω at f = 1 MHz. The ADC driver acts as a buffer and a low pass filter to reduce the overall system noise. To utilize the full dynamic range of the ADC, the ADC input has to be driven to full scale input voltage.

As signals travel through the traces of a printed circuit board (PCB) and long cables, system noise accumulates in the signals and a differential ADC rejects any signals noise that appears as a common mode voltage. There are a couple of advantages to using differential signals rather than single-ended signals. First, differential signals double the dynamic range of the ADC and second, they offer better harmonic distortion performance. There are several ways to produce differential signals from a dual op amp configuration. One method is to utilize the single-ended to differential conversion technique and the other is the differential to differential conversion technique. The first method requires a single input source and the second method requires differential input source.

A real world input source can have non-ideal impedance thus the buffer amplifier, with very low output impedance, is required to drive the input of the ADC. To minimize the droop in the input voltage, external shunt capacitance (C_L) should be about ten times larger than the internal input capacitance of the ADC and external series resistance (R_L) should be large enough to maintain the phase delay at the output of the op amp and hence maintain the stability (See Figure 69). Most applications benefit from the inclusion of a series isolation resistor connected between the op amp output and ADC input. This series resistor helps to limit the output current of the op amp. The value chosen for this series resistor is very important, as a higher value will increase the load impedance seen by the op amp and improve the total harmonic distortion (THD) performance of the op amp; however, the ADC prefers a low impedance source driving it. Thus, the optimum value for this series resistor must be found so that it will offer the best performance in terms of THD, SNR and SFDR of the combined op amp and ADC.

Important Specifications of Op Amp and ADC

When interfacing an ADC with an op amp it is imperative to understand the specifications that are important to get the expected performance results. Modern ADC AC specifications such as THD, SNR, settling time and SFDR are critical for filtering, test and measurement, video and reconstruction applications. The high performance op amp's settling time, THD, and noise performance must be better than that of the ADC it is driving to maintain the proper system accuracy with minimal or no error.

Some system applications require low THD, low SFDR and wide dynamic range (SNR), whereas some system applications require high SNR and they may sacrifice THD and SFDR to focus on the noise performance.

Noise is a very important specification for both the op amp and the ADC. There are three main sources of noise that contribute to the overall performance of the ADC: Quantization noise, noise generated by the ADC itself (particularly at higher frequencies) and the noise generated by the application circuit. The impedance of the input source affects the noise performance of the op amp. Theoretically, an ADC's signal to noise ratio (SNR) can be found from the equation:

$$\text{SNR (in dB)} = 6.02*N+1.72 \tag{1}$$

where N is the resolution of the ADC. For example, according to this equation a 12-bit ADC has an SNR of 74 dB. However, the practical SNR number would be about 72 dB. In order to achieve better SNR, the ADC driver noise should be as small as possible. The LMH6611/LMH6612 have the low voltage noise of only 10 nV/$\sqrt{\text{Hz}}$.

The combined settling time of the op amp and the ADC must be within 1 LSB. The 0.01% settling time of the LMH6611/LMH6612 is 100 ns.

The ADC driver's THD should be inherently lower than that of the ADC. The LMH6611/LMH6612 have an SFDR of 96 dBc at 2 V_{PP} output and 1 MHz input frequency.

Signal to Noise and Distortion (SINAD) is a parameter which is the combination of the SNR and THD specifications. SINAD is defined as the RMS value of the output signal to the RMS value of all of the other spectral components below half the clock frequency, including harmonics but excluding DC. It can be calculated from SNR and THD according to the equation:

$$\text{SINAD} = 20 * \text{LOG}\sqrt{10^{\frac{-\text{SNR}}{10}} + 10^{\frac{\text{THD}}{10}}} \tag{2}$$

Because SINAD compares all undesired frequency components with the input frequency, it is an overall measure of an ADC's dynamic performance. The following sections will discuss the three different ADC driver architectures in detail.

SINGLE TO SINGLE ADC DRIVER

This architecture has a single-ended input source connected to the input of the op amp and the single-ended output of the op amp is then fed to the single-ended input of the ADC. The low noise of only 10 nV/$\sqrt{\text{Hz}}$ and a wide bandwidth of 345 MHz make the LMH6611 an excellent choice for driving the 12-bit ADC121S101 500 KSPS to 1 MSPS ADC, which has a successive approximation architecture with internal sample and hold circuits. Figure 67 shows the schematic of the LMH6611 in a 2nd order multiple-feedback with gain of −1 (inverting) configuration, driving an ADC121S101. The inverting configuration is preferred over the non-inverting configuration, as it offers more linear output response. Table 1 shows the performance data of the LMH6611 combined with the ADC121S101. The ADC driver's cutoff frequency of 500 kHz is found from the equation:

$$f_0 = \frac{1}{2\pi} \times \sqrt{\frac{1}{R_2 \times R_5 \times C_2 \times C_5}} \tag{3}$$

The op amp's gain is set by the equation:

$$\text{GAIN} = -\frac{R_2}{R_1} \tag{4}$$

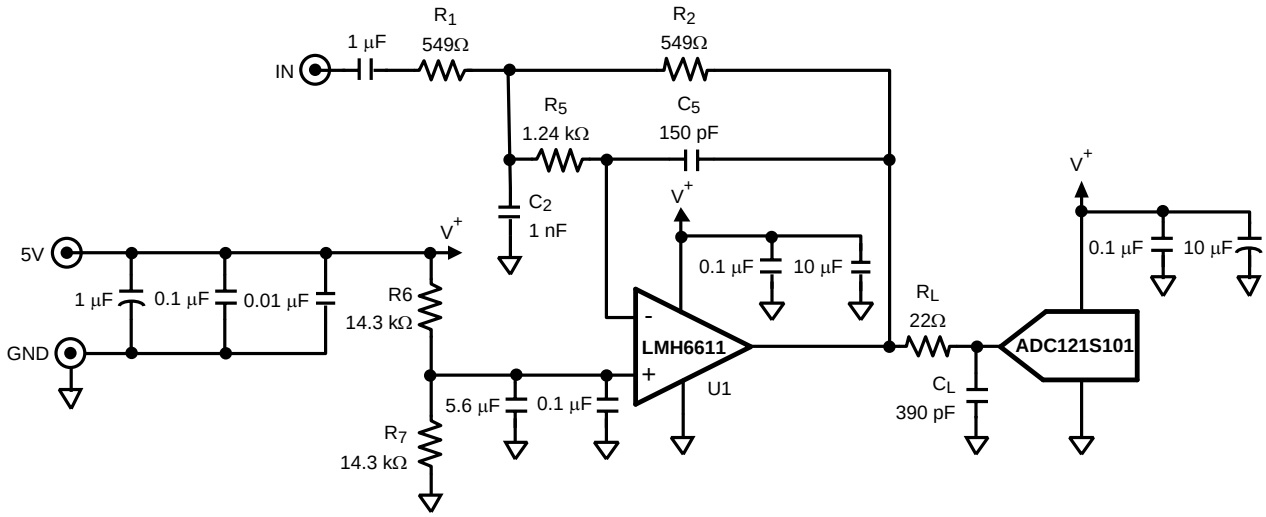


Figure 69. Single to Single ADC Driver

Table 1. Performance of the LMH6611 Combined with the ADC121S101

Amplifier Output/ADC Input	SINAD (dB)	SNR (dB)	THD (dB)	SFDR (dBc)	ENOB	Notes
4	70.2	71.6	−75.7	77.6	11.4	ADC121S101 @ f = 200 kHz

When the op amp and the ADC are using the same supply, it is important that both devices are well bypassed. A 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor should be located as close as possible to each supply pin. A sample layout is shown in Figure 70. The 0.1 µF capacitors (C13 and C6) and the 10 µF capacitors (C11 and C5) are located very close to the supply pins of the LMH6611 and the ADC121S101.

The following are recommendations for the design of PCB layout in order to obtain the optimum high frequency performance:

- Place ADC and amplifier as close together as possible.
- Put the supply bypassing capacitors as close as possible to the device (<1”).
- Utilize surface mount instead of through-hole components and ground and power planes.
- Keep the traces short where possible.
- Use terminated transmission lines for long traces.

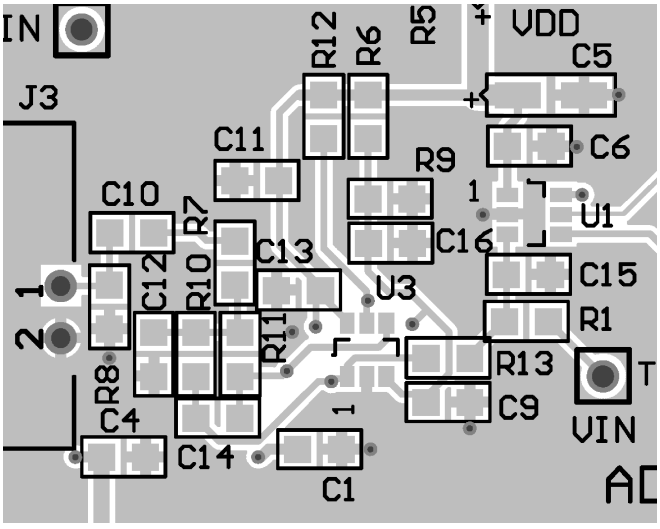


Figure 70. LMH6611 and ADC121S101 Layout

SINGLE-ENDED TO DIFFERENTIAL ADC DRIVER

The single-ended to differential ADC driver in Figure 68 utilizes an LMH6612 dual op amp to buffer a single-ended source to drive an ADC with differential inputs. One of the op amps is configured as a unity gain buffer that drives the inverting (IN−) input of the op amp U2 and non-inverting (IN+) input of the ADC121S625. U2 inverts the input signal and drives the inverting input of the ADC121S625. The ADC driver is configured for a gain of +2 to reduce the noise without sacrificing THD performance. The common mode voltage of 2.5V is set up at the non-inverting inputs of both op amps U1 and U2. This configuration produces differential ±2.5 V_{PP} output signals, when the single-ended input signal of 0 to V_{REF} is AC coupled into the non-inverting terminal of the op amp and each non-inverting terminal of the op amp is biased at the mid-scale of 2.5V. The two output RC anti-aliasing filters are used between both the outputs of U1 and U2 and the input of the ADC121S625 to minimize the effect of undesired high frequency noise coming from the input source. Each RC filter has the cutoff frequency of approximately 22 MHz.

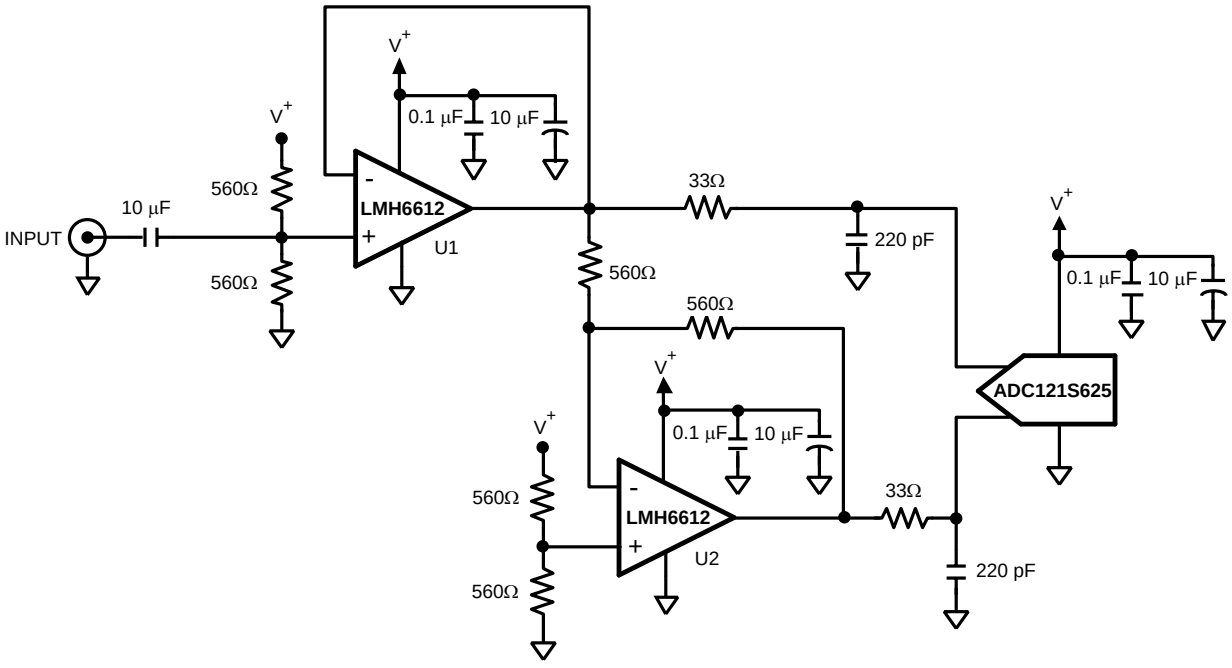


Figure 71. Single-Ended to Differential ADC Driver

The performance of the LMH6612 with the ADC121S625 is shown in Table 2.

Table 2. Performance of the LMH6612 Combined with the ADC121S625

Amplifier Output/ADC Input	SINAD (dB)	SNR (dB)	THD (dB)	SFDR (dBc)	ENOB	Notes
2.5	68.8	69	−81.5	75.1	11.2	ADC121S625 @ f = 20 kHz

DIFFERENTIAL TO DIFFERENTIAL ADC DRIVER

The LMH6612 dual op amp can be configured as a differential to differential ADC driver to buffer a differential source to a differential input ADC as shown in Figure 72. The differential to differential ADC driver can be formed using two single to single ADC drivers. Each output from these drivers goes to a separate input of the differential ADC. Here, each single to single ADC driver uses the same components and is configured for a gain of -1 (inverting).

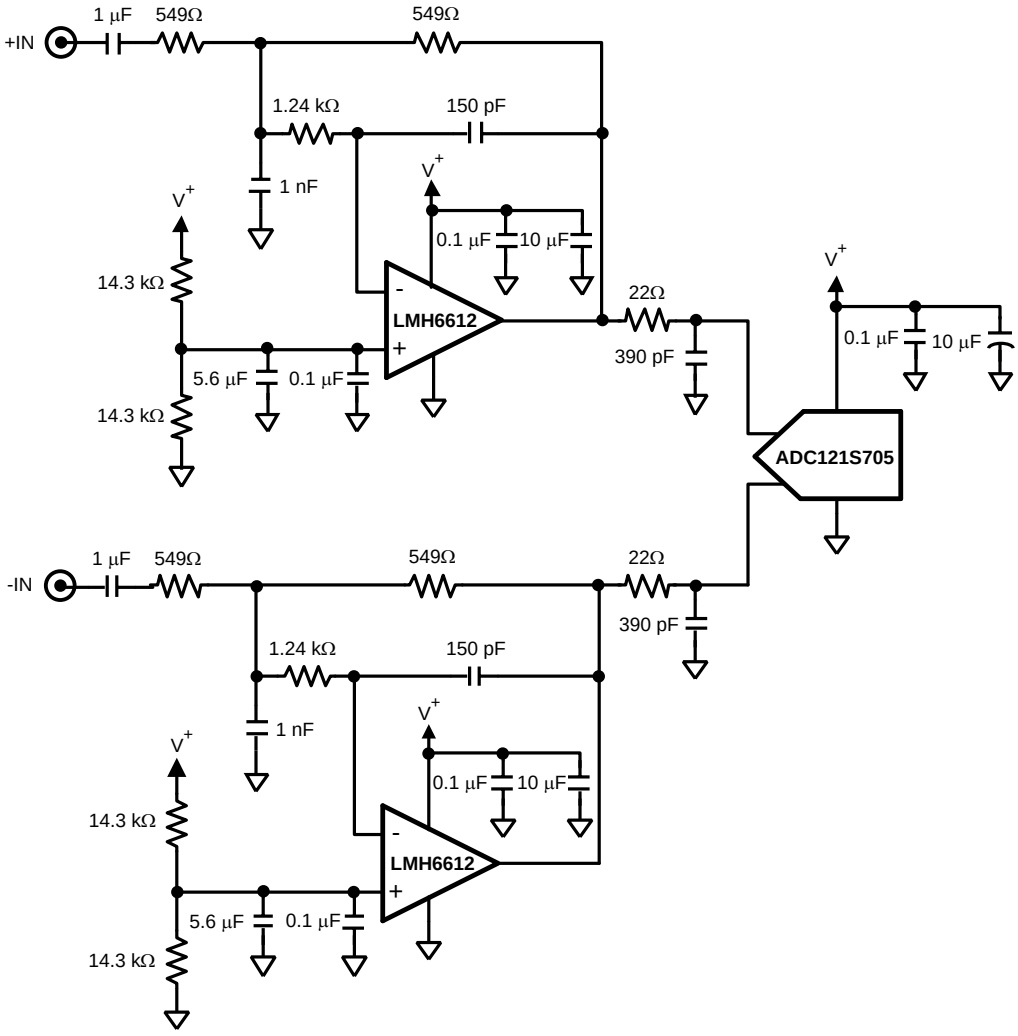


Figure 72. Differential to Differential ADC Driver

The following table summarizes the performance of the LMH6612 combined with the ADC121S625 at two different frequencies. In order to utilize the full dynamic range of the ADC, the maximum input of 2.5 V_{PP} is applied to the ADC input. Figure 73 shows the FFT plot of the LMH6612 and ADC121S625 combination tested at f = 20 kHz input frequency.

Table 3. Performance of the LMH6612 Combined with the ADC121S625

Amplifier Output/ADC Input	SINAD (dB)	SNR (dB)	THD (dB)	SFDR (dBc)	ENOB	Notes
2.5	72.2	72.3	−87.7	92.1	11.7	ADC121S625 @ f = 20 kHz
2.5	72.2	72.2	−87.8	90.8	11.7	ADC121S625 @ f = 200 kHz

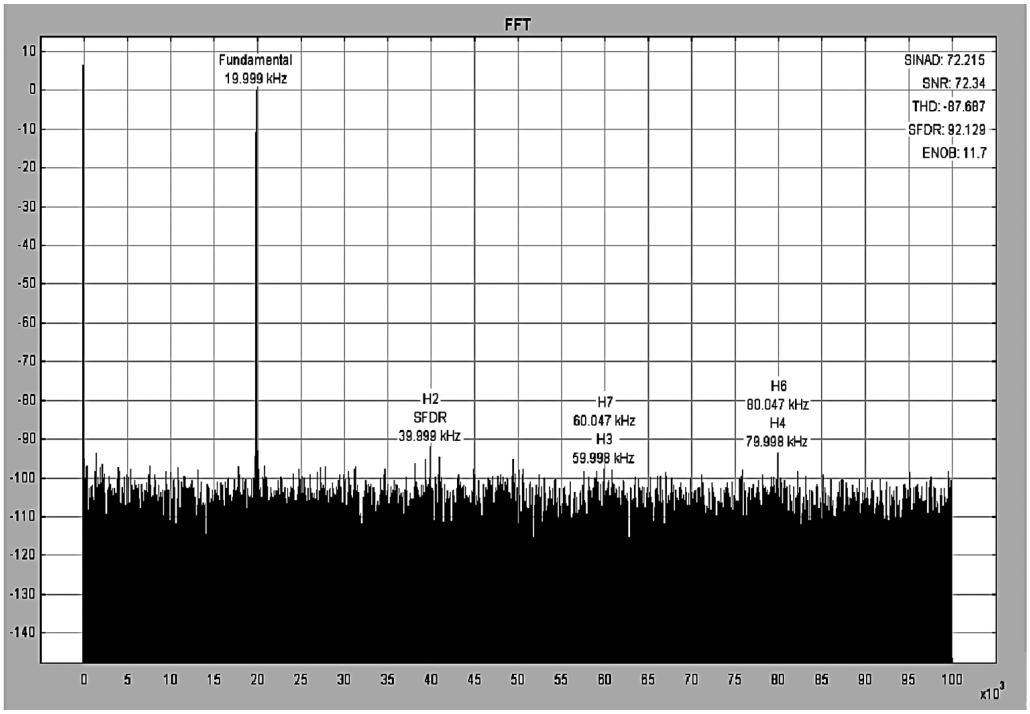


Figure 73. The FFT Plot of Differential to Differential ADC Driver

DC LEVEL SHIFTING

Often a signal must be both amplified and level shifted while using a single supply for the op amp. The circuit in Figure 74 can do both of these tasks. The procedure for specifying the resistor values is as follows.

1. Determine the input voltage.
2. Calculate the input voltage midpoint, $V_{INMID} = V_{INMIN} + (V_{INMAX} – V_{INMIN})/2$.
3. Determine the output voltage needed.
4. Calculate the output voltage midpoint, $V_{OUTMID} = V_{OUTMIN} + (V_{OUTMAX} – V_{OUTMIN})/2$.
5. Calculate the gain needed, gain = $(V_{OUTMAX} – V_{OUTMIN})/(V_{INMAX} – V_{INMIN})$
6. Calculate the amount the voltage needs to be shifted from input to output, $\Delta V_{OUT} = V_{OUTMID} – \text{gain} \times V_{INMID}$.
7. Set the supply voltage to be used.
8. Calculate the noise gain, noise gain = gain + $\Delta V_{OUT}/V_S$.
9. Set R_F.
10. Calculate R_1, $R_1 = R_F/\text{gain}$.
11. Calculate R_2, $R_2 = R_F/(\text{noise gain-gain})$.
12. Calculate R_G, $R_G = R_F/(\text{noise gain} – 1)$.

Check that both the V_{IN} and V_{OUT} are within the voltage ranges of the LMH6611.

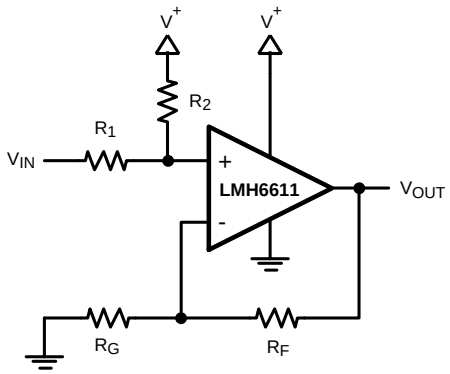


Figure 74. DC Level Shifting

The following example is for a V_{IN} of 0V to 1V with a V_{OUT} of 2V to 4V.

1. V_{IN} = 0V to 1V
2. V_{INMID} = 0V + (1V – 0V)/2 = 0.5V
3. V_{OUT} = 2V to 4V
4. V_{OUTMID} = 2V + (4V – 2V)/2 = 3V
5. Gain = (4V – 2V)/(1V – 0V) = 2
6. ΔV_{OUT} = 3V – 2 x 0.5V = 2
7. For the example the supply voltage will be +5V.
8. Noise gain = 2 + 2/5V = 2.4
9. R_F = 2 kΩ
10. R_1 = 2 kΩ/2 = 1 kΩ
11. R_2 = 2 kΩ/(2.4-2) = 5 kΩ
12. R_G = 2 kΩ/(2.4 – 1) = 1.43 kΩ

4th ORDER MULTIPLE FEEDBACK LOW-PASS FILTER

Figure 75 shows the LMH6612 used as the amplifier in a multiple feedback low pass filter. This filter is set up to have a gain of +1 and a −3 dB point of 1 MHz. Values can be determined by using the WEBENCH® Active Filter Designer found at www.ti.com/amplifiers

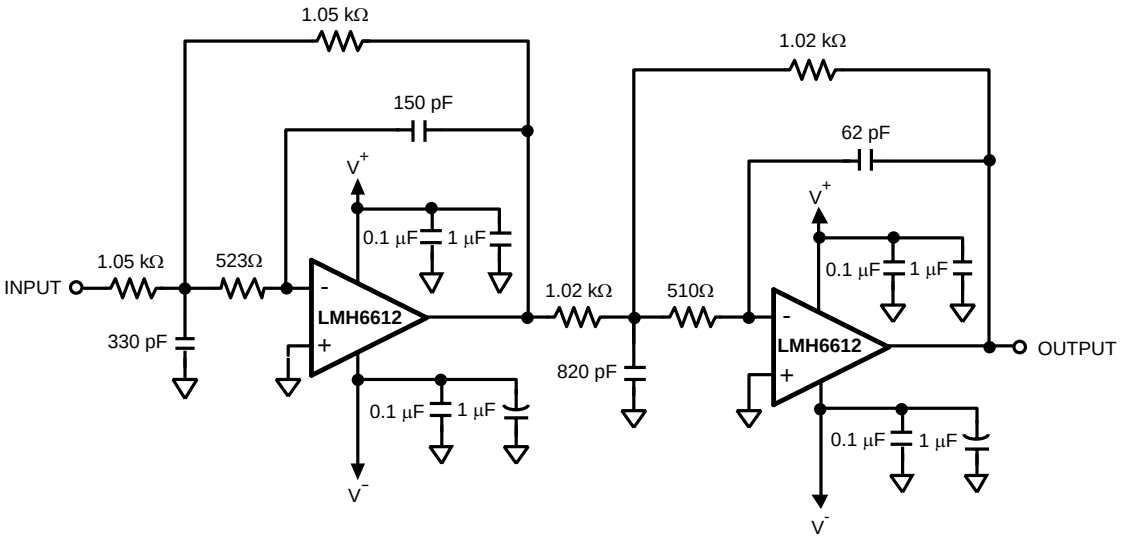


Figure 75. 4th Order Multiple Feedback Low-Pass Filter

CURRENT SENSE AMPLIFIER AND OPTIMIZING ACCURACY IN PRECESION APPLICATIONS

With it's rail-to-rail output capability, low V_{OS}, and low I_B the LMH6611 is an ideal choice for a current sense amplifier application. Figure 76 shows the schematic of the LMH6611 set up in a low-side sense configuration which provides a conversion gain of 2V/A. Voltage error due to V_{OS} can be calculated to be V_{OS} x (1 + R_F/R_G) or 1.5 mV x 21 = 31.5 mV. Voltage error due to I_O is I_O x R_F or 0.5 µA x 1 kΩ = 0.5 mV. Hence worst case total voltage error is 12.6 mV + 0.5 mV or 13.1 mV which translates into a current error of 13.1 mV/(2 V/A) = 6.55 mA.

This circuit employs DC source resistance matching at the two input terminals in order to minimize the output DC error caused by input bias current. Another technique to reduce output offset in a non-inverting amplifier configuration is to introduce a DC offset current into the inverting input of the amplifier. To ensure minimal impact on frequency response be sure to inject the DC offset current through large resistors. Conversely if optimizing an inverting amplifier configuration simply apply offset adjustment to the non-inverting input.

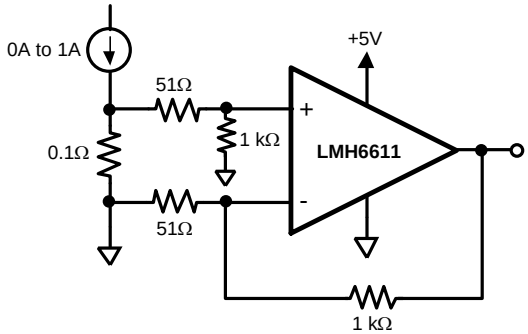


Figure 76. Current Sense Amplifier

TRANSIMPEDANCE AMPLIFIER

By definition, a photodiode produces either a current or voltage output from exposure to a light source. A Transimpedance Amplifier (TIA) is utilized to convert this low-level current to a usable voltage signal. The TIA often will need to be compensated to insure proper operation.

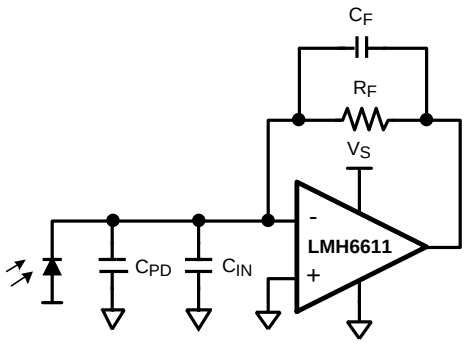


Figure 77. Photodiode Modeled with Capacitance Elements

Figure 77 shows the LMH6611 modeled with photodiode and the internal op amp capacitances. The LMH6611 allows circuit operation of a low intensity light due to its low input bias current by using larger values of gain (R_F). The total capacitance (C_T) on the inverting terminal of the op amp includes the photodiode capacitance (C_{PD}) and the input capacitance of the op amp (C_{IN}). This total capacitance (C_T) plays an important role in the stability of the circuit. The noise gain of this circuit determines the stability and is defined by:

$$NG = \frac{1 + sR_F (C_T + C_F)}{1 + sC_FR_F} \tag{5}$$

$$\text{Where, } f_Z \cong \frac{1}{2\pi R_F C_T} \text{ and } f_P = \frac{1}{2\pi R_F C_F} \tag{6}$$

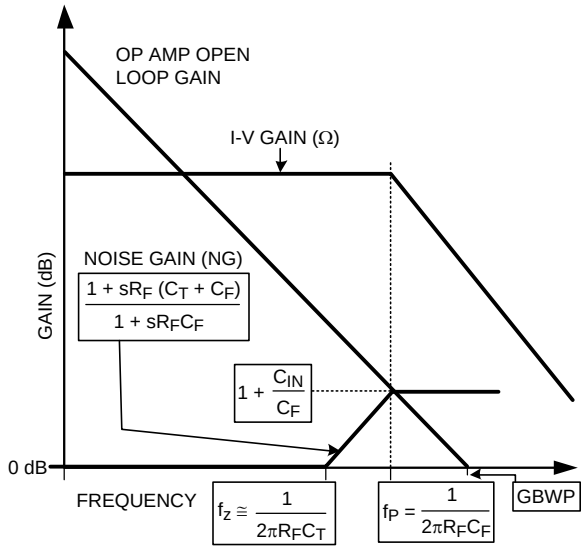


Figure 78. Bode Plot of Noise Gain Intersecting with Op Amp Open Loop Gain

Figure 78 shows the bode plot of the noise gain intersecting the op amp open loop gain. With larger values of gain, C_T and R_F create a zero in the transfer function. At higher frequencies the circuit can become unstable due to excess phase shift around the loop.

A pole at f_P in the noise gain function is created by placing a feedback capacitor (C_F) across R_F. The noise gain slope is flattened by choosing an appropriate value of C_F for optimum performance.

Theoretical expressions for calculating the optimum value of C_F and the expected −3 dB bandwidth are:

$$C_F = \sqrt{\frac{C_T}{2\pi R_F (GBWP)}} \quad (7)$$

$$f_{-3\ dB} = \sqrt{\frac{GBWP}{2\pi R_F C_T}} \quad (8)$$

Equation 8 indicates that the −3 dB bandwidth of the TIA is inversely proportional to the feedback resistor. Therefore, if the bandwidth is important then the best approach would be to have a moderate transimpedance gain stage followed by a broadband voltage gain stage.

Table 4 shows the measurement results of the LMH6611 with different photodiodes having various capacitances (C_{PD}) and a feedback resistance (R_F) of 1 kΩ.

Table 4. TIA (Figure 66) Compensation and Performance Results(1)

C_{PD} (pF)	C_T (pF)	$C_{F\ CAL}$ (pF)	$C_{F\ USED}$ (pF)	$f_{-3\ dB\ CAL}$ (MHz)	$f_{-3\ dB\ MEAS}$ (MHz)	Peaking (dB)
22	24	5.42	5.6	29.3	27.1	0.5
47	49	7.75	8	20.5	21	0.5
100	102	11.15	12	14.2	15.2	0.5
222	224	20.39	18	9.6	10.7	0.5
330	332	20.2	22	7.9	9	0.8

(1) GBWP = 130 MHz, $C_T = C_{PD} + C_{IN}$, C_{IN} = 2 pF, V_S = ±2.5V

Figure 79 shows the frequency response for the various photodiodes in Table 4.

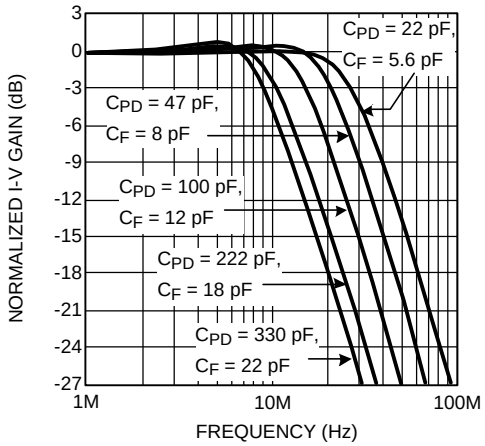


Figure 79. Frequency Response for Various Photodiode and Feedback Capacitors

When analyzing the noise at the output of the TIA, it is important to note that the various noise sources (that is, op amp noise voltage, feedback resistor thermal noise, input noise current, photodiode noise current) do not all operate over the same frequency band. Therefore, when the noise at the output is calculated, this should be taken into account. The op amp noise voltage will be gained up in the region between the noise gain's zero and pole (f_Z and f_P in Figure 78). The higher the values of R_F and C_T, the sooner the noise gain peaking starts and therefore its contribution to the total output noise will be larger. It is advantageous to minimize C_{IN} by proper choice of op amp or by applying a reverse bias across the diode but this will be at the expense of excess dark current and noise.

EVALUATION BOARD

TI provides the following evaluation board as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with this board:

Device	Package	Board Part #
LMH6611MK	SOT	LMH730216
LMH6612MA	SOIC	LMH730036

REVISION HISTORY

Changes from Revision I (March 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	33

Changes from Revision J (September 2013) to Revision K	Page
• Changed from 0.1 uV/°C to 4 µV/°C	3
• Changed from 0.1 uV/°C to 4 µV/°C	5
• Changed from 0.4 uV/°C to 4 µV/°C	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6611MK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AX4A	Samples
LMH6611MKE/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AX4A	Samples
LMH6611MKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AX4A	Samples
LMH6612MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMH66 12MA	Samples
LMH6612MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMH66 12MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

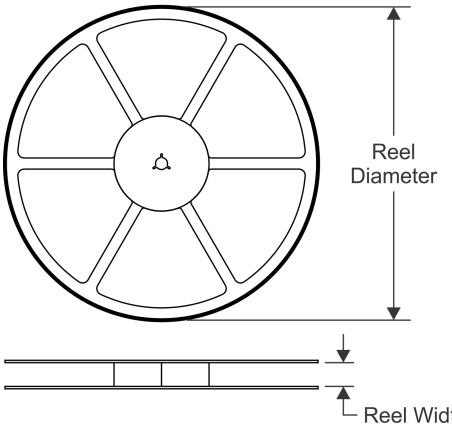
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

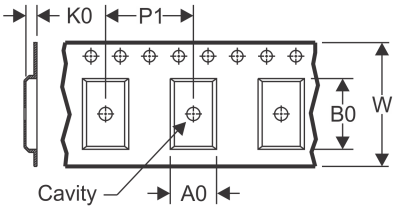
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

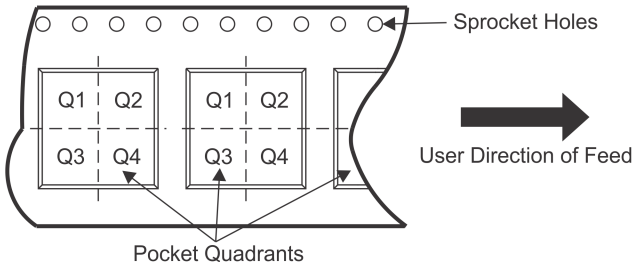


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

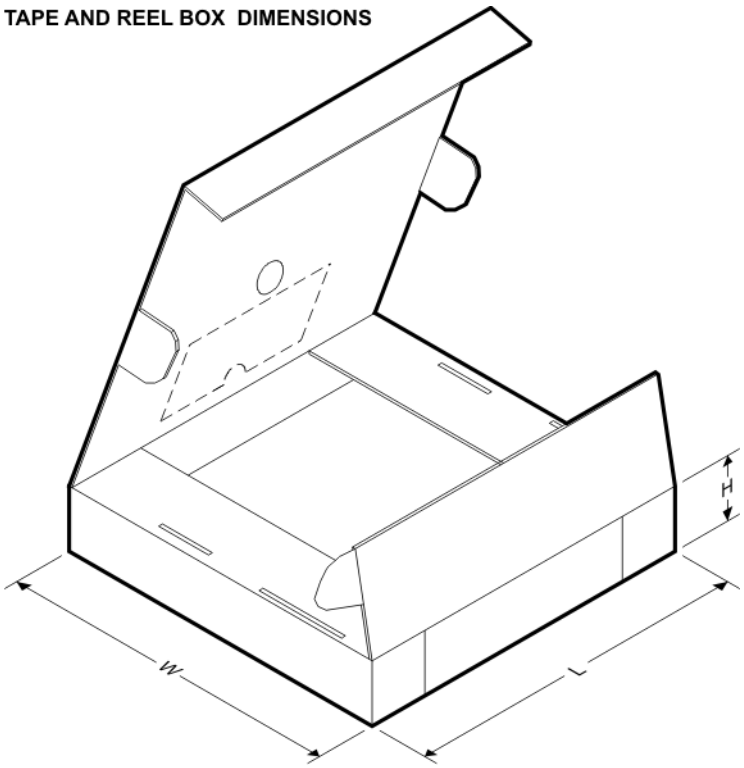
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6611MK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6611MKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6611MKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6612MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

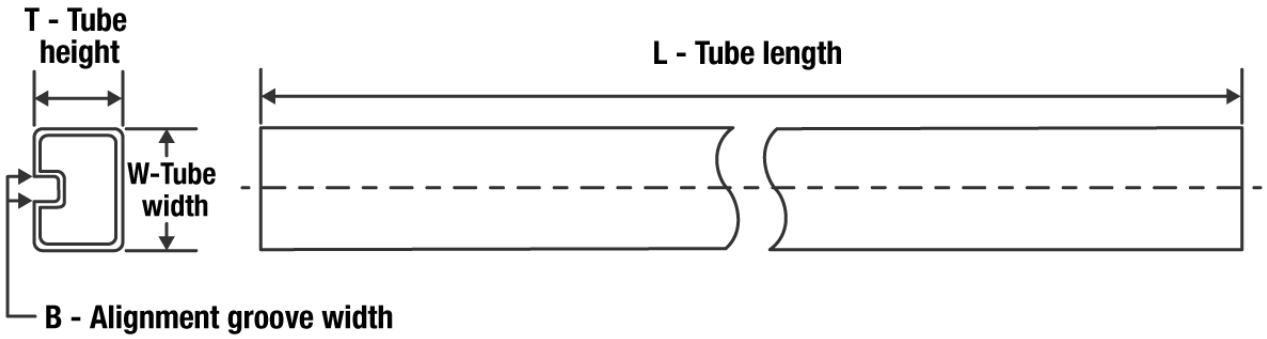
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6611MK/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LMH6611MKE/NOPB	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
LMH6611MKX/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMH6612MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

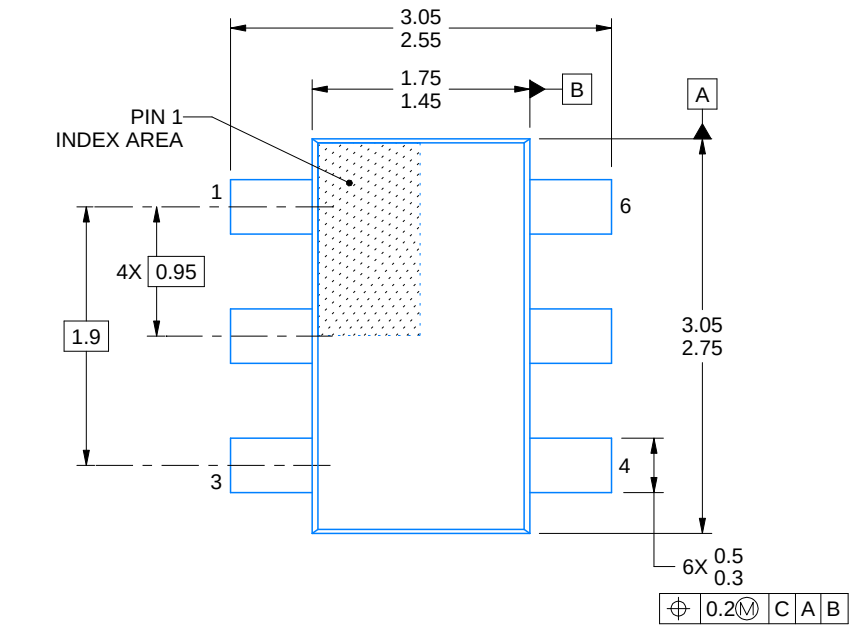
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6612MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

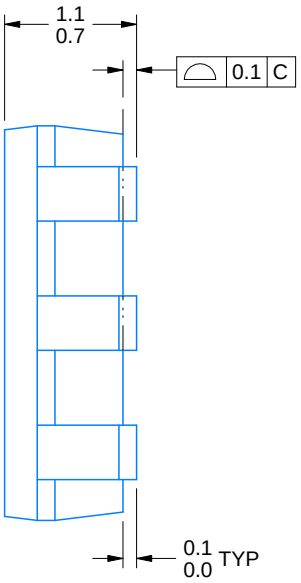
PACKAGE OUTLINE

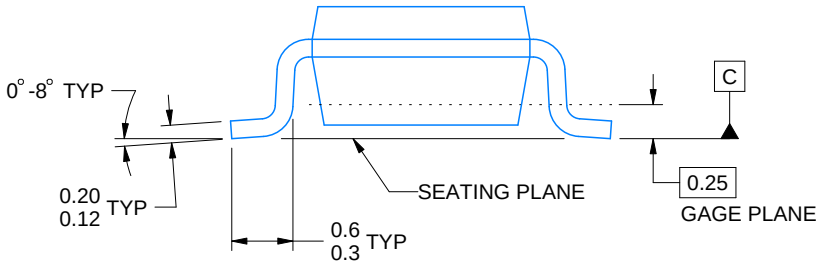
DDC0006A

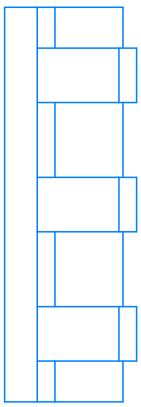
SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR







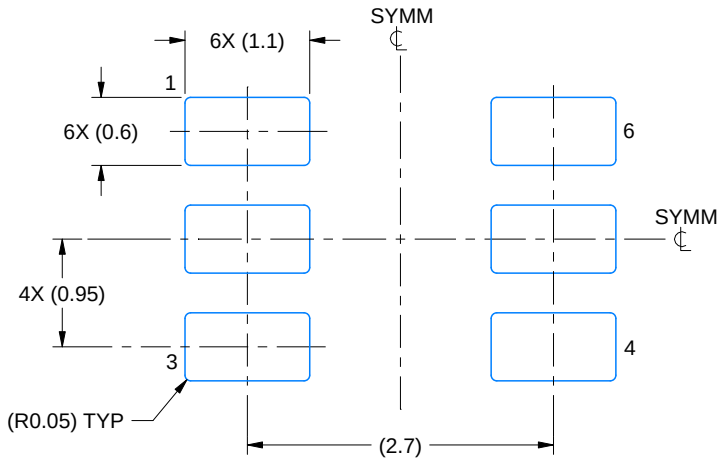


ALTERNATIVE PACKAGE
SINGULATION VIEW

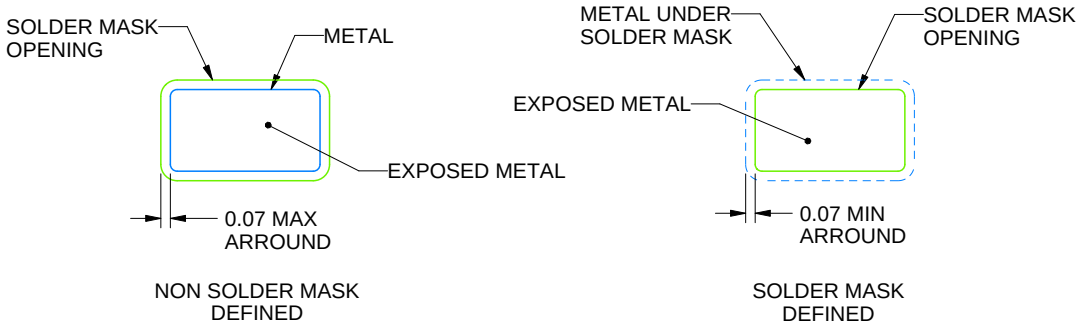
4214841/D 06/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

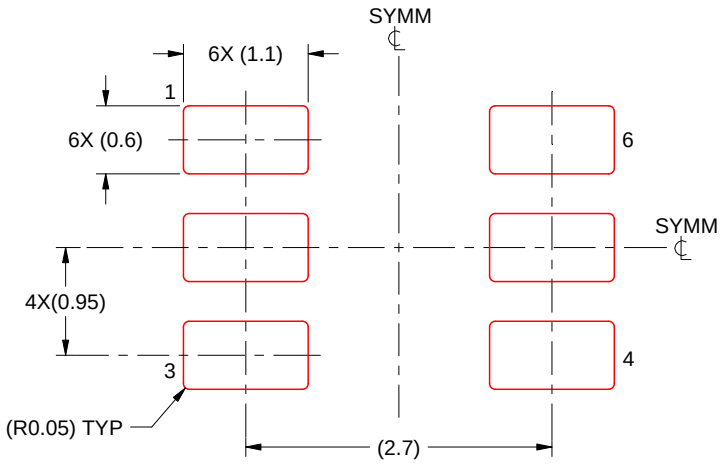


SOLDERMASK DETAILS

4214841/D 06/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

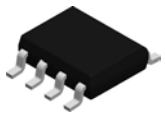


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/D 06/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

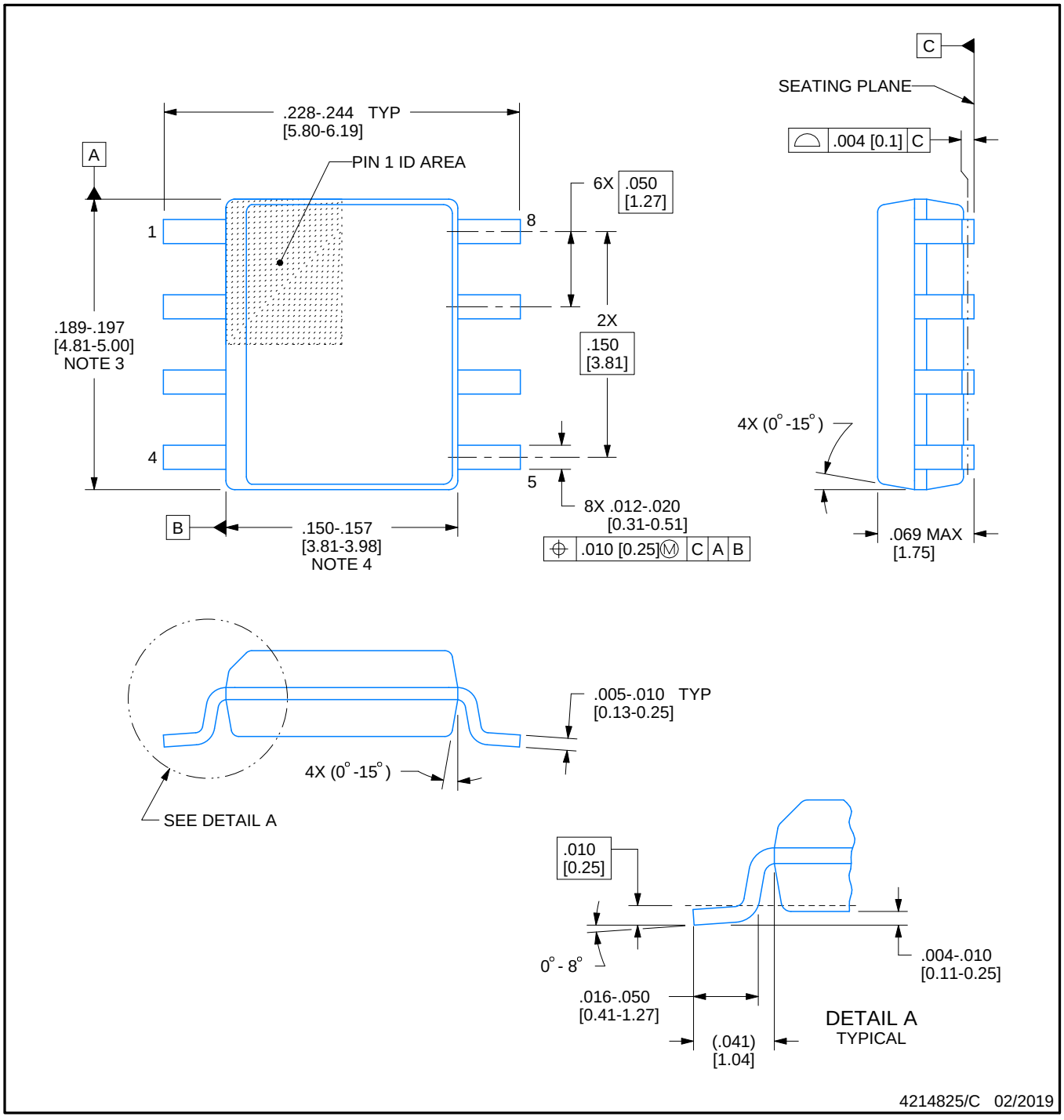


PACKAGE OUTLINE

D0008A

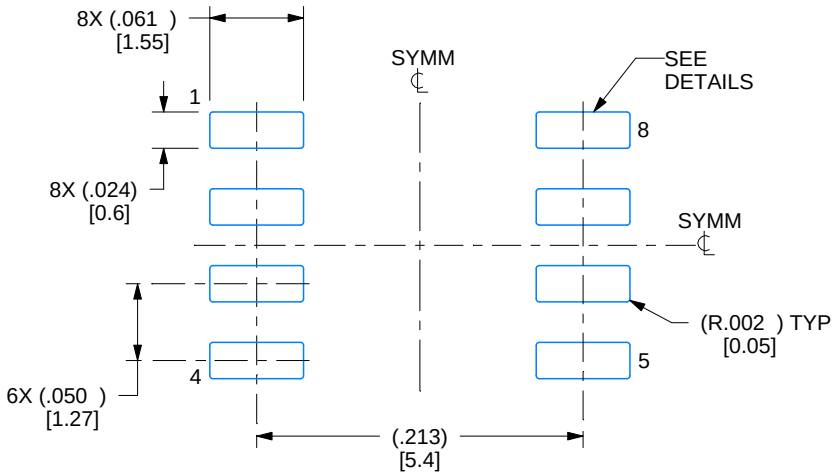
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

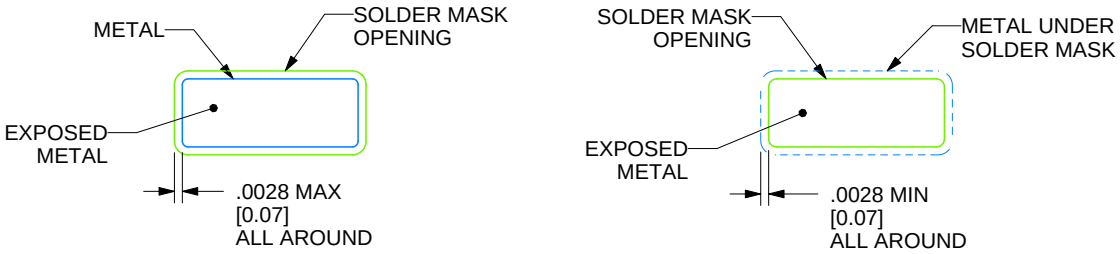


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

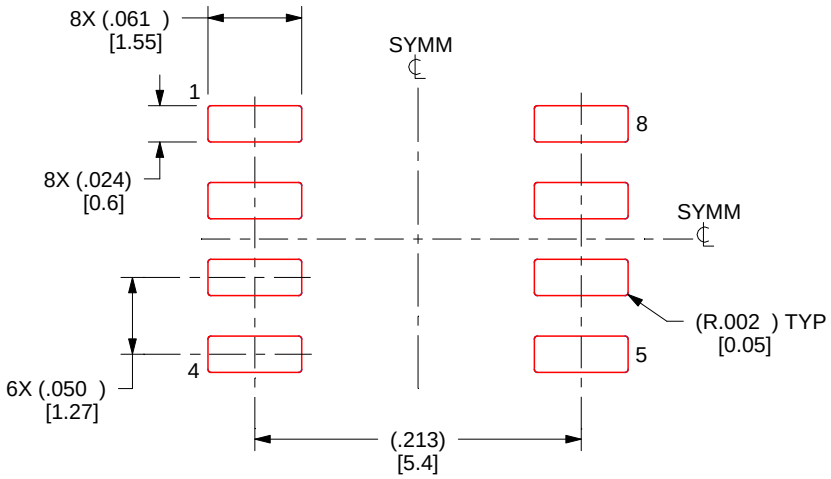
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265