

IRHYS67130CM (JANSR2N7588T3)

PD-96986E

Radiation Hardened Power MOSFET Thru-Hole (Low-Ohmic TO-257AA) 100V, 20A, N-channel, R6 Technology

Features

- Single event effect (SEE) hardened
- Low $R_{DS(on)}$
- Low total gate charge
- Fast switching
- Simple drive requirements
- Hermetically sealed
- Electrically isolated
- Ceramic eyelets
- Light weight
- ESD rating: Class 1C per MIL-STD-750, Method 1020

Potential Applications

- Isolated DC-DC converters
- Motor drives
- Electric propulsion
- Thermal management

Product Validation

Qualified to JANS screening flow according to MIL-PRF-19500 for space applications

Description

IR HiRel R6 technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 90 (MeV·cm²/mg). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHYS67130CM	Low-Ohmic TO-257AA	COTS	100 krad(Si)
IRHYS67130CMSCS	Low-Ohmic TO-257AA	S-Level	100 krad(Si)
JANSR2N7588T3	Low-Ohmic TO-257AA	JANS	100 krad(Si)
IRHYS63130CM	Low-Ohmic TO-257AA	COTS	300 krad(Si)
IRHYS63130CMSCS	Low-Ohmic TO-257AA	S-Level	300 krad(Si)
JANSF2N7588T3	Low-Ohmic TO-257AA	JANS	300 krad(Si)

Product Summary

- **BV_{DSS} :** 100V
- **I_D :** 20A*
- **$R_{DS(on), max}$:** 42mΩ
- **Q_G, max :** 50nC
- **REF:** MIL-PRF-19500/755



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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 12V, T_C = 25^{\circ}C$	Continuous Drain Current	20*	A
$I_{D2} @ V_{GS} = 12V, T_C = 100^{\circ}C$	Continuous Drain Current	19	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ¹	80	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	107	mJ
I_{AR}	Avalanche Current ¹	20	A
E_{AR}	Repetitive Avalanche Energy ¹	7.5	mJ
dv/dt	Peak Diode Reverse Recovery ³	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^{\circ}C$
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	4.3 (Typical)	

* Current is limited by package

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.² $V_{DD} = 25V$, starting $T_J = 25^{\circ}C$, $L = 0.54mH$, Peak $I_L = 20A$, $V_{GS} = 12V$ ³ $I_{SD} \leq 20A$, $di/dt \leq 575A/\mu s$, $V_{DD} \leq 100V$, $T_J \leq 150^{\circ}C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	42	m Ω	$V_{GS} = 12V, I_{D2} = 19A^1$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 1mA$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-8.72	—	mV/ $^\circ\text{C}$	
G_{fs}	Forward Transconductance	14	—	—	S	$V_{DS} = 15V, I_{D2} = 19A^1$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	$V_{DS} = 80V, V_{GS} = 0V$
		—	—	25		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_G	Total Gate Charge	—	—	50	nC	$I_{D1} = 20A$ $V_{DS} = 50V$ $V_{GS} = 12V$
Q_{GS}	Gate-to-Source Charge	—	—	15		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	12		
$t_{d(on)}$	Turn-On Delay Time	—	—	20	ns	$I_{D1} = 20A^{**}$ $V_{DD} = 50V$ $R_G = 7.5\Omega$ $V_{GS} = 12V$
t_r	Rise Time	—	—	50		
$t_{d(off)}$	Turn-Off Delay Time	—	—	35		
t_f	Fall Time	—	—	15		
$L_s + L_D$	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	1710	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	343	—		
C_{rss}	Reverse Transfer Capacitance	—	6.5	—		

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Device Characteristics

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	20	A	
I _{SM}	Pulsed Source Current (Body Diode) ¹	—	—	80	A	
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 20A, V _{GS} = 0V ²
t _{rr}	Reverse Recovery Time	—	—	250	ns	T _J = 25°C, I _F = 20A, V _{DD} ≤ 25V di/dt = 100A/μs
Q _{rr}	Reverse Recovery Charge	—	1.8	—	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to- Ambient (Typical socket mount)	—	—	80	

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation ^{3, 4}

Symbol	Parameter	Up to 300 krad (Si) ⁵		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	V	$V_{GS} = 0\text{V}$, $I_D = 1.0\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0\text{mA}$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -20\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	10	μA	$V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) ²	—	45	$\text{m}\Omega$	$V_{GS} = 12\text{V}$, $I_{D2} = 19\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-257AA) ²	—	42	$\text{m}\Omega$	$V_{GS} = 12\text{V}$, $I_{D2} = 19\text{A}$
V_{SD}	Diode Forward Voltage	—	1.2	V	$V_{GS} = 0\text{V}$, $I_F = 20\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300\text{ }\mu\text{s}$; Duty Cycle $\leq 2\%$

³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 12\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 80\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁵ Part numbers IRHYS67130CM (JANSR2N7588T3), IRHYS63130CM (JANSF2N7588T3)

IRHYS67130CM (JANSR2N7588T3)

Radiation Hardened Power MOSFET Thru-Hole (Low-Ohmic TO-257AA)

Device Characteristics

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm ² /mg)	Energy (MeV)	Range (μm)	V _{DS} (V)					
			V _{GS} = 0V	V _{GS} = -5V	V _{GS} = -10V	V _{GS} = -15V	V _{GS} = -19V	V _{GS} = -20V
39 ± 5%	315 ± 5%	40 ± 5%	100	100	100	100	100	40
61 ± 5%	345 ± 5%	32 ± 7.5%	100	100	100	30	—	—
90 ± 5%	375 ± 7.5%	29 ± 7.5%	100	100	—	—	—	—

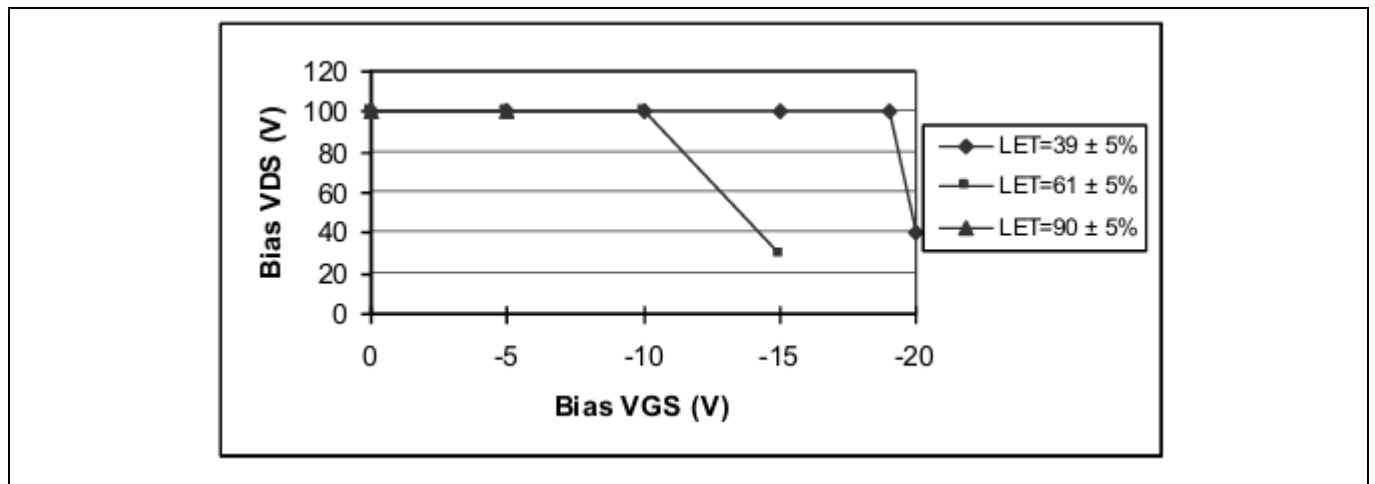


Figure 1 Typical Single Event Effect, Safe Operating Area

IRHYS67130CM (JANSR2N7588T3)

Radiation Hardened Power MOSFET Thru-Hole (Low-Ohmic TO-257AA)

Electrical Characteristics Curves (Pre-irradiation)

3 Electrical Characteristics Curves (Pre-irradiation)

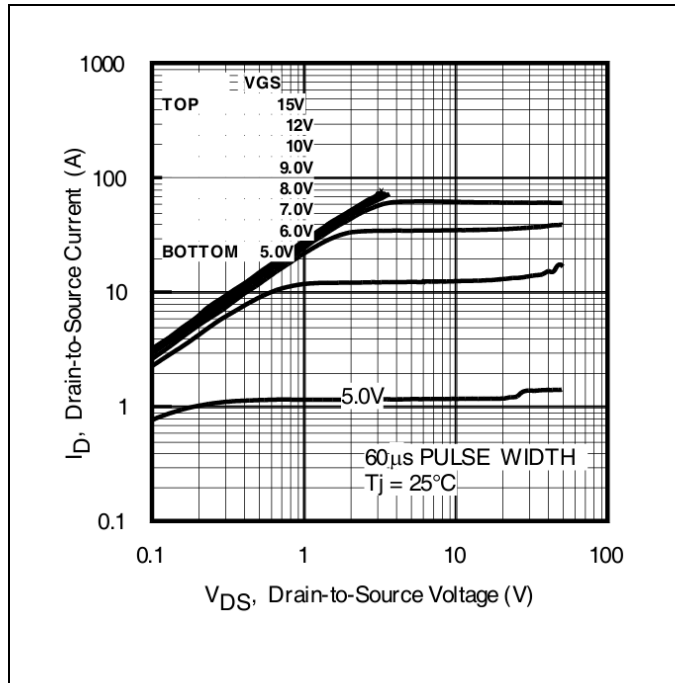


Figure 2 Typical Output Characteristics

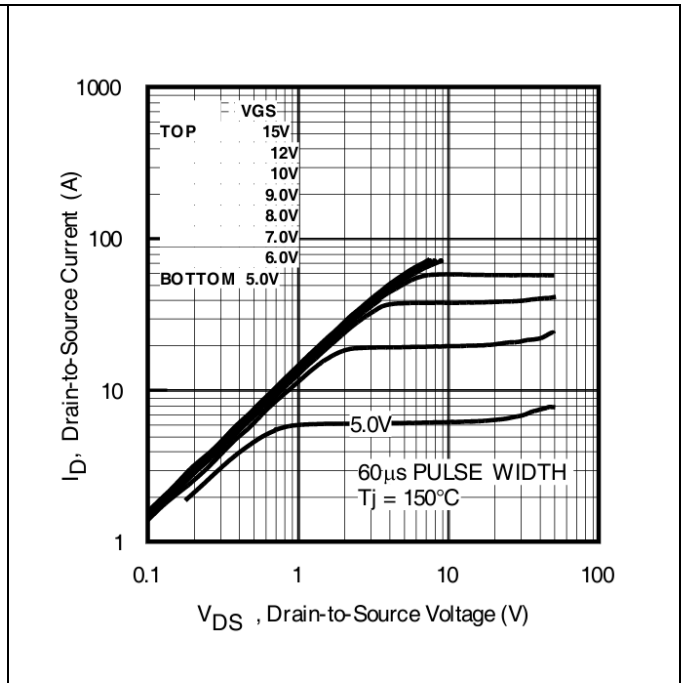


Figure 3 Typical Output Characteristics

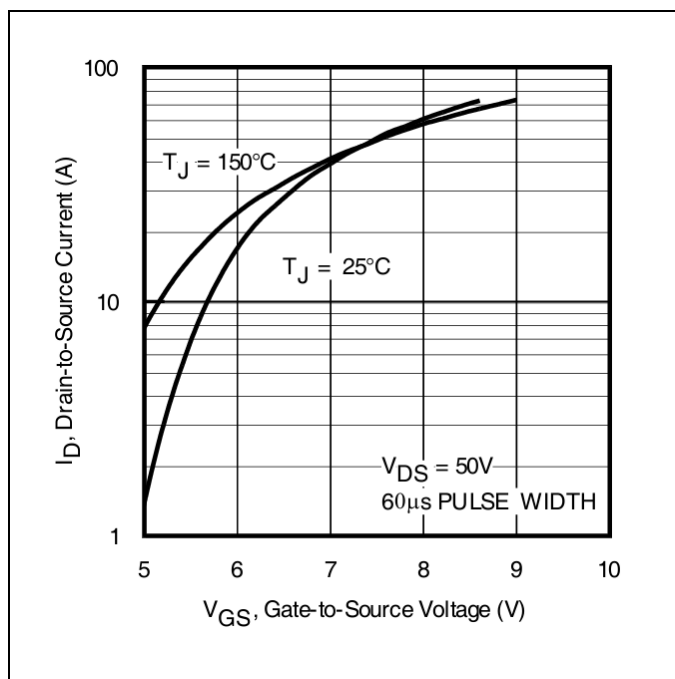


Figure 4 Typical Transfer Characteristics

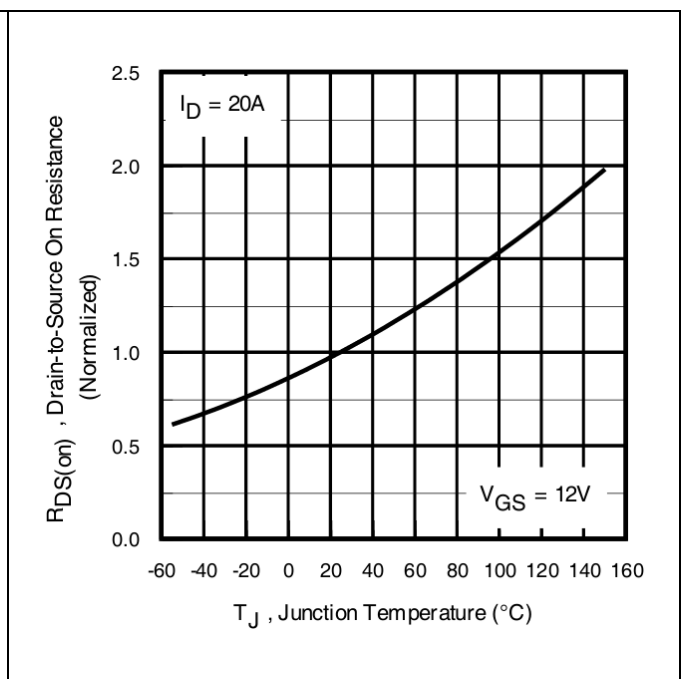


Figure 5 Normalized On-Resistance Vs. Temperature

IRHYS67130CM (JANSR2N7588T3)

Radiation Hardened Power MOSFET Thru-Hole (Low-Ohmic TO-257AA)

Electrical Characteristics Curves (Pre-irradiation)

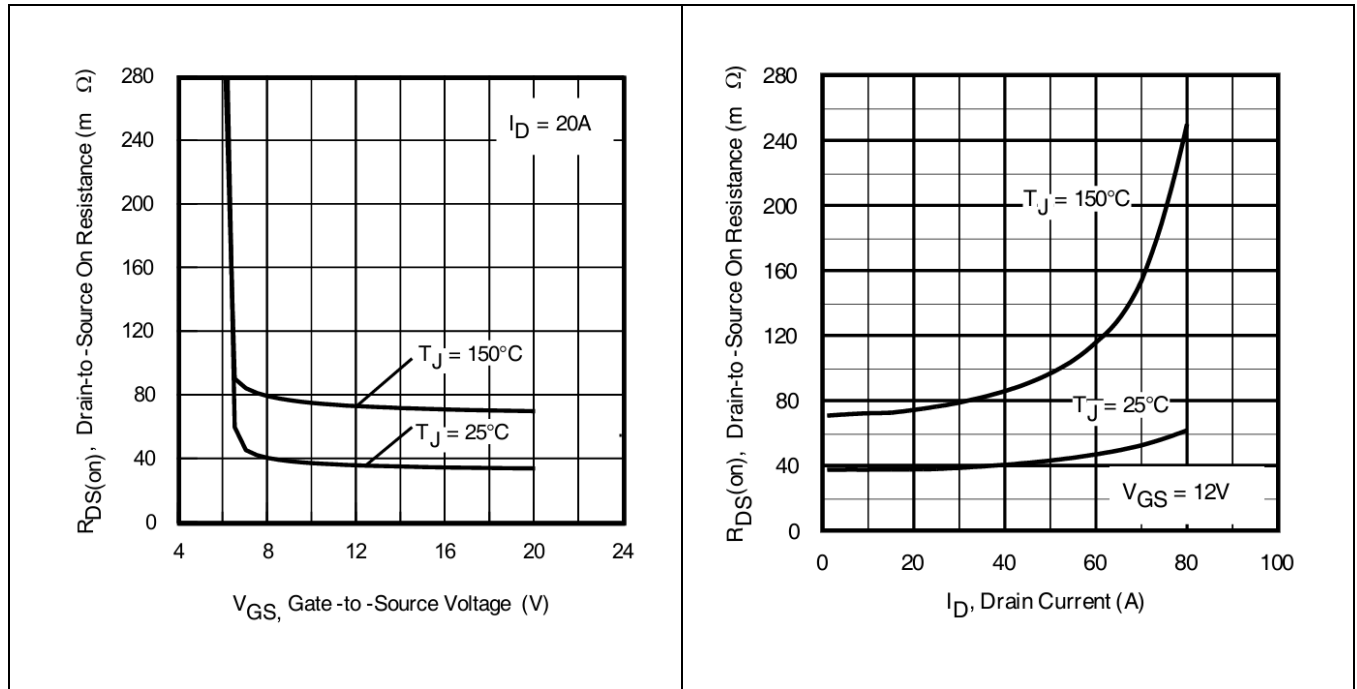


Figure 6 Typical On-Resistance Vs. Gate Voltage

Figure 7 Typical On-Resistance Vs. Drain Current

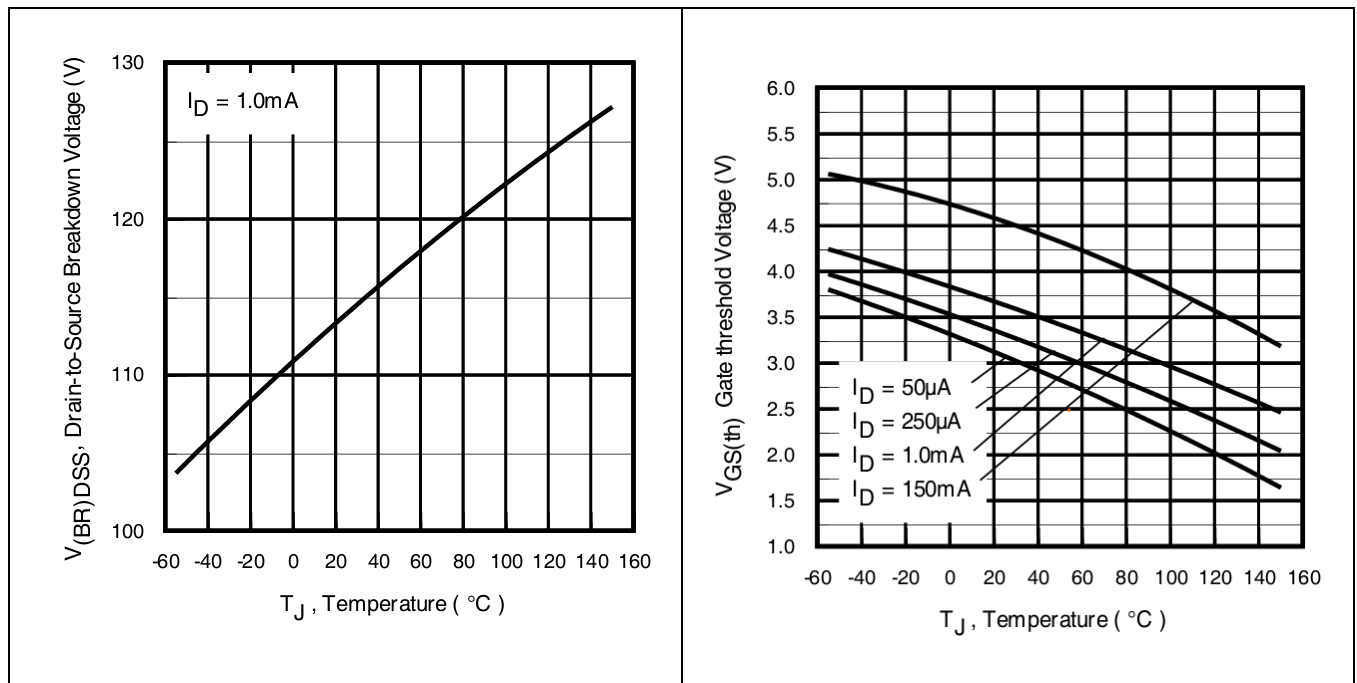


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

Figure 9 Typical Threshold Voltage Vs. Temperature

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Radiation Hardened Power MOSFET Thru-Hole (Low-Ohmic TO-257AA)

Electrical Characteristics Curves (Pre-irradiation)

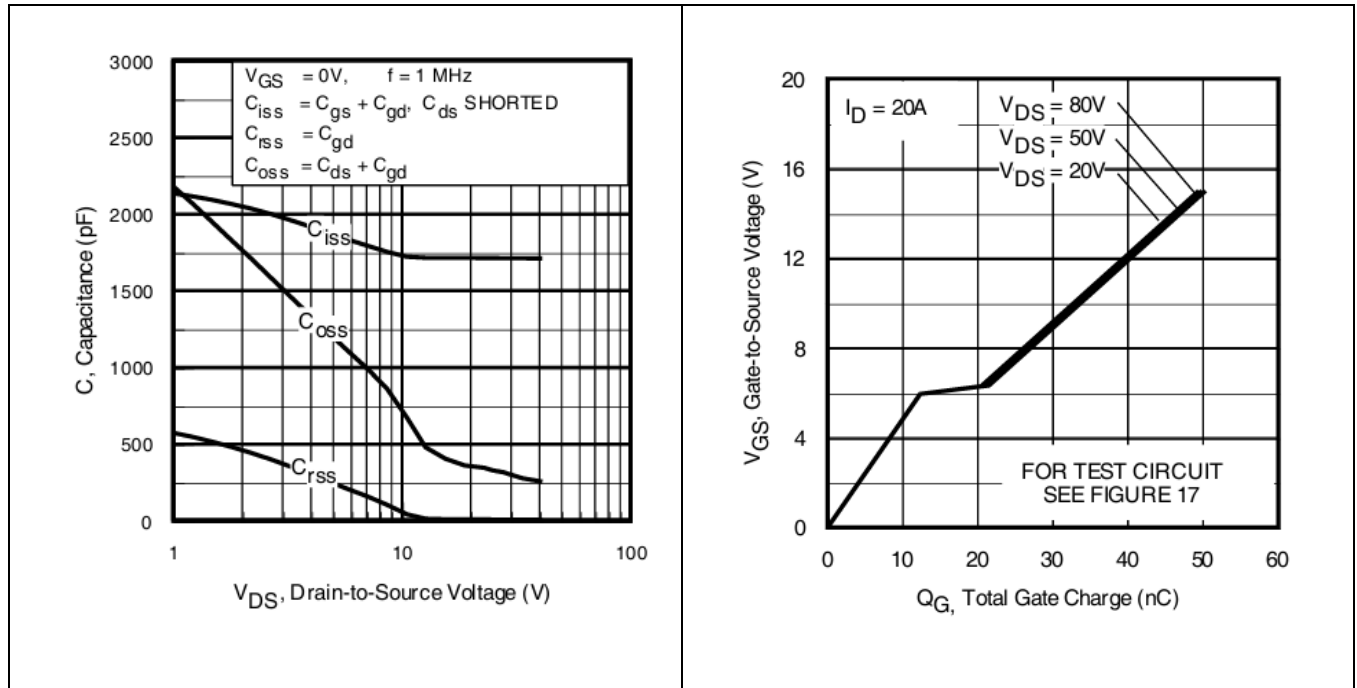


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

Figure 11 Typical Gate Charge Vs. Typical Gate-to-Source Voltage

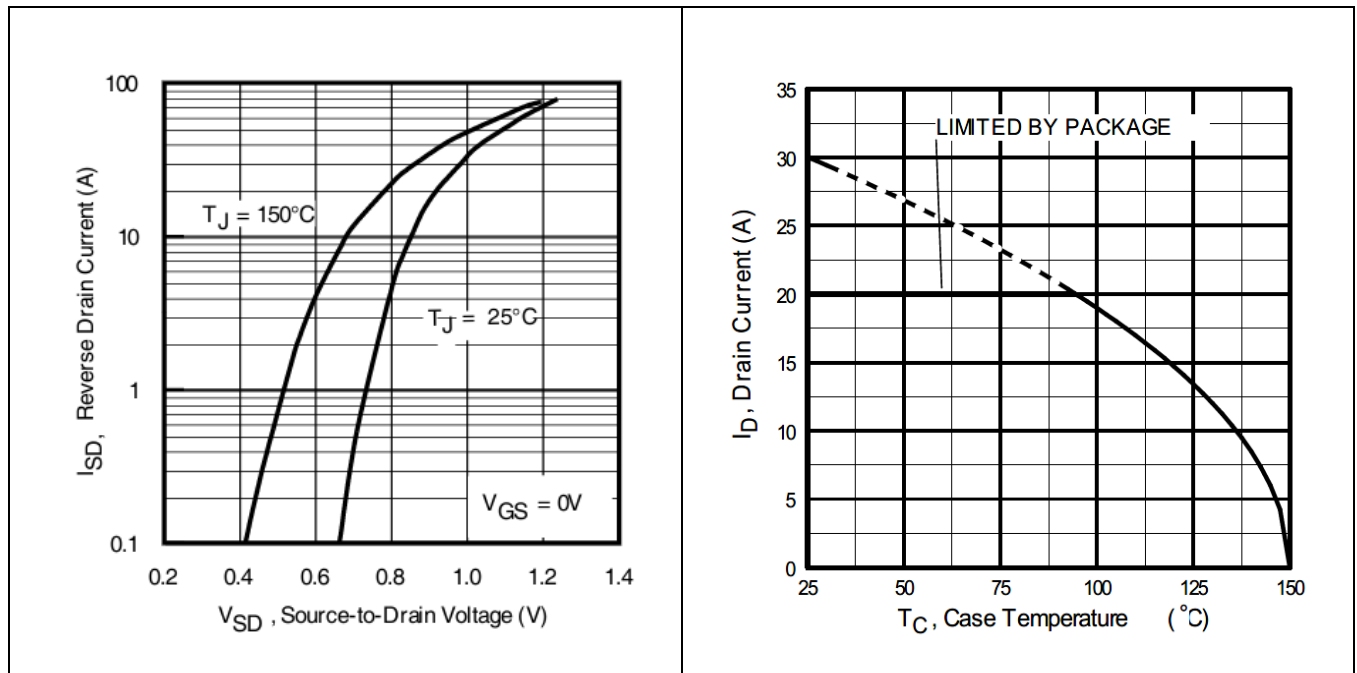


Figure 12 Typical Source-Drain Current Vs. Diode Forward Voltage

Figure 13 Maximum Drain Current Vs. Case Temperature

IRHYS67130CM (JANSR2N7588T3)

Radiation Hardened Power MOSFET Thru-Hole (Low-Ohmic TO-257AA)

Electrical Characteristics Curves (Pre-irradiation)

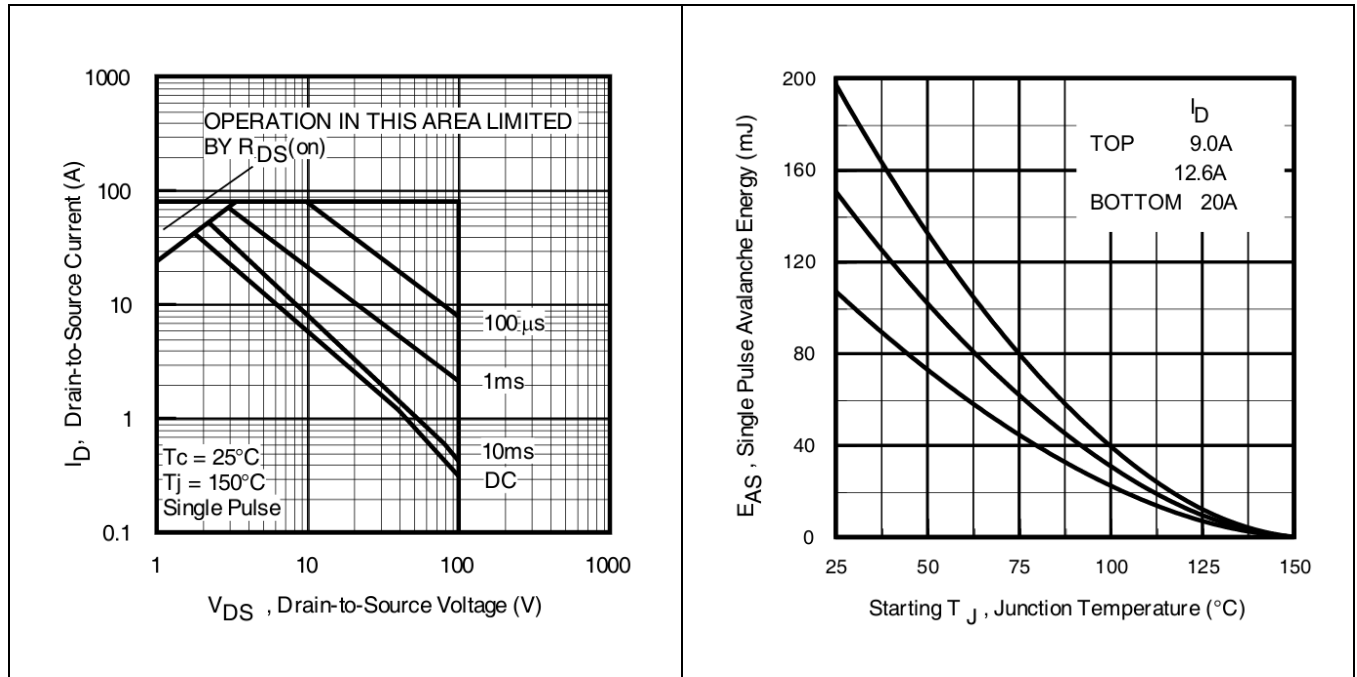


Figure 14 Maximum Safe Operating Area

Figure 15 Maximum Avalanche Energy Vs. Junction Temperature

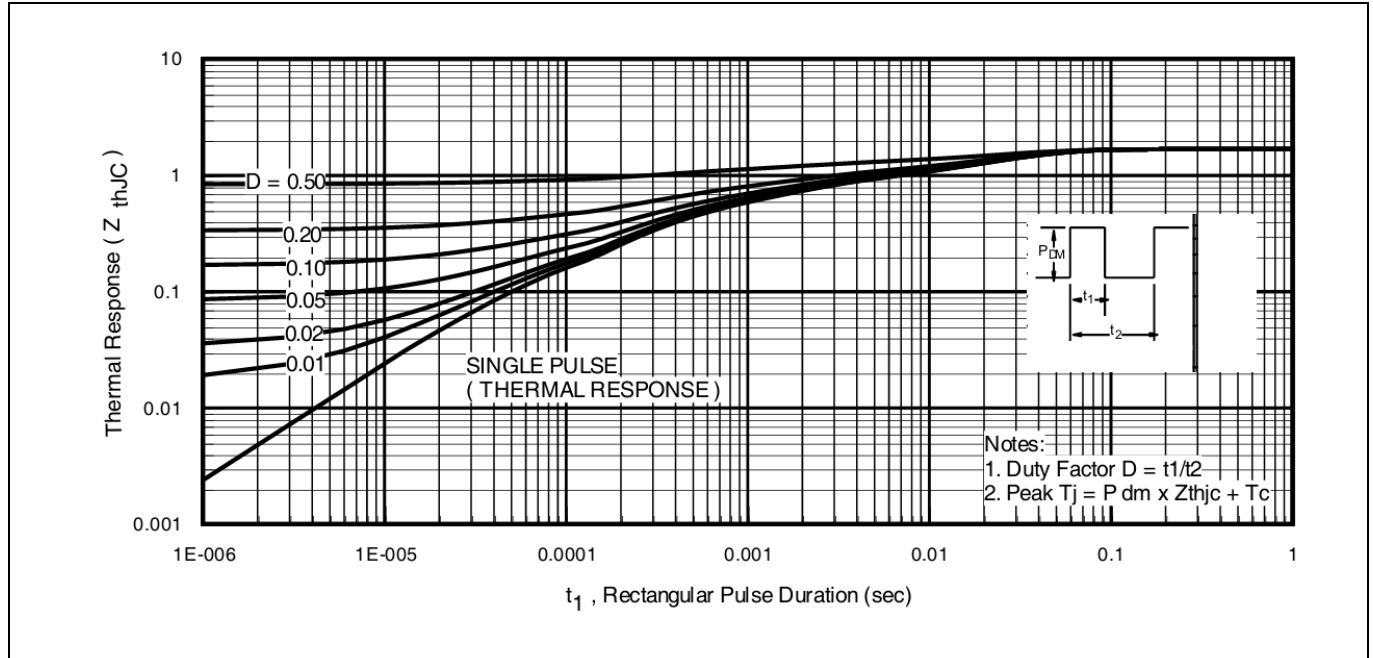


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRHYS67130CM (JANSR2N7588T3)

Radiation Hardened Power MOSFET Thru-Hole (Low-Ohmic TO-257AA)

Test Circuits (Pre-irradiation)

4 Test Circuits (Pre-irradiation)

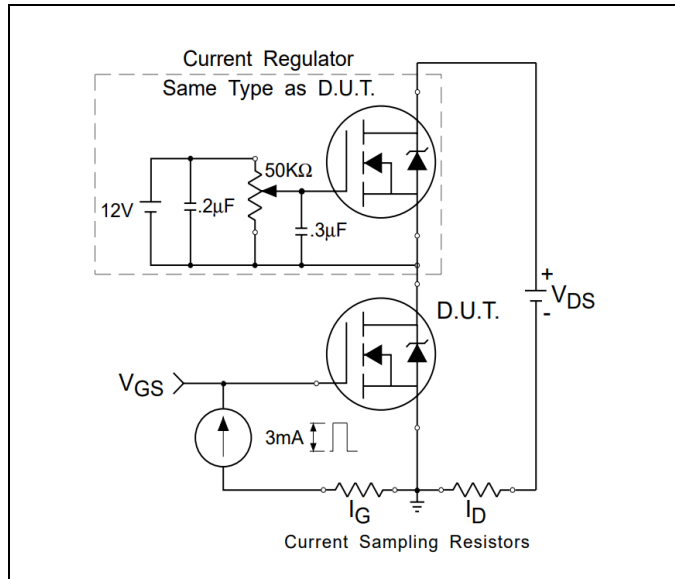


Figure 17 Gate Charge Test Circuit

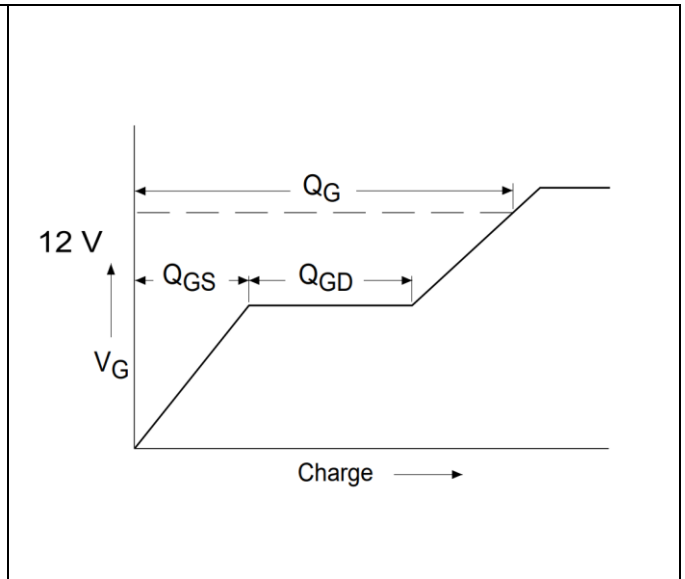


Figure 18 Gate Charge Waveform

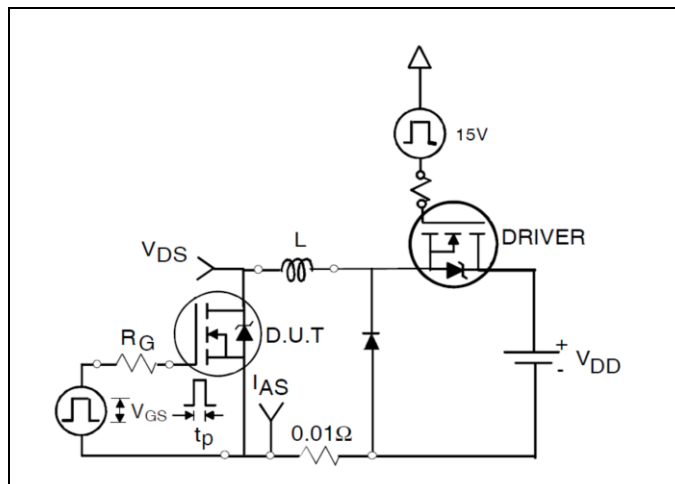


Figure 19 Unclamped Inductive Test Circuit

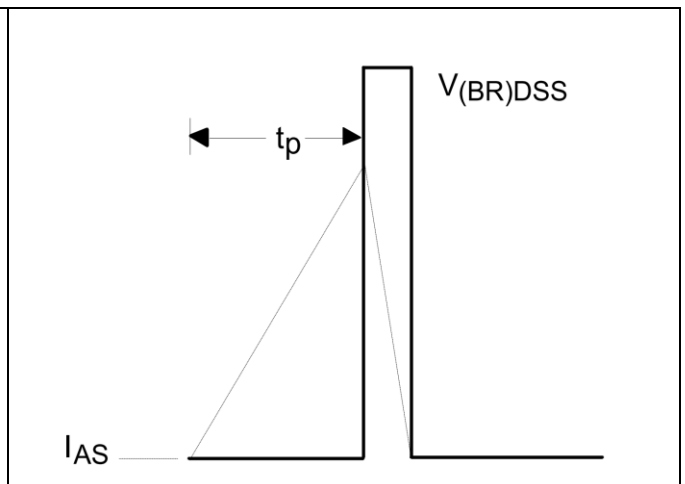


Figure 20 Unclamped Inductive Waveform

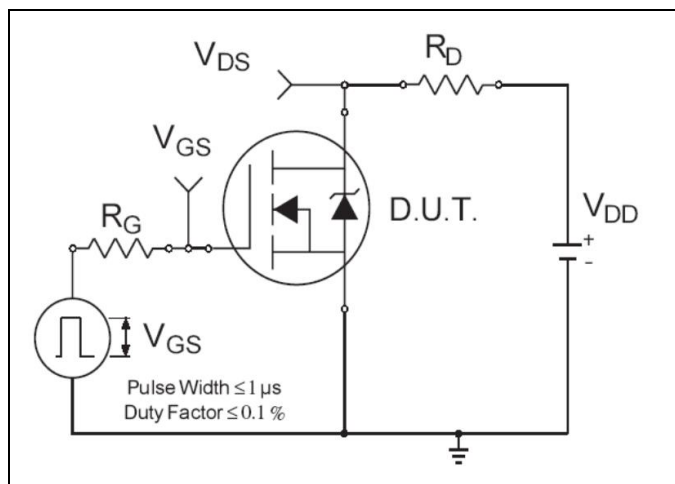


Figure 21 Switching Time Test Circuit

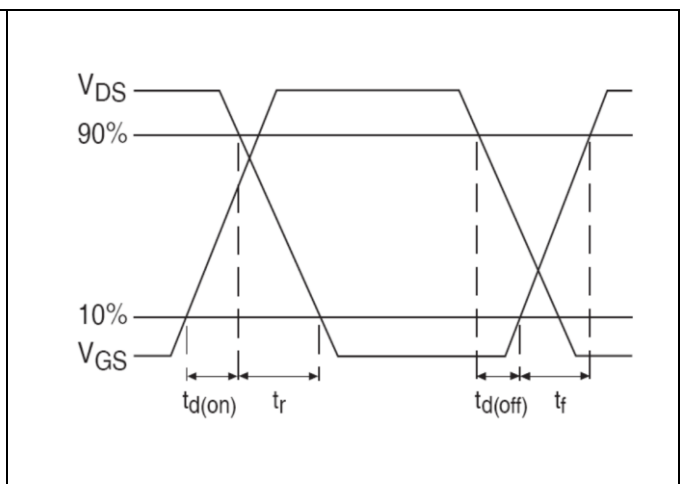
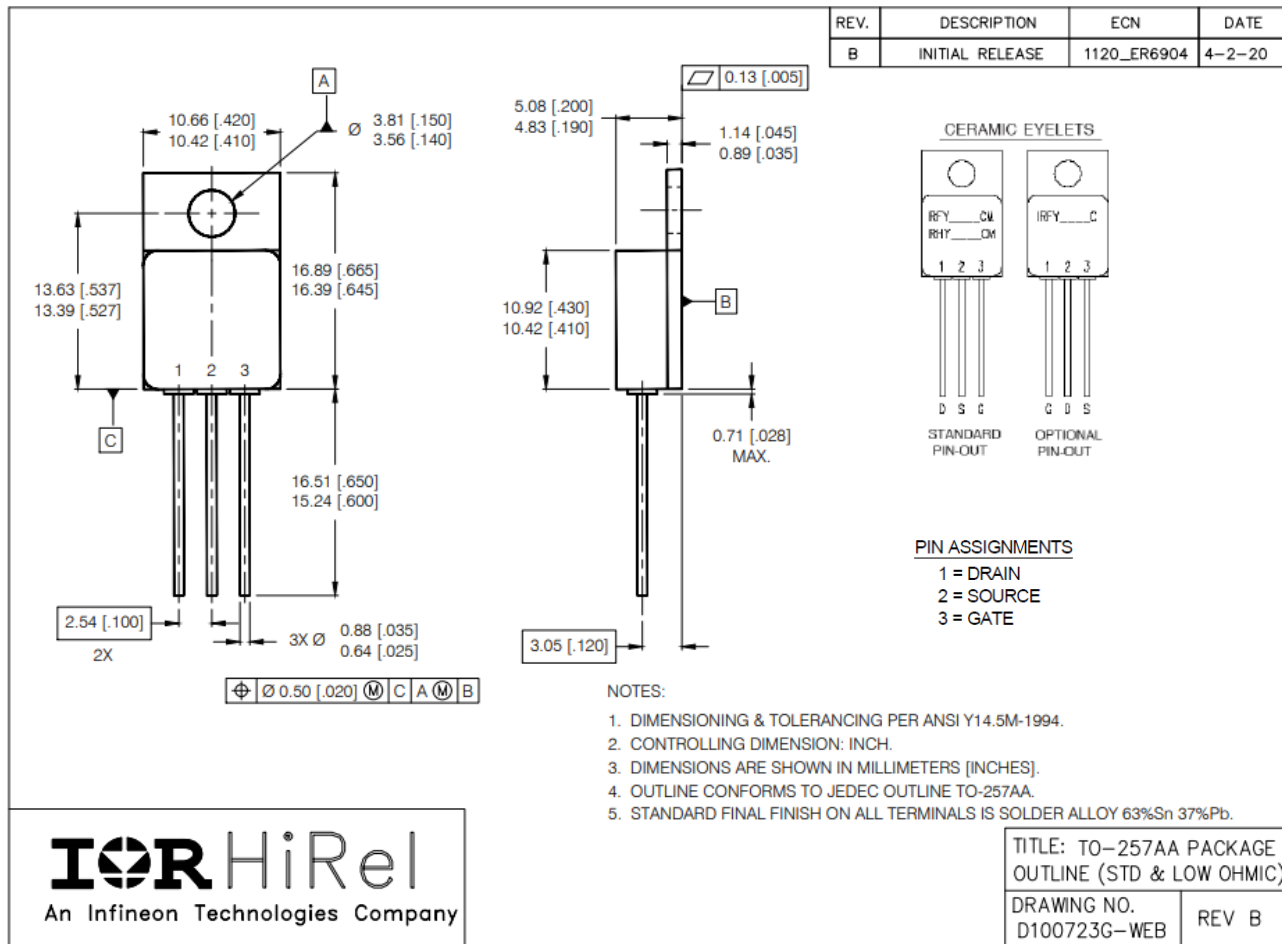


Figure 22 Switching Time Waveforms

Package Outline

5 Package Outline

Note: For the most updated package outline, please see the website: [Low-Ohmic TO-257AA](#)



BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

Revision history**Revision history**

Document version	Date of release	Description of changes
	03/08/2005	Datasheet (PD-96986)
Rev A	06/15/2010	Updated based on ECN-17282
Rev B	01/02/2018	Updated based on ECN-1120_05603
Rev C	12/10/2019	Updated based on ECN-1120_07627-3
Rev D	05/15/2023	Updated based on ECN-1120_09508
Rev E	08/03/2023	Updated based on ECN-1120_09603

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