IRHNA57260SE (JANSR2N7473U2)

PD-91839N

Radiation Hardened Power MOSFET
Surface Mount (SMD-2)
200V, 53.5A, N-channel, R5 Technology

Features

- Single event effect (SEE) hardened
- Low $R_{DS(on)}$
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Ceramic Package
- Light weight
- Surface Mount
- ESD rating: Class 3B per MIL-STD-750, Method 1020

Product Summary

- **BV_{DSS}:** 200V
- **I_D:** 53.5A
- **$R_{DS(on),max}$:** 38mΩ
- **$Q_{G,max}$:** 155nC
- **REF:** MIL-PRF-19500/684

SMD-2

Potential Applications

- DC-DC converter
- Motor drives
- Thermal management

Product Validation

Qualified to JANS screening flow according to MIL-PRF-19500 for space applications

Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV·cm^2/mg). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHNA57260SE	SMD-2	COTS	100 krad (Si)
JANSR2N7473U2	SMD-2	JANS	100 krad (Si)
IRHNA53260SE	SMD-2	COTS	300 krad (Si)
JANSF2N7473U2	SMD-2	JANS	300 krad (Si)

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	53.5	A
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	34	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	214	A
P_D @ T_C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	380	mJ
I_{AR}	Avalanche Current [1]	53.5	A
E_{AR}	Repetitive Avalanche Energy [1]	25	mJ
dv/dt	Peak Diode Reverse Recovery [3]	9.2	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5 sec)	
	Weight	3.3 (Typical)	g

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] V_{DD} = 50V, starting T_J = 25°C, L = 0.27mH, Peak I_L = 53.5A, V_{GS} = 12V

[3] $I_{SD} \leq$ 53.5A, di/dt ≤ 190A/µs, $V_{DD} \leq$ 200V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	38	mΩ	V_{GS} = 12V, I_{D2} = 34A [1]
$V_{GS(th)}$	Gate Threshold Voltage	2.5	—	4.5	V	V_{DS} = V_{GS}, I_D = 1.0mA
Gfs	Forward Transconductance	35	—	—	S	V_{DS} = 15V, I_{D2} = 34A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS} = 160V, V_{GS} = 0V
		—	—	25		V_{DS} = 160V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	155	nC	I_{D1} = 53.5A V_{DS} = 100V V_{GS} = 12V
Q_{GS}	Gate-to-Source Charge	—	—	45		
Q_{GD}	Gate-to-Drain (‘Miller’) Charge	—	—	75		
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	I_{D1} = 53.5A ** V_{DD} = 100V R_G = 2.35Ω V_{GS} = 12V
t_r	Rise Time	—	—	125		
$t_{d(off)}$	Turn-Off Delay Time	—	—	80		
t_f	Fall Time	—	—	50		
L_s +L_D	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	6044	—	pF	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	913	—		
C_{rss}	Reverse Transfer Capacitance	—	65	—		

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	53.5	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	214	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 53.5A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	—	450	ns	T_J = 25°C, I_F = 53.5A, V_{DD} ≤ 50V di/dt = 100A/µs
Q_{rr}	Reverse Recovery Charge	—	4.6	—	µC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	0.5	°C/W
$R_{\theta\text{-PCB}}$	Junction-to-PC Board (soldered to 1inch square cu clad board)	—	1.6	—	

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 300 krad (Si) [5]		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	—	10	µA	V_{DS} = 160V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) [2]	—	39	mΩ	V_{GS} = 12V, I_{D2} = 34A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-2) [2]	—	38	mΩ	V_{GS} = 12V, I_{D2} = 34A
V_{SD}	Diode Forward Voltage	—	1.2	V	V_{GS} = 0V, I_F = 53.5A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} = 12V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = 160V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[5] Part numbers IRHNA57260SE (JANSR2N7473U2) and IRHNA53260SE (JANSF2N7473U2)

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm²/mg)	Energy (MeV)	Range (µm)	V_{DS} (V)				
			V_{GS} = 0V	V_{GS} = -5V	V_{GS} = -10V	V_{GS} = -15V	V_{GS} = -20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	200	200	200	200	200
61 ± 5%	330 ± 7.5%	31 ± 10%	200	200	200	185	120
84 ± 5%	350 ± 10%	28 ± 7.5%	200	200	150	50	25

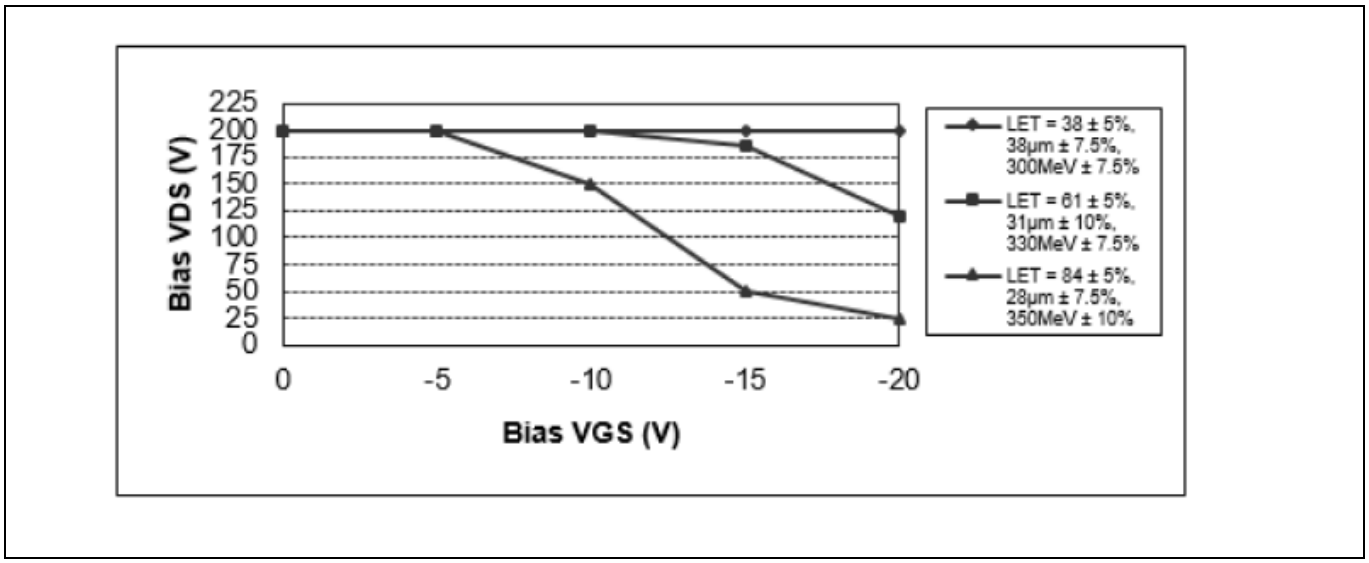


Figure 1 Typical Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

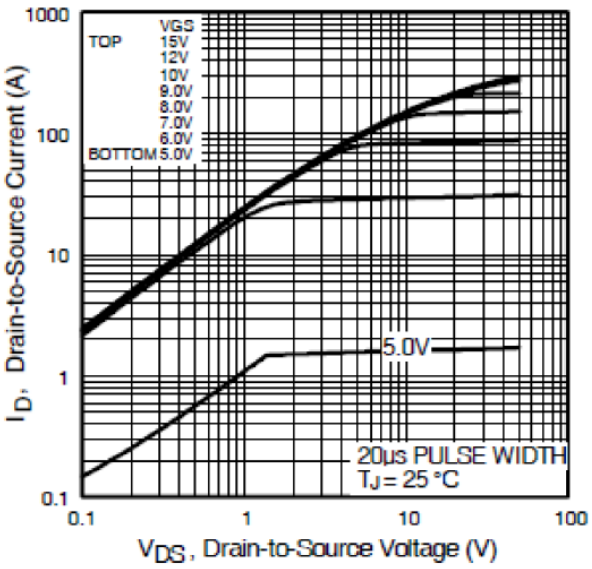


Figure 2 Typical Output Characteristics

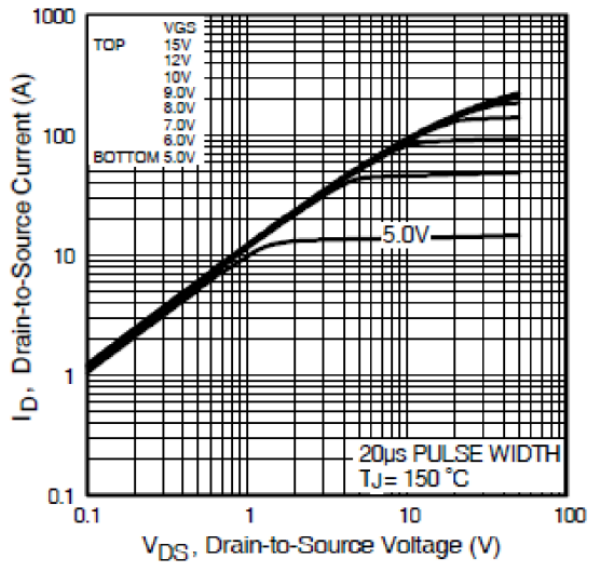


Figure 3 Typical Output Characteristics

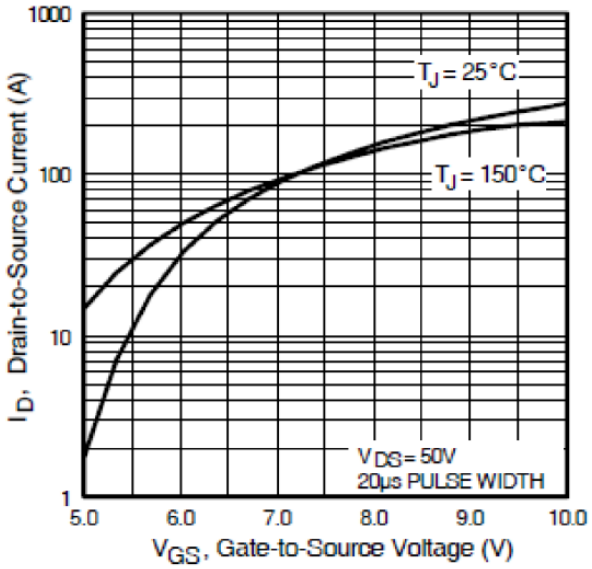


Figure 4 Typical Transfer Characteristics

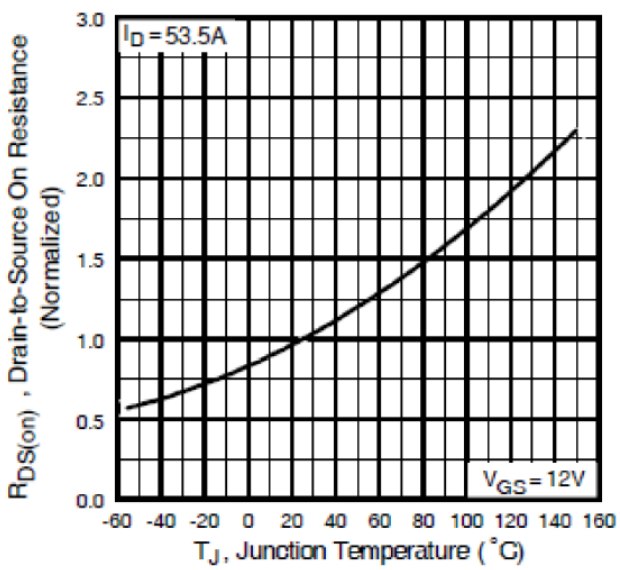


Figure 5 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

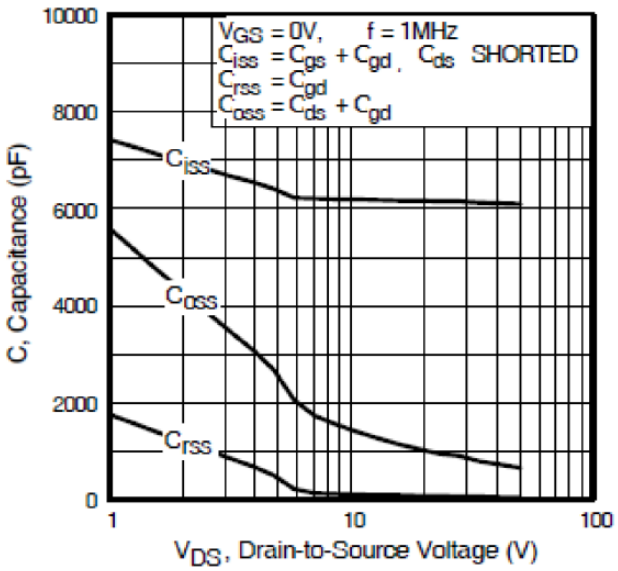


Figure 6 Typical Capacitance Vs. Drain-to-Source Voltage

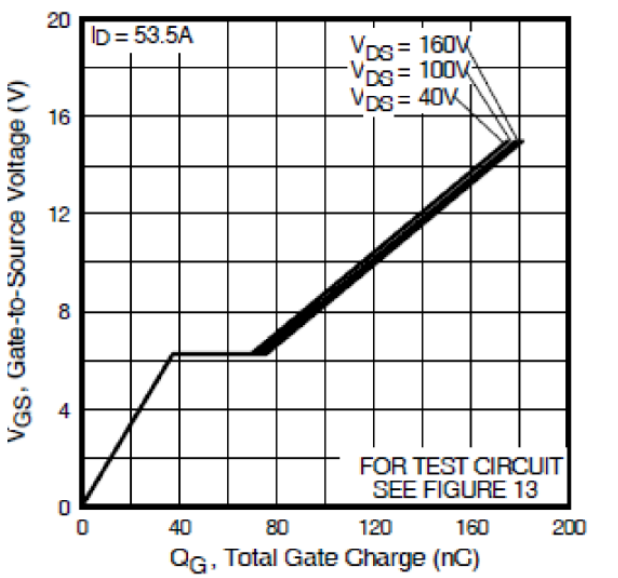


Figure 7 Typical Gate-to-Source Voltage Vs. Typical Gate Charge

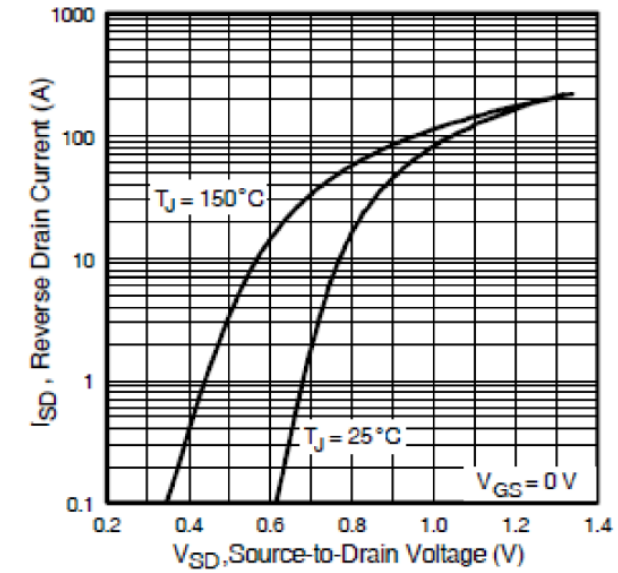


Figure 8 Typical Source-Drain Current Vs. Diode Forward Voltage

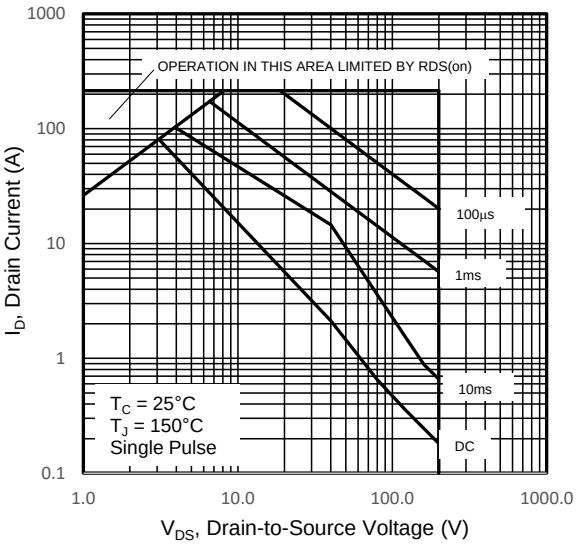


Figure 9 Maximum Safe Operating Area

Electrical Characteristics Curves (Pre-irradiation)

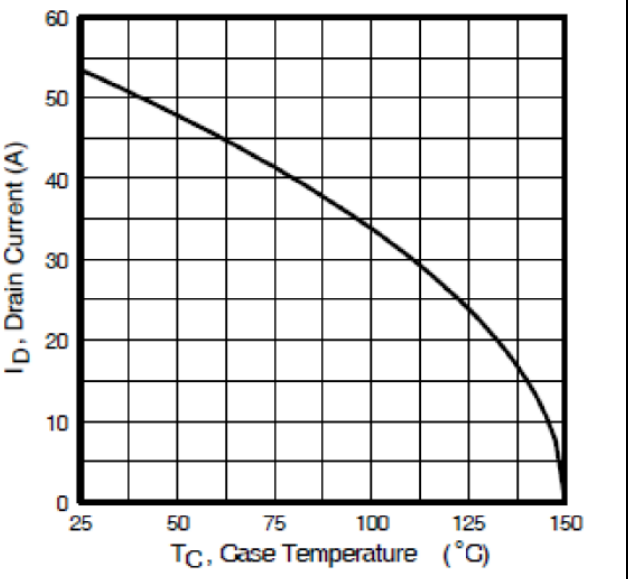


Figure 10 Maximum Drain Current Vs. Case Temperature

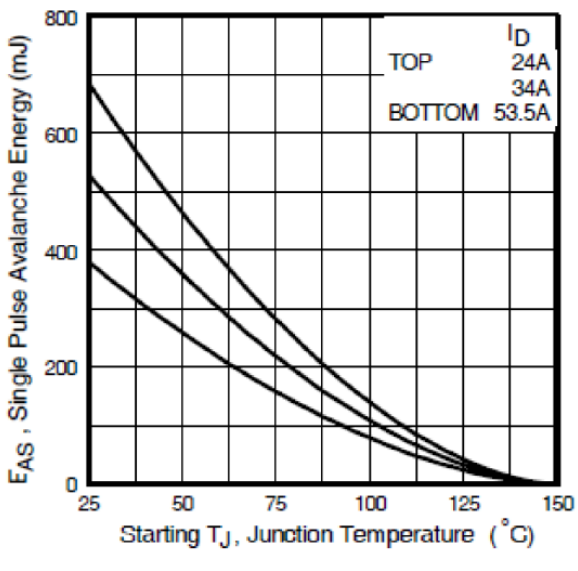


Figure 11 Maximum Avalanche Energy Vs. Junction Temperature

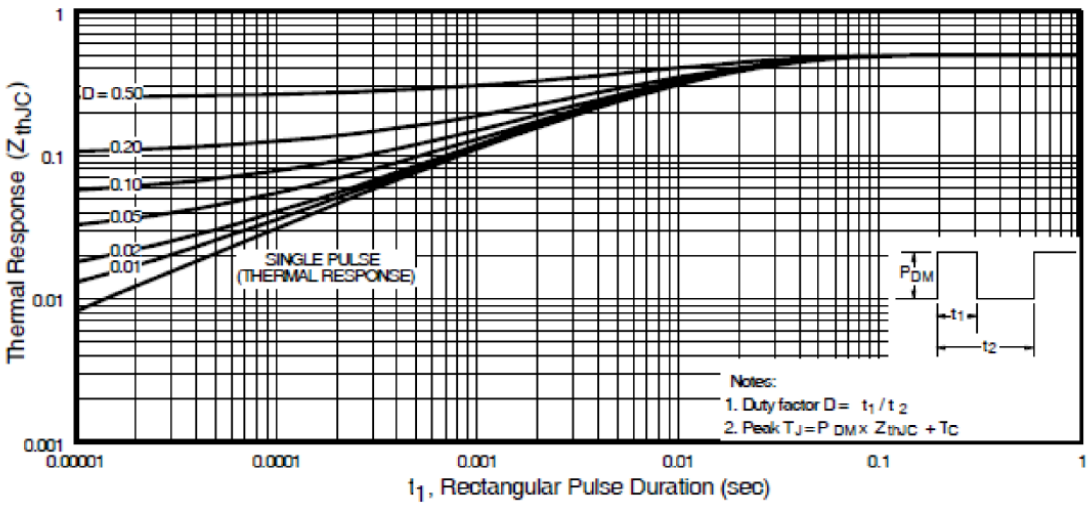


Figure 12 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

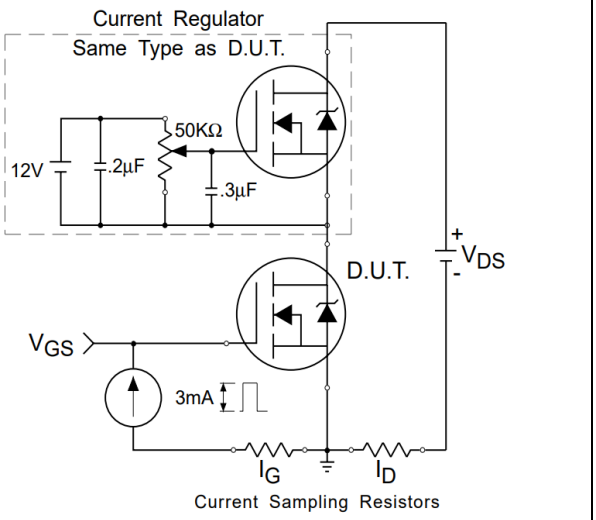


Figure 13 Gate Charge Test Circuit

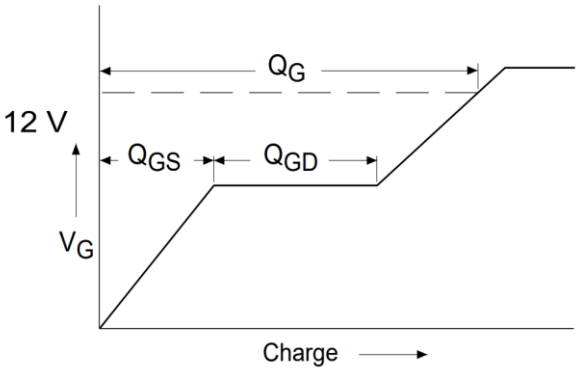


Figure 14 Gate Charge Waveform

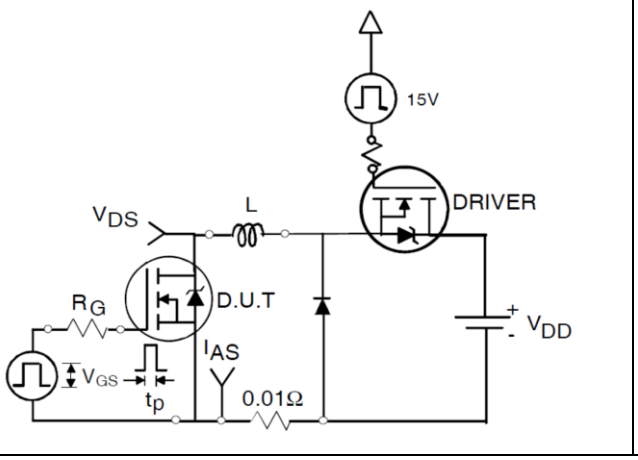


Figure 15 Unclamped Inductive Test Circuit

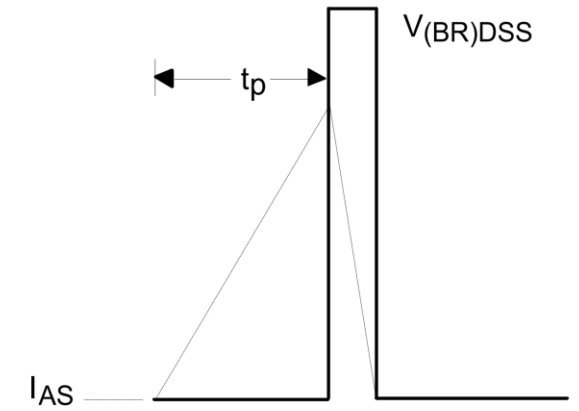


Figure 16 Unclamped Inductive Waveform

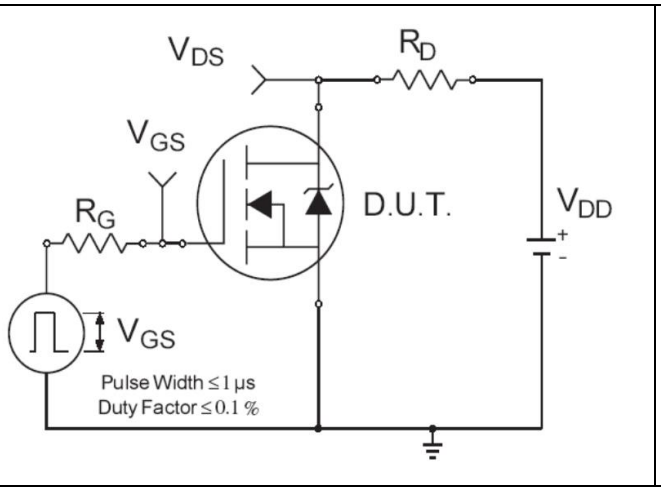


Figure 17 Switching Time Test Circuit

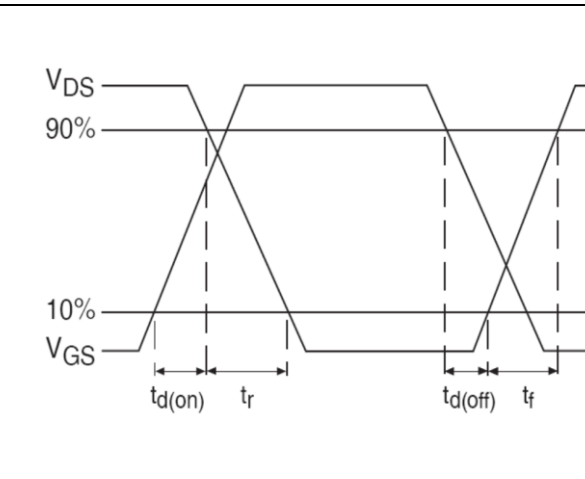
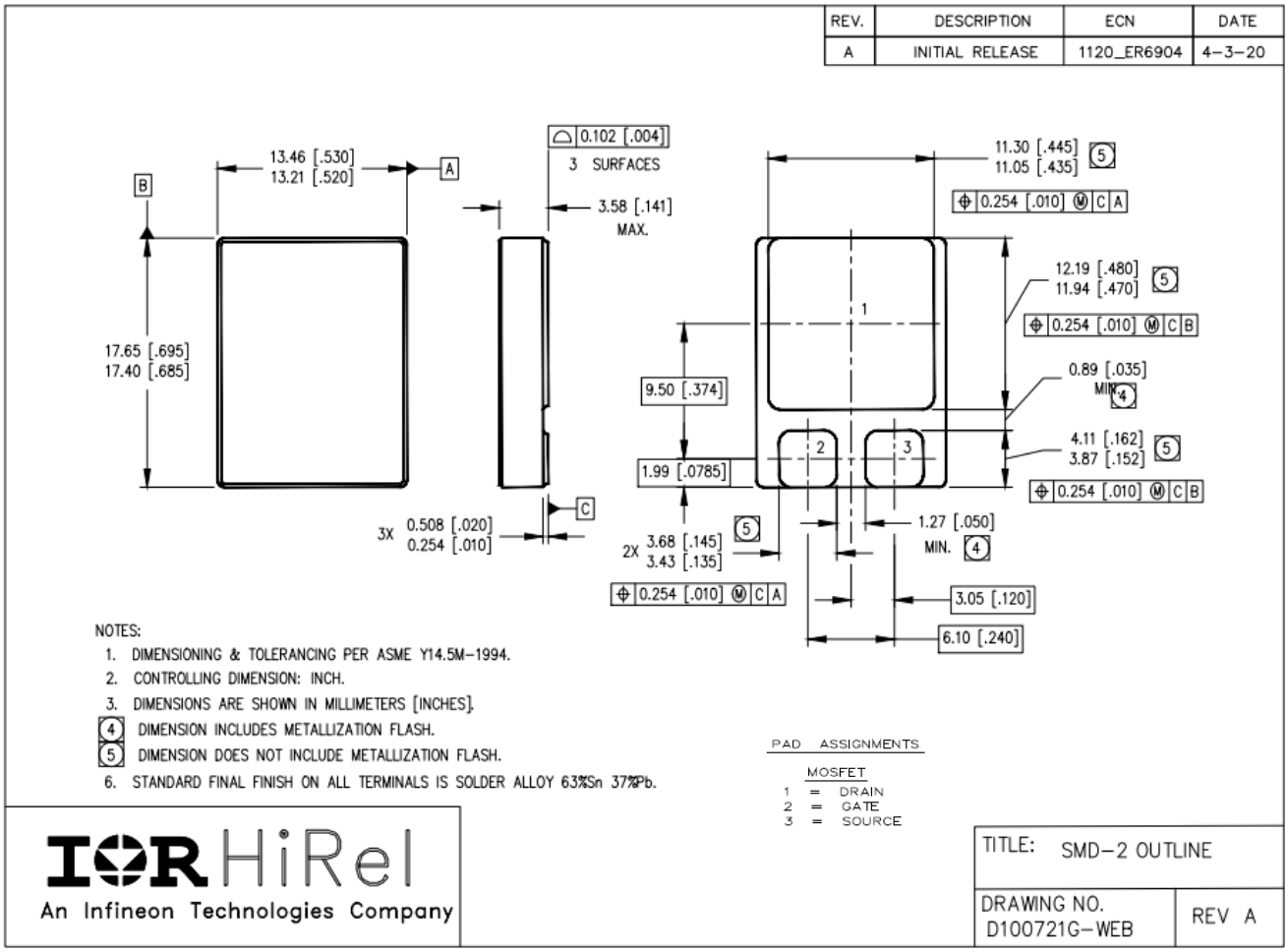


Figure 18 Switching Time Waveforms

5 Package Outline

Note: For the most updated package outline, please see the website: SMD-2



Revision history

Document version	Date of release	Description of changes
	10/26/1998	Datasheet (PD-91839)
Rev A	07/07/1999	Updated new format
Rev B	07/12/1999	Updated ID for Gatechrge, Switch time, Trr/Qrr
Rev C	11/19/1999	Updated format
Rev D	12/16/1999	Updated Rdson
Rev E	04/10/2000	Updated case outline
Rev F	08/21/2001	Updated switch time test condition
Rev G	05/22/2002	Updated Rdson Max
Rev H	09/10/2003	Added QPL part number
Rev I	05/19/2004	Updated SOA curve
Rev J	04/25/2006	Updated based on ECN-13968
Rev K	09/12/2007	Updated based on ECN-15354
Rev L	11/12/2020	Updated based on ECN-1120_08235
Rev M	01/04/2023	Updated based on ECN-1120_09361
Rev N	12/20/2023	Updated based on ECN-1120_09778

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