

ESP32-S2-SOLO-2

ESP32-S2-SOLO-2U

Datasheet

2.4 GHz Wi-Fi (802.11 b/g/n) module

Built around ESP32-S2 series of SoC, Xtensa® single-core 32-bit LX7 microprocessor

Flash up to 16 MB, optional 2 MB PSRAM in chip package

36 GPIOs, rich set of peripherals

On-board PCB antenna or external antenna connector



Version 0.1
Espressif Systems
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1 Module Overview

1.1 Features

CPU and On-Chip Memory

- ESP32-S2 or ESP32-S2R2 embedded, Xtensa® single-core 32-bit LX7 microprocessor, up to 240 MHz
- 128 KB ROM
- 320 KB SRAM
- 16 KB SRAM in RTC
- 2 MB embedded PSRAM (ESP32-S2R2 only)

Wi-Fi

- 802.11 b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μ s guard interval support
- Operating frequency: 2412 ~ 2484 MHz

Peripherals

- GPIO, SPI, LCD, UART, I2C, I2S, Camera interface, IR, pulse counter, LED PWM, TWAI®

(compatible with ISO 11898-1, i.e. CAN Specification 2.0), full-speed USB OTG, ADC, DAC, touch sensor, temperature sensor

Integrated Components on Module

- 40 MHz crystal oscillator
- 4 MB SPI flash

Antenna Options

- On-board PCB antenna (ESP32-S2-SOLO-2)
- External antenna via a connector (ESP32-S2-SOLO-2U)

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature:
 - 85 °C version: -40 ~ 85 °C
 - 105 °C version: -40 ~ 105 °C (ESP32-S2-SOLO-2-H4) and ESP32-S2-SOLO-2-U-H4 only)

1.2 Description

ESP32-S2-SOLO-2 and ESP32-S2-SOLO-2U are two powerful, generic Wi-Fi MCU modules that have a rich set of peripherals. They are an ideal choice for a wide variety of application scenarios relating to Internet of Things (IoT), wearable electronics and smart home.

The ordering information is as follows:

Table 1: Ordering Information

Module	Ordering Code	Chip Embedded	Flash	Module Dimensions (mm)
ESP32-S2-SOLO-2 (ANT)	ESP32-S2-SOLO-2-N4 (85 °C version)	ESP32-S2	4 MB	18.0 x 25.5 x 3.1
	ESP32-S2-SOLO-2-H4 (105 °C version)			
	ESP32-S2-SOLO-2-N4R2 (85 °C version)	ESP32-S2R2		
ESP32-S2-SOLO-2U (CONN)	ESP32-S2-SOLO-2U-N4 (85 °C version)	ESP32-S2	4 MB	18.0 x 19.2 x 3.2
	ESP32-S2-SOLO-2U-H4(105 °C version)			
	ESP32-S2-SOLO-2U-N4R2 (85 °C version)	ESP32-S2R2		

¹ These modules can be shipped with different flash sizes.

² 105 °C version modules can integrate the ESP32-S2 chip and 4 MB flash only.

ESP32-S2-SOLO-2 comes with an on-board PCB antenna (ANT), and ESP32-S2-SOLO-2U with an external antenna connector (CONN). Both ESP32-S2-SOLO-2 and ESP32-S2-SOLO-2U have three variants:

- integrating the ESP32-S2 chip (which has no embedded flash and PSRAM), and a flash that operates at -40 ~ 85 °C
- integrating the ESP32-S2 chip (which has no embedded flash and PSRAM), and a flash that operates at -40 ~ 105 °C
- integrating the ESP32-S2R2 chip (which is embedded with a 2 MB PSRAM) , and a flash that operates at -40 ~ 85 °C

The three variants differ in the chip integrated and the ambient operating temperature. In this datasheet unless otherwise stated, ESP32-S2-SOLO-2 refers to all variants of ESP32-S2-SOLO-2, whereas ESP32-S2-SOLO-2U refers to all variants of ESP32-S2-SOLO-2U.

The ESP32-S2 chip and the ESP32-S2R2 chip falls into the same category, namely ESP32-S2 series. ESP32-S2 series of chips has an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. It has a low-power co-processor that can be used instead of the CPU to save power while performing tasks that do not require much computing power, such as monitoring of peripherals.

ESP32-S2 integrates a rich set of peripherals, ranging from SPI, I2S, UART, I2C, LED PWM, TWAI®, LCD, Camera interface, ADC, DAC, touch sensor, temperature sensor, as well as up to 43 GPIOs. It also includes a full-speed USB On-The-Go (OTG) interface to enable USB communication.

The ESP32-S2 chip and the ESP32-S2R2 chip vary only in whether a PSRAM is embedded. For details, please refer to Section *ESP32-S2 Series Comparison* in [ESP32-S2 Series Datasheet](#).

1.3 Applications

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- USB Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
- Smart Home Control Panel

- Smart Building
- Industrial Automation
- Smart Agriculture
- Audio Applications
- Health Care Applications
- Wi-Fi-enabled Toys
- Wearable Electronics
- Retail & Catering Applications
- Smart POS Machines

PRELIMINARY

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2 Block Diagram

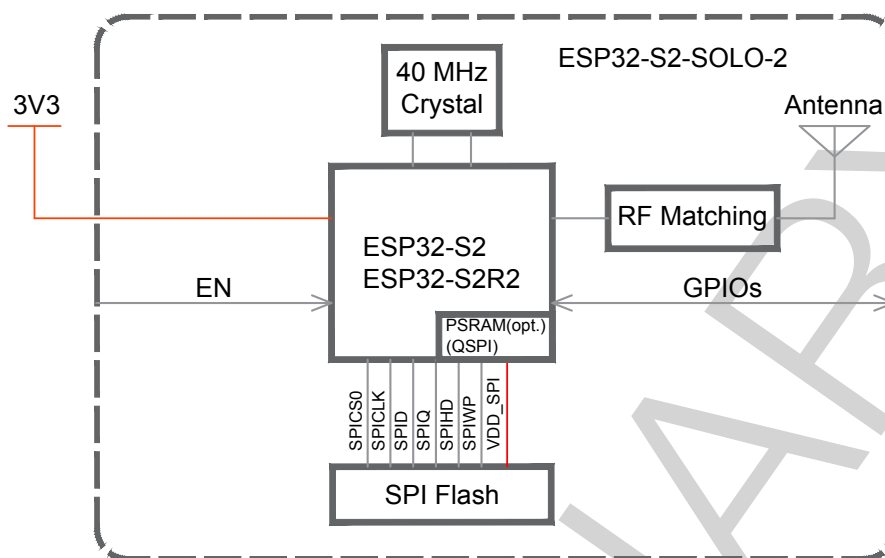


Figure 1: ESP32-S2-SOLO-2 Block Diagram

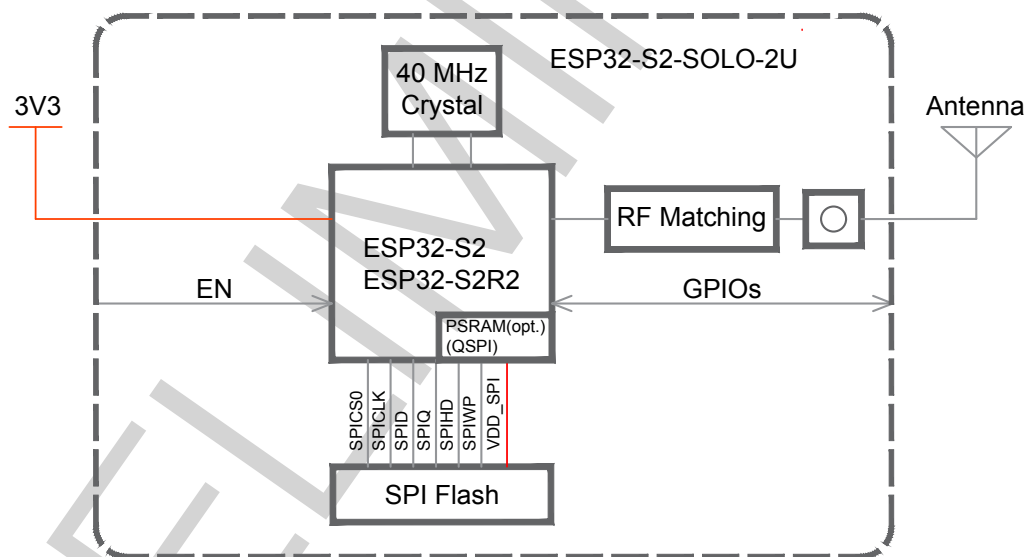


Figure 2: ESP32-S2-SOLO-2U Block Diagram

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 7.1 *Physical Dimensions*.

The pin layout is applicable for ESP32-S2-SOLO-2 and ESP32-S2-SOLO-2U, but the latter has no keepout zone.

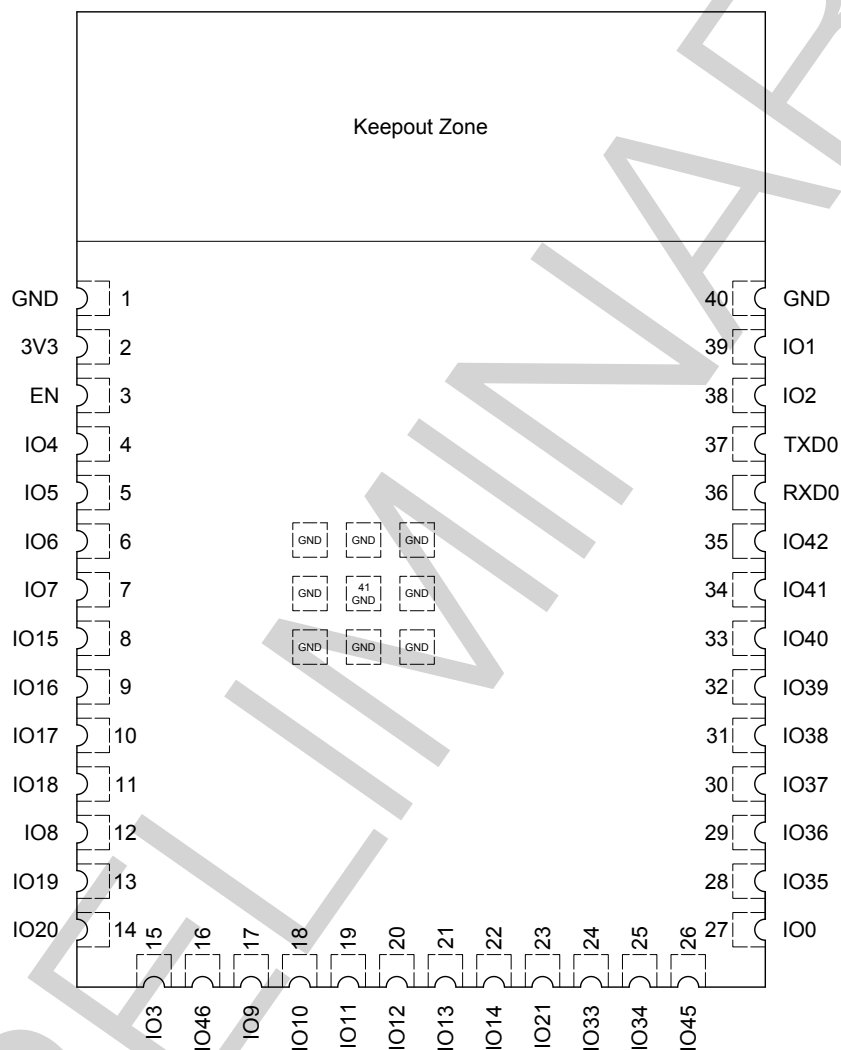


Figure 3: Pin Layout (Top View)

3.2 Pin Description

The module has 41 pins. See pin definitions in Table 2.

For peripheral pin configurations, please refer to [ESP32-S2 Series Datasheet](#).

Table 2: Pin Definitions

Name	No.	Type ¹	Function
GND	1	P	Ground
3V3	2	P	Power supply
EN	3	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO4	4	I/O/T	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
IO5	5	I/O/T	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
IO6	6	I/O/T	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
IO7	7	I/O/T	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
IO15	8	I/O/T	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
IO16	9	I/O/T	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
IO17	10	I/O/T	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6, DAC_1
IO18	11	I/O/T	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, DAC_2, CLK_OUT3
IO8	12	I/O/T	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7
IO19	13	I/O/T	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
IO20	14	I/O/T	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
IO3	15	I/O/T	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
IO46	16	I	GPIO46
IO9	17	I/O/T	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPIHD
IO10	18	I/O/T	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4
IO11	19	I/O/T	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID, FSPIIO5
IO12	20	I/O/T	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6
IO13	21	I/O/T	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7
IO14	22	I/O/T	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS
IO21	23	I/O/T	RTC_GPIO21, GPIO21
IO33	24	I/O/T	SPIIO4, GPIO33, FSPIHD
IO34	25	I/O/T	SPIIO5, GPIO34, FSPICS0
IO45	26	I/O/T	GPIO45
IO0	27	I/O/T	RTC_GPIO0, GPIO0
IO35	28	I/O/T	SPIIO6, GPIO35, FSPID
IO36	29	I/O/T	SPIIO7, GPIO36, FSPICLK
IO37	30	I/O/T	SPIDQS, GPIO37, FSPIQ
IO38	31	I/O/T	GPIO38, FSPIWP
IO39	32	I/O/T	MTCK, GPIO39, CLK_OUT3
IO40	33	I/O/T	MTDO, GPIO40, CLK_OUT2
IO41	34	I/O/T	MTDI, GPIO41, CLK_OUT1
IO42	35	I/O/T	MTMS, GPIO42
RXD0	36	I/O/T	U0RXD, GPIO44, CLK_OUT2
TXD0	37	I/O/T	U0TXD, GPIO43, CLK_OUT1
IO2	38	I/O/T	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
IO1	39	I/O/T	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0

Cont'd on next page

Table 2 – cont'd from previous page

Name	No.	Type ¹	Function
GND	40	P	Ground
EPAD	41	P	Ground

¹ P: power supply; I: input; O: output; T: high impedance.

3.3 Strapping Pins

Note:

The content below is excerpted from Section Strapping Pins in [ESP32-S2 Series Datasheet](#). For the strapping pin mapping between the chip and modules, please refer to Chapter 5 [Module Schematics](#).

ESP32-S2 has three strapping pins:

- GPIO0
- GPIO45
- GPIO46

Software can read the values of corresponding bits from register "GPIO_STRAPPING".

During the chip's system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

GPIO0, GPIO45 and GPIO46 are connected to the chip's internal weak pull-up/pull-down during the chip reset. Consequently, if they are unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of these strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-S2.

After reset, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed boot-mode configuration of the strapping pins.

Table 3: Strapping Pins

VDD_SPI Voltage ^{1 2}			
Pin	Default	3.3 V	1.8 V
GPIO45	Pull-down	0	1
Bootling Mode ³			
Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0
GPIO46	Pull-down	Don't-care	0
Enabling/Disabling ROM Messages Print During Bootling ^{4 5}			
Pin	Default	Enabled	Disabled
GPIO46	Pull-down	See note 5	See note 5

Note:

1. The functionality of strapping pin GPIO45 to select VDD_SPI voltage may be disabled by setting VDD_SPI_FORCE eFuse to 1. In such a case the voltage is selected with eFuse bit VDD_SPI_TIEH.
2. Since ESP32-S2FH2, ESP32-S2FH4, ESP32-S2FN4R2, and ESP32-S2R2 come with both/either 3.3 V SPI flash and/or PSRAM, VDD_SPI must be configured to 3.3 V.
3. The strapping combination of GPIO46 = 1 and GPIO0 = 0 is invalid and will trigger unexpected behavior.
4. ROM code can be printed over U0TXD (by default) or DAC_1, depending on the eFuse bit.
5. When eFuse UART_PRINT_CONTROL value is:
 - 0, print is normal during boot and not controlled by GPIO46.
 - 1 and GPIO46 is 0, print is normal during boot; but if GPIO46 is 1, print is disabled.
 - 2 and GPIO46 is 0, print is disabled; but if GPIO46 is 1, print is normal.
 - 3, print is disabled and not controlled by GPIO46.

4 Electrical Characteristics

The values presented in this section are preliminary and may change with the final release of this datasheet.

4.1 Absolute Maximum Ratings

Stresses above those listed in *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	−0.3	3.6	V
T _{STORE}	Storage temperature	−40	105	°C

4.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I _{VDD}	Current delivered by external power supply	0.5	—	—	A
T _A	Operating ambient temperature	85 °C version 105 °C version	−40	— 85 105	°C

4.3 DC Characteristics (3.3 V, 25 °C)

Table 6: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C _{IN}	Pin capacitance	—	2	—	pF
V _{IH}	High-level input voltage	0.75 × VDD ¹	—	VDD ¹ + 0.3	V
V _{IL}	Low-level input voltage	−0.3	—	0.25 × VDD ¹	V
I _{IH}	High-level input current	—	—	50	nA
I _{IL}	Low-level input current	—	—	50	nA
V _{OH} ²	High-level output voltage	0.8 × VDD ¹	—	—	V
V _{OL} ²	Low-level output voltage	—	—	0.1 × VDD ¹	V
I _{OH}	High-level source current (VDD ¹ = 3.3 V, V _{OH} ≥ 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I _{OL}	Low-level sink current (VDD ¹ = 3.3 V, V _{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R _{PU}	Pull-up resistor	—	45	—	kΩ
R _{PD}	Pull-down resistor	—	45	—	kΩ

V_{IH_nRST}	Chip reset release voltage	$0.75 \times VDD^1$	—	$VDD^1 + 0.3$	V
V_{IL_nRST}	Chip reset voltage	-0.3	—	$0.25 \times VDD^1$	V

¹ VDD is the I/O voltage for pins of a particular power domain.

² V_{OH} and V_{OL} are measured using high-impedance load.

4.4 Wi-Fi Radio

4.4.1 Wi-Fi RF Standards

Table 7: Wi-Fi RF Standards

Name		Description
Center frequency range of operating channel ¹		2412 ~ 2484 MHz
Wi-Fi wireless standard		IEEE 802.11b/g/n
Data rate	20 MHz	802.11b: 1, 2, 5.5 and 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n: MCS0-7, 72.2 Mbps (Max)
	40 MHz	802.11n: MCS0-7, 150 Mbps (Max)
Antenna type		PCB antenna, external antenna connector

¹ Device should operate in the center frequency range allocated by regional regulatory authorities. Target center frequency range is configurable by software.

² For the modules that use external antenna connectors, the output impedance is 50 Ω . For other modules without external antenna connectors, the output impedance is irrelevant.

4.4.2 Wi-Fi RF Transmitter (TX) Specifications

Target TX power is configurable based on device or certification requirements. The default characteristics are provided in Table 8.

Table 8: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	19.5	—
802.11b, 11 Mbps	—	19.5	—
802.11g, 6 Mbps	—	18.0	—
802.11g, 54 Mbps	—	18.0	—
802.11n, HT20, MCS0	—	18.0	—
802.11n, HT20, MCS7	—	17.0	—
802.11n, HT40, MCS0	—	18.0	—
802.11n, HT40, MCS7	—	16.5	—

Table 9: TX EVM Test

Rate	Min (dB)	Typ (dB)	SL ¹ (dB)
802.11b, 1 Mbps, @19.5 dBm	—	-25.0	-10
802.11b, 11 Mbps, @19.5 dBm	—	-25.0	-10
802.11g, 6 Mbps, @18 dBm	—	-25.0	-5
802.11g, 54 Mbps, @18 dBm	—	-27.0	-25
802.11n, HT20, MCS0, @18 dBm	—	-25.0	-5
802.11n, HT20, MCS7, @17 dBm	—	-29.5	-27
802.11n, HT40, MCS0, @18 dBm	—	-25.0	-5
802.11n, HT40, MCS7, @16.5 dBm	—	-29.5	-27

¹ SL stands for standard limit value.

4.4.3 Wi-Fi RF Receiver (RX) Specifications

Table 10: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	-97	—
802.11b, 2 Mbps	—	-95	—
802.11b, 5.5 Mbps	—	-93	—
802.11b, 11 Mbps	—	-88	—
802.11g, 6 Mbps	—	-92	—
802.11g, 9 Mbps	—	-91	—
802.11g, 12 Mbps	—	-89	—
802.11g, 18 Mbps	—	-87	—
802.11g, 24 Mbps	—	-84	—
802.11g, 36 Mbps	—	-80	—
802.11g, 48 Mbps	—	-76	—
802.11g, 54 Mbps	—	-75	—
802.11n, HT20, MCS0	—	-92	—
802.11n, HT20, MCS1	—	-88	—
802.11n, HT20, MCS2	—	-85	—
802.11n, HT20, MCS3	—	-83	—
802.11n, HT20, MCS4	—	-79	—
802.11n, HT20, MCS5	—	-75	—
802.11n, HT20, MCS6	—	-74	—
802.11n, HT20, MCS7	—	-72	—
802.11n, HT40, MCS0	—	-89	—
802.11n, HT40, MCS1	—	-86	—
802.11n, HT40, MCS2	—	-83	—
802.11n, HT40, MCS3	—	-80	—
802.11n, HT40, MCS4	—	-76	—

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Table 10 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11n, HT40, MCS5	—	-72	—
802.11n, HT40, MCS6	—	-71	—
802.11n, HT40, MCS7	—	-69	—

Table 11: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—

Table 12: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps	—	35	—
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	14	—
802.11n, HT20, MCS0	—	31	—
802.11n, HT20, MCS7	—	13	—
802.11n, HT40, MCS0	—	19	—
802.11n, HT40, MCS7	—	8	—

5 Module Schematics

This is the reference design of the module.

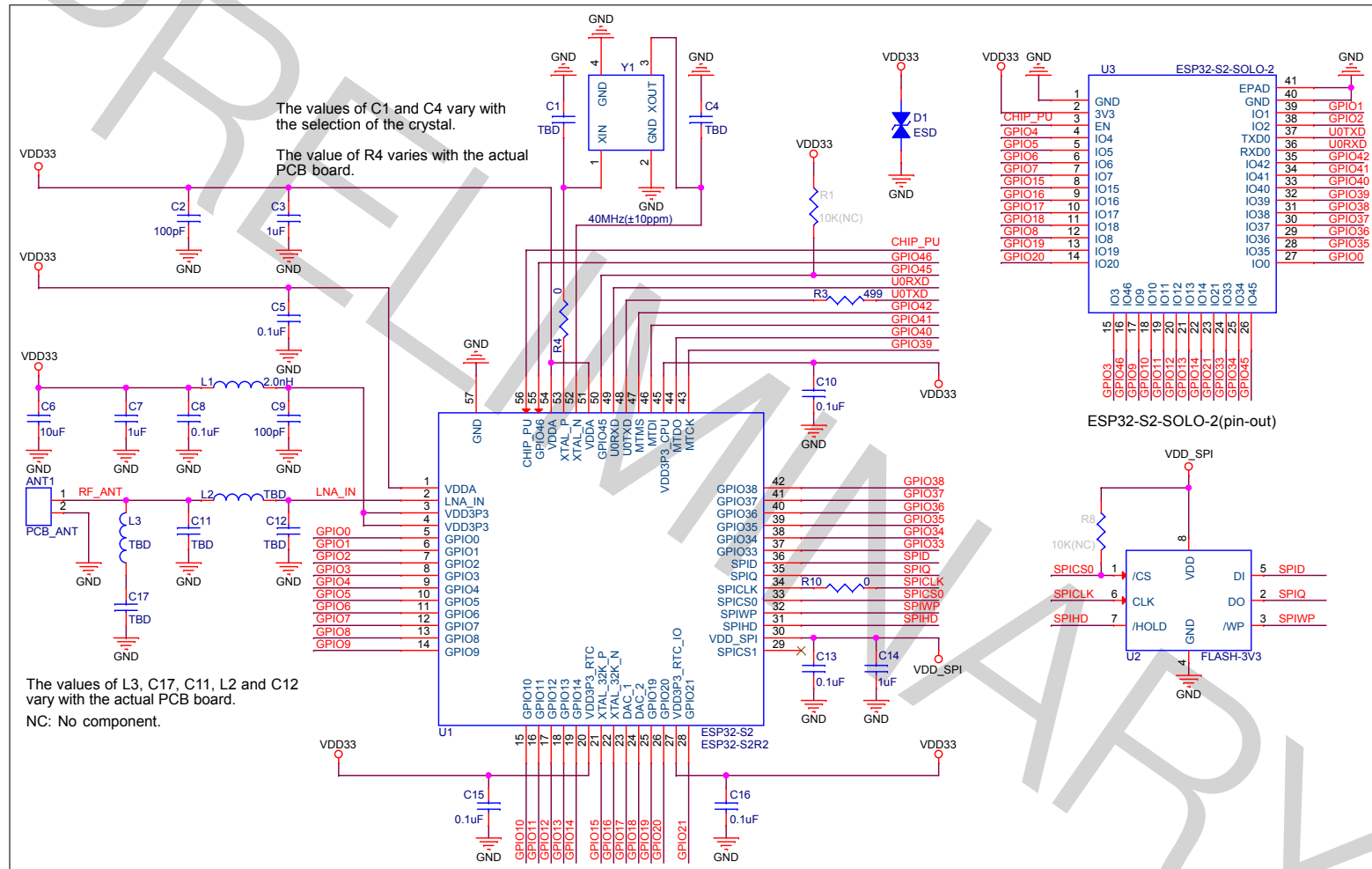
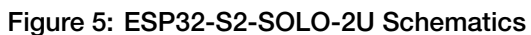


Figure 4: ESP32-S2-SOLO-2 Schematics



6 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

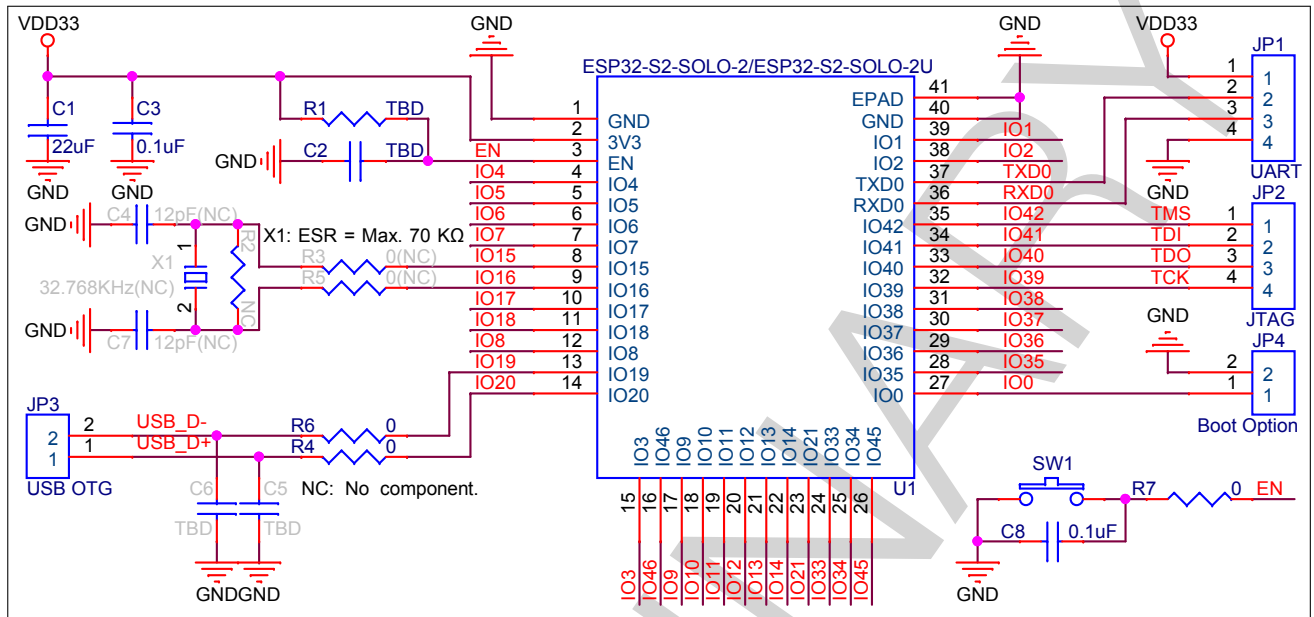


Figure 6: Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste.
- To ensure that the power supply to the ESP32-S2 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually $R = 10\text{ k}\Omega$ and $C = 1\text{ }\mu\text{F}$. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S2's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in [ESP32-S2 Series Datasheet](#).

7 Physical Dimensions and PCB Land Pattern

7.1 Physical Dimensions

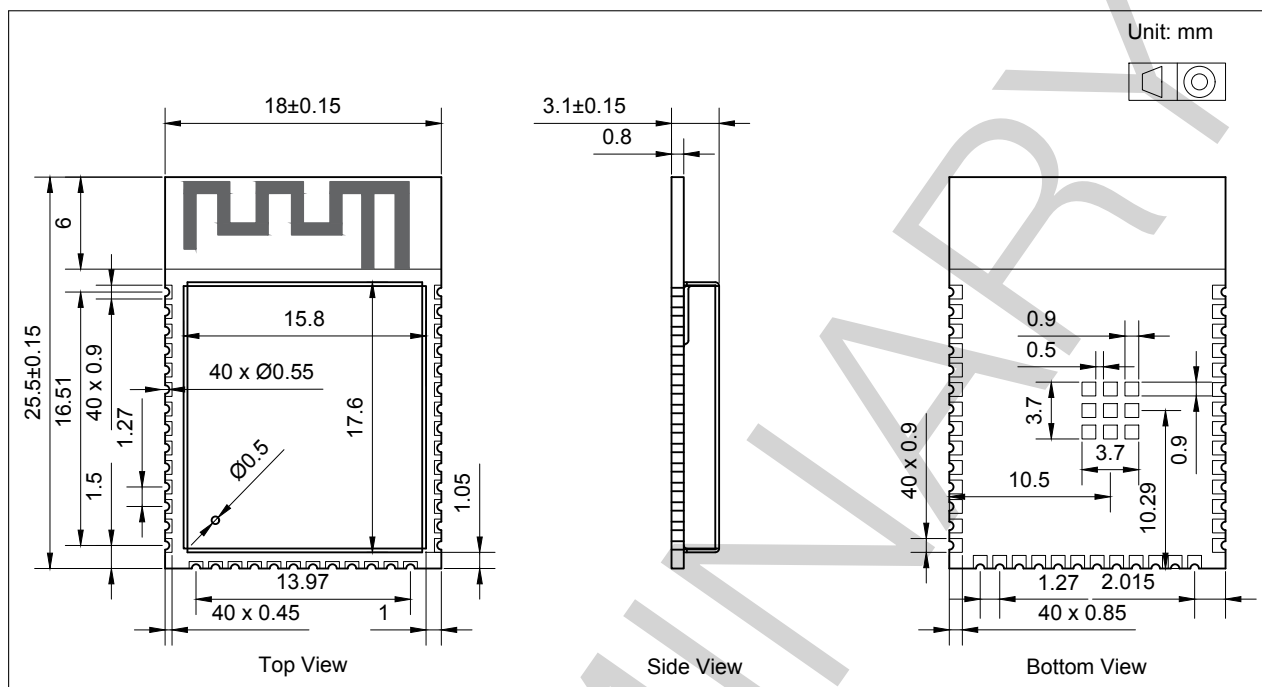


Figure 7: ESP32-S2-SOLO-2 Physical Dimensions

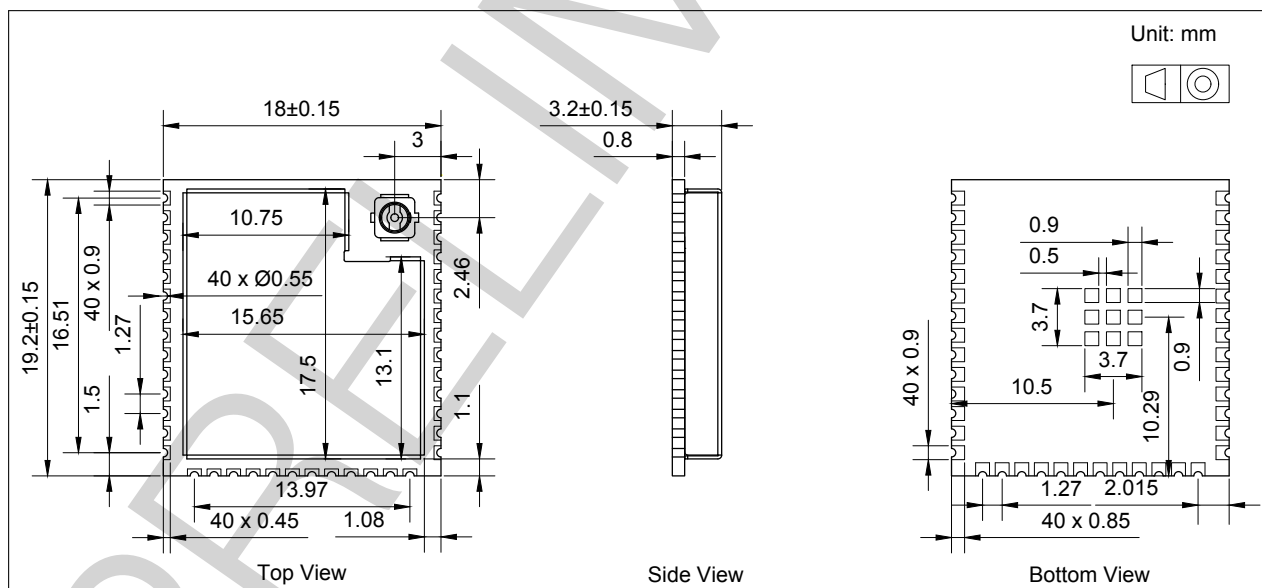


Figure 8: ESP32-S2-SOLO-2U Physical Dimensions

Note:

For information about tape, reel, and product marking, please refer to [Espressif Module Package Information](#).

7.2 Recommended PCB Land Pattern

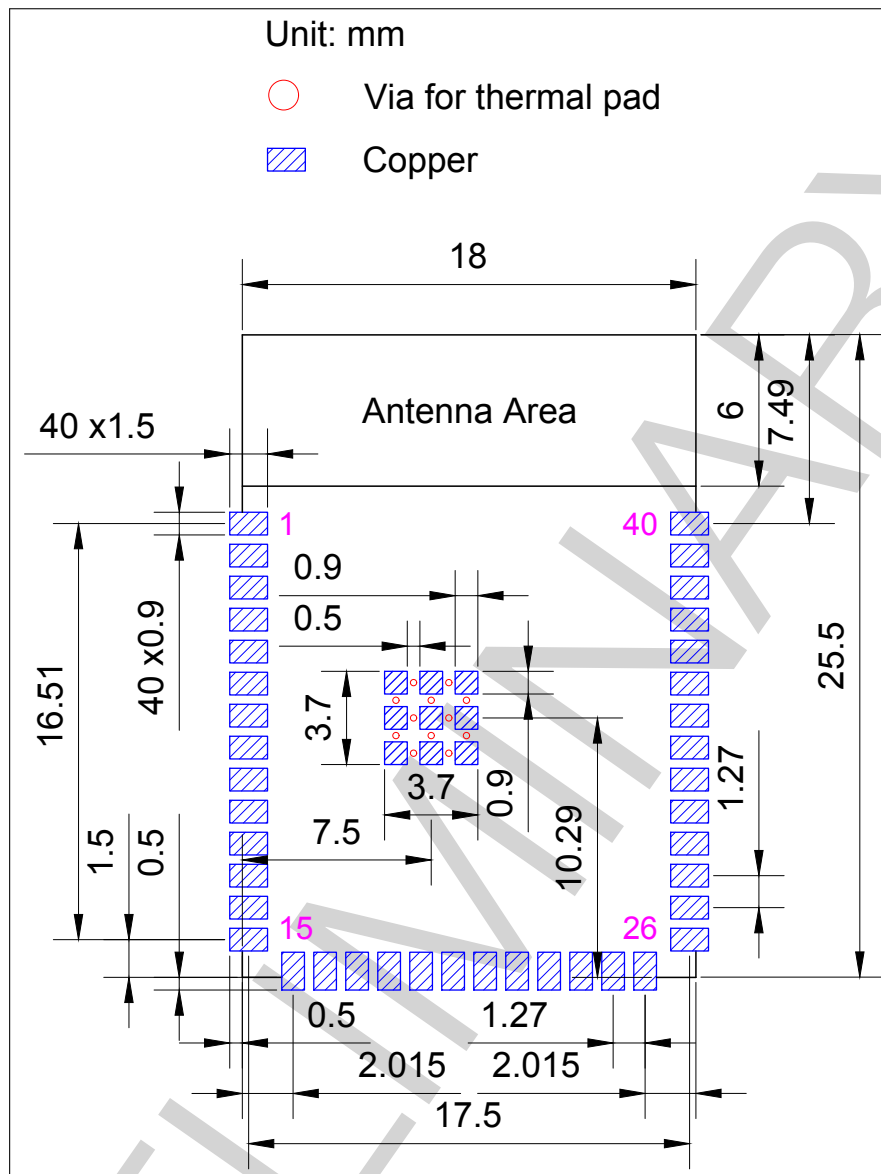


Figure 9: ESP32-S2-SOLO-2 Recommended PCB Land Pattern

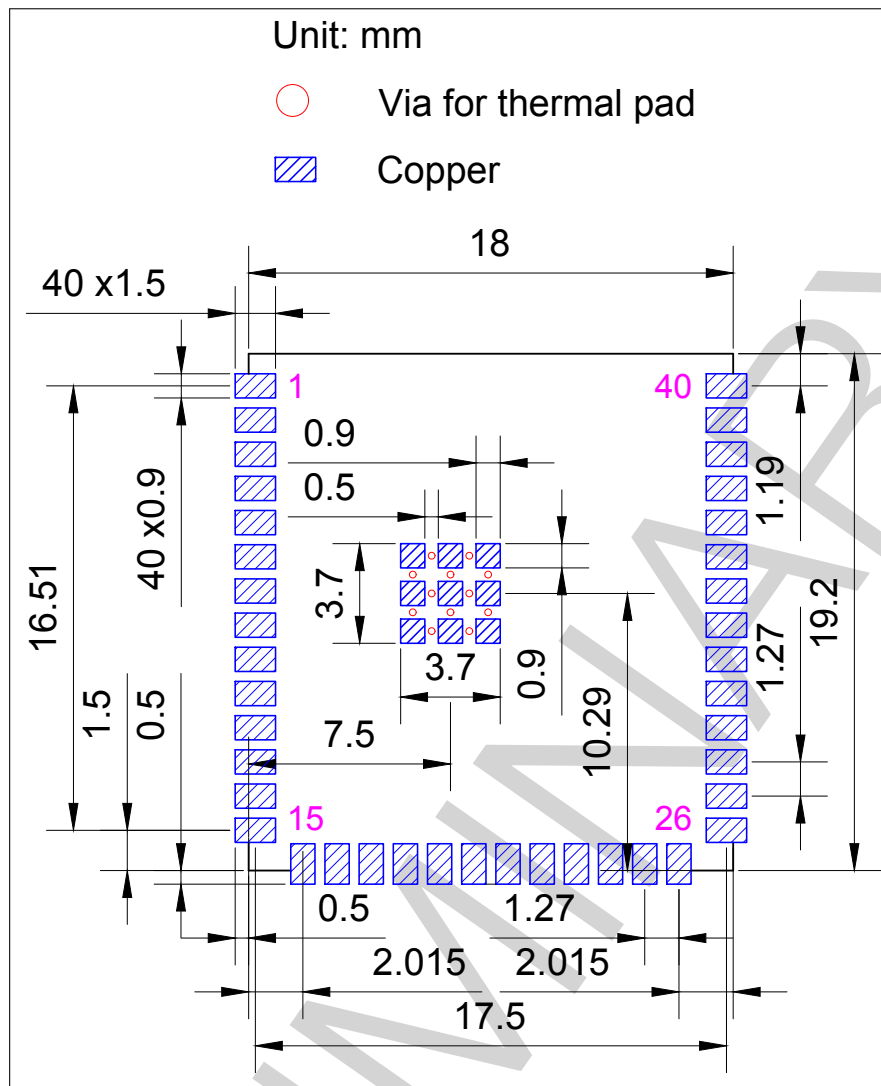


Figure 10: ESP32-S2-SOLO-2U Recommended PCB Land Pattern

7.3 Dimensions of External Antenna Connector

ESP32-S2-SOLO-2U uses the first generation external antenna connector as shown in Figure 11. This connector is compatible with the following connectors:

- U.FL Series connector from Hirose
- MHF I connector from I-PEX
- AMC connector from Amphenol

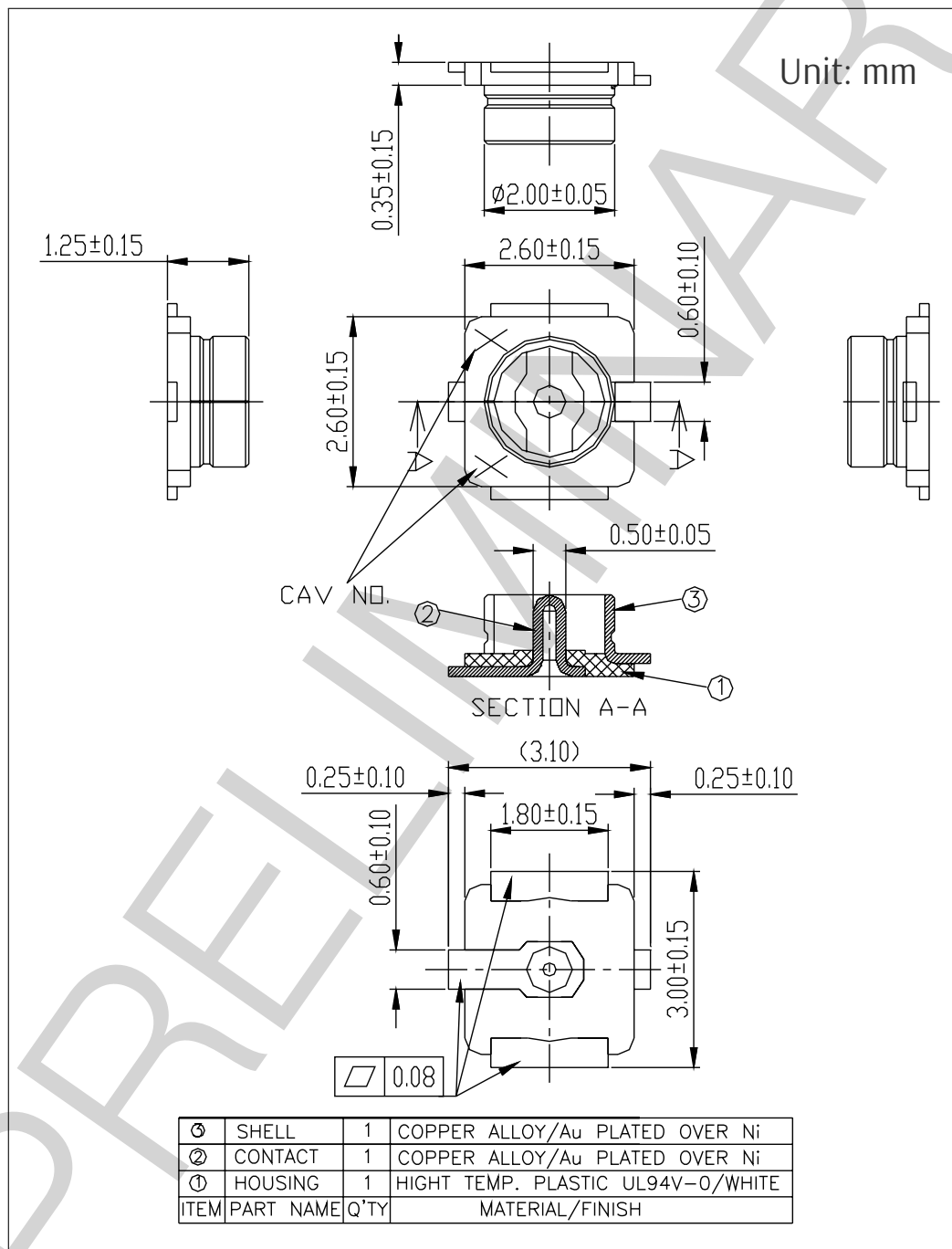


Figure 11: Dimensions of External Antenna Connector

8 Product Handling

8.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of $< 40\text{ }^{\circ}\text{C}$ and $/90\%\text{RH}$. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions $25\pm 5\text{ }^{\circ}\text{C}$ and $/60\%\text{RH}$. If the above conditions are not met, the module needs to be baked.

8.2 Electrostatic Discharge (ESD)

- Human body model (HBM): $\pm 2000\text{ V}$
- Charged-device model (CDM): $\pm 500\text{ V}$
- Air discharge: $\pm 6000\text{ V}$
- Contact discharge: $\pm 4000\text{ V}$

8.3 Reflow Profile

Solder the module in a single reflow.

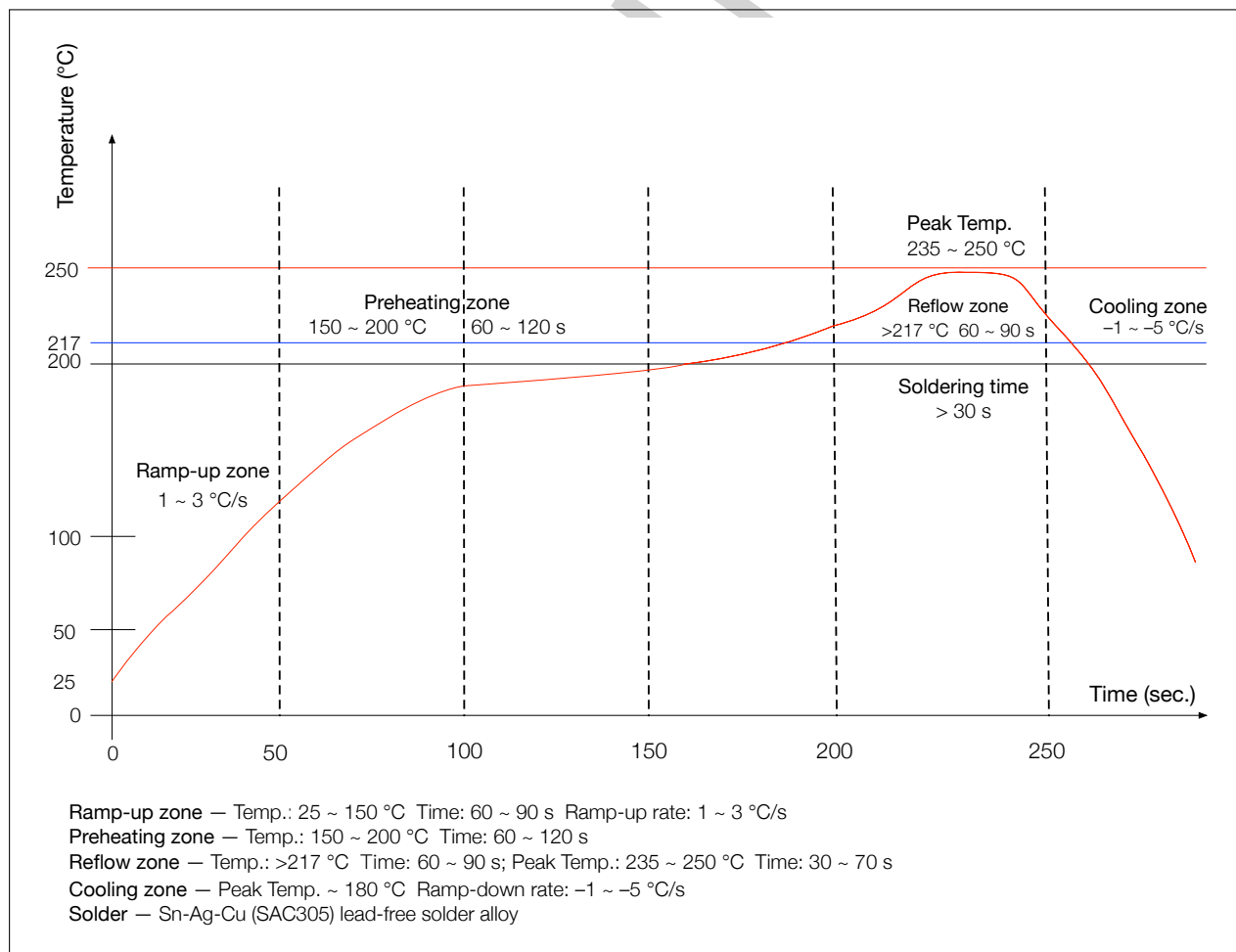


Figure 12: Reflow Profile

9 Related Documentation and Resources

Related Documentation

- [ESP32-S2 Series Datasheet](#) – Specifications of the ESP32-S2 hardware.
- [ESP32-S2 Technical Reference Manual](#) – Detailed information on how to use the ESP32-S2 memory and peripherals.
- [ESP32-S2 Hardware Design Guidelines](#) – Guidelines on how to integrate the ESP32-S2 into your hardware product.
- *Certificates*
<https://espressif.com/en/support/documents/certificates>
- *ESP32-S2 Product/Process Change Notifications (PCN)*
<https://espressif.com/en/support/documents/pcns>
- *ESP32-S2 Advisories* – Information on security, bugs, compatibility, component reliability.
<https://espressif.com/en/support/documents/advisories>
- *Documentation Updates and Update Notification Subscription*
<https://espressif.com/en/support/download/documents>

Developer Zone

- [ESP-IDF Programming Guide for ESP32-S2](#) – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
<https://github.com/espressif>
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
<https://esp32.com/>
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
<https://blog.espressif.com/>
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
<https://espressif.com/en/support/download/sdks-demos>

Products

- *ESP32-S2 Series SoCs* – Browse through all ESP32-S2 SoCs.
<https://espressif.com/en/products/socs?id=ESP32-S2>
- *ESP32-S2 Series Modules* – Browse through all ESP32-S2-based modules.
<https://espressif.com/en/products/modules?id=ESP32-S2>
- *ESP32-S2 Series DevKits* – Browse through all ESP32-S2-based devkits.
<https://espressif.com/en/products/devkits?id=ESP32-S2>
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
<https://products.espressif.com/#/product-selector?language=en>

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Revision History

Date	Version	Release notes
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