An Infineon Technologies Company

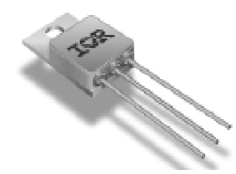
IRFY9140C, IRFY9140CM

POWER MOSFET
THRU-HOLE (TO-257AA)

100V, P-CHANNEL
HEXFET MOSFET TECHNOLOGY

Product Summary

Part Number	RDS(on)	I_D	Eyelets
IRFY9140C	0.20Ω	-15.8A	Ceramic
IRFY9140CM	0.20Ω	-15.8A	Ceramic



TO-257AA

Description

HEXFET MOSFET technology is the key to IR HiRel advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high trans conductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heat sink. This improves thermal efficiency and reduces drain capacitance.

Features

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Eyelets
- Ideally Suited For Space Level Applications
- ESD Rating: Class 2 per MIL-STD-750, Method 1020

Absolute Maximum Ratings

	Parameter		Units
I_D @ V_{GS} = -10V, T_C = 25°C	Continuous Drain Current	-15.8	A
I_D @ V_{GS} = -10V, T_C = 100°C	Continuous Drain Current	-10	
I_{DM}	Pulsed Drain Current ①	-60	
P_D @T_C = 25°C	Maximum Power Dissipation	100	W
	Linear Derating Factor	0.8	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	640	mJ
I_{AR}	Avalanche Current ①	-15.8	A
E_{AR}	Repetitive Avalanche Energy ①	10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in/1.6mm from case for 10sec)	
	Weight	4.3 (Typical)	g

For Footnotes refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.1	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.20	Ω	V_{GS} = -10V, I_D = -10A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
Gfs	Forward Transconductance	6.2	—	—	S	V_{DS} = -15V, I_D = -10A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V_{DS} = -80V, V_{GS} = 0V
		—	—	-250		V_{DS} = -80V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_G	Total Gate Charge	—	—	60	nC	I_D = -15.8A
Q_{GS}	Gate-to-Source Charge	—	—	13		V_{DS} = -50V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	35.2		V_{GS} = -10V
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = -50V
tr	Rise Time	—	—	85		I_D = -15.8A
$t_{d(off)}$	Turn-Off Delay Time	—	—	85		R_G = 7.5Ω
t_f	Fall Time	—	—	65		V_{GS} = -10V
Ls +L_D	Total Inductance	—	6.8	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	1400	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	600	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	200	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-15.8	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-60		
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_J = 25°C,I_S = -15.8A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	—	280	ns	T_J = 25°C, I_F = -15.8A, V_{DD} ≤ -50V
Q_{rr}	Reverse Recovery Charge	—	—	3.6	μC	di/dt = -100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	—	—	1.25	°C/W	
$R_{\theta CS}$	Case-to-sink	—	0.21	—		
$R_{\theta JA}$	Junction-to-Ambient	—	—	80		Typical socket mount

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = -50V, starting T_J = 25°C, L =5.1mH, Peak I_L = -15.8A, V_{GS} = -10V

③ I_{SD} ≤ -15.8A, di/dt ≤ -200A/μs, V_{DD} ≤ -100V, T_J ≤ 150°C

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

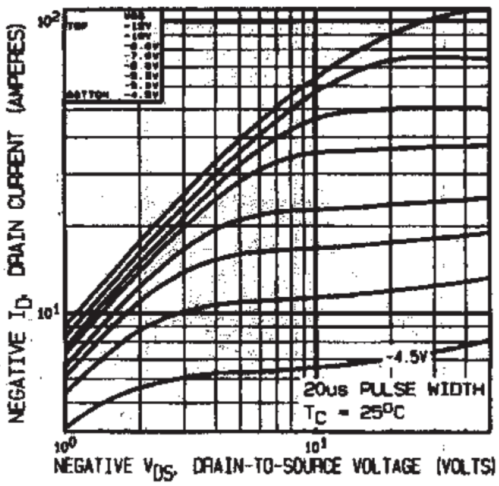


Fig 1. Typical Output Characteristics

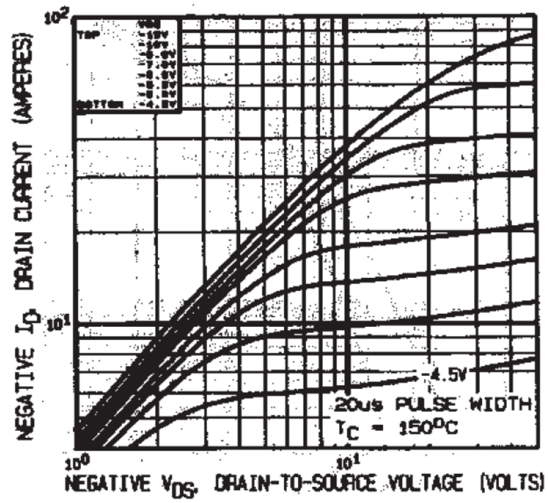


Fig 2. Typical Output Characteristics

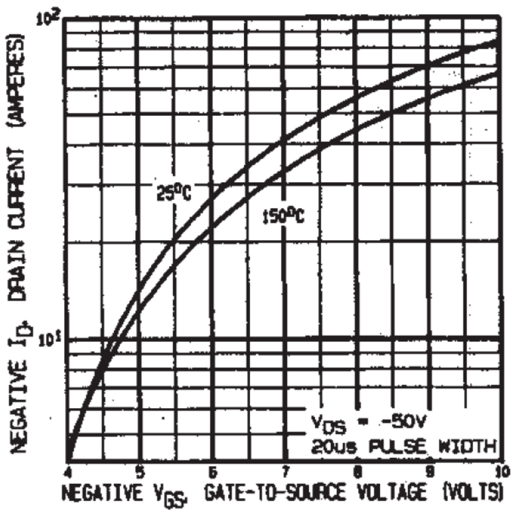


Fig 3. Typical Transfer Characteristics

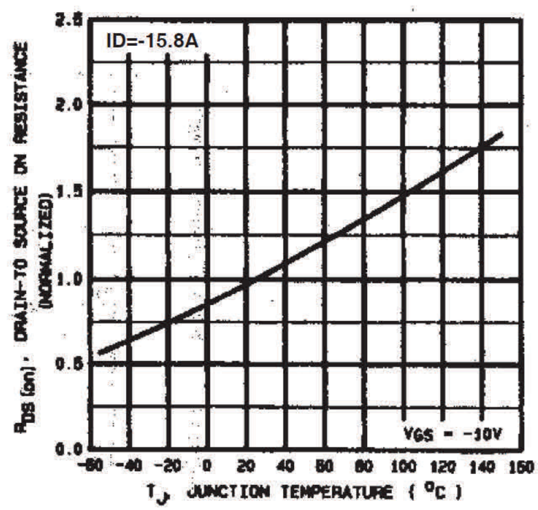


Fig 4. Normalized On-Resistance Vs. Temperature

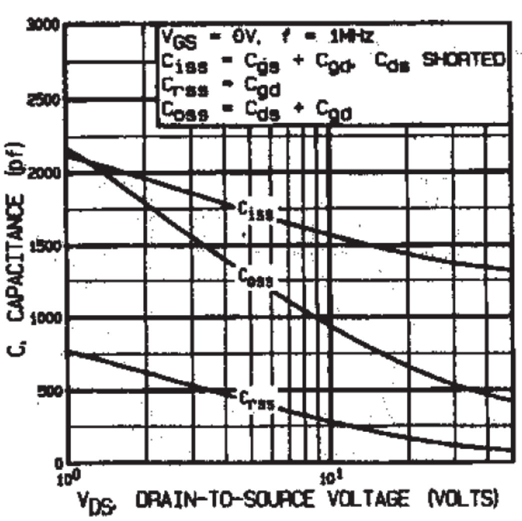


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

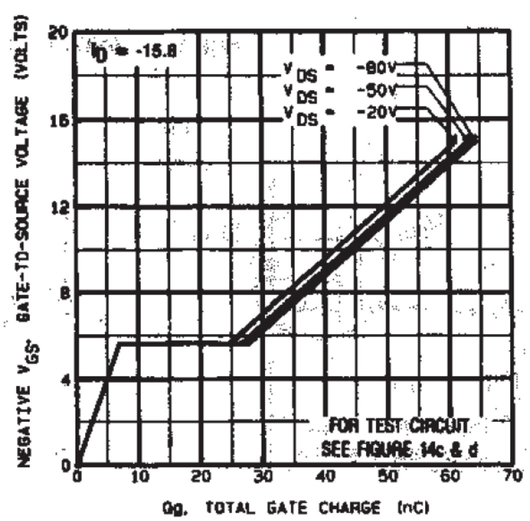


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

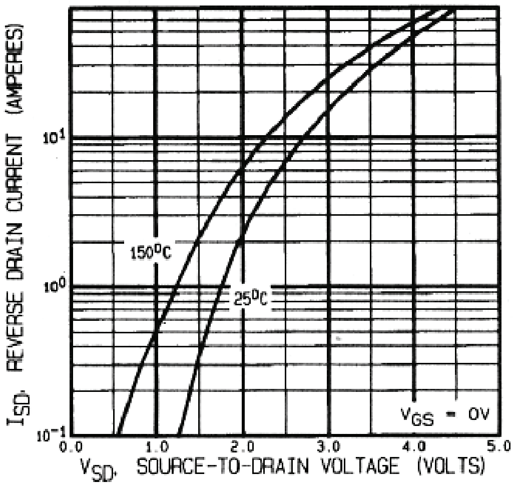


Fig 7. Typical Source-Drain Diode Forward Voltage

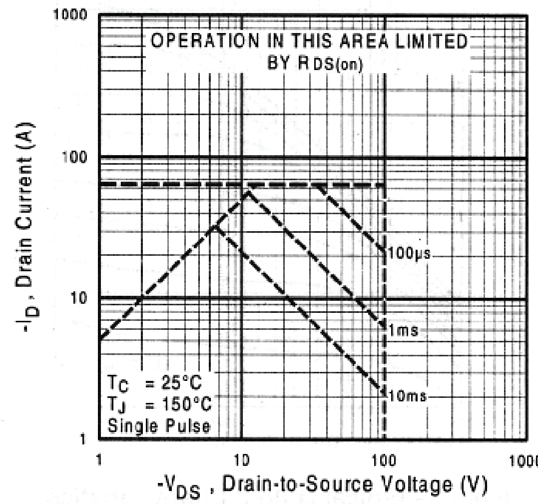


Fig 8. Maximum Safe Operating Area

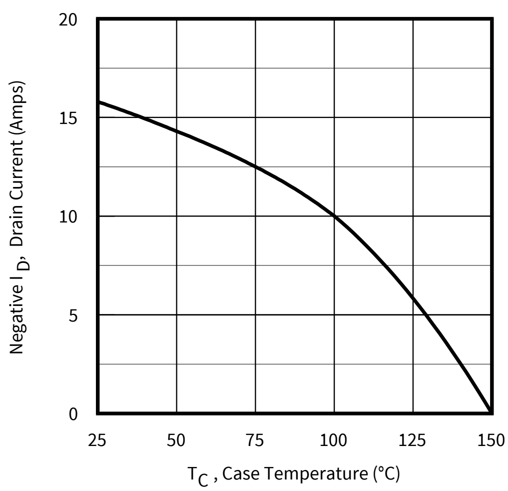


Fig 9. Maximum Drain Current Vs. Case Temperature

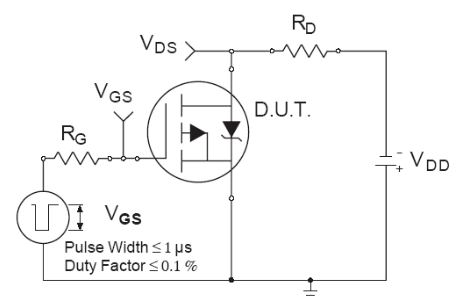


Fig 10a. Switching Time Test Circuit

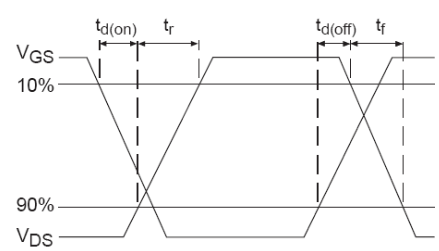


Fig 10b. Switching Time Waveforms

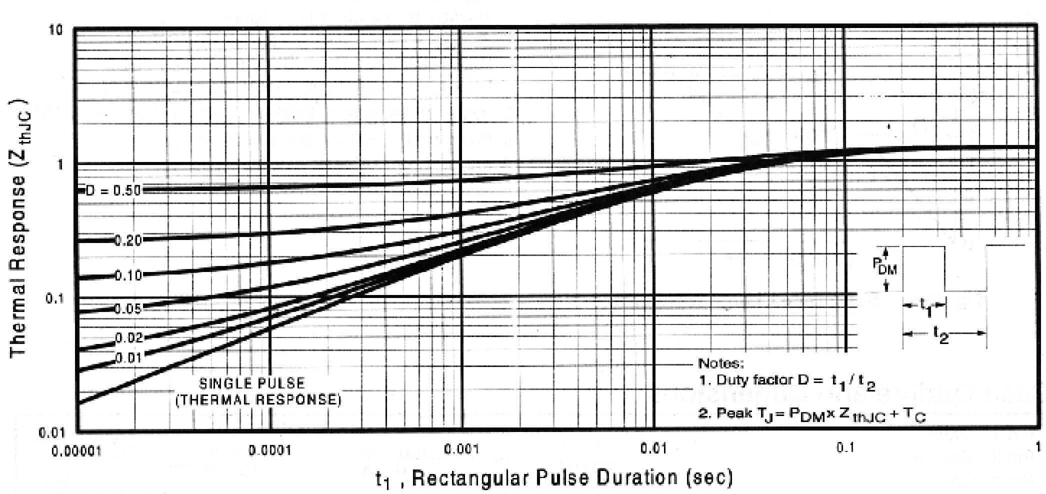


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

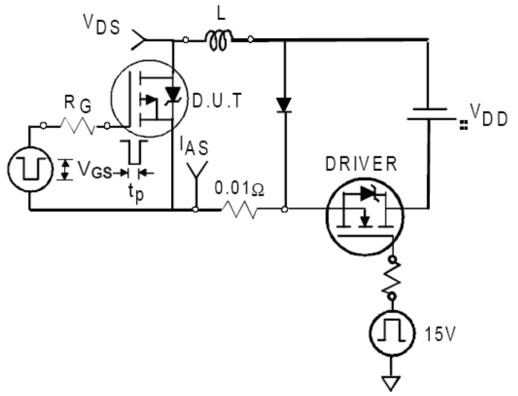


Fig 12a. Unclamped Inductive Test Circuit

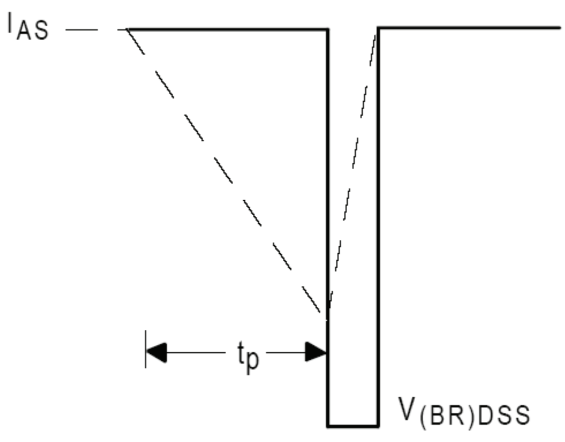


Fig 12b. Unclamped Inductive Waveforms

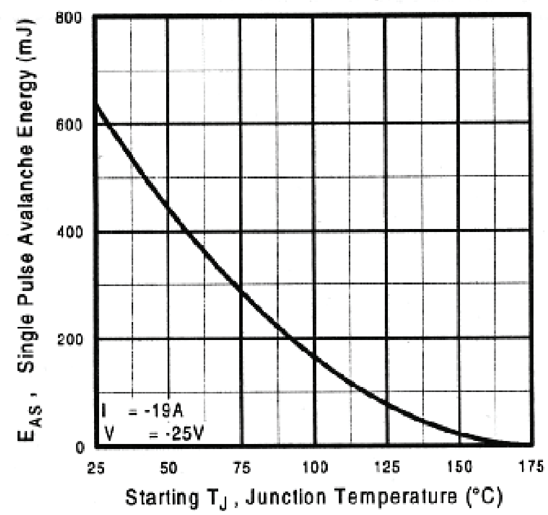


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

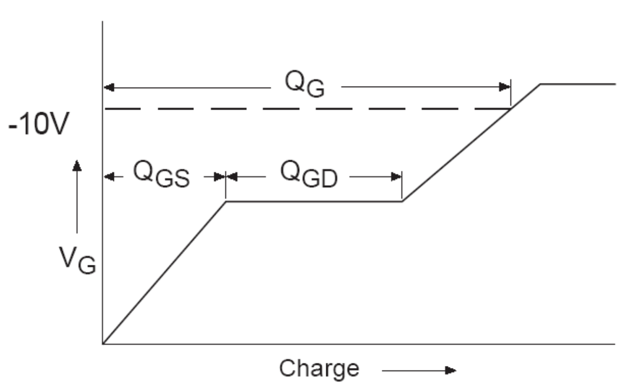


Fig 13a. Basic Gate Charge Waveform

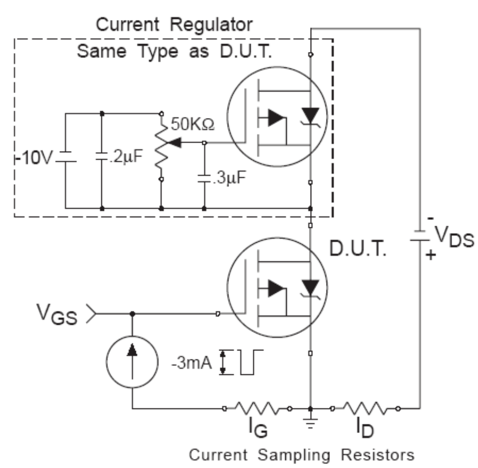
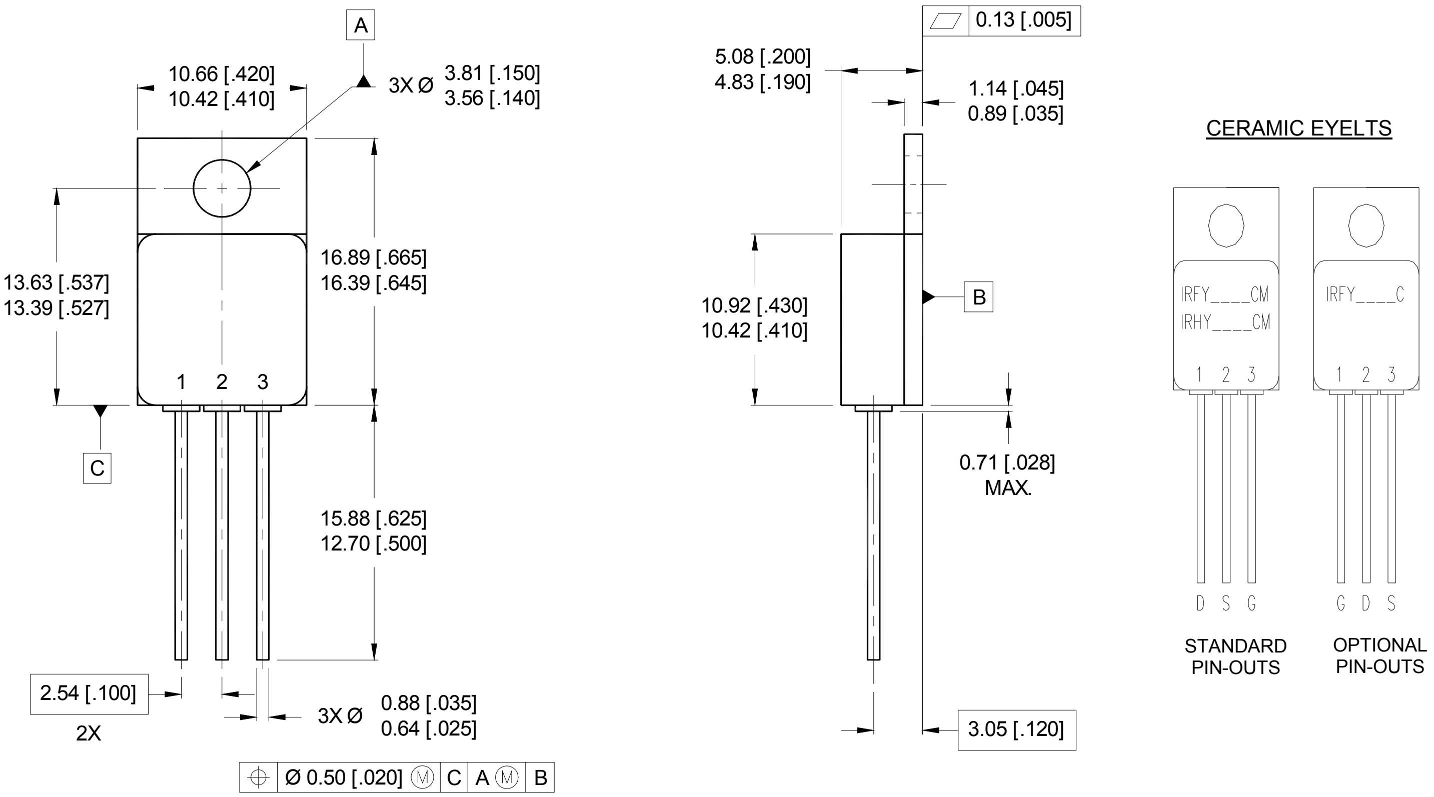


Fig 13b. Gate Charge Test Circuit

Case Outline and Dimensions — TO-257AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.

LEAD ASSIGNMENT

1 = DRAIN
2 = SOURCE
3 = GATE

IR HiRel
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