IRFN250 (JANTX2N7225U)

PD-91549D

Power MOSFET
Surface Mount (SMD-1)
200V, 27.4A, N-channel, HEXFET™ MOSFET Technology

Features

- Simple drive requirements
- Hermetically sealed
- Electrically isolated
- Surface mount
- Dynamic dv/dt rating
- Light weight

Product Summary

- **BV_{DSS}:** 200V
- **I_D:** 27.4A
- **$R_{DS(on),max}$:** 100mΩ
- **$Q_{G,\ max}$:** 115nC
- **REF:** MIL-PRF-19500/592

SMD-1

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified to JANTXV screening flow according to MIL-PRF-19500 for high-reliability applications

Description

IR HiRel HEXFET™ technology is advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET™ transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, fast switching and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET™ transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level
IRFN250	SMD-1	COTS
JANTX2N7225U	SMD-1	JANTX
JANTXV2N7225U	SMD-1	JANTXV

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = 10V, T_C = 25°C	Continuous Drain Current	27.4	A
I_{D2} @ V_{GS} = 10V, T_C = 100°C	Continuous Drain Current	17	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	110	A
P_D @ T_C = 25°C	Maximum Power Dissipation	150	W
	Linear Derating Factor	1.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	500	mJ
I_{AR}	Avalanche Current [1]	27.4	A
E_{AR}	Repetitive Avalanche Energy [1]	15	mJ
dv/dt	Peak Diode Reverse Recovery [3]	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	2.6 (Typical)	g

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] V_{DD} = 25V, starting T_J = 25°C, L = 1.3mH, Peak I_L = 27.4A, V_{GS} = 10V
[3] $I_{SD} \leq$ 27.4A, di/dt ≤ 190A/µs, $V_{DD} \leq$ 200V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics

Table 3 Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.29	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	100	mΩ	V_{GS} = 10V, I_{D2} = 17A [1]
		—	—	105		V_{GS} = 10V, I_{D1} = 27.4A [1]
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
Gfs	Forward Transconductance	9.0	—	—	S	V_{DS} = 15V, I_{D2} = 17A
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	µA	V_{DS} = 160V, V_{GS} = 0V
		—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	115	nC	I_{D1} = 27.4A V_{DS} = 100V V_{GS} = 10V
Q_{GS}	Gate-to-Source Charge	—	—	22		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	60		
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	I_{D1} = 27.4A ** V_{DD} = 100V R_G = 2.35Ω V_{GS} = 10V
t_r	Rise Time	—	—	190		
$t_{d(off)}$	Turn-Off Delay Time	—	—	170		
t_f	Fall Time	—	—	130		
$L_s + L_D$	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad.
C_{iss}	Input Capacitance	—	3500	—	pF	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	700	—		
C_{rss}	Reverse Transfer Capacitance	—	110	—		

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	27.4	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	110	A	
V_{SD}	Diode Forward Voltage	—	—	1.9	V	$T_J = 25°C$, $I_S = 27.4A$, $V_{GS} = 0V$ [2]
t_{rr}	Reverse Recovery Time	—	—	950	ns	$T_J = 25°C$, $I_F = 27.4A$, $V_{DD} \leq 30V$ di/dt = 100A/µs
Q_{rr}	Reverse Recovery Charge	—	6.0	—	µC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	0.83	°C/W
$R_{\theta J\text{-}PCB}$	Junction-to-PC board (Soldered to a copper-clad PC board)	—	3.0	—	

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

3 Electrical Characteristics Curves

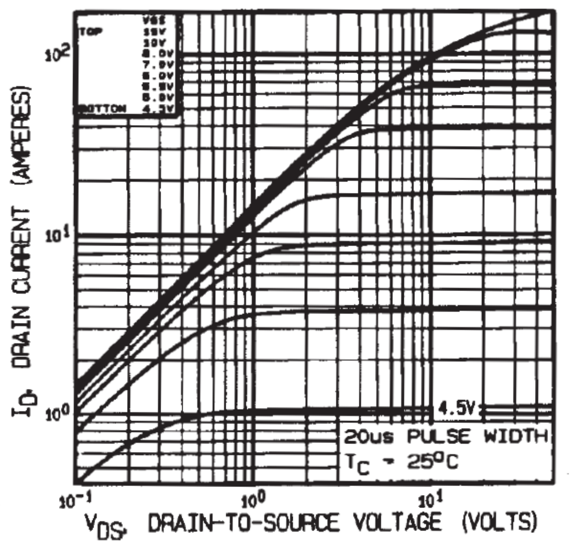


Figure 1 Typical Output Characteristics

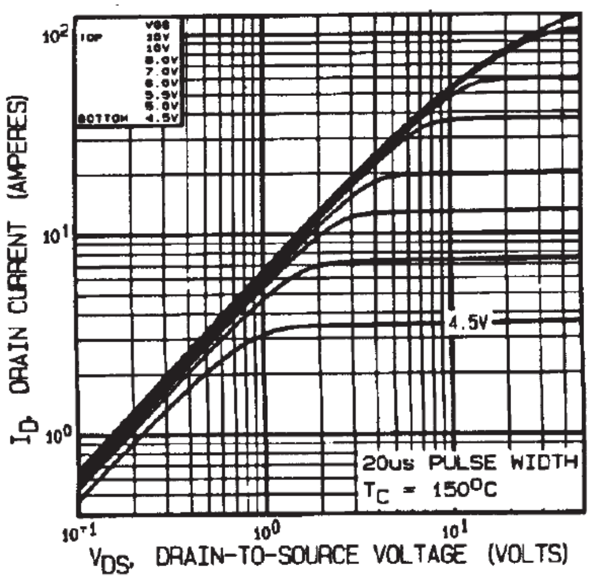


Figure 2 Typical Output Characteristics

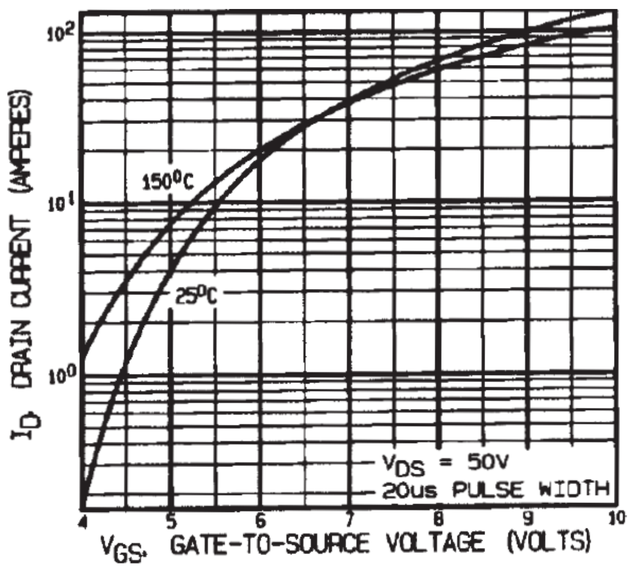


Figure 3 Typical Transfer Characteristics

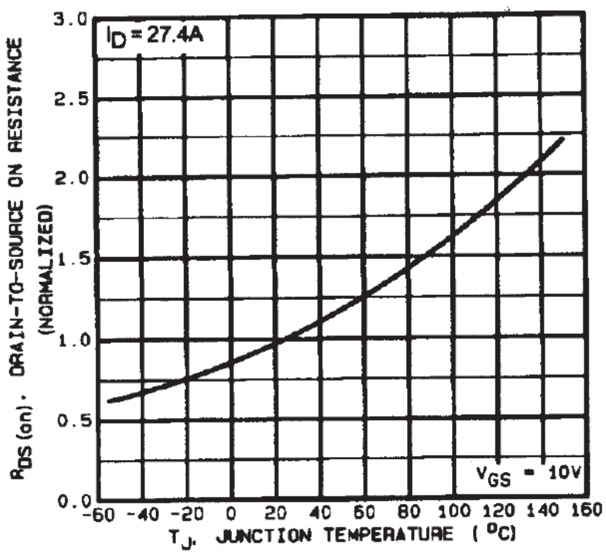


Figure 4 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves

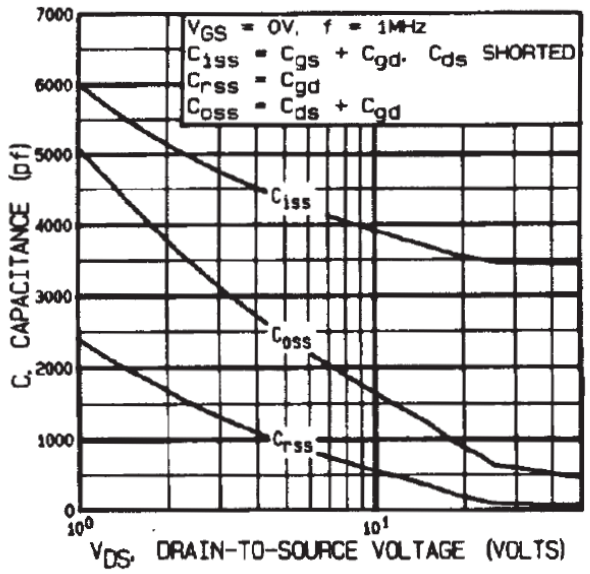


Figure 5 **Typical Capacitance Vs. Drain-to-Source Voltage**

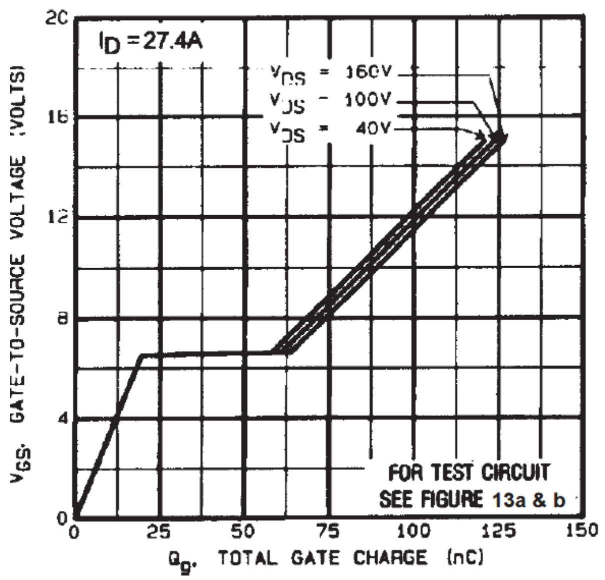


Figure 6 **Typical Gate Charge Vs. Gate-to-Source Voltage**

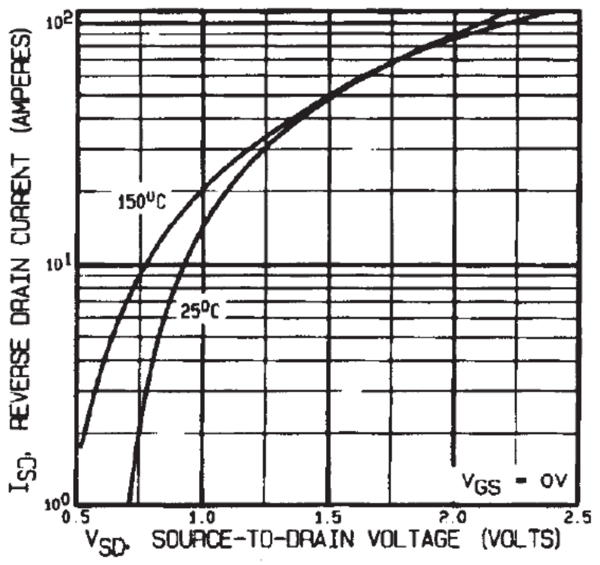


Figure 7 **Typical Source-Drain Current Vs. Diode Forward Voltage**

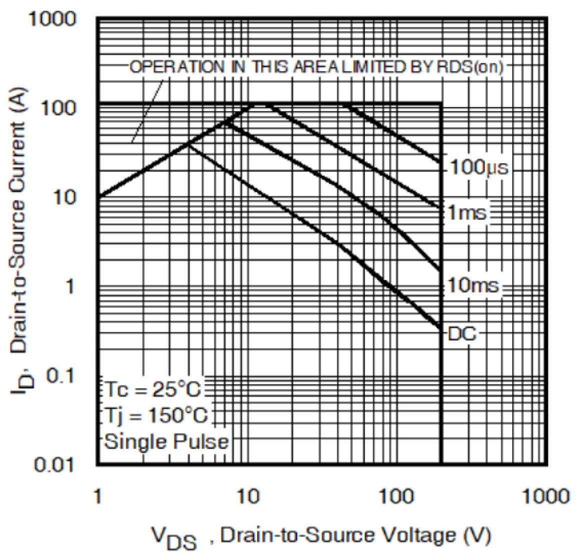


Figure 8 **Maximum Safe Operating Area**

Electrical Characteristics Curves

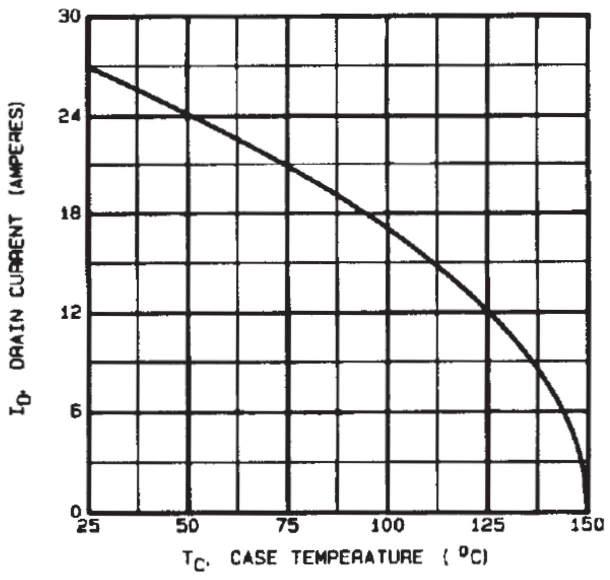


Figure 9 Maximum Drain Current Vs. Case Temperature

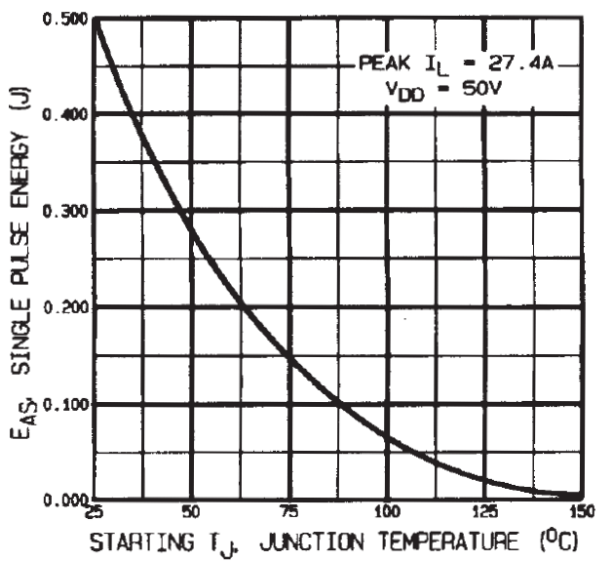


Figure 10 Maximum Avalanche Energy Vs. Junction Temperature

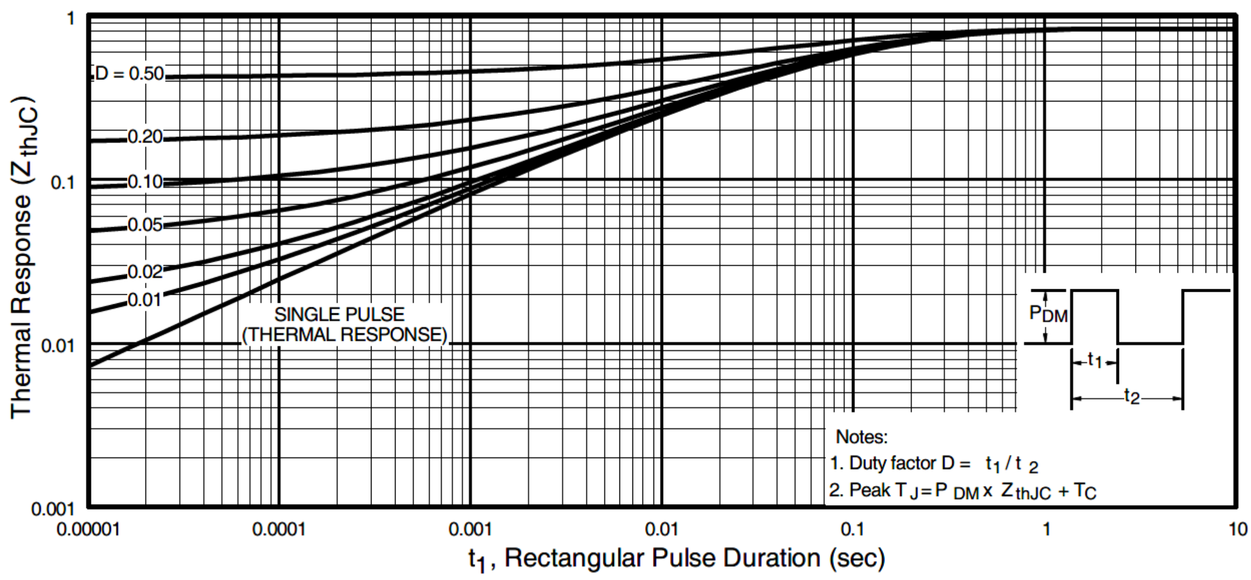


Figure 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits

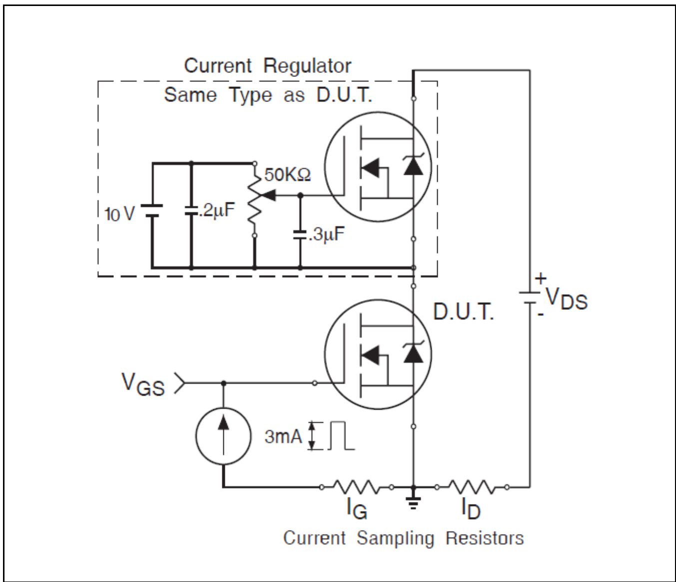


Figure 12 Gate Charge Test Circuit

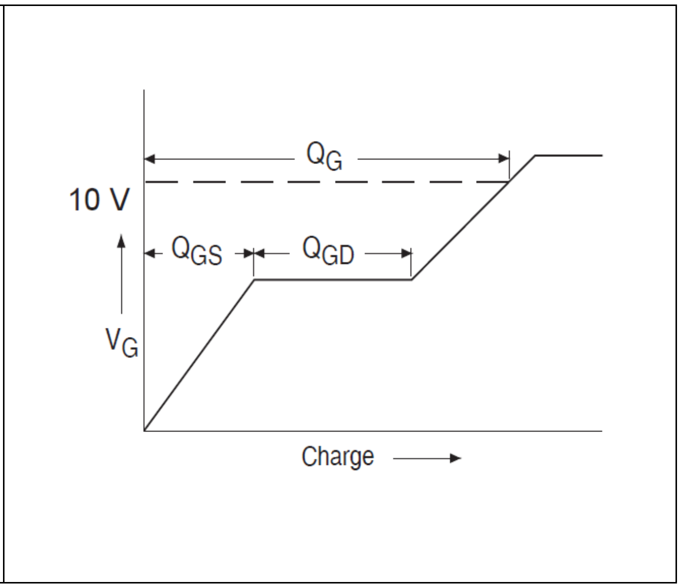


Figure 13 Gate Charge Waveform

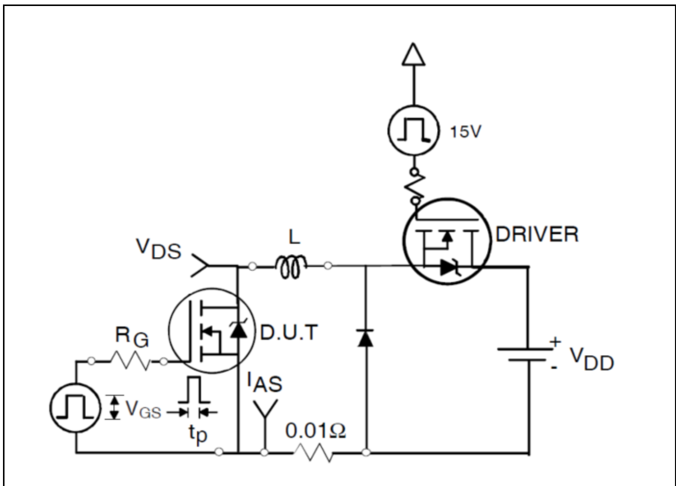


Figure 14 Unclamped Inductive Test Circuit

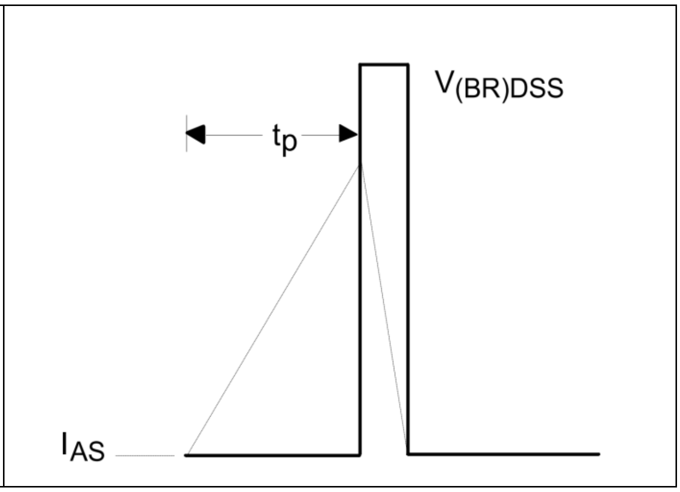


Figure 15 Unclamped Inductive Waveform

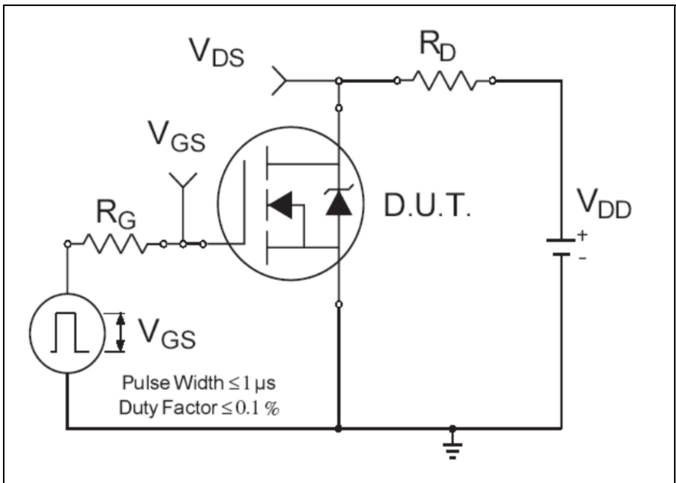


Figure 16 Switching Time Test Circuit

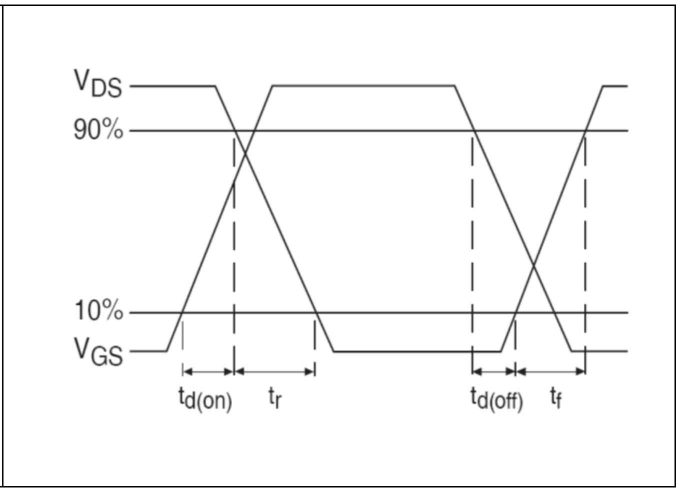
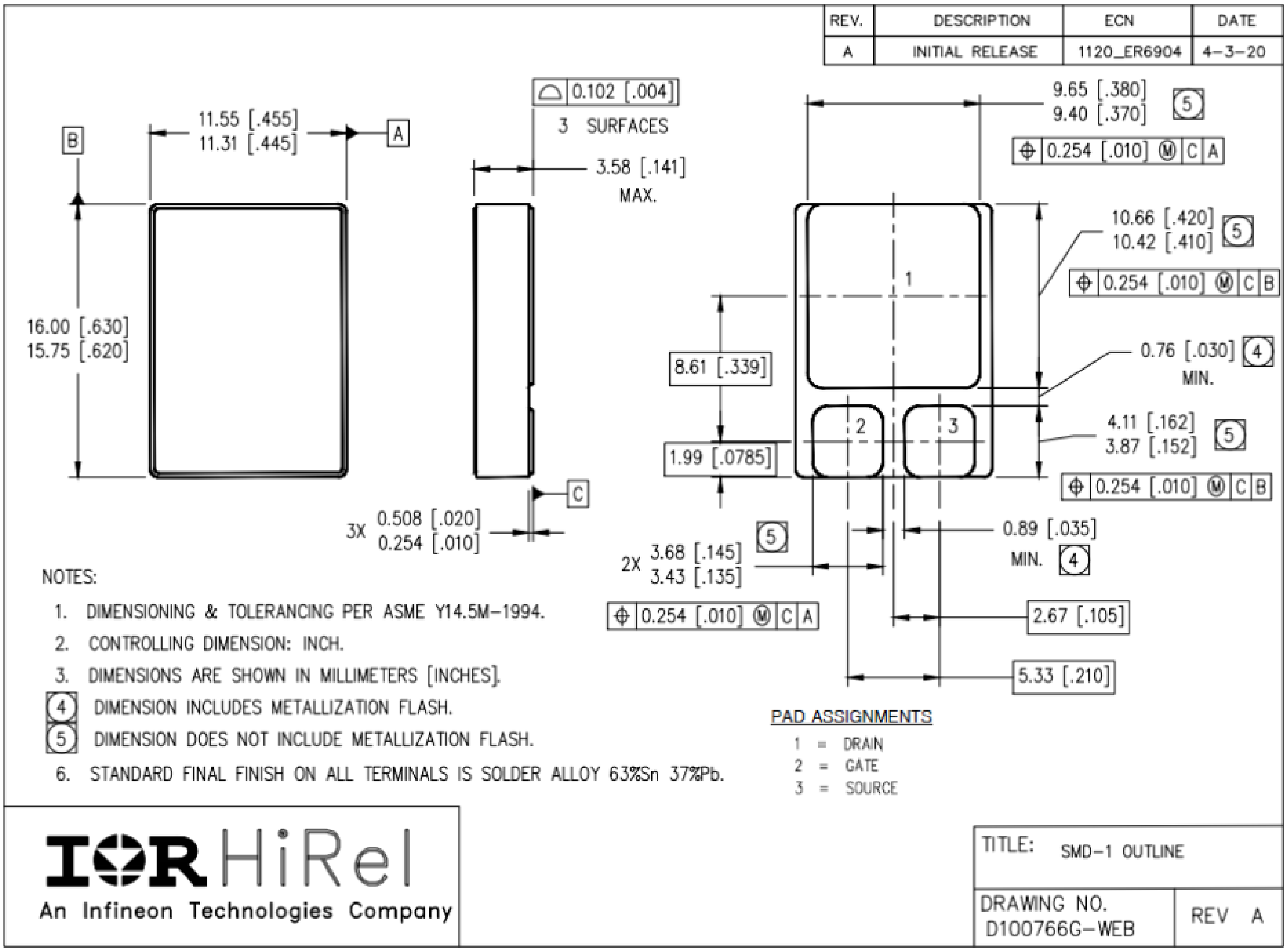


Figure 17 Switching Time Waveforms

5 Package Outline

Note: For the most updated package outline, please see the website: SMD-1



Revision history

Document version	Date of release	Description of changes
Rev B	12/22/1999	Datasheet (PD-91549)
Rev C	01/28/2002	Updated Switchtie test condition VGS =10V
Rev D	08/06/2024	Updated based on ECN-1120_10008

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Email: erratum@infineon.com

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