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RIC7S113

Radiation hardened high and low side gate driver

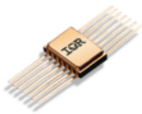
Features

- Independent high and low side gate driver
- Independent bias supply for logic and power with ±5V offset
- Wide bias supply voltage range
- Undervoltage lockout for both channels
- CMOS Schmitt trigger inputs with internal pull-down resistor
- Integrated level shift for high side drive
- Cycle by cycle edge triggered shutdown logic pin
- Matched propagation delay for both channels
- Hermetically sealed package
- Lightweight
- Total ionizing dose (TID) hardness
    - High dose rate (50-300 rad(Si)/s) of 100 krad(Si)
- Single event effect (SEE) hardness
    - No SEB, SEGR up to LET of 27.8 MeV·cm^2/mg, derated safe operating area (SOA) up to 81.9 MeV·cm^2/mg
    - SET characterized up to LET of 81.9 MeV·cm^2/mg

Product summary

- V_{OFFSET} (max) = 400 V
- V_{CC} = 10 V to 20 V
- V_{DD} = 5 V to 20 V
- $I_{OUTA/B}$ source/sink (typ) = 2 A / -2 A
- t_{on} (typ) = 120 ns
- t_{off} (typ) = 100 ns
- MT (typ) = 5 ns
- T_J = -55°C to 125°C

Package



Flatpack

LCC CIC

MO-036AB CIC

Potential applications

- Satellite bus and payload
- Power conditioning unit
- Power distribution unit
- DC-DC converter
- Motor drive

Ordering information

Table 1 Ordering information

Orderable part number	Package type	Device class	Total ionizing dose level	Temperature range (°C)
RIC7S113A4SCS	Flatpack	Level S[1]	100krad(Si)	-55 to 125
RIC7S113A4SCB	Flatpack	Level B[1]	100krad(Si)	-55 to 125
RIC7S113A4	Flatpack	COTS	100krad(Si)	-55 to 125
RIC7S113C4CDK	Die	Class K[2]	100krad(Si)	-55 to 125
RIC7S113C4CDH	Die	Class H[2]	100krad(Si)	-55 to 125
RIC7S113C4CDV	Die	Visual Inspection Only	100krad(Si)	-55 to 125

Orderable part number	**Package type**	**Device class**	**Total ionizing dose level**	**Temperature range (°C)**
RIC7S113E4SCS	LCC CIC	Level S[1]	100krad(Si)	-55 to 125
RIC7S113E4SCB	LCC CIC	Level B[1]	100krad(Si)	-55 to 125
RIC7S113E4	LCC CIC	COTS	100krad(Si)	-55 to 125
RIC7S113L4SCS	MO-036AB CIC	Level S[1]	100krad(Si)	-55 to 125
RIC7S113L4SCB	MO-036AB CIC	Level B[1]	100krad(Si)	-55 to 125
RIC7S113L4	MO-036AB CIC	COTS	100krad(Si)	-55 to 125
RIC7S113EVAL1	Evaluation Board			

[1] Per MIL-PRF-38535

[2] Per MIL-PRF-38534

Description

RIC7S113 is a rad hard high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. It is intended for harsh radiation environments such as space, with electrical parameters specified pre and post-irradiation up to 100 krad(Si) and single effect effects (SEE) characterized up to a linear energy transfer (LET) of 81.9 MeV·cm^2/mg.

RIC7S113 enables high performance from key parameters. The high gate drive strength, low propagation delay and matching timing for high and low side drive help reduce loss in the power switch. Enhanced robustness from Schmitt trigger inputs, high allowable offset supply voltage transient slew rate, separate logic and gate drive supplies and wide voltage range between the various bias power returns help improve noise immunity. RIC7S113 also is flexible to meet a variety of different system requirements, with input pins that are compatible with CMOS logic and external logic shutdown pin.

The high voltage support of up to 400 V allows for use in a range of high voltage applications, such as DC-DC converters and motor drive inverters in topologies such as half bridge and full bridge among others.

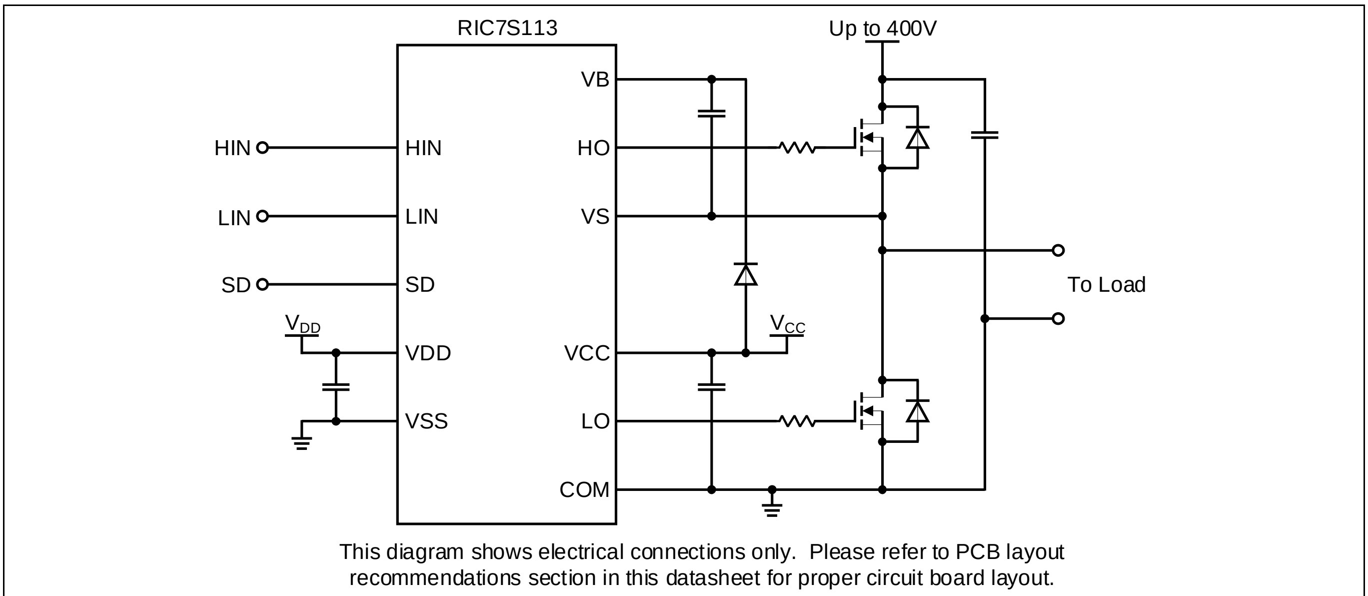


Figure 1 **Typical half bridge application block diagram**

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1 Block diagram

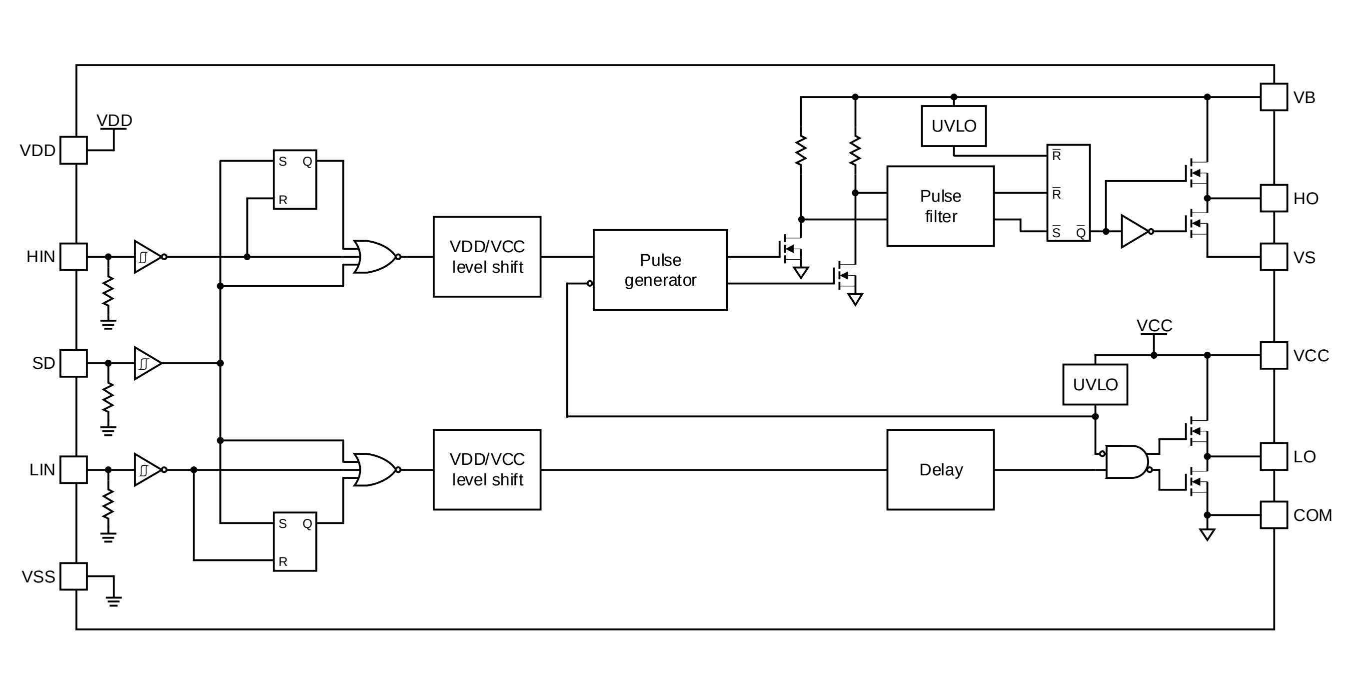
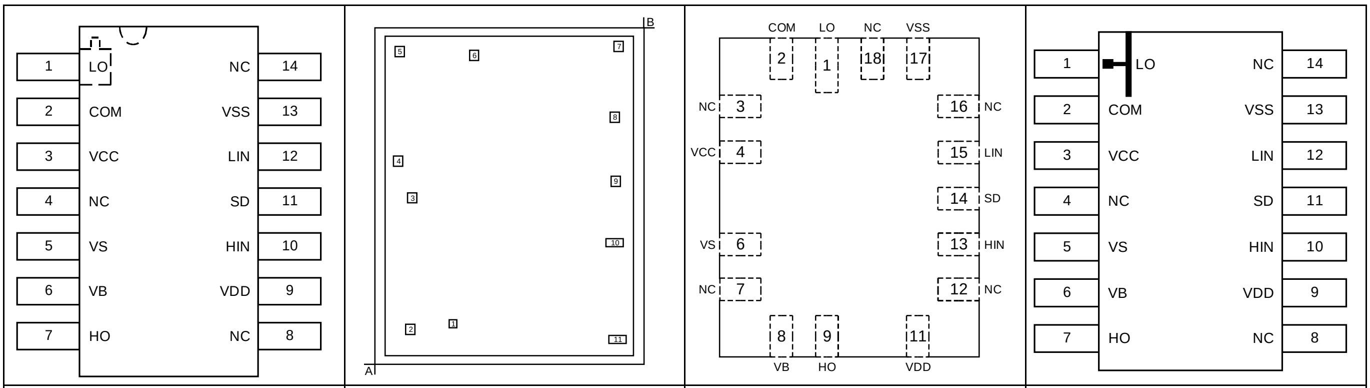


Figure 2 Block diagram

2 Pin configuration and functionality

2.1 Pin configuration



14 lead Flatpack	Die	18 pin LCC CIC	MO-036AB CIC
RIC7S113A4	RIC7S113C4	RIC7S113E4	RIC7S113L4

Figure 3 RIC7S113 pin assignments (top view)

Table 2 Die information for RIC7S113

Parameter		Length (µm)
Front metal	Aluminum	2.0
Back metal	Ti	0.1
	NiV	0.2
	Ag	0.6
Die size	x	2540.00
	y	3215.00
	x, y tolerance	±200
	Thickness	305
	Thickness tolerance	±20

Table 3 Bond pad coordinates for RIC7S113C4

Pad number	Pad name	x (µm)[1]	y (µm)[1]	Δx (µm)[2]	Δy (µm)[2]	Tolerance (µm)
1	HO	0.00	0.00	148.00	155.00	±5
2	VB	-422.00	-45.00	150.00	150.00	±5
3	VS	-401.00	1228.00	148.00	155.00	±5
4	VCC	-530.00	1582.00	150.00	150.00	±5
5	COM	-522.00	2658.00	148.00	155.00	±5
6	LO	183.00	2607.00	148.00	155.00	±5
7	VSS	1576.00	2684.00	152.00	152.00	±5
8	LIN	1537.00	2002.00	152.00	152.00	±5
9	SD	1537.00	1401.00	152.00	152.00	±5
10	HIN	1537.00	797.00	152.00	152.00	±5
11	VDD	1567.00	-149.00	152.00	152.00	±5

Pad number	Pad name	x (µm)[1]	y (µm)[1]	Δx (µm)[2]	Δy (µm)[2]	Tolerance (µm)
Ref point A		-671.70	-222.70			±200
Ref point B		1868.30	2992.30			±200

[1] Bottom left corner of bond pad (corner closest to reference point A)

[2] Distance from end to end of bond pad along corresponding dimension.

2.2 Pin functionality

Table 4 Pin functionality

Pin RIC7S113A4 RIC7S113L4	Pad RIC7S113C4	Pin RIC7S113E4	Symbol	Description
1	6	1	LO	Low side gate drive output
2	5	2	COM	Low side gate drive return
3	4	4	VCC	Low side gate drive supply
5	3	6	VS	High side floating supply return
6	2	8	VB	High side floating supply
7	1	9	HO	High side gate drive output
9	11	11	VDD	Logic supply
10	10	13	HIN	Logic input for high side gate driver output (HO), in phase with HO
11	9	14	SD	Logic input for shutdown
12	8	15	LIN	Logic input for low side gate driver output (LO), in phase with LO
13	7	17	VSS	Logic return
4, 8, 14		3, 7, 12, 16, 18	NC	No connect. This pin may be connected to VSS, COM or left floating
Lid	Backside	Lid		No connection. It may be connected to VSS, COM or left floating

3 Electrical parameters

3.1 Absolute maximum ratings

Absolute maximum ratings indicate limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table.

Table 5 Absolute maximum ratings

Symbol	Definition	Min	Max	Units
V_B	High side floating supply voltage	-0.5	V_S+20	V
V_S	High side floating supply offset voltage		400	V
V_{HO}	High side floating output voltage	V_S-0.5	V_B+0.5	V
V_{CC}	Low side fixed supply voltage	-0.5	20	V
V_{LO}	Low side output voltage	-0.5	V_{CC}+0.5	V
V_{DD}	Logic supply voltage	-0.5	V_{SS}+20	V
V_{SS}	Logic supply offset voltage	V_{CC}-20	V_{CC}+0.5	V
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS}-0.5	V_{DD}+0.5	V
dV_S/dt	Allowable offset supply voltage transient[1]		50	V/ns
T_J	Operating junction temperature	-55	125	°C
T_S	Storage temperature	-55	150	°C
T_L	Lead temp (soldering, 10s, 0.063in (1.6mm) from case)		300	°C
W	Weight RIC7S113A4	0.6 (typ)		g
W	Weight RIC7S113E4	0.42 (typ)		g
W	Weight RIC7S113L4	1.3 (typ)		g

[1] Refer to Figure 8 for test circuit

3.2 ESD ratings

Table 6 ESD ratings

Symbol	Definition	Value	Units
V_{ESD}	ESD Human Body Model (HBM), Class 1C per MIL-STD-883, Method 3015	1.0	kV

3.3 Thermal characteristics

All ratings are measured under board mounted and still air conditions.

Table 7 Thermal Characteristics

Symbol	Definition	Min	Typ	Max	Units
RIC7S113A4					
$R_{\Theta JC}$	Thermal resistance, junction to case		12	15.9	°C/W
$R_{\Theta JLEAD}$	Thermal resistance, junction to lead[1]		150		°C/W
$R_{\Theta JLID}$	Thermal resistance, junction to lid[1]		27		°C/W
RIC7S113E4					
$R_{\Theta JC}$	Thermal resistance, junction to case		12	15.6	°C/W

Symbol	Definition	Min	Typ	Max	Units
$R_{\Theta JLEAD}$	Thermal resistance, junction to lead[1]		23		°C/W
$R_{\Theta JLID}$	Thermal resistance, junction to lid[1]		29		°C/W
RIC7S113L4					
$R_{\Theta JC}$	Thermal resistance, junction to case		13	16.4	°C/W
$R_{\Theta JLEAD}$	Thermal resistance, junction to lead[1]		120		°C/W
$R_{\Theta JLID}$	Thermal resistance, junction to lid[1]		24		°C/W

[1] Guaranteed by design, not tested

3.4 Recommended operating conditions

For proper operation the device should be used within the recommended operating conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated. The V_S and V_{SS} offset ratings are tested with V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V.

Table 8 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_B	High side floating supply absolute voltage	V_S+10	V_S+20	V
V_S	High side floating supply offset voltage	-4	400	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{DD}	Logic supply voltage	V_{SS}+5	V_{SS}+20	V
V_{SS}	Logic supply offset voltage	-5	5	V
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	V

3.5 Static electrical characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V and T_A = T_J = -55 to 125°C unless otherwise stated. V_{IN} ($V_{IH,}$ V_{IL}), V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input pins (HIN, LIN and SD). The V_O and I_O parameters are referenced to COM or V_S and are applicable to the respective output pins (HO or LO). **Parameter ratings that are stated post-irradiation apply over a total ionizing dose (TID) of 100krad(Si) with exposure at a high dose rate (HDR) of 50-300 rad(Si)/s.**

Table 9 Static electrical characteristics

Symbol	Definition	Group A Subgroup[1]	Min	Typ	Max	Units	Test Conditions
Bias power							
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	1	7.5		9.7	V	T_J=25°C, **Post-irradiation**
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	1	7.0		9.4	V	T_J=25°C, **Post-irradiation**
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	1	7.4		9.6	V	T_J=25°C
		1	7.4		9.9	V	T_J=25°C, **Post-irradiation**

Symbol	Definition	Group A Subgroup[1]	Min	Typ	Max	Units	Test Conditions
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	1	7.0		9.4	V	T_J=25°C
		1	7.0		9.6	v	T_J=25°C, **Post-irradiation**
I_{QBS}	Quiescent V_{BS} supply current	1			230	µA	V_{IN}=0 V or VDD, T_J=25°C, **Post-irradiation**
		2, 3			500	µA	V_{IN}=0 V or VDD
I_{QCC}	Quiescent V_{CC} supply current	1			340	µA	V_{IN}=0 V or VDD, T_J=25°C, **Post-irradiation**
		2, 3			600	µA	V_{IN}=0 V or VDD
I_{QDD}	Quiescent V_{DD} supply current	1			30	µA	V_{IN}=0 V or VDD, T_J=25°C, **Post-irradiation**
		2, 3			60	µA	V_{IN}=0 V or VDD
I_{LK}	Offset supply leakage current	1			50	µA	VB=VS=400 V, T_J=25°C, **Post-irradiation**
		2, 3			250	µA	VB=VS=400 V
Input							
V_{IH}	Logic "1" input voltage	1	3.1			V	VDD=5 V, T_J=25°C, **Post-irradiation**
		2, 3	3.3			V	VDD=5V
		1	6.4			V	VDD=10 V, T_J=25°C, **Post-irradiation**
		2, 3	6.8			V	VDD=10 V
		1	9.5			V	VDD=15 V, T_J=25°C, **Post-irradiation**
		2, 3	10			V	VDD=15 V
		1	12.5			V	VDD=20 V, T_J=25°C, **Post-irradiation**
		2, 3	13.3			V	VDD=20 V
V_{IL}	Logic "0" input voltage	1			1.6	V	VDD=5 V, T_J=25°C, **Post-irradiation**
		2, 3			1.6	V	VDD=5 V
		1			3.8	V	VDD=10 V, T_J=25°C, **Post-irradiation**
		2, 3			3.6	V	VDD=10 V
		1			6.0	V	VDD=15 V, T_J=25°C, **Post-irradiation**
		2, 3			5.7	V	VDD=15 V
V_{IL}	Logic "0" input voltage	1			8.3	V	VDD=20 V, T_J=25°C, **Post-irradiation**
		2, 3			7.9	V	VDD=20 V
I_{IN+}	Logic "1" input bias current	1			40	µA	V_{IN}=V_{DD}, T_J=25°C, **Post-irradiation**

Symbol	Definition	Group A Subgroup[1]	Min	Typ	Max	Units	Test Conditions
I_{IN+}	Logic “1” input bias current	2, 3			70	µA	$V_{IN}=V_{DD}$
I_{IN-}	Logic “0” input bias current	1			1.0	µA	V_{IN}=0V, T_J=25°C, **Post-irradiation**
		2, 3			10	µA	V_{IN}=0 V
Output							
V_{OH}	High level output voltage (V_{CC}-V_{LO}, V_B-V_{HO})	1			1.2	V	$V_{IN}=V_{IH}$, I_O=0 A, T_J=25°C, **Post-irradiation**
		2, 3			1.5	V	$V_{IN}=V_{IH}$, I_O=0 A
V_{OL}	High level output voltage ($V_{LO,}$ V_{HO})	1			0.1	V	$V_{IN}=V_{IL}$, I_O=0 A, T_J=25°C, **Post-irradiation**
		2, 3			0.1		$V_{IN}=V_{IL}$, I_O=0 A
I_{O+}	Output high short circuit pulsed current[2]	1, 2, 3	2.0			A	V_O=0V, V_{IN}=VDD, PW≤10 µs, **Post-irradiation**
I_{O-}	Output low short circuit pulsed current[2]	1, 2, 3	2.0			A	V_O=0V, V_{IN}=0V, PW≤10 µs, **Post-irradiation**

[1] Per MIL-STD-883 Method 5005

[2] Parameter not subject to production test. Parameter guaranteed by design and characterization

3.6 Dynamic electrical characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V, VSS=COM and T_A = T_J = -55 to 125°C unless otherwise stated. **Parameter ratings that are stated post-irradiation apply over a total ionizing dose (TID) of 100krad(Si) with exposure at a high dose rate (HDR) of 50-300 rad(Si)/s.**

Table 10 Dynamic electrical characteristics

Symbol	Definition	Group A Subgroup[1]	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	9		120	150	ns	VS=0 V, T_J=25°C
		10, 11			260	ns	VS=0 V
t_{off}	Turn-off propagation delay	9		100	125	ns	VS=400 V, T_J=25°C
		10, 11			220	ns	VS=400 V
t_{sd}	Shutdown propagation delay	9		110	140	ns	VS=400 V, T_J=25°C
		10, 11			235	ns	VS=400 V
t_r	Turn-on rise time	9		25	35	ns	C_L=1000 pF, T_J=25°C
		10, 11			50	ns	C_L=1000 pF
t_f	Turn-off fall time	9		17	25	ns	C_L=1000 pF, T_J=25°C
t_f	Turn-off fall time	10, 11			40	ns	C_L=1000 pF
MT	Delay matching, HS & LS turn-on/off	9		5	20	ns	$\lvert H_{ton}-L_{ton}\rvert$ or $\lvert H_{toff}-L_{toff}\rvert$ T_J=25°C

[1] Per MIL-STD-883 Method 5005

4 Timing diagrams and test schematics

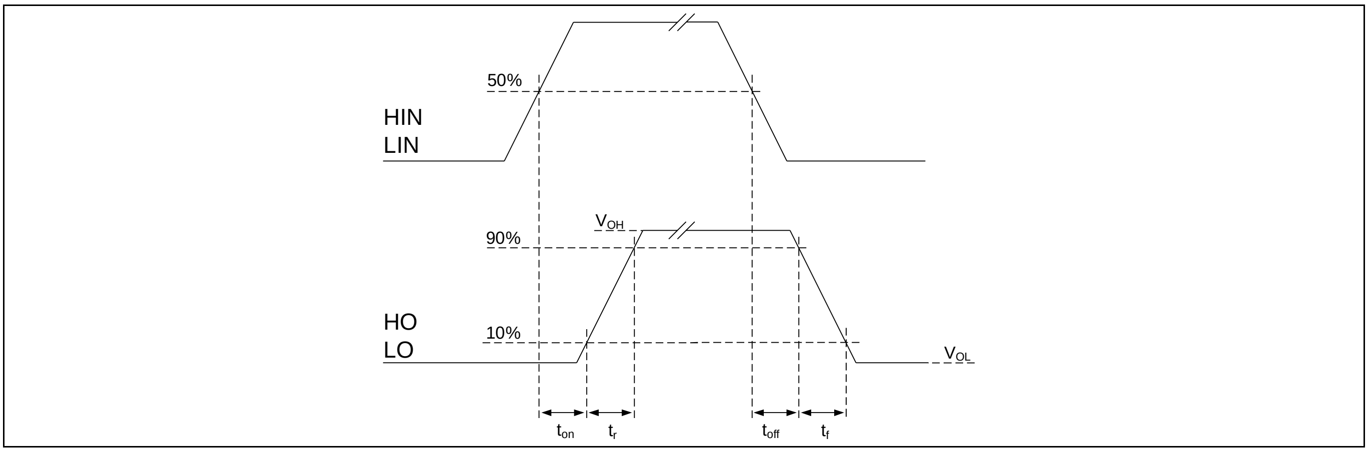


Figure 4 **Propagation delay, rise and fall time definition**

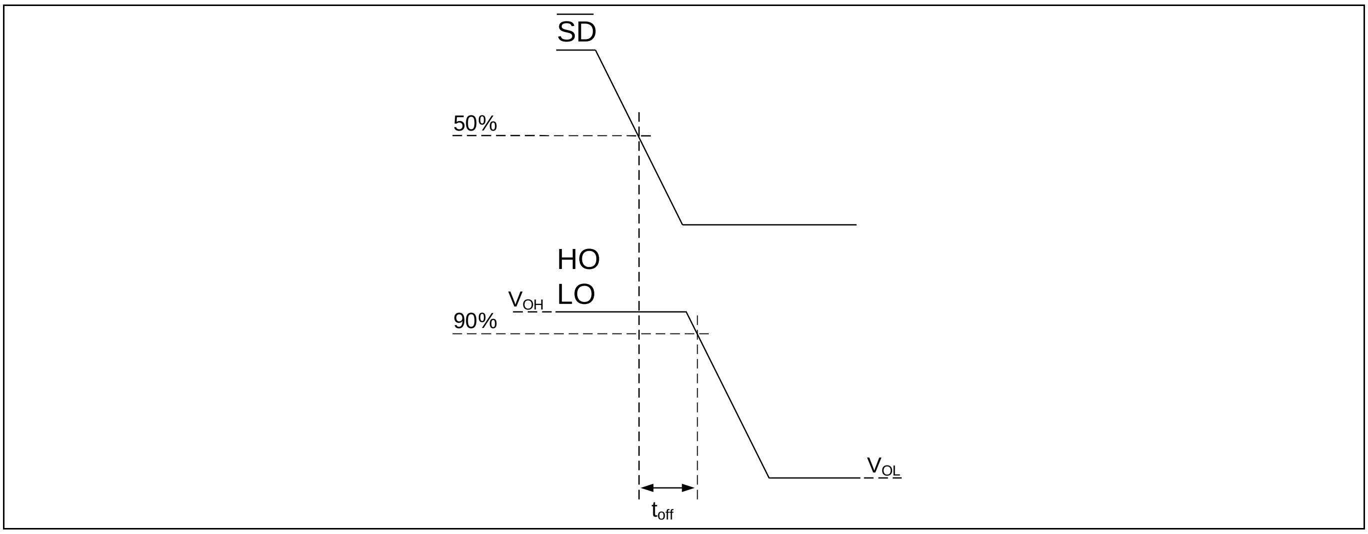


Figure 5 **Shutdown waveform definitions**

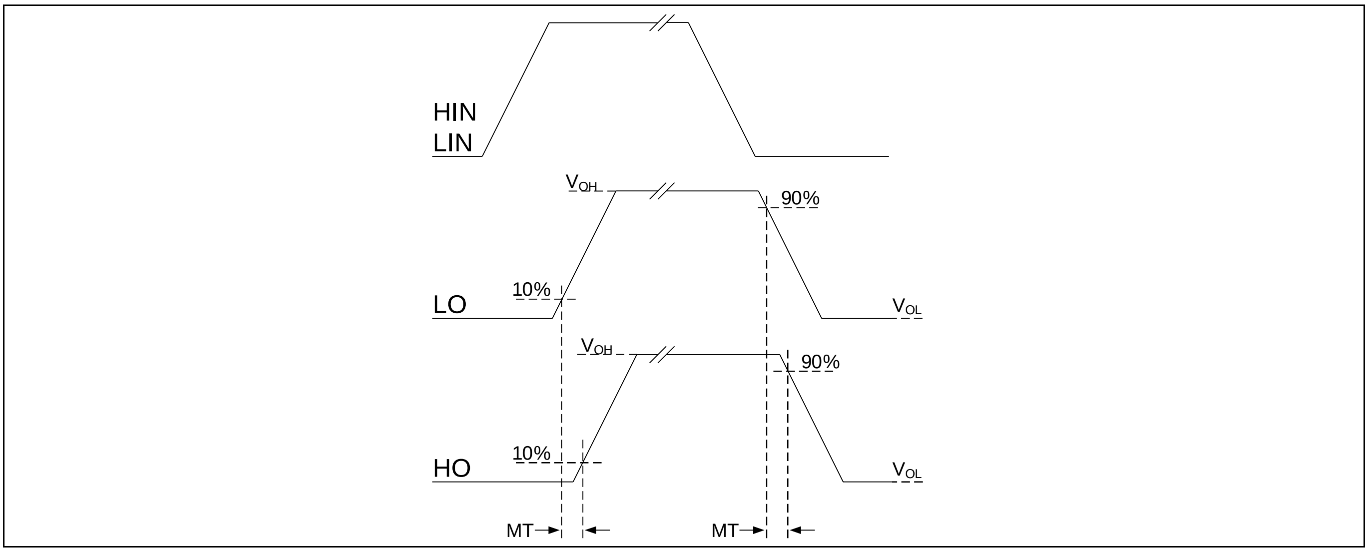


Figure 6 **Delay matching waveform definitions**

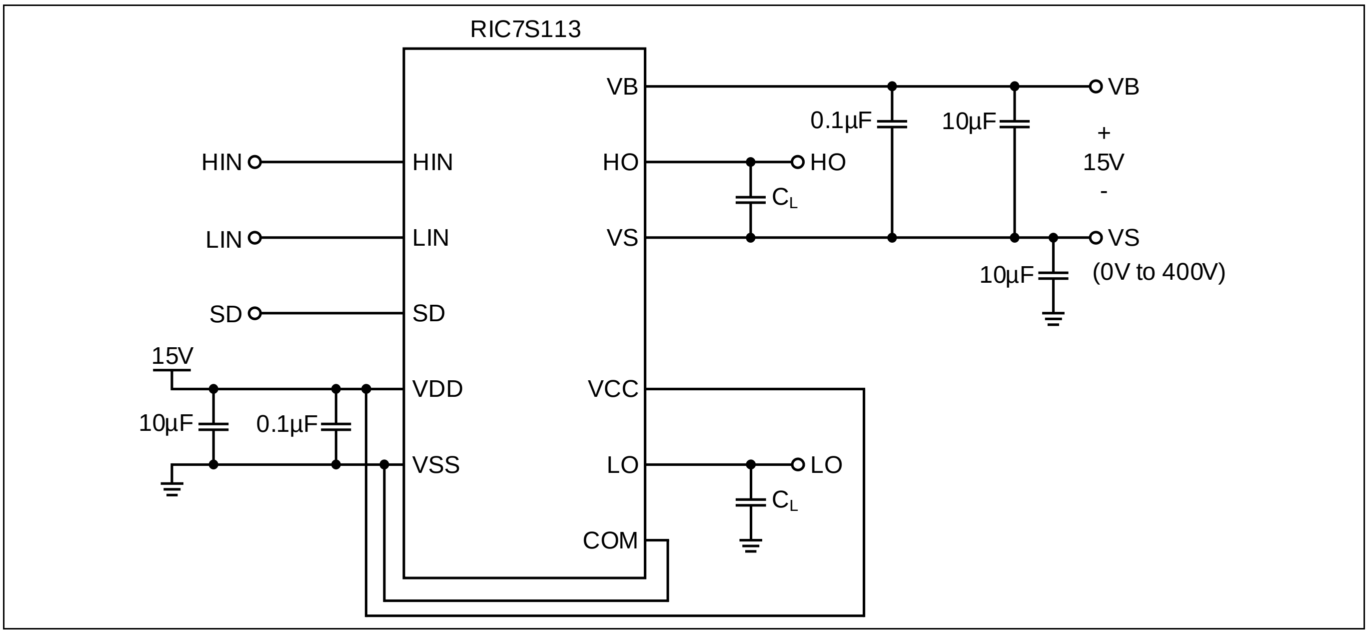


Figure 7 **Switching time test circuit**

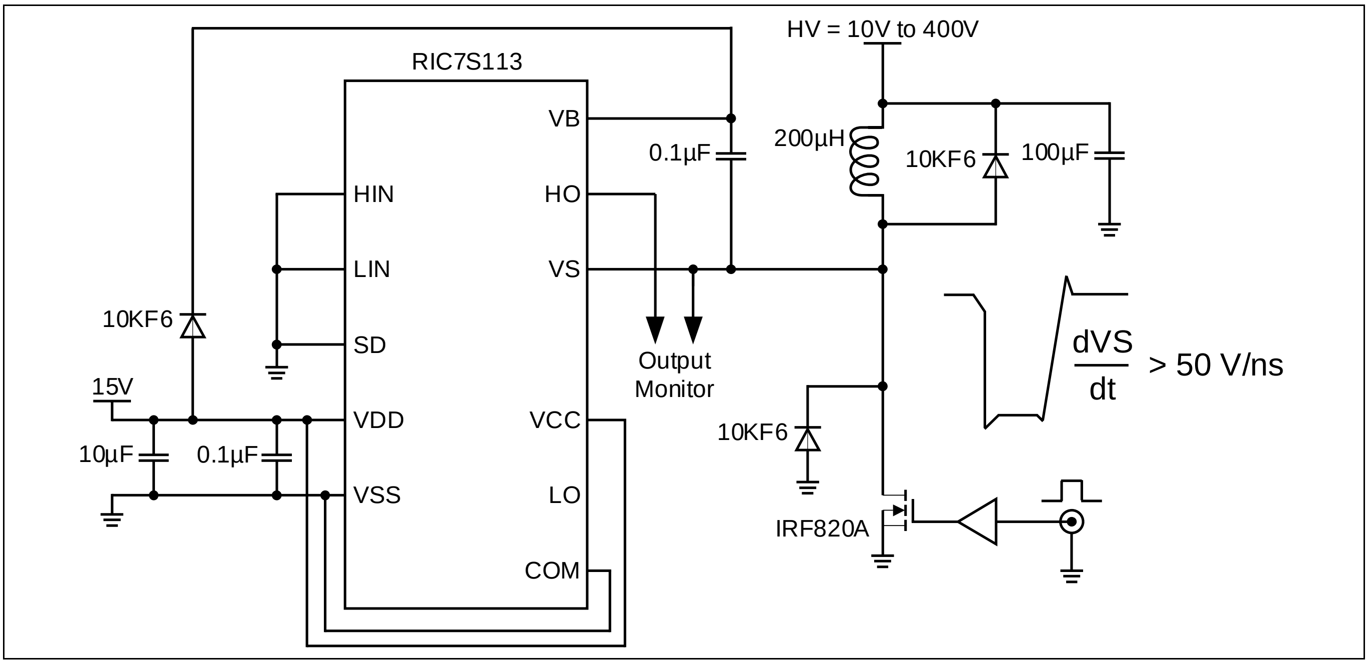


Figure 8 **Floating supply voltage transient test circuit**

5 Typical characteristics

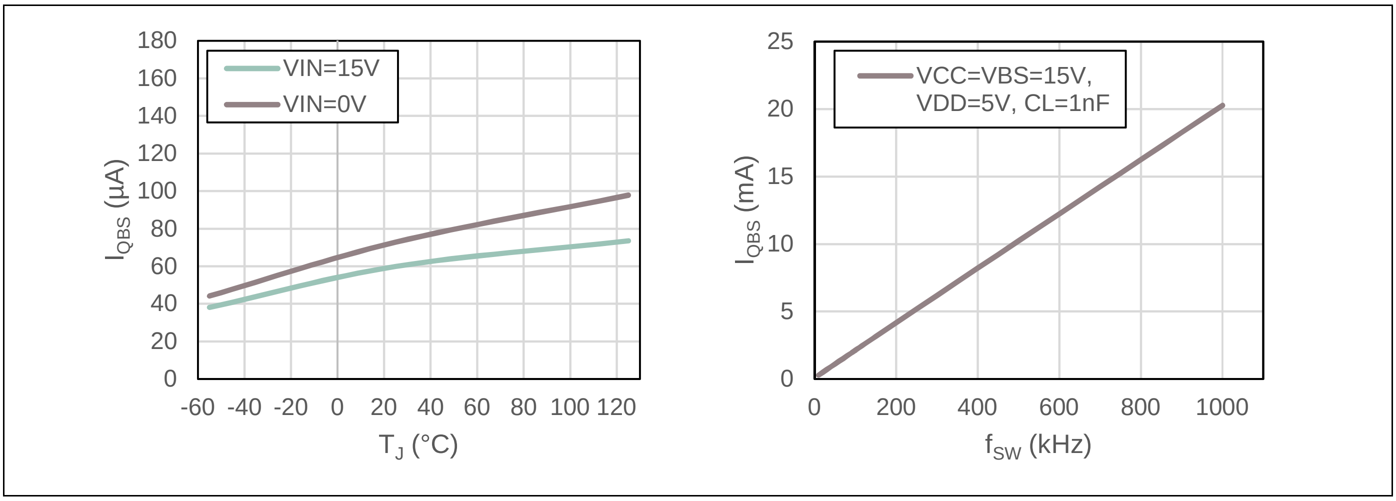


Figure 9 I_{QBS} over temperature and frequency

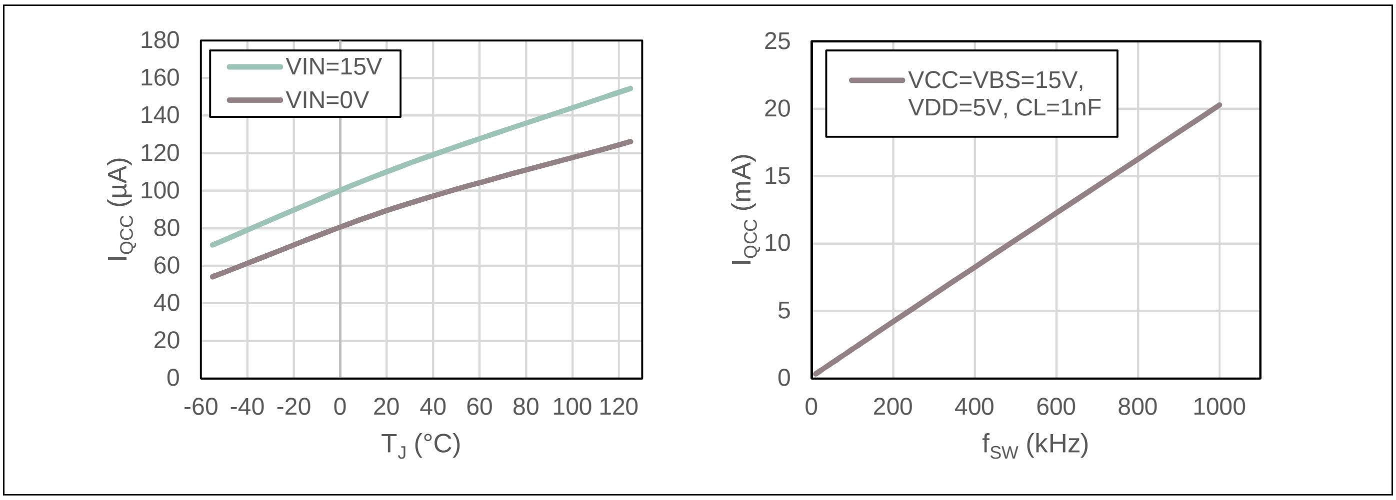


Figure 10 I_{QCC} over temperature and frequency

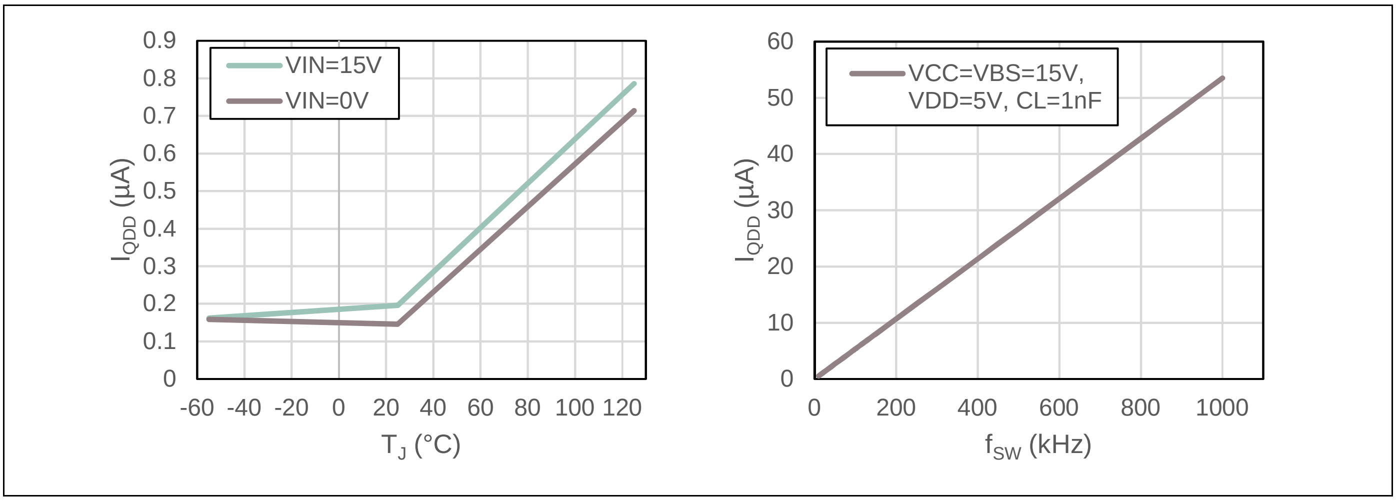


Figure 11 I_{QDD} over temperature and frequency

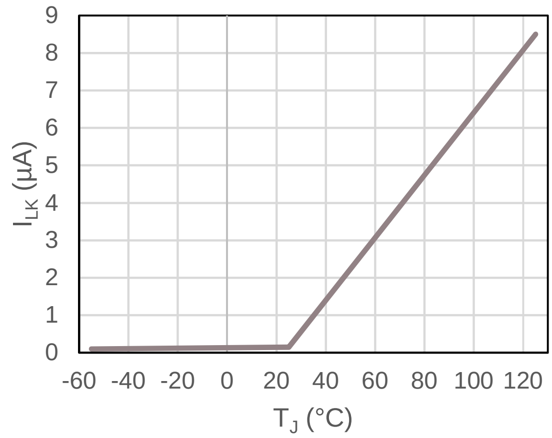


Figure 12 I_{LK} over temperature

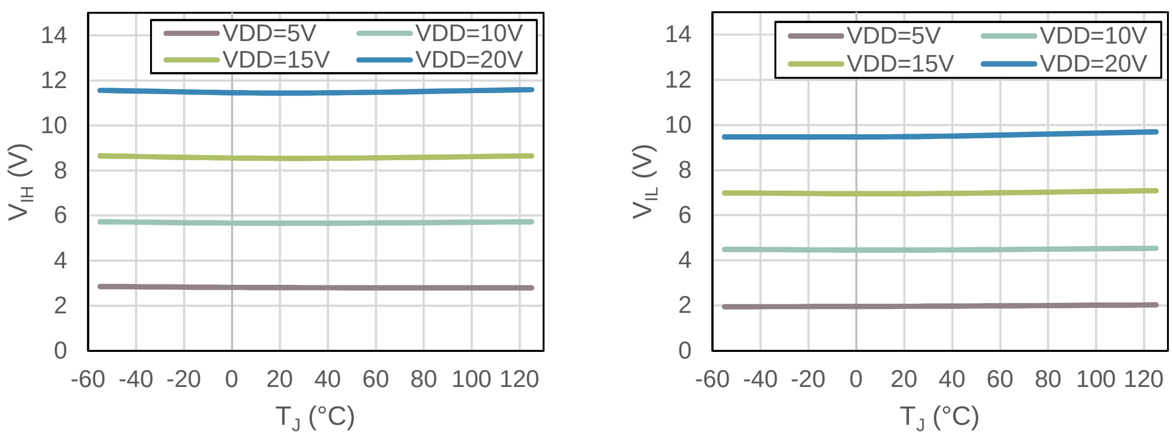


Figure 13 V_{IH} and V_{IL} over temperature

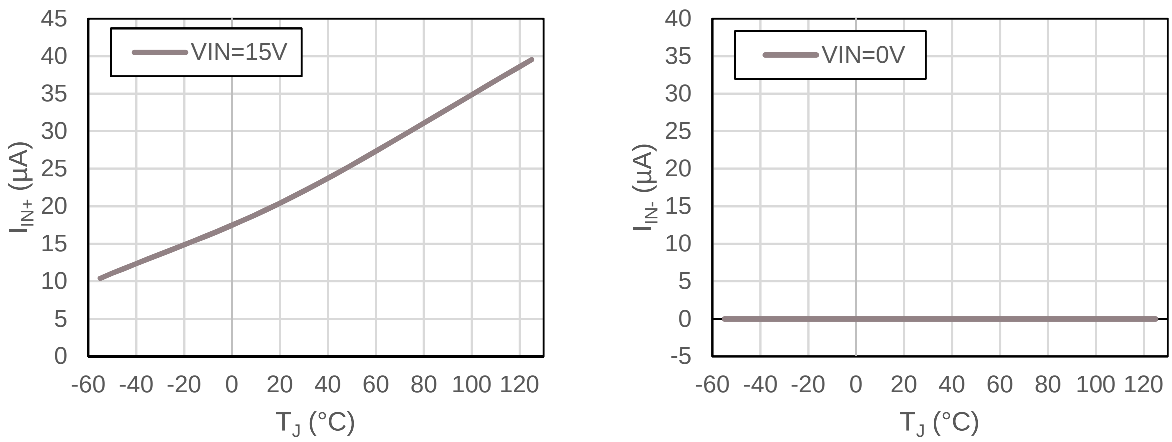


Figure 14 I_{IN+} and I_{IN-} over temperature

Typical characteristics

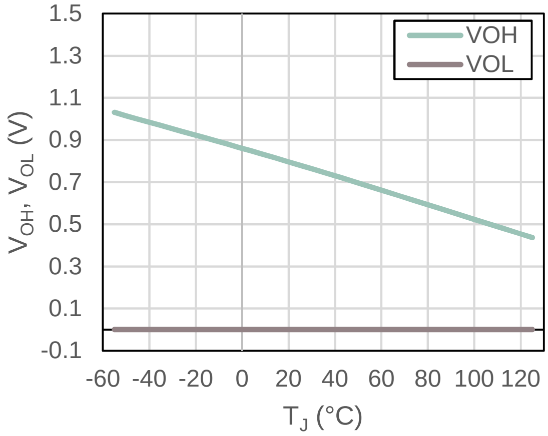


Figure 15 **V_{OH} and V_{OL} over temperature**

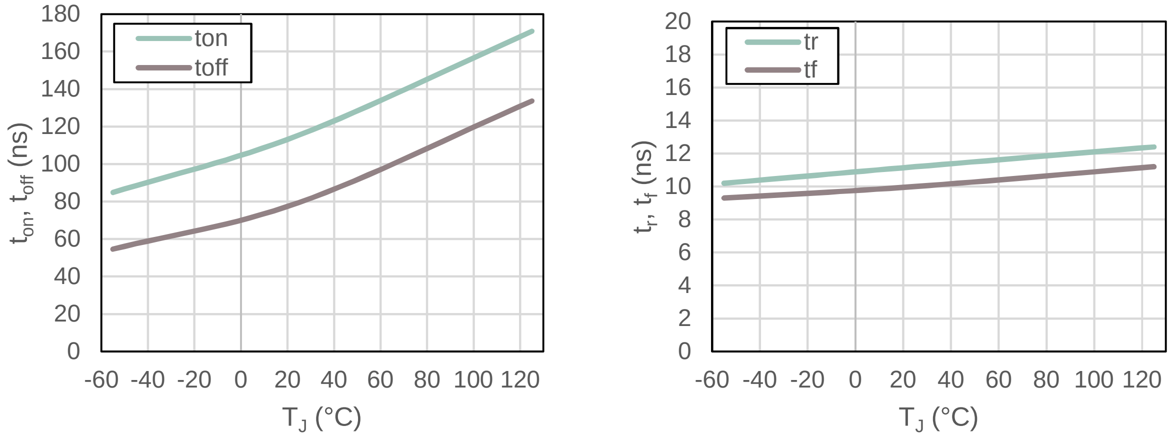


Figure 16 **t_{on}, t_{off}, t_r and t_f over temperature**

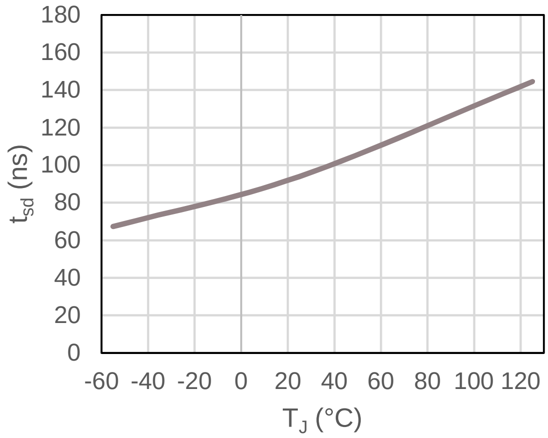


Figure 17 **t_{sd} over temperature**

6 Application information and additional details

RIC7S113 is a rad hard high and low side driver that supports voltages up to 400 V. It features high current slew rate and low source impedance on the output, thus generating high current pulses with very small rise times. This facilitates high efficient driving of power FET, such as the R9 MOSFET and rad hard PowerMOS, along with IGBT. An evaluation board RIC7S113EVAL1 demonstrates the performance of RIC7S113 with BUY65CS08J-01. Details of this design, including test results, are in the RIC7S113EVAL1 user guide.

For more information on general definitions for terms used throughout this datasheet, please refer to the application note Understanding HVIC Datasheet Specifications.

6.1 Radiation performance

RIC7S113 is designed to work in space and other applications where there is significant ionizing radiation and energetic particles in the environment that can affect microcircuit performance. RIC7S113 is characterized for operation up to a total ionizing dose (TID) of 100 krad, with electrical parameters including limits post-irradiation. It is also characterized for single event effects (SEE) up to 81.9 MeV·cm²/mg.

The packaged versions of RIC7S113 have several NC pins and metal lid. All of these metal points are isolated from one another and are electrically floating. Typically in space and other irradiation environments, it is desired for all conductors to be connected to known potentials, since floating metal can build up charge and lead to undesired effects. To satisfy this requirement all the NC pins and metal lid can be connected to COM or VSS. It is recommended to ensure that any connection made does not violate any creepage or clearance spacing requirement.

6.1.1 Total ionizing dose (TID)

RIC7S113 is tested over total ionizing dose (TID) to verify robustness to ionizing protons and electrons radiation environments, such as space. The radiation hardness assurance (RHA) program at IR HiRel uses a Cobalt-60 (60 Co) source and heavy ion irradiation. Every wafer is tested per MIL-STD-883, Method 1019, test condition A "Ionizing Radiation (Total Dose) Test Procedure." Both pre- and post-irradiation performance are tested to the limits specified in the electrical characteristics. For details on TID hardness refer to the RIC7S113 TID test report.

6.1.2 Single event effects (SEE)

RIC7S113 has been characterized in heavy ion environment for single event effects (SEE) for both destructive events, such as single event burnout (SEB) and single event gate rupture (SEGR), as well as transient events, such as single event transient (SET) and single event functional interrupt (SEFI). Summary of results are shown below, and details are in the RIC7S113 SEE test report.

Table 11 Single event effect (SEE) safe operating area (SOA)

Ion	LET (MeV·cm²/mg)	Energy (MeV)	Range (µm)	V_{CC}, V_{DD} (V)	V_S (V)		
					V_B=10V	V_B=15V	V_B=17.5V
^{84}Kr	27.8	1084	139.8	20	400	400	400
^{129}Xe	54.5	1591	117.3	20	275	175	125
^{197}Au	81.9	2432	130.5	17.5	100	75	50

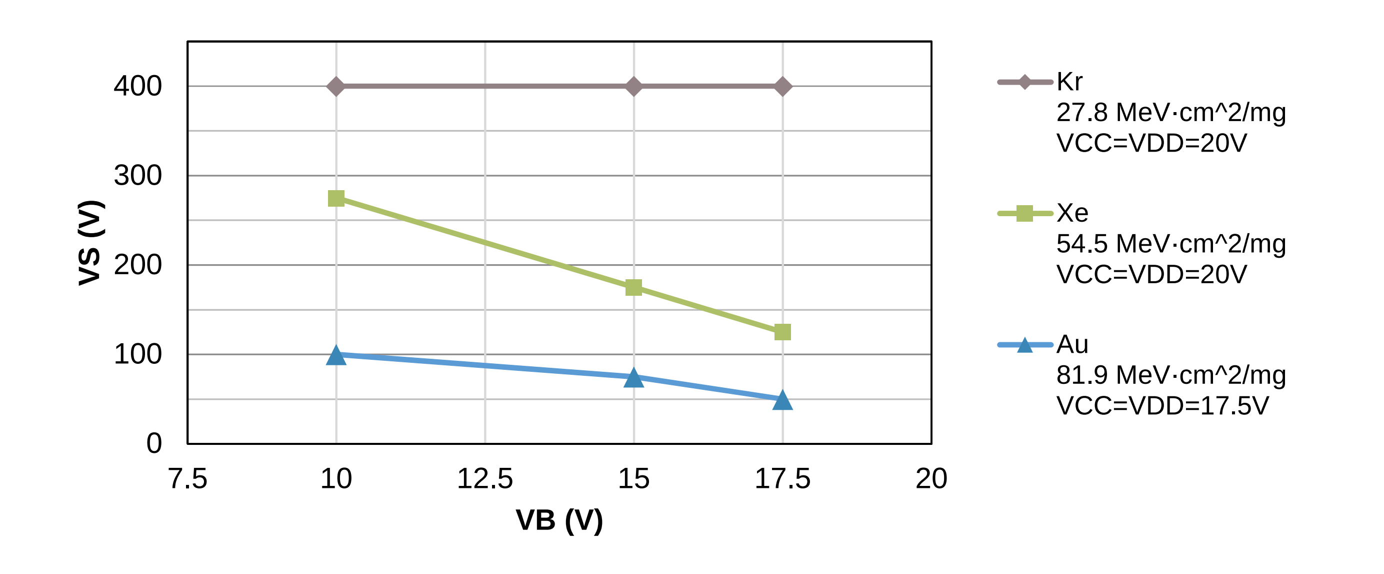


Figure 18 Single event effect (SEE) safe operating area (SOA)

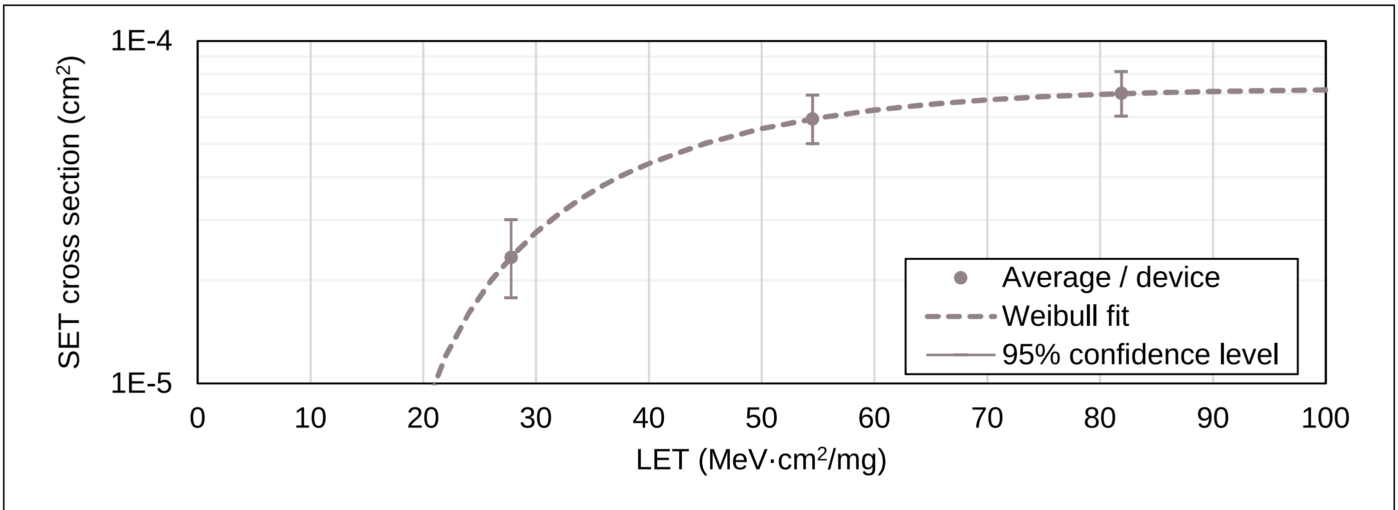


Figure 19 Single event transient (SET) cross section of LO and HO for dynamic tests

6.2 Bias power

RIC7S113 has three different bias power pins with respective returns: VDD to VSS for input logic power, VCC to COM for low side drive power and VB to VS for high side drive power. By dividing logic and power bias power to different pins, the current loops for each supply are separated. This helps prevent noise from the gate drive from interfering with sensitive logic signals. VSS and COM can be shorted together, and it is recommended to make this connection in a place where power stage and input logic current loops will not interfere with one another.

6.2.1 Bootstrap for high side bias power

For the high side drive a separate bias supply V_B is required. This separate bias is required since the return point for the high side drive V_S is floating and can vary during operation. The simplest and most common technique to generate the high side bias supply is with a bootstrap diode and capacitor. The way this circuit works is that when the low side switch Q_L is on, and high side switch Q_H is off, the bootstrap capacitor C_B is charged up to slightly under V_{CC}. When the switches change state, and Q_L is off and Q_H is on, C_B and the charge on it swings up with Q_H. The charge on C_B is then used to keep Q_H on.

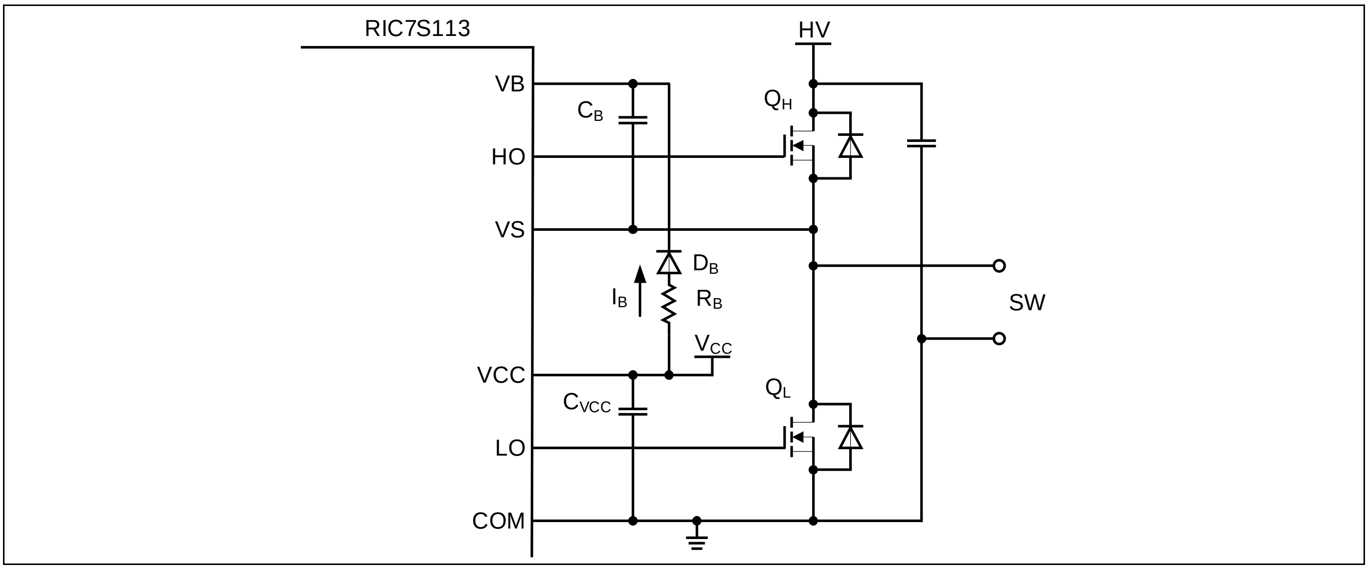


Figure 20 Example bootstrap circuit for high side bias power

For the bootstrap capacitor C_B, the following equation can be used to determine the minimum capacitance, where Q_{GTOT} is the total charge on HO pin and ΔV_{BS} is the maximum allowed voltage drop of V_{BS} when Q_H is high.

$$C_B > \frac{Q_{GTOT}}{\Delta V_{BS}}$$

For Q_{GTOT}, the following equation can be used to determine the total charge.

$$Q_{GTOT} = Q_G + Q_{LS} + \left(I_{QBS} + I_{LKGS} + I_{LK} + I_{LKDIODE} + I_{LKCB}\right) t_{HON}$$

Where

- Q_G is the total gate charge of high side FET, which is specified in the FET datasheet
- Q_{LS} is the internal level shift charge of RIC7S113, which can be approximated to be 5 nC
- I_{QBS} is the floating section quiescent current of RIC7S113, which is specified in Table 9 in the electrical characteristics
- I_{LKGS} is the gate to source leakage current of high side FET, which is specified in the FET datasheet
- I_{LK} is the floating section leakage current of RIC7S113, which is specified in Table 9 in the electrical characteristics
- $I_{LKDIODE}$ is the leakage current of D_B, which is specified in the diode datasheet
- I_{LKCB} is the leakage current of C_B, which is specified in the capacitor datasheet (0 A can be assumed for a ceramic capacitor)
- t_{HON} is the time that the Q_H is on

For ΔV_{BS}, the following equation can be used to determine the voltage decay.

$$\Delta V_{BS} \leq V_{CC} - V_f - V_{GSmin} - V_{DSon}$$

Where

- V_{CC} is the external V_{CC} voltage, typically the same supply that powers Q_L
- V_F is the forward voltage drop of D_B, which is specified in the diode datasheet

- V_{GSmin} is the desired minimum gate to source drive voltage. This voltage must be above V_{BSUV-}, which is specified in Table 9 in the electrical characteristics
- V_{DSon} is the drain to source voltage of Q_L when it is on

For the bootstrap diode D_B, the voltage rating needs to be high enough to withstand the maximum voltage on VS, which is typically HV when the switches are configured in a half bridge, plus the high side bias voltage V_{BS}. An ultrafast or Schottky diode is recommended to reduce reverse recovery loss from this diode. An external resistor R_B in series with D_B is recommended since it limits the peak current thru D_B. The exact size of R_B needs to tradeoff between maintaining the peak current under the rating of D_B while charging C_B to the desired voltage when Q_L is on. The recommended maximum resistance for R_B is shown below.

$$R_B < \frac{t_{HON}}{3 \times C_B}$$

The following equations can be used to calculate the peak and average bootstrap current, respectively which can be used to estimate power loss for D_B and R_B.

$$I_{Bpk} = \frac{V_{BS}}{R_B}$$

$$I_{Bavg} = \frac{Q_{GTOT}}{t_{HON}}$$

For more information, including calculations with IGBT switches, please refer to the application note Using Monolithic High Voltage Gate Drivers and HV Floating MOS-Gate Driver ICs.

6.2.2 Negative turn off drive

RIC7S113 optionally supports negative turn off voltage with an external negative voltage V_{NEG} applied to COM, as shown in Figure 21. It is recommended to keep the negative voltage -5 V or higher to ensure that RIC7S113 stays within the recommended operating conditions and never exceeds the absolute maximum ratings.

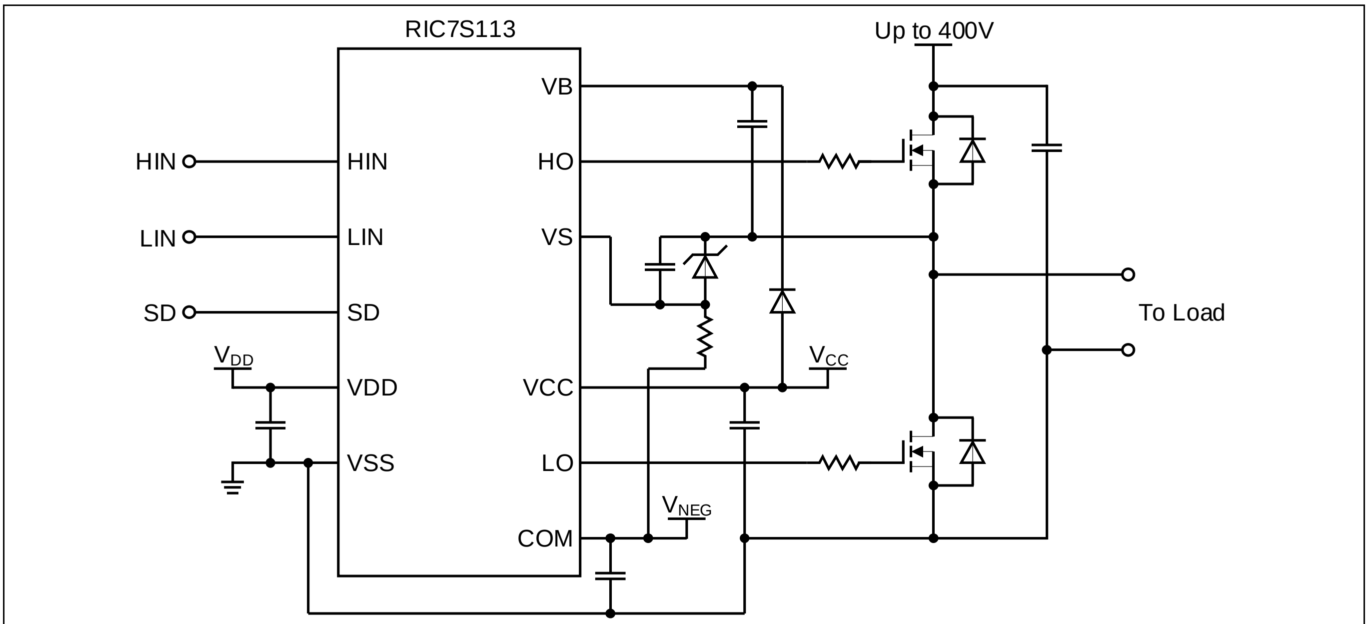


Figure 21 Example negative turn off voltage

For more information on negative turn off, please refer to the application note Using Standard Control ICs to Generate Negative Gate Bias for MOSFETs and IGBTs.

6.3 Input

There are 3 logics inputs, HIN, LIN and SD. HIN and LIN control their corresponding outputs HO and LO, respectively, and SD externally disables operation for both drivers. The relationship between input and output is shown in Figure 22. Note that when shutdown is enabled (SD pulled high), HO and LO will stay low until shutdown is disabled (SD pulled low), then a rising low to high signal is applied to LIN or HIN.

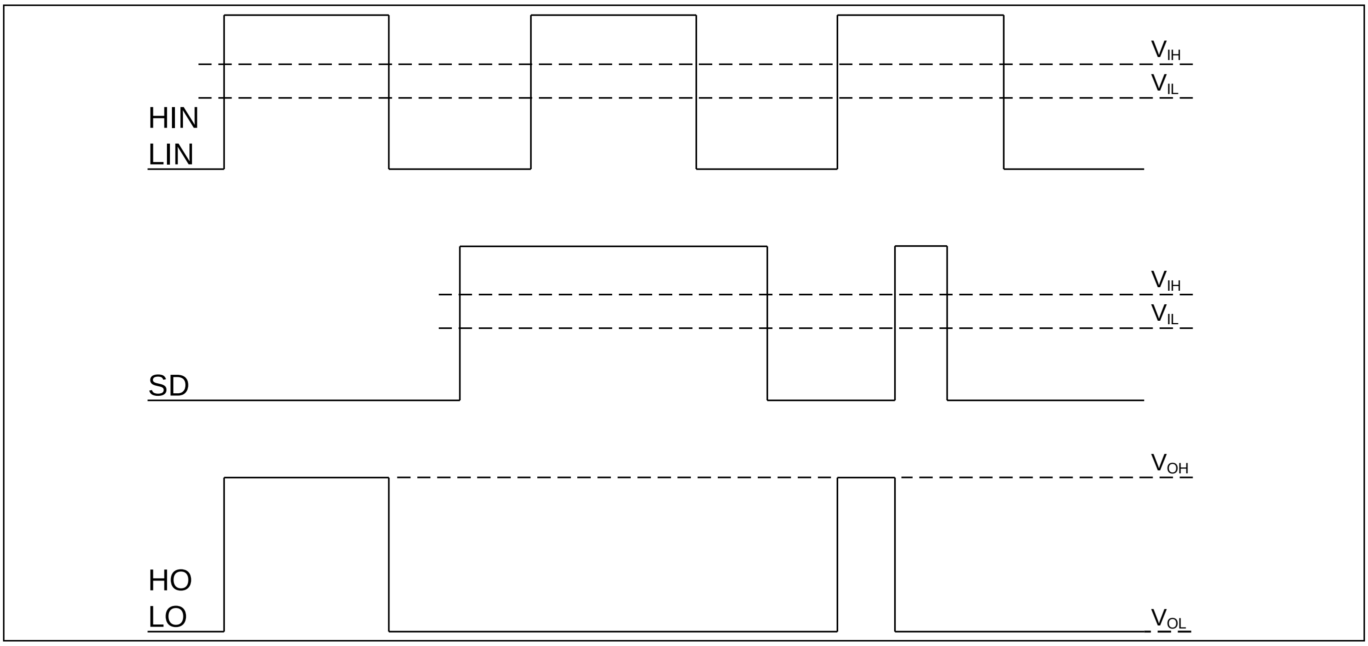


Figure 22 Input/output logic timing diagram

All three inputs support CMOS logic and have low current consumption. They feature Schmitt triggers, which adds hysteresis to enhance noise immunity. This helps ensure that an input signal with low rise time and noise will result in a clean, desired output. They also have internal pull-down resistors, which help ensure that the output voltage is low during initial startup or any instance where the input logic signal has high impedance.

In high noise environments an external RC filter can be placed in front of HIN, LIN and SD. It is recommended to keep the cutoff frequency of this filter as high as possible to prevent phase delays from impacting system performance.

6.3.1 Pulse width

For proper operation it is recommended to keep the minimum logic "1" pulse width for HIN and LIN above 75 ns.

6.4 Output

Each output of RIC7S113 is a high speed 2 A driver, consisting of two n-channel MOSFETs in a totem pole configuration. This configuration helps reduces the turn on and off delay, which in turn lowers switching losses of the power switch that is being driven.

The drive voltage level is dependent on the respective supply voltage, where the drive voltage V_O is the corresponding supply voltage V_{BIAS} (V_{CC} for LO, V_{BS} for HO) minus V_{OH} (which is specified in Table 9 in the electrical characteristics).

$$V_O = V_{BIAS} - V_{OH}$$

6.4.1 External drive resistor

While not always required, an external gate drive resistor is often times used to reduce generated EMI, reduce voltage ringing and lower temperature rise in RIC7S113. This resistance has an undesired side effect of potentially increasing switching loss in the power FET, so to optimize tradeoffs it is important to determine the best value for this resistance.

6.4.1.1 EMI

An external resistor slows down the time it takes to turn on and off the power FET, which in turn reduces the high voltage slew rate seen on the drain of the power FET. This reduction in slew rate lowers the voltage overshoot and ringing often times seen in switched mode power supplies, which is a major source of EMI. The exact resistance depends on the specifics of the design, since EMI filtering is a system level challenge that can be resolved through a combination of many different techniques. Further information on EMI filter design is in the following application note EMC and System-ESD Design Guidelines for Board Layout.

6.4.1.2 Gate voltage ringing

Parasitic inductance from PCB trace and package leads, among others, create a LC resonant tank with the capacitance at the gate of the power FET. This resonant tank causes voltage overshoot and ringing during normal PWM operation. To prevent this ringing from reducing performance or damaging components, a gate drive resistor is often times used to dampen the LC resonant tank. For some designs the internal resistance in RIC7S113 is sufficient, but for others an additional external resistor is needed for proper dampening. The following application note CoolMOS™ gate drive and switching dynamics goes into further details and how to determine the appropriate external resistor.

6.4.1.3 Power loss

During normal operation, the power FET's repeated charging and discharging of the total gate charge causes losses in RIC7S113. If no external resistor is used, these losses are all in RIC7S113 and the corresponding temperature rise can limit the operating range. An external resistor dissipates some of these losses, which in turn reduces the temperature rise in RIC7S113 and extends the effective ambient temperature range. The total loss in RIC7S113 can be calculated with the equations below.

$$P_{on\_int} = \frac{1}{2} \times Q_g \times V_O \times f_{sw} \times \frac{R_{on\_int}}{R_{on\_int} + R_{on\_ext}}$$

$$P_{off\_int} = \frac{1}{2} \times Q_g \times V_O \times f_{sw} \times \frac{R_{off\_int}}{R_{off\_int} + R_{off\_ext}}$$

Where

- Q_g is the total gate charge, which is specified in the FET datasheet
- V_O is the output drive voltage, which can be calculated using the equation in section 6.4
- f_{sw} is the switching frequency, which is selected during the design process
- R_{on_int} is the internal source resistance of RIC7S113, which is typically 2.5 Ω
- R_{on_ext} is the external turn on resistance, which is selected during the design process
- R_{off_int} is the internal turn off resistance of RIC7S113, which is typically 2.5 Ω
- R_{off_ext} is the external turn off resistance, which is selected during the design process

As the equation shows, by increasing the external resistor R_{on_ext} and R_{off_ext} the power loss in RIC7S113 is reduced. Likewise, the power loss for each external resistor can be calculated by modifying these equations.

$$P_{on\_ext} = \frac{1}{2} \times Q_g \times V_{OUT\ A/B} \times f_p \times \frac{R_{on\_ext}}{R_{on\_int} + R_{on\_ext}}$$

$$P_{off\_ext} = \frac{1}{2} \times Q_g \times V_{OUT\ A/B} \times f_p \times \frac{R_{off\_ext}}{R_{off\_int} + R_{off\_ext}}$$

6.4.2 Separate turn on and off resistance

Often times it is determined and desired to have a separate external resistor for turn on and turn off. This can be achieved by using a fast diode in series with a resistor in parallel with another resistor.

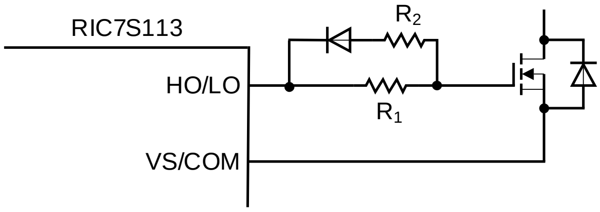


Figure 23 External gate drive resistor with separate turn on and off speed

The corresponding external turn on R_{on} and turn off R_{off} resistance can be calculated with the following equations.

$$R_{on} = R_1$$

$$R_{off} = R_1 || R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

For the diode selection, it is recommended to select a blocking voltage that is high enough to support V_{OUT} plus any voltage overshoot. For high frequency operation a Schottky diode is recommended to reduce losses.

6.5 Switching and timing relationship

The high and low side drive are independently operated from HO and LO pins, respectively. RIC7S113 features propagation delay matching MT between the two drivers. This matching helps reduce the required dead time, which in turn helps reduce the losses during switching transition. For PWM input it is recommended to have a dead time, where both inputs are logic low, that is larger than MT.

6.6 PCB layout recommendations

To achieve high performance a good PCB layout is required. A poor layout can introduce parasitic inductance and capacitance, which couple with electrical noise that interferes with operation. Below are some recommendations to reduce these undesired effects, with example show in figure 23 and figure 24.

- Input RC filter: if RC filter used on input pins place as close to input pins HIN, LIN and SD to VSS as possible
- Bias power bypass capacitor: place bypass/bootstrap capacitors (VDD to VSS, VCC to LO, VB to VS) as close to RIC7S113 as possible with short trace lengths to both pins
- Minimize gate drive loop: keep trace from HO/LO to gate of FET, source of FET to VS/COM short as possible
- Power FET source Kelvin connection: have an independent trace from COM/VS to the source pin of the corresponding FET (or as close to the source pin as possible)
- Isolate noise: keep sensitive logic signals (HIN, LIN, SD) far away from the high voltage switch node (any potential connected to VS) and other high electrical noise sources

- Ground plane: to reduce noise coupling, any ground plane should not be placed underneath or near the high voltage floating side
- Isolate ground loops: keep separate ground for logic and power, with logic pins HIN, LIN and SD referenced to VSS, power output LO referenced to COM and power output HO referenced to VS
- Minimize parasitic inductance: keep key high current loops (gate drive, power stage) as small as possible to reduce parasitic inductance, which can cause voltage overshoot and ringing

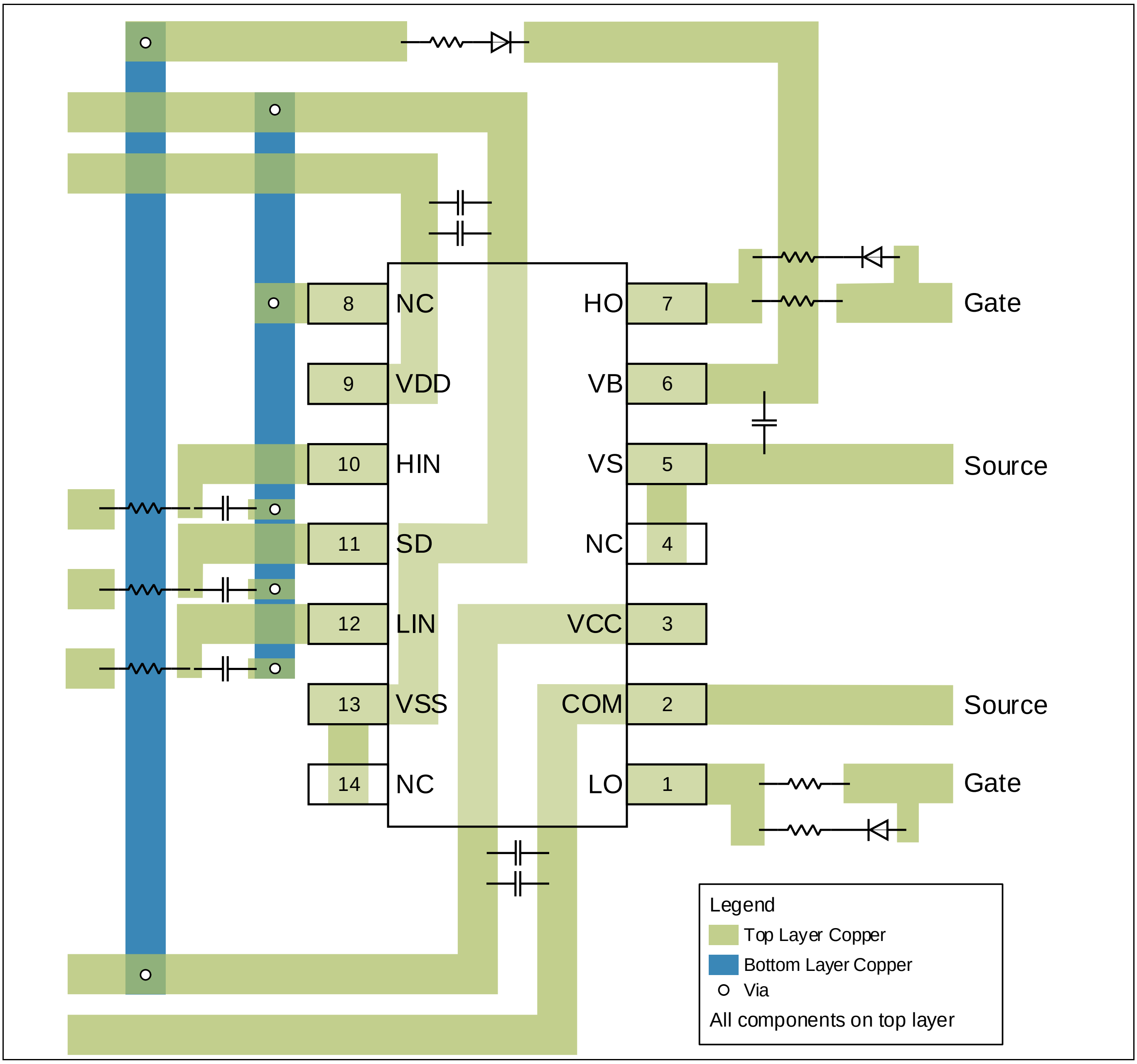


Figure 24 **Recommended PCB layout for RIC7S113A4 (Flatpack) and RIC7S113L4 (MO-036AB CIC)**

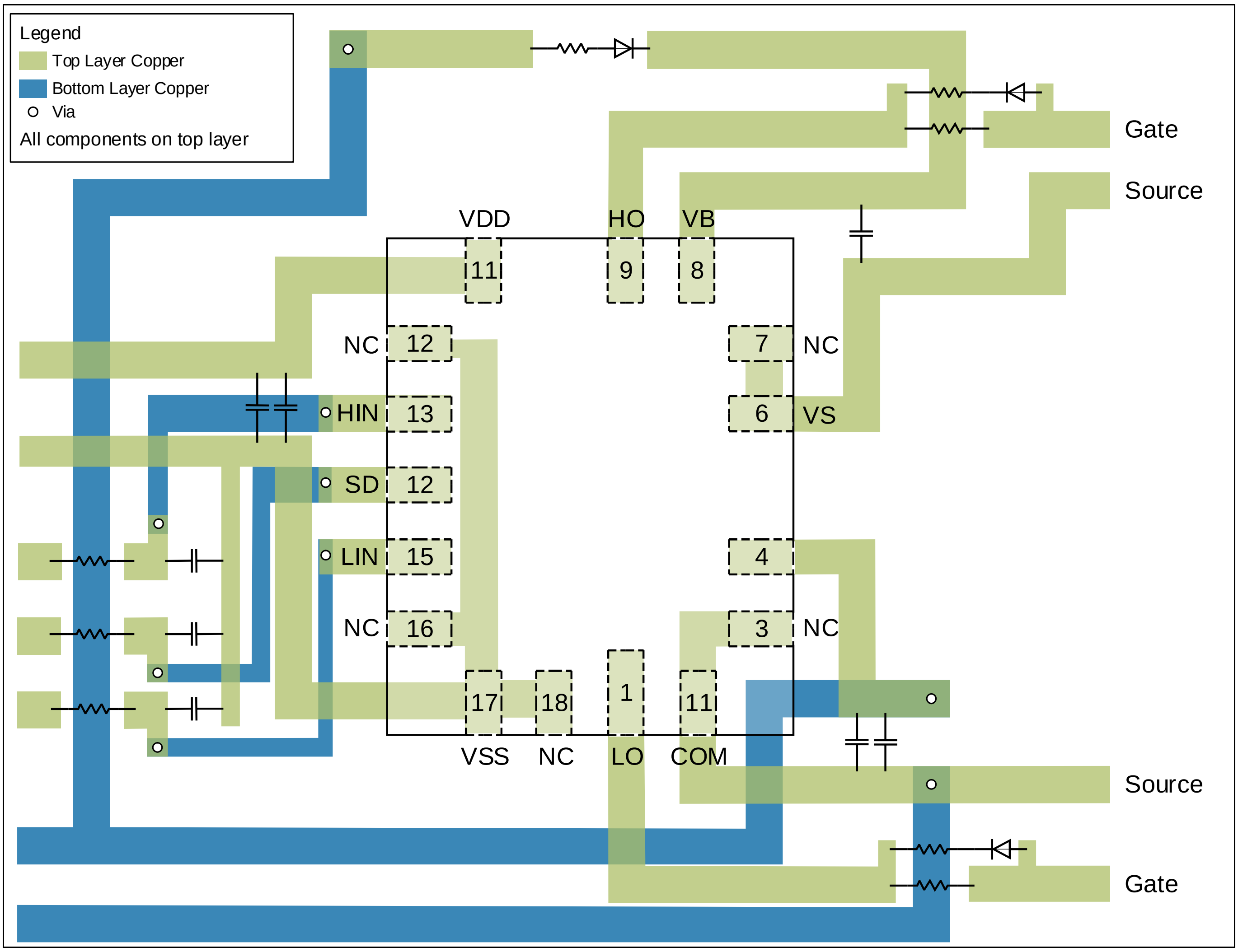
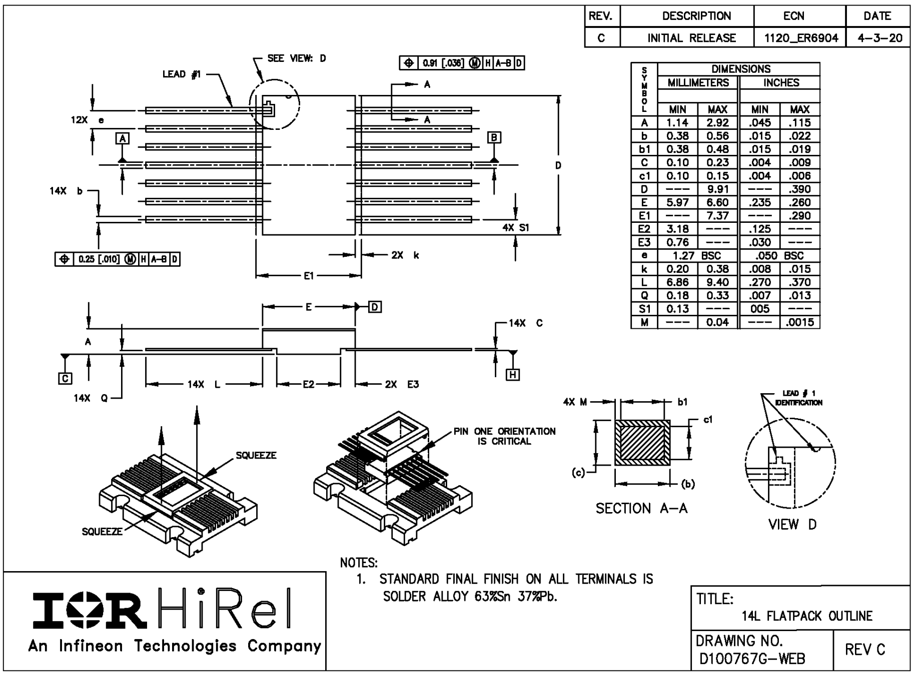


Figure 25 Recommended PCB layout for RIC7S113E4 (LCC CIC)

7 Package details

7.1 Flatpack

For latest package outline drawing please refer to [14L Flatpack package outline](#).



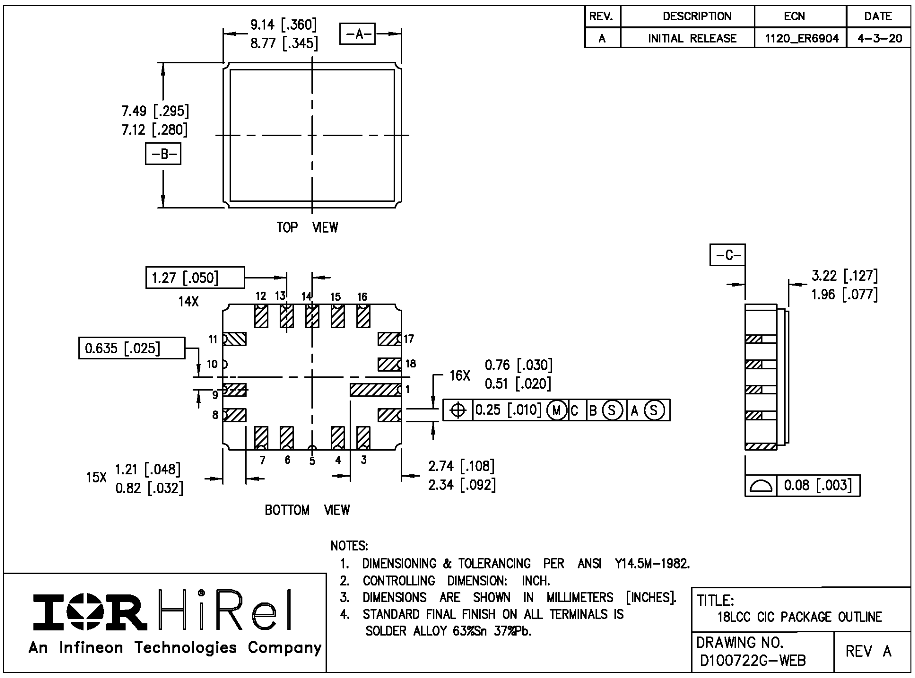
REV.	DESCRIPTION	ECN	DATE
C	INITIAL RELEASE	1120_ER6904	4–3–20

SYMBOL	DIMENSIONS MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.14	2.92	.045	.115
b	0.38	0.56	.015	.022
b1	0.38	0.48	.015	.019
C	0.10	0.23	.004	.009
c1	0.10	0.15	.004	.006
D	---	9.91	---	.390
E	5.97	6.60	.235	.260
E1	---	7.37	---	.290
E2	3.18	---	.125	---
E3	0.76	---	.030	---
e	1.27 BSC		.050 BSC	
k	0.20	0.38	.008	.015
L	6.86	9.40	.270	.370
Q	0.18	0.33	.007	.013
S1	0.13	---	005	---
M	---	0.04	---	.0015

Figure 26 **14-lead Flatpack package outline**

7.2 LCC CIC

For latest package outline drawing please refer to [18-pin LCC CIC package outline](#).



REV.	DESCRIPTION	ECN	DATE
A	INITIAL RELEASE	1120_ER6904	4–3–20

Figure 27 **18-pin LCC CIC package outline**

7.3 MO-036AB CIC

For latest package outline drawing please refer to MO-036AB CIC package outline.

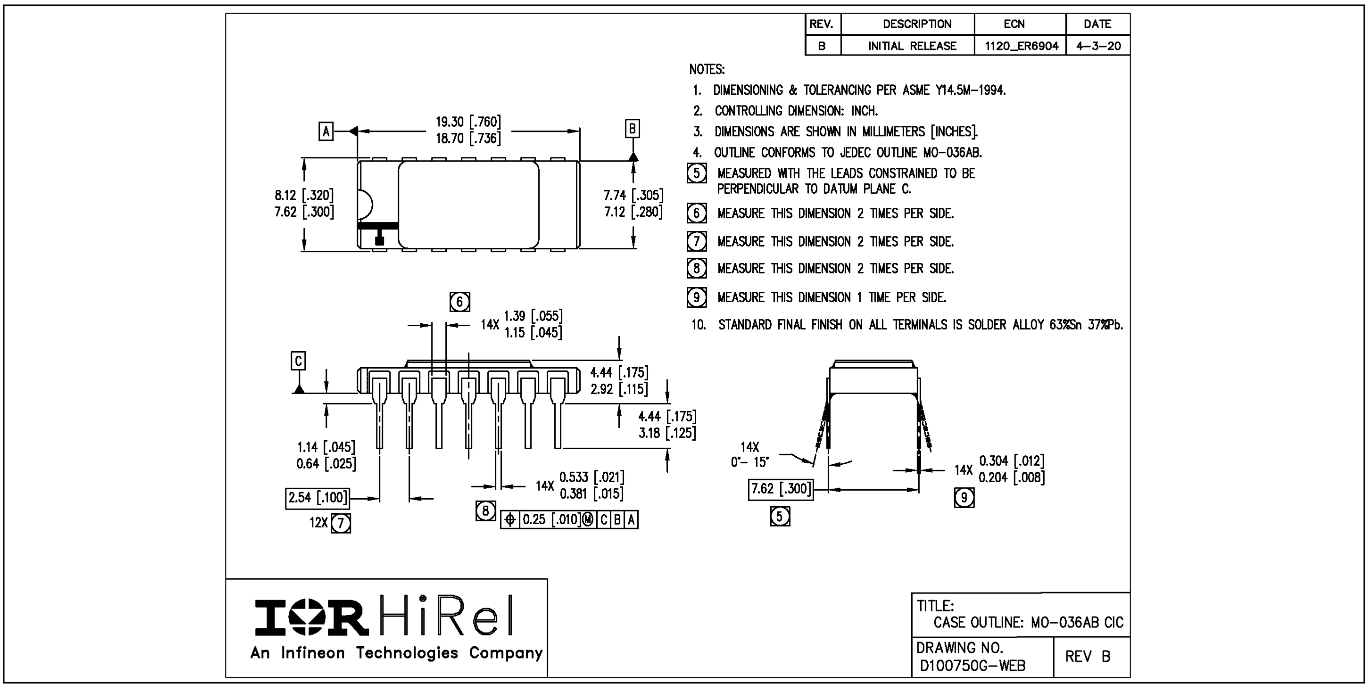


Figure 28 MO-036AB CIC package outline

Revision history

Document revision	Date	Description of changes
	08/14/2015	Datasheet (PD-97827)
Rev A	10/30/2015	Updated based on ECN-1120_03984
Rev B	07/26/2021	Updated based on ECN-1120_08653
Rev C	05/11/2022	Updated based on ECN-1120_09050
Rev D	01/27/2023	Updated based on ECN-1120_09401

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