0.3 GHz to 6 GHz, 39.5 dBm, GaN Power Amplifier

FEATURES

- Internally matched, 0.3 GHz to 6 GHz, 39.5 dBm, GaN power amplifier
- RF input and RF output AC-coupled
- Integrated drain bias inductors
- Output power: 39.5 dBm typical from 0.5 GHz to 5 GHz (P_{IN} = 16.0 dBm)
- Power gain: 23.5 dB typical from 0.5 GHz to 5 GHz (P_{IN} = 16.0 dBm)
- PAE: 40% typical from 0.5 GHz to 5 GHz (P_{IN} = 16.0 dBm)
- Small signal gain: 33.5 dB typical from 0.5 GHz to 5 GHz
- Supply voltage: 28 V
- Quiescent current: 300 mA

APPLICATIONS

- Electronic warfare
- Communications
- Radar

FUNCTIONAL BLOCK DIAGRAM

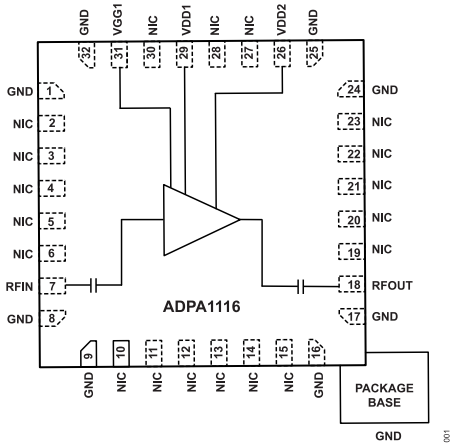

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADPA1116 is a 0.3 GHz to 6 GHz power amplifier with a saturated output power (P_{OUT}) of 39.5 dBm, power added efficiency (PAE) of 40%, and a power gain of 23.5 dB typical from 0.5 GHz to 5 GHz at an input power (P_{IN}) of 16.0 dBm. The RF input and RF output are internally matched and AC-coupled. A drain bias voltage of 28 V is applied to the VDD1 and VDD2 pins, which have integrated bias inductors. The drain current is set by applying a negative voltage to the VGG1 pin.

The ADPA1116 is fabricated on a gallium nitride (GaN) process, is housed in a 32-lead lead frame chip scale package, premolded cavity [LFCSP_CAV], and is specified for operation from −40°C to +85°C

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REVISION HISTORY

4/2024—Revision 0: Initial Version

ELECTRICAL SPECIFICATIONS

0.3 GHz TO 0.5 GHz FREQUENCY RANGE

T_{CASE} = 25°C, supply voltage (V_{DD}) = 28 V, target quiescent current (I_{DQ}) = 300 mA, and frequency range = 0.3 GHz to 0.5 GHz, unless otherwise stated.

Table 1. 0.3 GHz to 0.5 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.3		0.5	GHz	
GAIN					
Small Signal Gain (S21)	28.5	32.5		dB	
Gain Flatness		±2.3		dB	
Gain Variation over Temperature		0.04		dB/°C	
RETURN LOSS					
Input (S11)		9		dB	
Output (S22)		7.5		dB	
POWER					P_{IN} = 16.0 dBm
Output (P_{OUT})	35.5	38		dBm	
Gain		22		dB	
Power Added Efficiency (PAE)		35		%	
I_{DQ}		300		mA	Adjust the gate control voltage (V_{GG1}) between −3 V and −1 V to achieve an I_{DQ} = 300 mA typical

0.5 GHz TO 5 GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD} = 28 V, I_{DQ} = 300 mA, and frequency range = 0.5 GHz to 5 GHz, unless otherwise stated.

Table 2. 0.5 GHz to 5 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.5		5	GHz	
GAIN					
S21	29.5	33.5		dB	
Gain Flatness		±1.3		dB	
Gain Variation over Temperature		0.04		dB/°C	
RETURN LOSS					
S11		12		dB	
S22		13		dB	
POWER					P_{IN} = 16.0 dBm
P_{OUT}	37.5	39.5		dBm	
Gain	21.5	23.5		dB	
PAE		40		%	
I_{DQ}		300		mA	Adjust V_{GG1} between −3 V and −1 V to achieve an I_{DQ} = 300 mA typical

ELECTRICAL SPECIFICATIONS

5 GHz TO 6 GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD} = 28 V, I_{DQ} = 300 mA, and frequency range = 5 GHz to 6.0 GHz, unless otherwise stated.

Table 3. 5 GHz to 6 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	5		6	GHz	
GAIN					
S21		33		dB	
Gain Flatness		±0.8		dB	
Gain Variation over Temperature		0.05		dB/°C	
RETURN LOSS					
S11		12		dB	
S22		7.5		dB	
POWER					P_{IN} = 16.0 dBm
P_{OUT}		38.5		dBm	
Gain		22.5		dB	
PAE		37		%	
I_{DQ}		300		mA	Adjust V_{GG1} between −3 V and −1 V to achieve an I_{DQ} = 300 mA typical

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
Bias Voltage	
Drain (V_{DD})	35 V
Gate (V_{GG1})	−8.0 V DC to 0 V DC
RF Input Power (RFIN)	23 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C, Derate 205 mW/°C Above 85°C	28.7 W
Temperature	
Nominal Peak Channel, T_{CASE} = 85°C, P_{IN} = 16 dBm, P_{DISS} = 13.3 W at 3 GHz	149.9°C
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Maximum Channel	225°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance where the case is the exposed metal ground pad on the underside of the device.

Table 5. Thermal Resistance

Package Type[1]	θ_{JC}	Unit
CG-32-2	4.88	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel to the ground pad with the ground pad held constant at the operating temperature of 85°C.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA1116

Table 6. ADPA1116, 32-Lead LFCSP_CAV

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

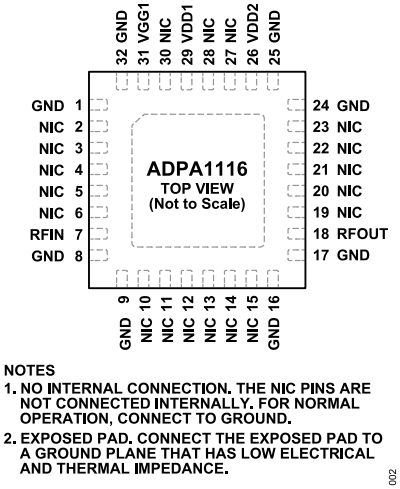

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16, 17, 24, 25, 32	GND	Ground. The GND pins must be connected to RF and DC ground. See Figure 5 for the interface schematic.
2 to 6, 10 to 15, 19 to 23, 27, 28, 30	NIC	No Internal Connection. The NIC pins are not connected internally. For normal operation, connect to ground.
7	RFIN	RF Input. The RFIN pin is AC-coupled and internally matched to 50 Ω. See Figure 3 for the interface schematic.
18	RFOUT	RF Output. The RFOUT pin is AC-coupled and internally matched to 50 Ω. See Figure 6 for the interface schematic.
26	VDD2	Drain Bias Pin for the Second Stage. See Figure 6 for the interface schematic.
29	VDD1	Drain Bias Pin for the First Stage. See Figure 7 for the interface schematic.
31	VGG1	Gate Bias for Both Stages of the Amplifier. The VGG1 pin is used to set the I_{DQ} of the amplifier. See Figure 4 for the interface schematic.
	EPAD	Exposed Pad. Connect the exposed pad to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

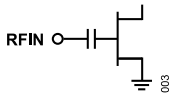

Figure 3. RFIN Interface Schematic

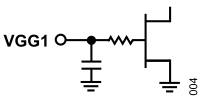

Figure 4. VGG1 Interface Schematic

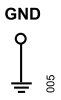

Figure 5. GND Interface Schematic

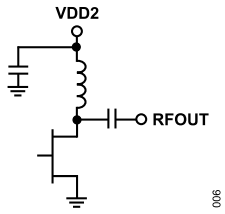

Figure 6. VDD2 and RFOUT Interface Schematic

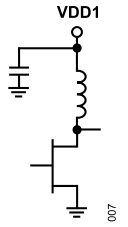

Figure 7. VDD1 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

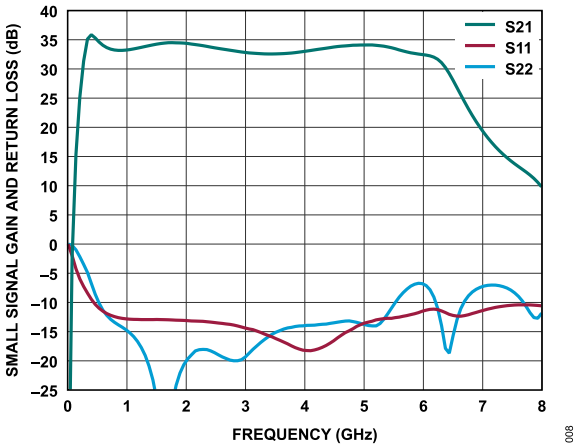

Figure 8. Small Signal Gain and Return Loss vs. Frequency, V_{DD} = 28 V, I_{DQ} = 300 mA

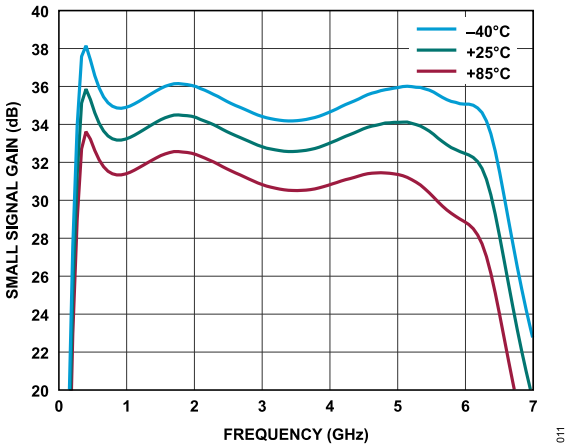

Figure 11. Small Signal Gain vs. Frequency for Various Temperatures, V_{DD} = 28 V, I_{DQ} = 300 mA

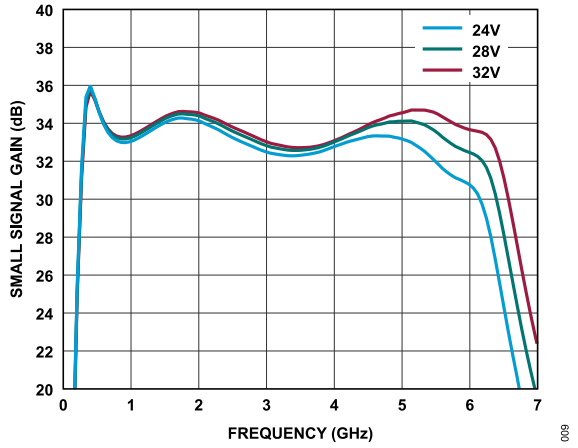

Figure 9. Small Signal Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 300 mA

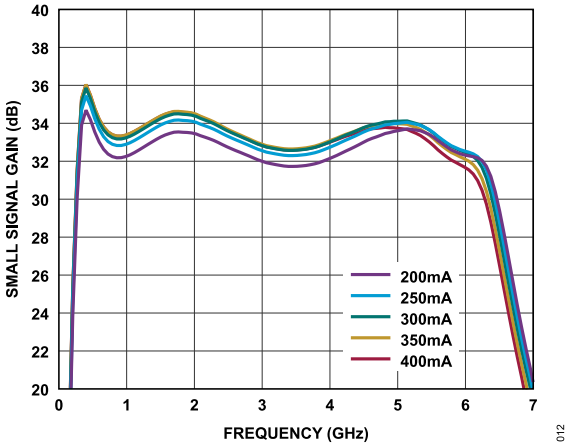

Figure 12. Small Signal Gain vs. Frequency for Various I_{DQ} Values, V_{DD} = 28 V

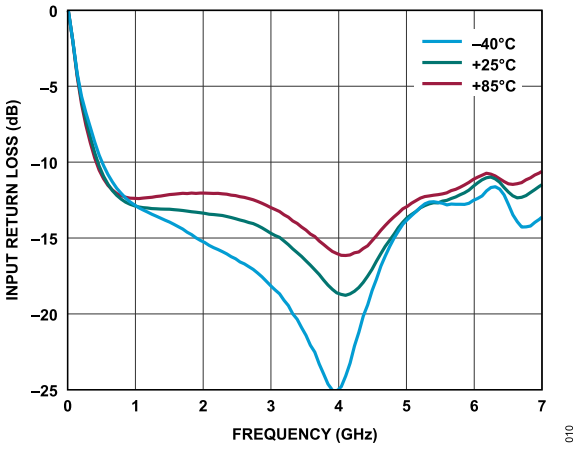

Figure 10. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 28 V, I_{DQ} = 300 mA

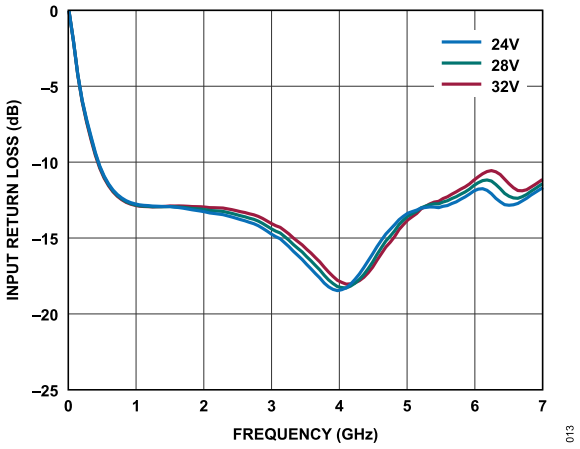

Figure 13. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 300 mA

TYPICAL PERFORMANCE CHARACTERISTICS

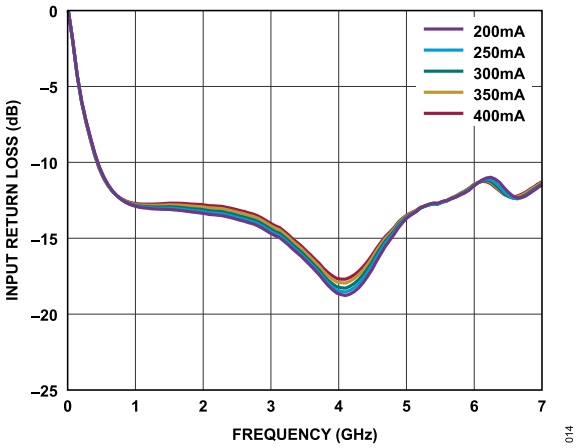

Figure 14. Input Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 28 V

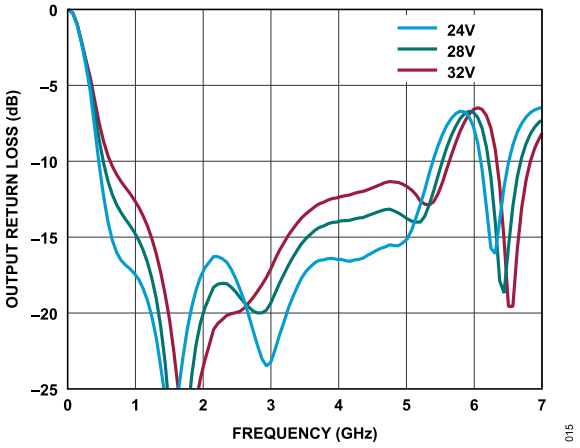

Figure 15. Output Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 300 mA

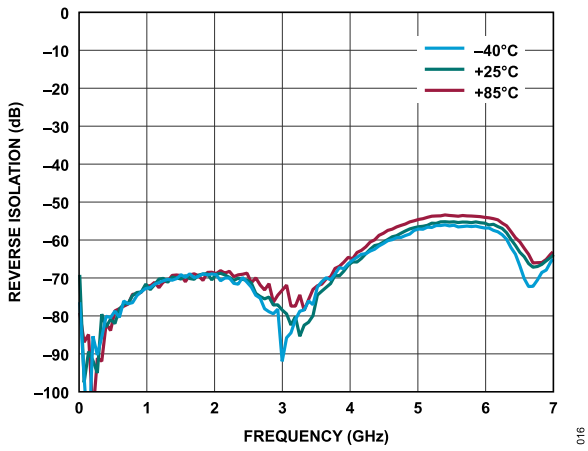

Figure 16. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 28 V, I_{DQ} = 300 mA

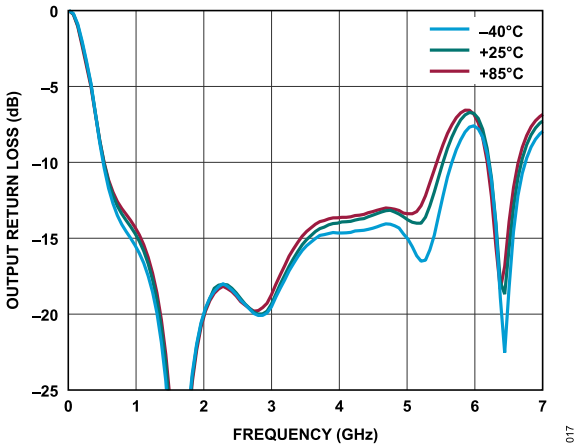

Figure 17. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 28 V, I_{DQ} = 300 mA

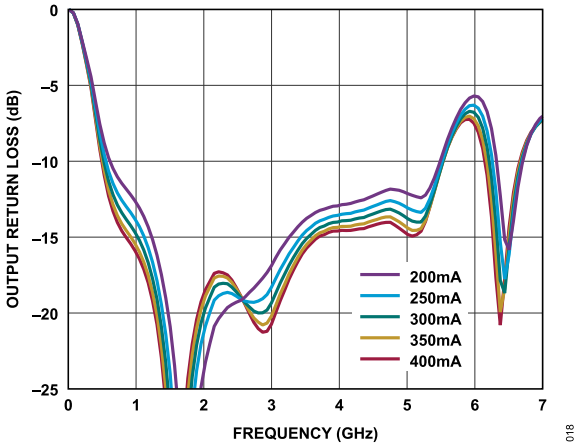

Figure 18. Output Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 28 V

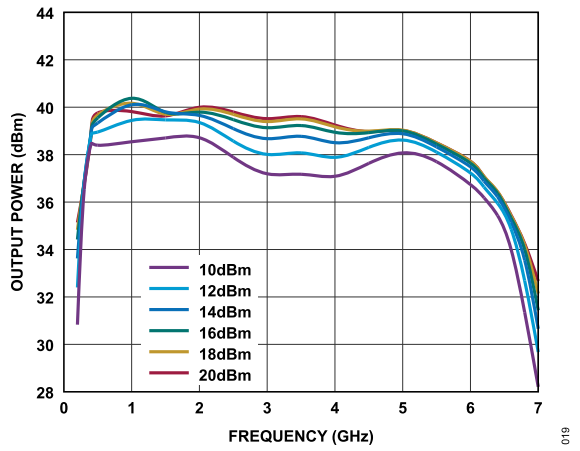

Figure 19. Output Power vs. Frequency for Various P_{IN} Levels, V_{DD} = 28 V, I_{DQ} = 300 mA

TYPICAL PERFORMANCE CHARACTERISTICS

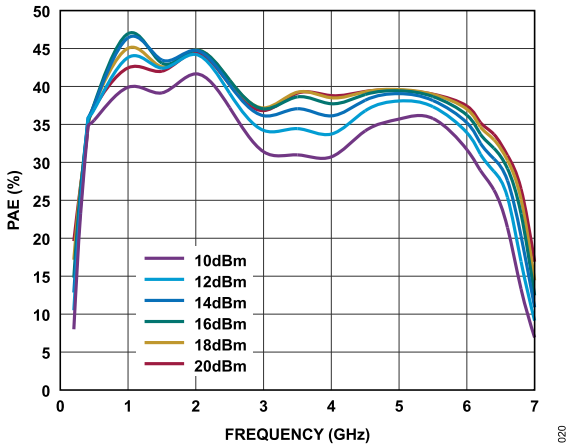

Figure 20. PAE vs. Frequency for Various P_{IN} Levels, V_{DD} = 28 V, I_{DQ} = 300 mA

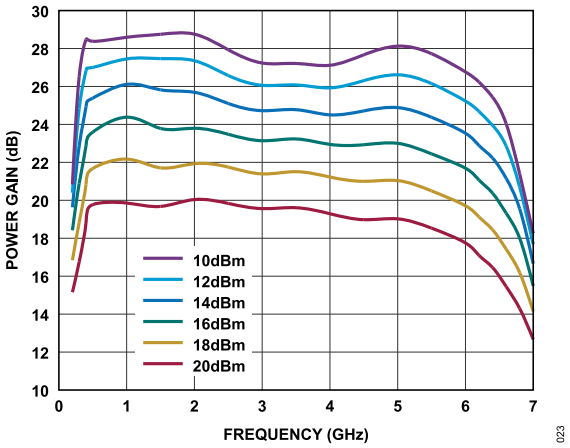

Figure 23. Power Gain vs. Frequency for Various P_{IN} Levels, V_{DD} = 28 V, I_{DQ} = 300 mA

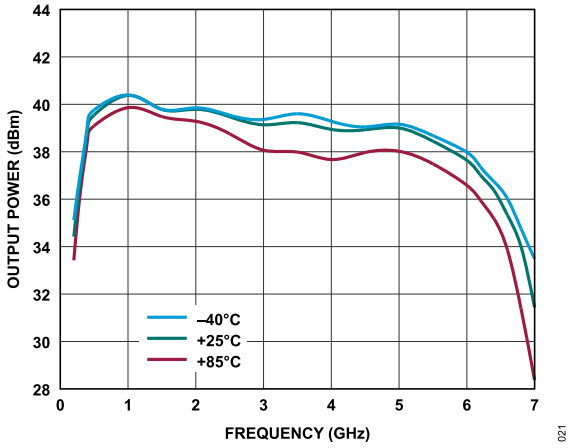

Figure 21. Output Power vs. Frequency for Various Temperatures, P_{IN} = 16 dBm, V_{DD} = 28 V, I_{DQ} = 300 mA

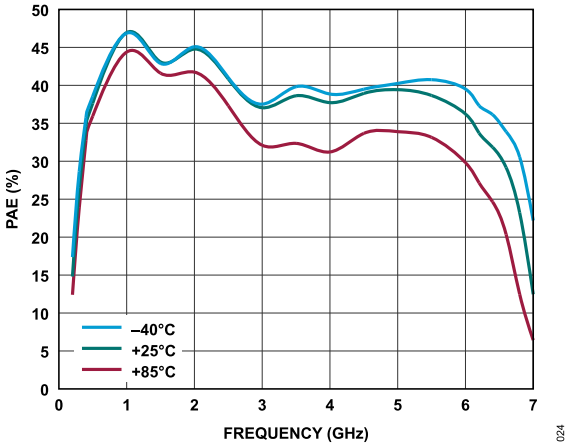

Figure 24. PAE vs. Frequency for Various Temperatures, P_{IN} = 16 dBm, V_{DD} = 28 V, I_{DQ} = 300 mA

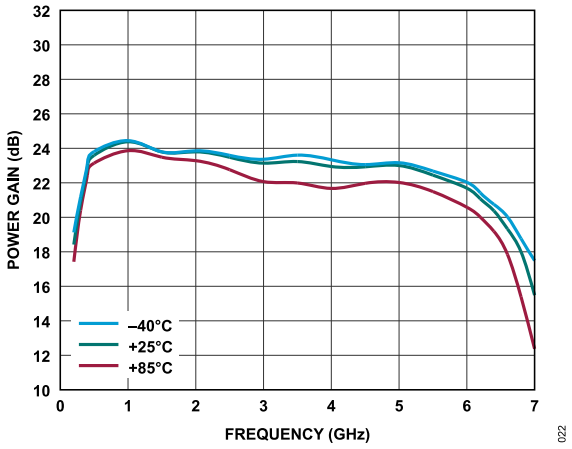

Figure 22. Power Gain vs. Frequency for Various Temperatures, P_{IN} = 16 dBm, V_{DD} = 28 V, I_{DQ} = 300 mA

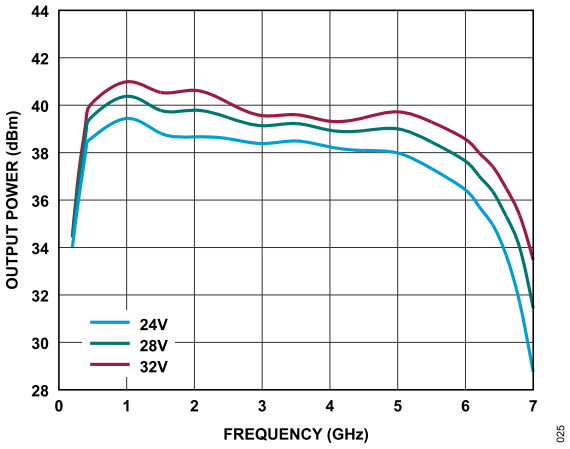

Figure 25. Output Power vs. Frequency for Various Supply Voltages, P_{IN} = 16 dBm, I_{DQ} = 300 mA

TYPICAL PERFORMANCE CHARACTERISTICS

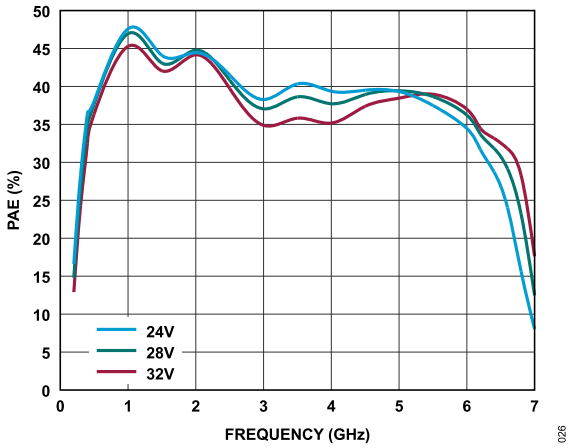

Figure 26. PAE vs. Frequency for Various Supply Voltages, P_{IN} = 16 dBm, I_{DQ} = 300 mA

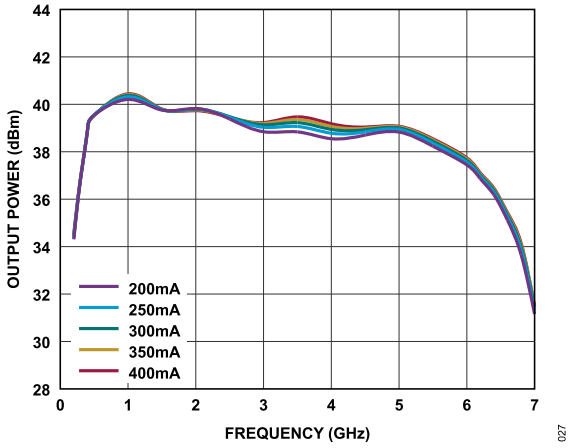

Figure 27. Output Power vs. Frequency for Various I_{DQ} Values, P_{IN} = 16 dBm, V_{DD} = 28 V

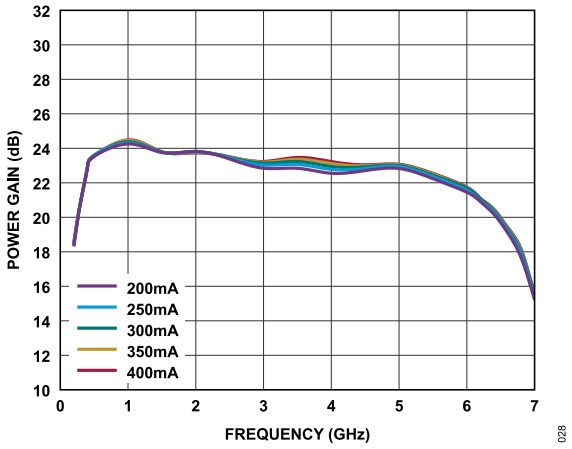

Figure 28. Power Gain vs. Frequency for Various I_{DQ} Values, P_{IN} = 16 dBm, V_{DD} = 28 V

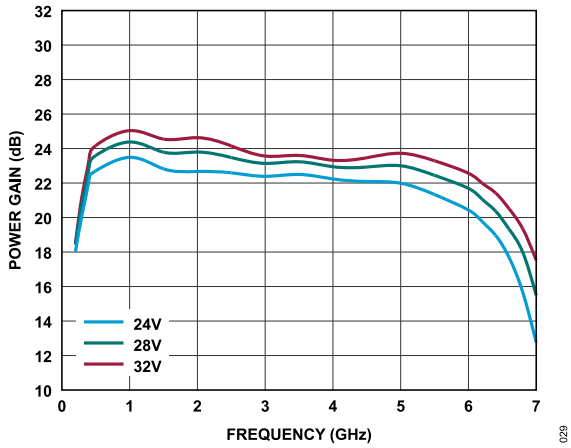

Figure 29. Power Gain vs. Frequency for Various Supply Voltages, P_{IN} = 16 dBm, I_{DQ} = 300 mA

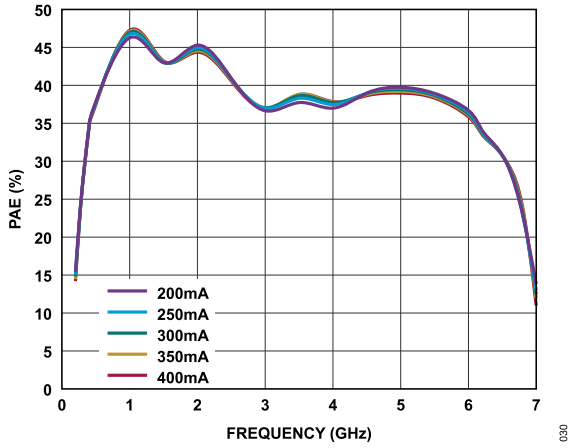

Figure 30. PAE vs. Frequency for Various I_{DQ} Values, P_{IN} = 16 dBm, V_{DD} = 28 V

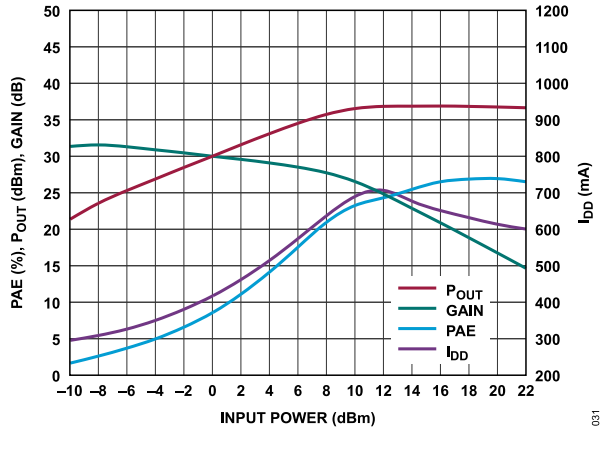

Figure 31. PAE, P_{OUT}, Gain, and Supply Current (I_{DD}) vs. Input Power at 0.3 GHz, V_{DD} = 28 V, I_{DQ} = 300 mA

TYPICAL PERFORMANCE CHARACTERISTICS

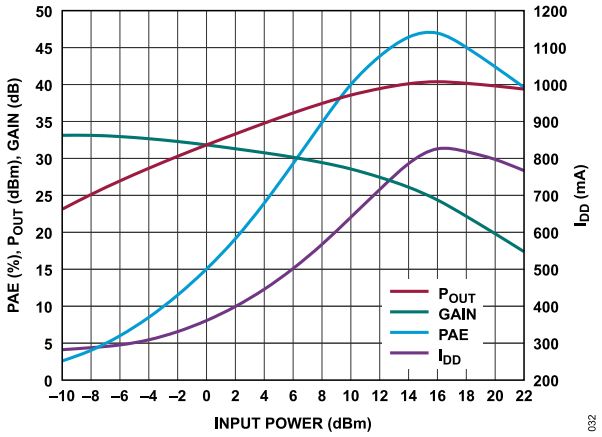

Figure 32. PAE, P_{OUT}, Gain, and I_{DD} vs. Input Power at 1.0 GHz, V_{DD} = 28 V, I_{DQ} = 300 mA

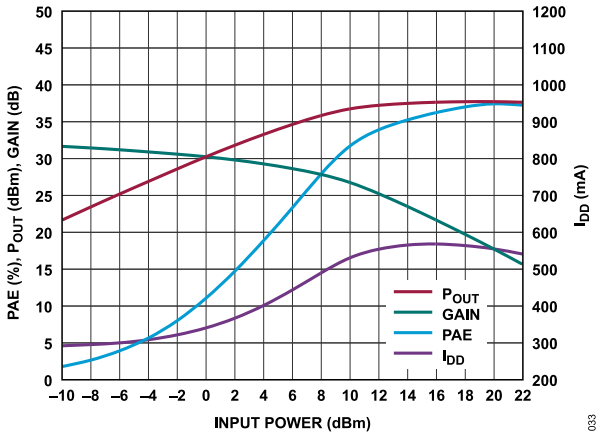

Figure 33. PAE, P_{OUT}, Gain, and I_{DD} vs. Input Power at 6.0 GHz, V_{DD} = 28 V, I_{DQ} = 300 mA

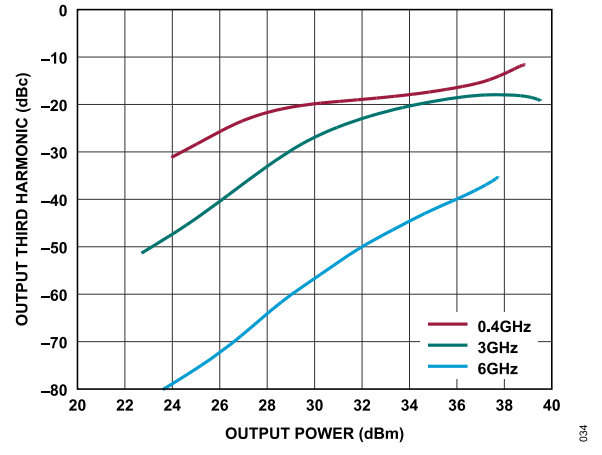

Figure 34. Output Third Harmonic vs. Output Power for Various Frequencies, V_{DD} = 28 V, I_{DQ} = 300 mA

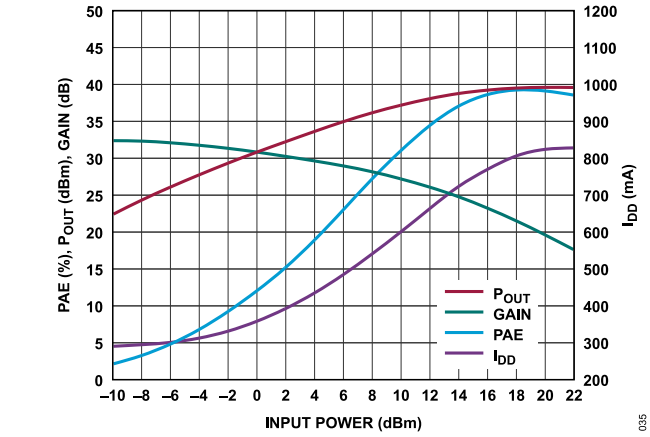

Figure 35. PAE, P_{OUT}, Gain, and I_{DD} vs. Input Power at 3.0 GHz, V_{DD} = 28 V, I_{DQ} = 300 mA

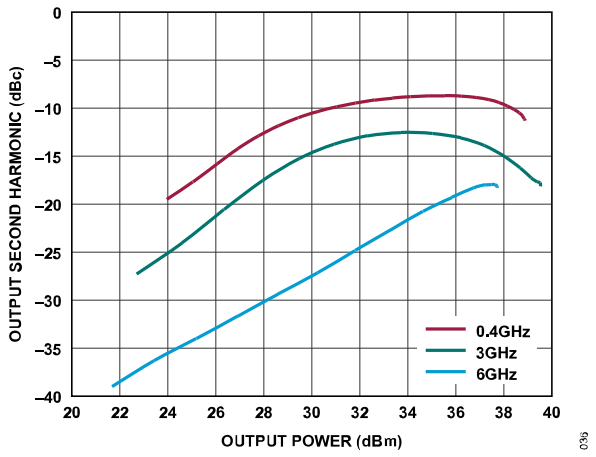

Figure 36. Output Second Harmonic vs. Output Power for Various Frequencies, V_{DD} = 28 V, I_{DQ} = 300 mA

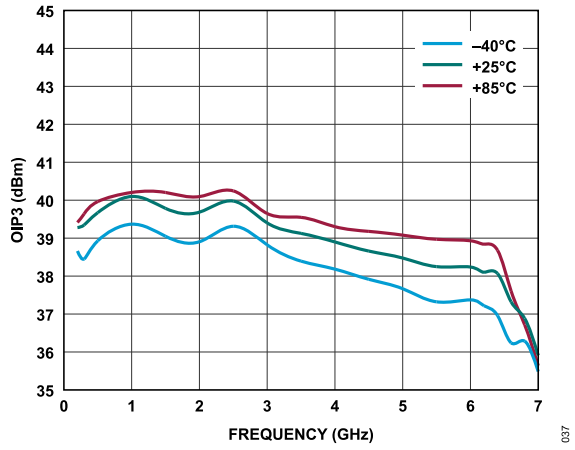

Figure 37. Output Third-Order Intercept Point (OIP3) vs. Frequency for Various Temperatures, P_{OUT} per Tone = 28 dBm, V_{DD} = 28 V, I_{DQ} = 300 mA

TYPICAL PERFORMANCE CHARACTERISTICS

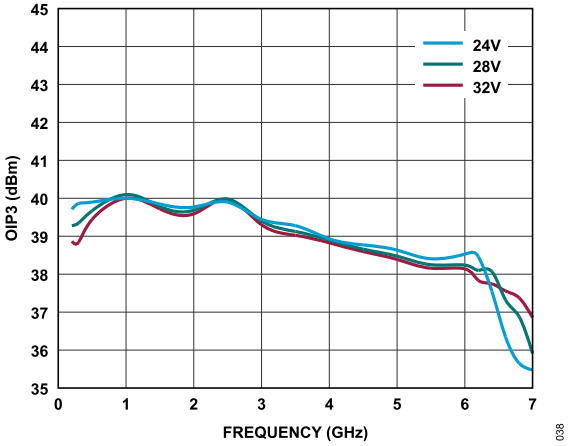

Figure 38. OIP3 vs. Frequency for Various Supply Voltages, P_{OUT} per Tone = 28 dBm, I_{DQ} = 300 mA

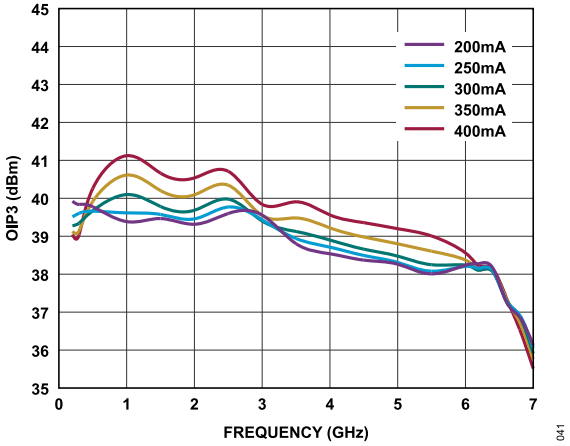

Figure 41. OIP3 vs. Frequency for Various I_{DQ} Values, P_{OUT} per Tone = 28 dBm, V_{DD} = 28 V

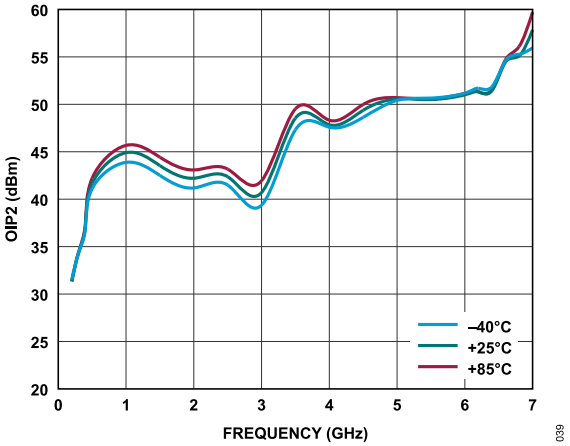

Figure 39. Output Second-Order Intercept Point (OIP2) vs. Frequency for Various Temperatures, P_{OUT} per Tone = 28 dBm, V_{DD} = 28 V, I_{DQ} = 300 mA

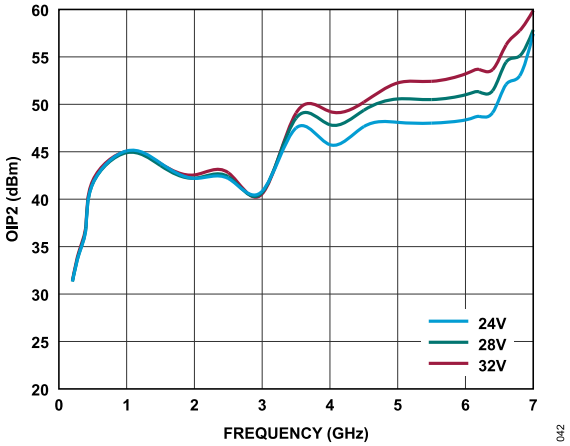

Figure 42. OIP2 vs. Frequency for Various Supply Voltages, P_{OUT} per Tone = 28 dBm, I_{DQ} = 300 mA

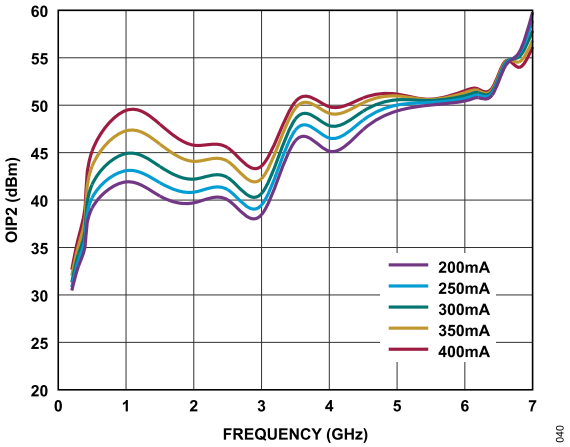

Figure 40. OIP2 vs. Frequency for Various I_{DQ} Values, P_{OUT} per Tone = 28 dBm, V_{DD} = 28 V

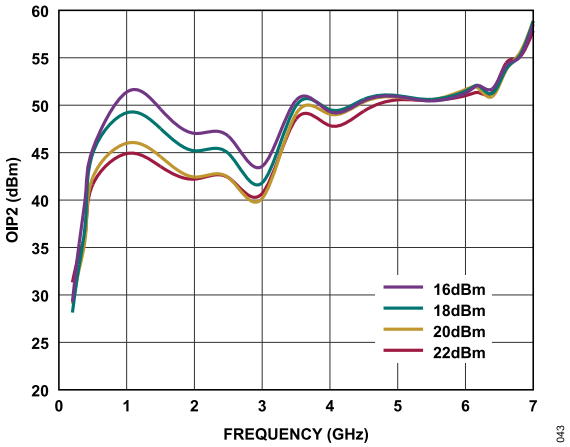

Figure 43. OIP2 vs. Frequency for Various P_{OUT} Values per Tone, V_{DD} = 28 V, V_{DQ} = 300 mA

TYPICAL PERFORMANCE CHARACTERISTICS

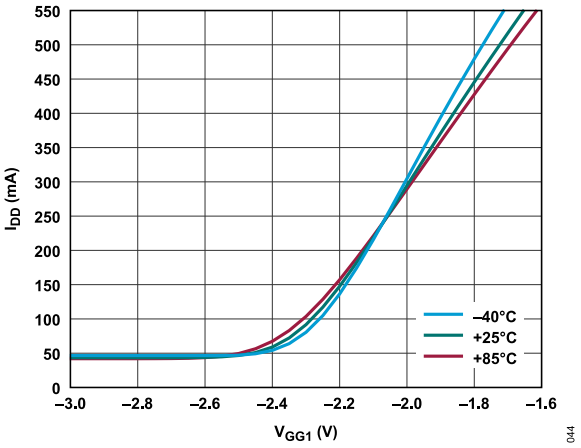

Figure 44. I_{DQ} vs. V_{GG1}, V_{DD} = 28 V

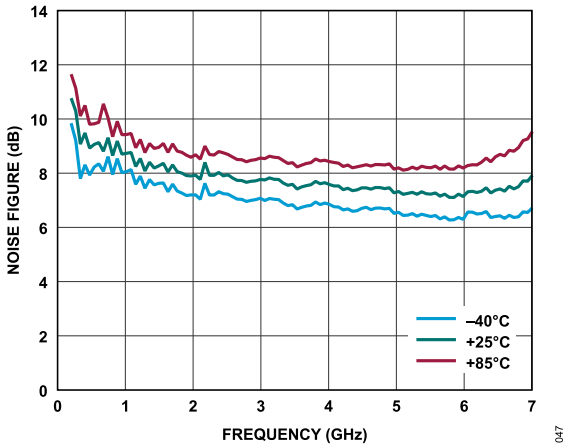

Figure 47. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 28 V, I_{DQ} = 300 mA

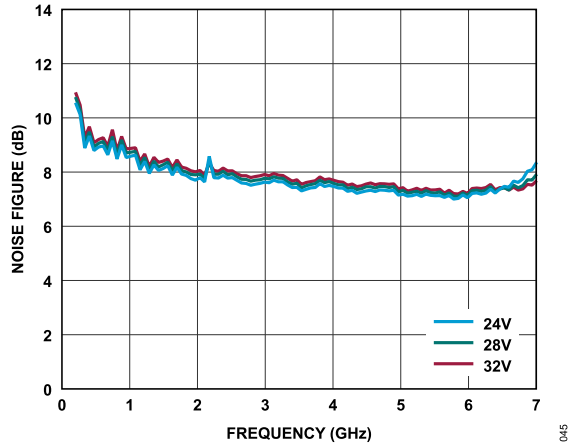

Figure 45. Noise Figure vs. Frequency for Various Supply Voltages, I_{DQ} = 300 mA

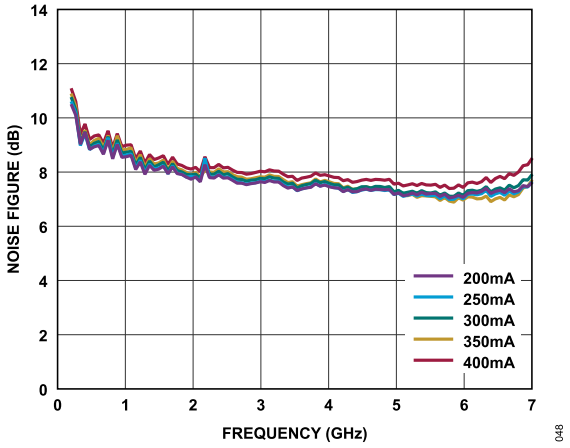

Figure 48. Noise Figure vs. Frequency for Various I_{DQ} Values, V_{DD} = 28 V

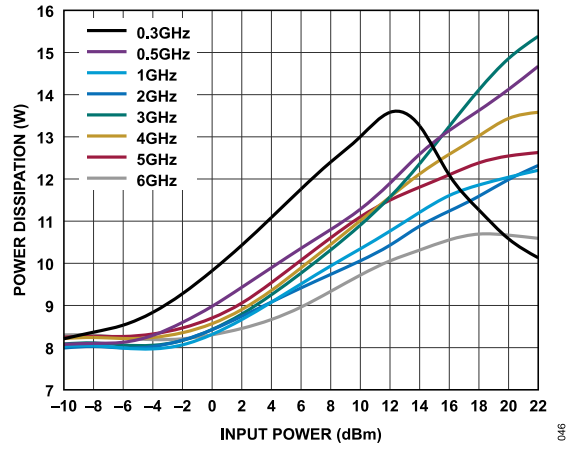

Figure 46. Power Dissipation vs. Input Power for Various Frequencies, T_{CASE} = 85°C, V_{DD} = 28 V, I_{DQ} = 300 mA

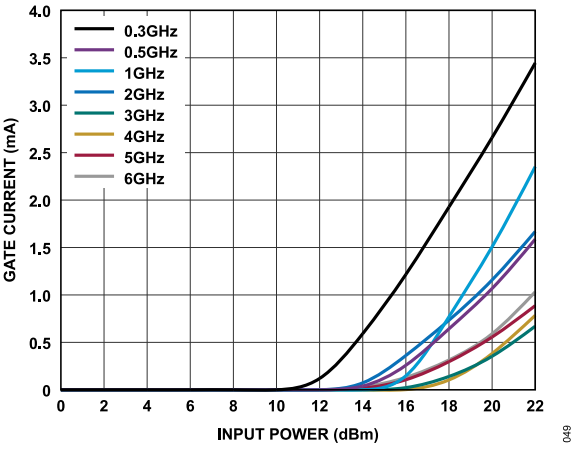

Figure 49. Gate Current vs. Input Power for Various Frequencies, V_{DD} = 28 V, I_{DQ} = 300 mA

THEORY OF OPERATION

The ADPA1116 is a GaN power amplifier with cascaded gain stages that are biased by a positive drain supply and an externally applied negative gate voltage. A nominal V_{DD} of 28 V is applied to the first and second stage drains, and a negative voltage is applied to the VGG1 pin to set the total I_{DQ} to 300 mA nominal.

When biased as described, the device operates in Class AB, resulting in the maximum PAE at saturation. The ADPA1116 features integrated RF chokes for each drain plus on-chip DC blocking of the RFIN and RFOUT ports.

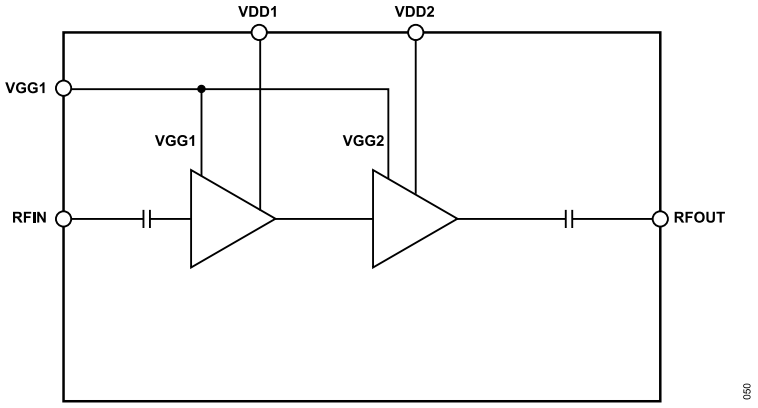

Figure 50. Basic Block Diagram

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 51 shows the typical application circuit for the ADPA1116.

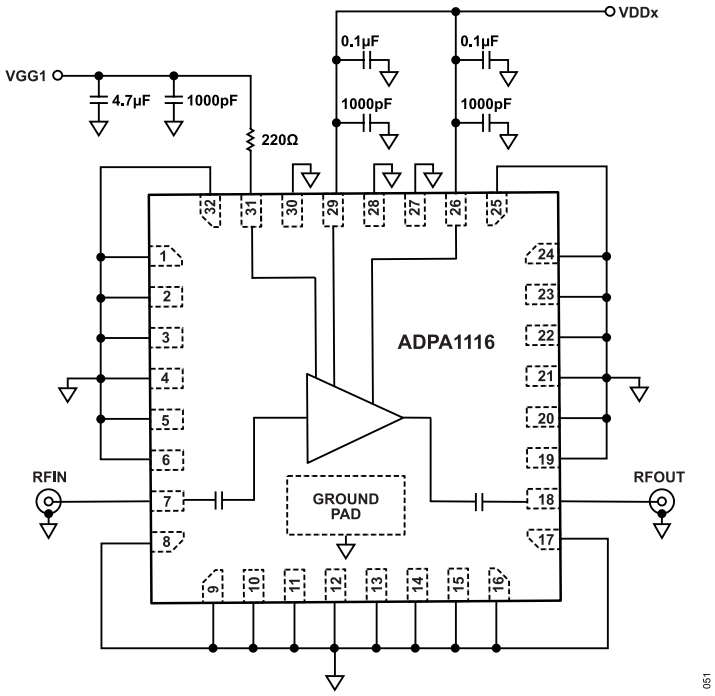

Figure 51. Typical Application Circuit

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The basic connections to operate the ADPA1116 are shown in Figure 51. The VDD1, VDD2, and VGG1 pins should be decoupled as shown in Figure 51. The gate voltage for all stages (−1.0 V to −3.0 V for biased operation and −6.0 V for pinch-off) is applied to the VGG1 pin. A drain supply voltage of 28 V nominal is applied to the VDD1 and VDD2 pins. Pin 2 through Pin 6, Pin 10 through Pin 15, Pin 19 through Pin 23, Pin 27, Pin 28, and Pin 32 are designated as NIC pins. Although these NIC pins are not internally connected, they were all connected to ground during the characterization of the device.

To turn on the ADPA1116, take the following steps:

1. Apply −6.0 V to VGG1 to put the channel in pinch-off.
2. Apply 28 V to VDD1 and VDD2 (I_{DQ} must be approximately 53 mA).
3. Increase the VGG1 voltage more positive until I_{DQ} is 300 mA (approximately −2.0 V). Note that if the desired gate voltage is known in advance, VGG1 can be set to that voltage directly without going through the pinch-off step.
4. Apply the RF signal.

To turn off the ADPA1116, take the following steps:

1. Turn off the RF signal.
2. Set VDD1 and VDD2 to 0 V.
3. Increase VGG1 to 0 V.

Note that the configuration shown in Figure 51, which is also the default configuration of the ADPA1116 evaluation board, was used to characterize the ADPA1116.

OUTLINE DIMENSIONS

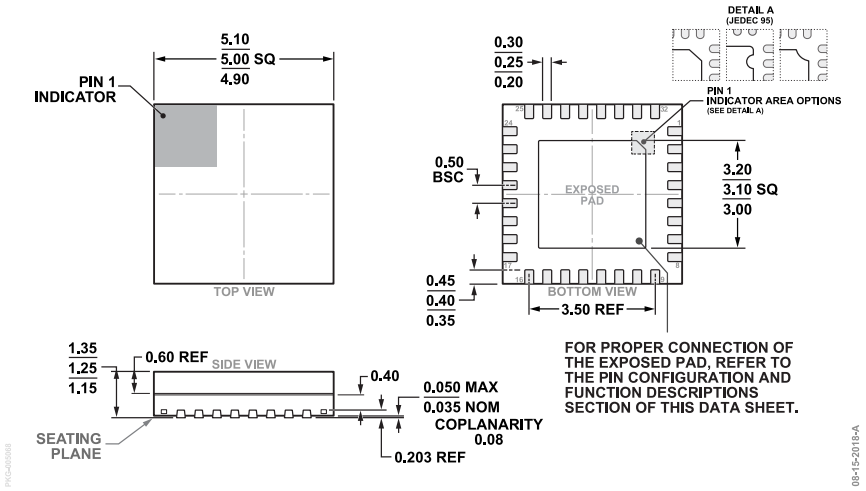

Figure 52. 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
5 mm × 5 mm Body and 1.25 mm Package Height
(CG-32-2)
Dimensions shown in millimeters

Updated: April 17, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADPA1116ACGZN	−40°C to +85°C	32-Lead LFCSP_CAV (5 mm × 5 mm with EPAD)	Reel, 500	CG-32-2
ADPA1116ACGZN-R7	−40°C to +85°C	32-Lead LFCSP_CAV (5 mm × 5 mm with EPAD)	Reel, 500	CG-32-2

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 8. Evaluation Boards

Model[1]	Description
ADPA1116-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.