43 dBm, 20 W, GaN Power Amplifier, 8.2 GHz to 11.8 GHz

FEATURES

- Internally matched and AC-coupled 20 W GaN power amplifier
- Integrated temperature-compensated RF power detector
- P_{OUT} with P_{IN} = 22 dBm: 43.5 dBm typical from 9.6 GHz to 11 GHz
- Small signal gain: 31 dB typical from 9.6 GHz to 11 GHz
- Power gain with P_{IN} = 22 dBm: 21.5 dB typical from 8.2 GHz to 11 GHz
- PAE: 46% typical from 9.6 GHz to 11 GHz
- Supply voltage: 28 V at 200 mA on 10% duty cycle
- 18-terminal, 7 mm × 7 mm, LCC_HS package

APPLICATIONS

- Weather radars
- Marine radars
- Military radars

GENERAL DESCRIPTION

The ADPA1122 is a gallium nitride (GaN), power amplifier that delivers 43 dBm (20 W) with more than 43% power added efficiency (PAE) across its 8.2 GHz to 11.8 GHz frequency range. The ADPA1122 provides ±0.5 dB of gain flatness from 9.6 GHz to 11 GHz.

The ADPA1122 is optimized for pulsed applications such as military, marine, and weather radar.

The ADPA1122 is packaged in an 18-terminal, 7 mm × 7 mm, ceramic leadless chip carrier with heat sink [LCC_HS] that exhibits low thermal resistance and is compatible with surface-mount manufacturing techniques.

FUNCTIONAL BLOCK DIAGRAM

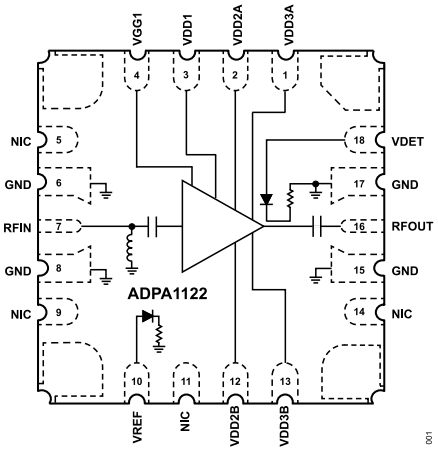

Figure 1. Functional Block Diagram

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REVISION HISTORY

3/2023—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, supply voltage (V_{DD}) = 28 V, target quiescent current (I_{DQ}) = 200 mA, pulse width = 100 µs, 10% duty cycle, and frequency range = 8.2 GHz to 9.6 GHz, unless otherwise noted.

Table 1. 8.2 GHz to 9.6 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	8.2		9.6	GHz	
GAIN					
Small Signal Gain	30	32.5		dB	
Gain Flatness		±0.6		dB	
RETURN LOSS					
Input		18		dB	
Output		14		dB	
POWER					Input power (P_{IN}) = 22 dBm
Output (P_{OUT})	41.5	43.5		dBm	
Gain	19.5	21.5		dB	
PAE		45		%	
I_{DQ}		200		mA	Adjust the gate control voltage (V_{GG1}) between −4 V and −2 V to achieve an I_{DQ} = 200 mA typical

T_A = 25°C, V_{DD} = 28 V, I_{DQ} = 200 mA, pulse width = 100 µs, 10% duty cycle, and frequency range = 9.6 GHz to 11 GHz, unless otherwise noted.

Table 2. 9.6 GHz to 11 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	9.6		11	GHz	
GAIN					
Small Signal Gain	28.5	31		dB	
Gain Flatness		±0.5		dB	
RETURN LOSS					
Input		15		dB	
Output		16		dB	
POWER					P_{IN} = 22 dBm
P_{OUT}	41.5	43.5		dBm	
Gain	19.5	21.5		dB	
PAE		46		%	
I_{DQ}		200		mA	Adjust V_{GG1} between −4 V and −2 V to achieve an I_{DQ} = 200 mA typical

SPECIFICATIONS

T_A = 25°C, V_{DD} = 28 V, I_{DQ} = 200 mA, pulse width = 100 µs, 10% duty cycle, and frequency range = 11 GHz to 11.8 GHz, unless otherwise noted.

Table 3. 11 GHz to 11.8 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	11		11.8	GHz	
GAIN					
Small Signal Gain	26.5	28.5		dB	
Gain Flatness		±1.5		dB	
RETURN LOSS					
Input		8		dB	
Output		9		dB	
POWER					P_{IN} = 22 dBm
P_{OUT}	40	42		dBm	
Gain	18	20		dB	
PAE		43		%	
I_{DQ}		200		mA	Adjust V_{GG1} between −4 V and −2 V to achieve an I_{DQ} = 200 mA typical

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
Bias Voltage	
Drain (VDD1, VDD2A, VDD2B, VDD3A, and VDD3B)	35 V dc
Gate (VGG1)	−8 V dc to 0 V dc
RFIN[1]	25 dBm
Maximum Drain Bias	
Pulse Width	500 µs
Duty Cycle	30%
Maximum Pulsed Power Dissipation (P_{DISS}), Drain Bias Pulse Width = 100 µs at 10% Duty Cycle, T_{CASE} = 85°C, Derate 250 mW/°C Above 85°C	35 W
Temperature	
Maximum Channel	225°C
Nominal Pulsed Peak Channel, T_{CASE} = 85°C, P_{IN} = 22 dBm, Drain Bias Pulse Width = 100 µs at 10% Duty Cycle, P_{DISS} = 31 W at 8.6 GHz	209°C
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C

[1] Input signal applied during V_{DD} pulse.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type[1, 2]	θ_{JC}	Unit
EH-18-1	4	°C/W

[1] θ_{JC} was determined under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

[2] Drain bias pulse width = 100 µs at 10% duty cycle.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA1122

Table 6. ADPA1122, 18-Terminal LCC_HS

ESD Model	Withstand Threshold (V)	Class
HBM	500	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

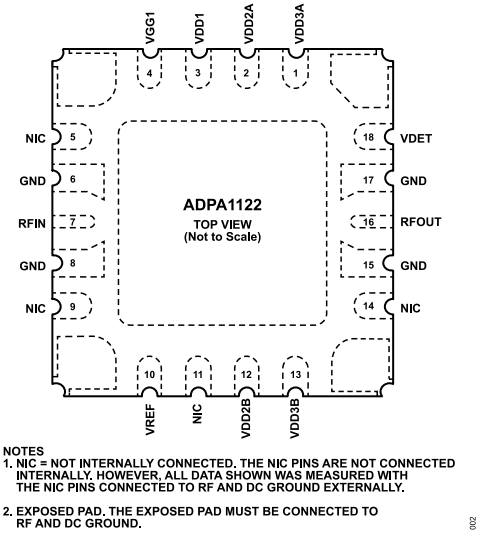

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 12, 13	VDD3A, VDD2A, VDD1, VDD2B, VDD3B	Power Supply Voltage for the Power Amplifier. First, second, and third stage drain bias. See Figure 3 for the interface schematic.
4	VGG1	Gate Bias Voltage. See Figure 4 for the interface schematic.
5, 9, 11, 14	NIC	Not Internally Connected. The NIC pins are not connected internally. However, all data shown was measured with the NIC pins connected to RF and dc ground externally.
6, 8, 15, 17	GND	Ground. The GND pins must be connected to RF and dc ground. See Figure 5 for the interface schematic.
7	RFIN	RF Input. The RFIN pin is ac-coupled in the signal path and is matched to 50 Ω. See Figure 6 for the interface schematic. If the RFIN pin is externally connected to a DC bias level other than 0 V, ac-couple the RFIN pin externally because of the internal DC path to ground.
10	VREF	Reference Diode for Temperature Compensation of VDET RF P_{OUT} Measurements. See Figure 8 for the interface schematic.
16	RFOUT	RF Output. The RFOUT pin is ac-coupled and is matched to 50 Ω. See Figure 7 for the interface schematic.
18	VDET	Detector Diode to Measure RF P_{OUT}. P_{OUT} detection via the VDET pin requires the application of a DC bias voltage through an external series resistor. Used in combination with the VREF pin, the difference voltage (VREF voltage (V_{REF}) − VDET voltage (V_{DET})) is a temperature compensated DC voltage that is proportional to the RF P_{OUT}. See Figure 9 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

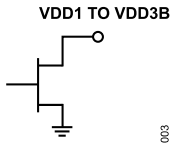

Figure 3. VDD1 to VDD3B Interface Schematic

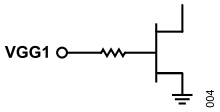

Figure 4. VGG1 Interface Schematic

Figure 5. GND Interface Schematic

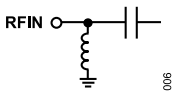

Figure 6. RFIN Interface Schematic

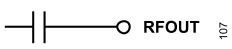

Figure 7. RFOUT Interface Schematic

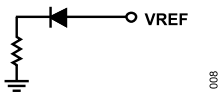

Figure 8. VREF Interface Schematic

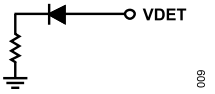

Figure 9. VDET Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

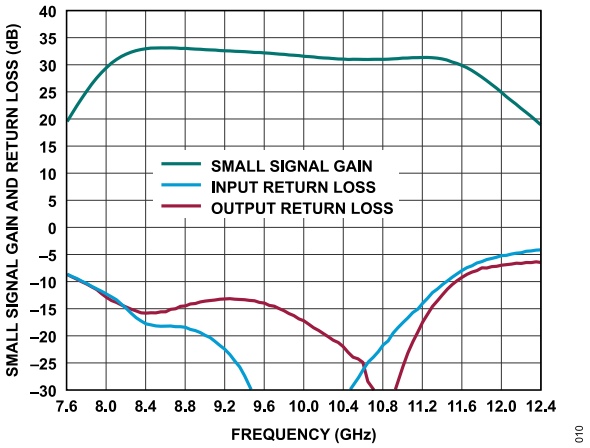

Figure 10. Small Signal Gain and Return Loss vs. Frequency

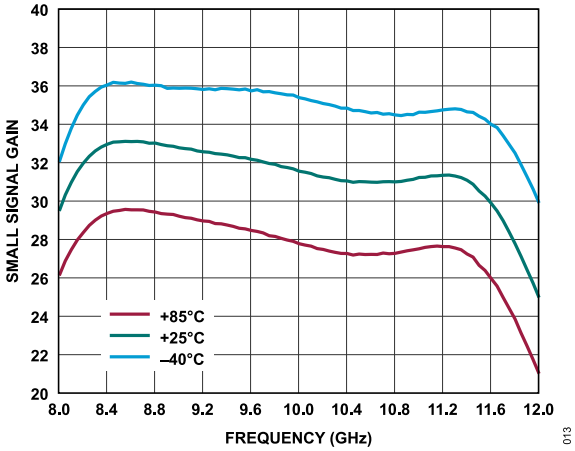

Figure 13. Small Signal Gain vs. Frequency for Various Temperatures

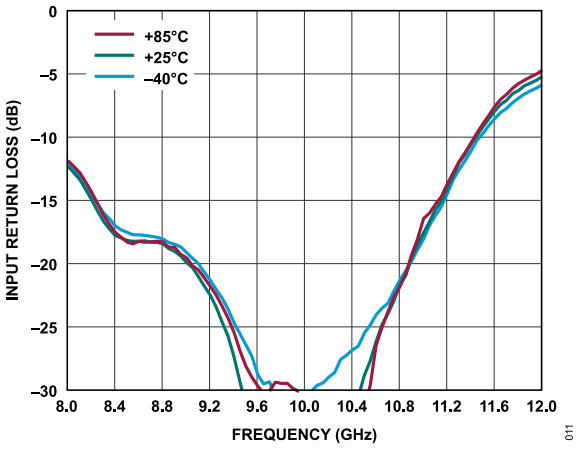

Figure 11. Input Return Loss vs. Frequency for Various Temperatures

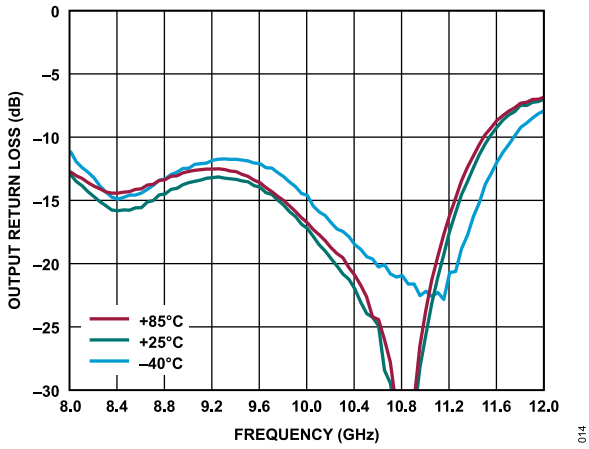

Figure 14. Output Return Loss vs. Frequency for Various Temperatures

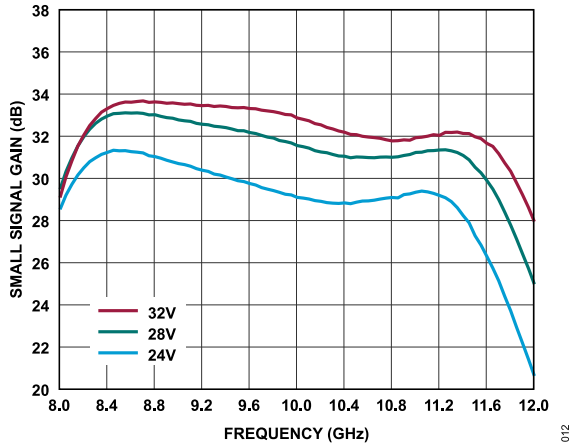

Figure 12. Small Signal Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 200 mA

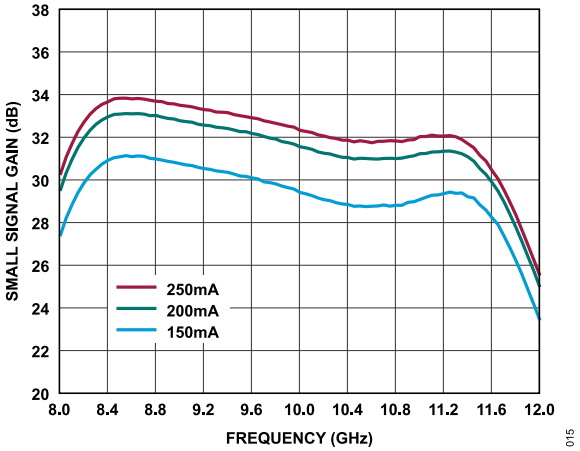

Figure 15. Small Signal Gain vs. Frequency for Various I_{DQ} Values at V_{DD} = 28 V

TYPICAL PERFORMANCE CHARACTERISTICS

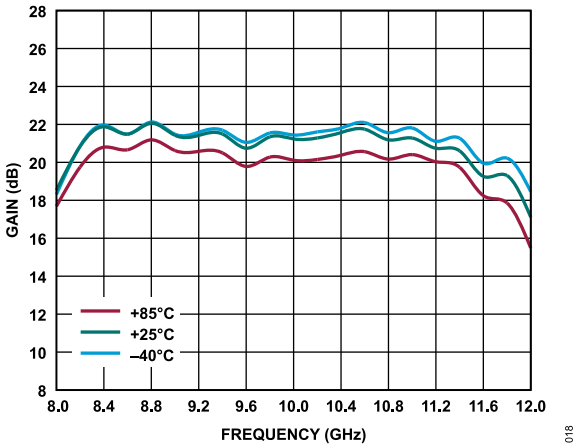

Figure 16. Gain vs. Frequency for Various Temperatures at P_{IN} = 22 dBm

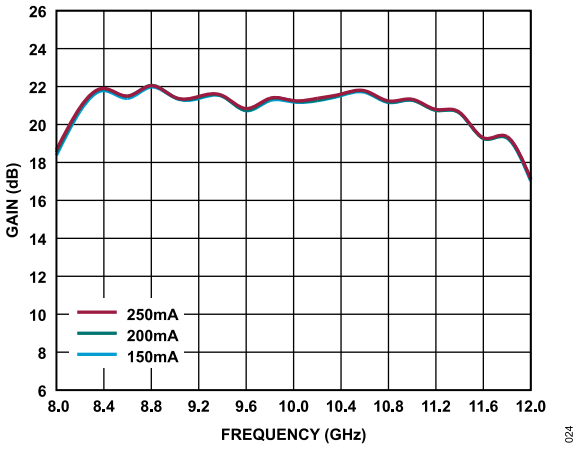

Figure 17. Gain at P_{IN} = 22 dBm vs. Frequency for Various I_{DQ} Values at V_{DD} = 28 V

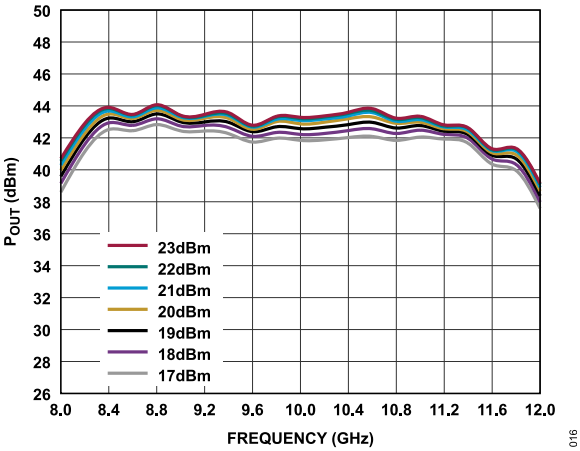

Figure 18. P_{OUT} vs. Frequency for Various P_{IN} Levels

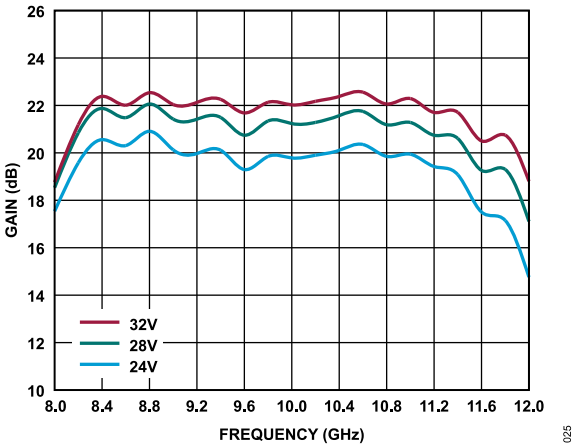

Figure 19. Gain at P_{IN} = 22 dBm vs. Frequency for Various Supply Voltages at I_{DQ} = 200 mA

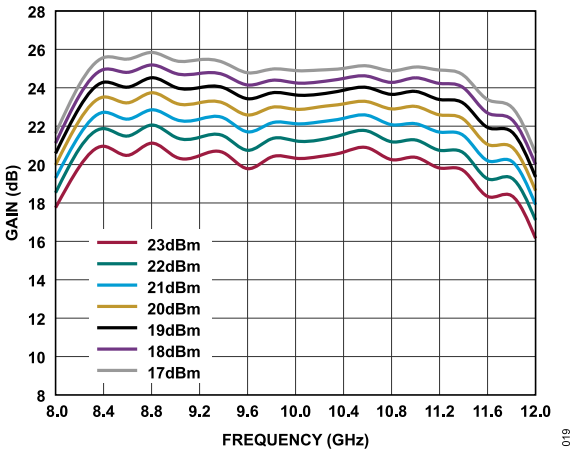

Figure 20. Gain vs. Frequency for Various P_{IN} Levels

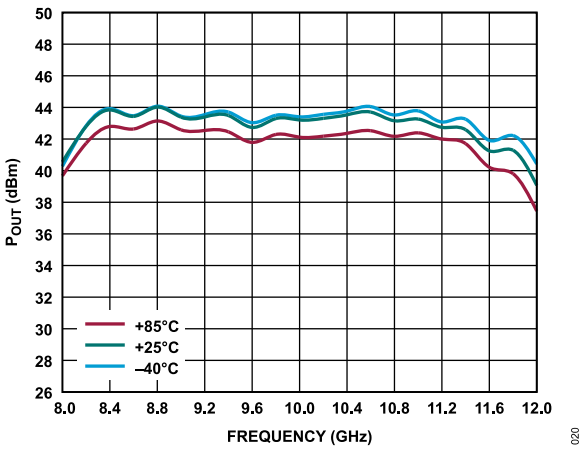

Figure 21. P_{OUT} vs. Frequency for Various Temperatures at P_{IN} = 22 dBm

TYPICAL PERFORMANCE CHARACTERISTICS

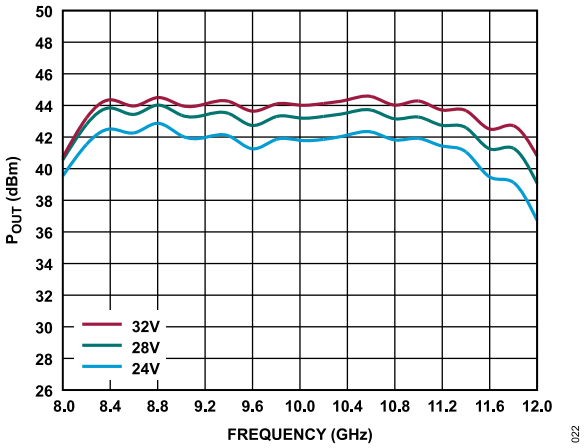

Figure 22. P_{OUT} at P_{IN} = 22 dBm vs. Frequency for Various Supply Voltages at I_{DQ} = 200 mA

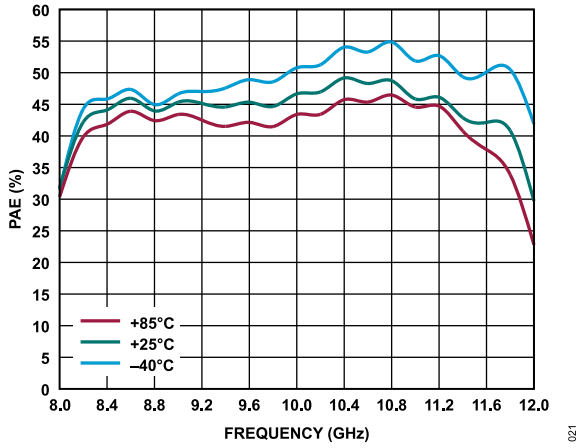

Figure 23. PAE vs. Frequency for Various Temperatures at P_{IN} = 22 dBm

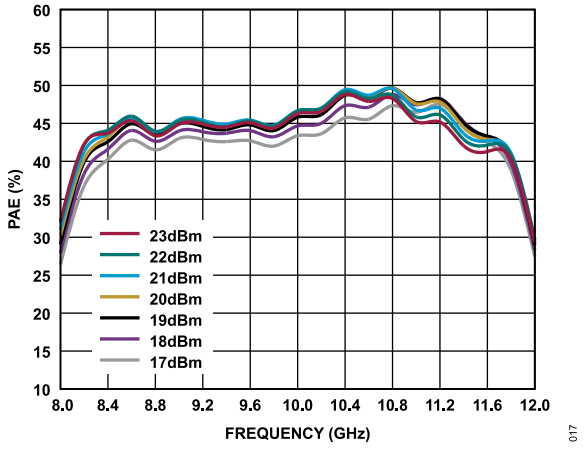

Figure 24. PAE vs. Frequency for Various P_{IN} Levels

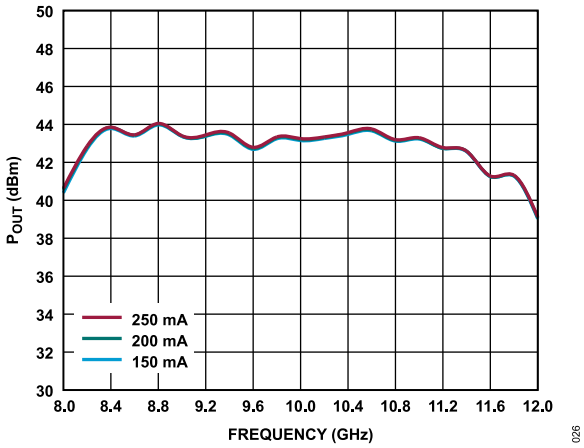

Figure 25. P_{OUT} at P_{IN} = 22 dBm vs. Frequency for Various I_{DQ} Values at V_{DD} = 28 V

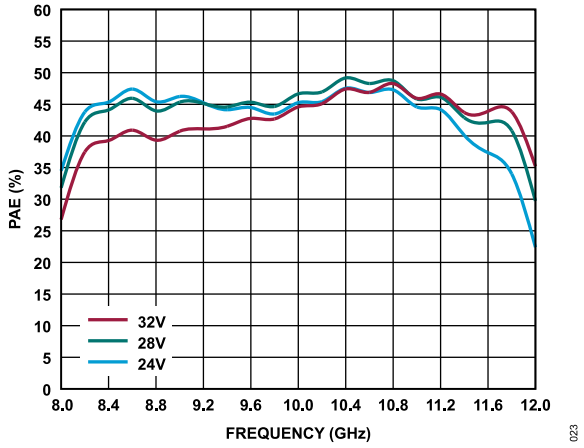

Figure 26. PAE at P_{IN} = 22 dBm vs. Frequency for Various Supply Voltages at I_{DQ} = 200 mA

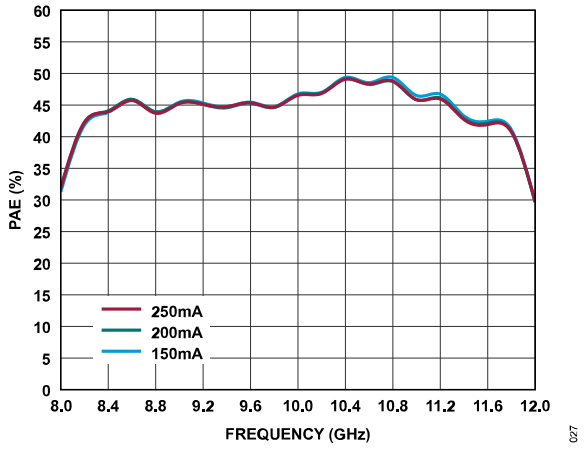

Figure 27. PAE at P_{IN} = 22 dBm vs. Frequency for Various I_{DQ} Values at V_{DD} = 28 V

TYPICAL PERFORMANCE CHARACTERISTICS

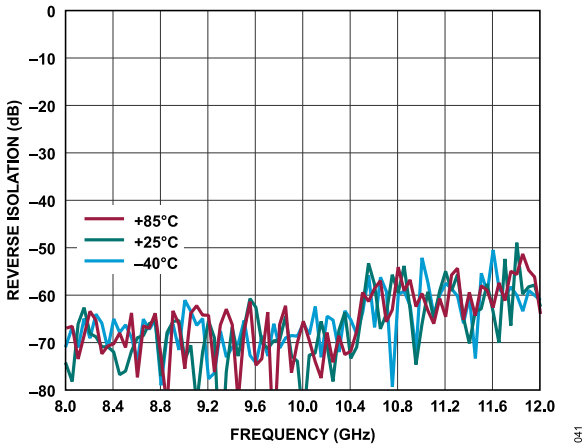

Figure 28. Reverse Isolation vs. Frequency for Various Temperatures

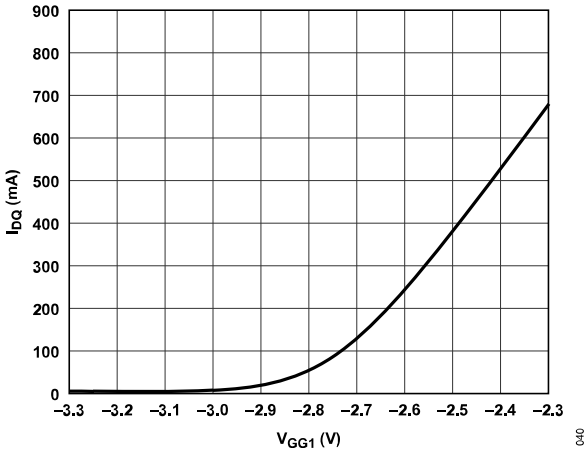

Figure 29. I_{DQ} vs. V_{GG1}, V_{DD} = 28 V

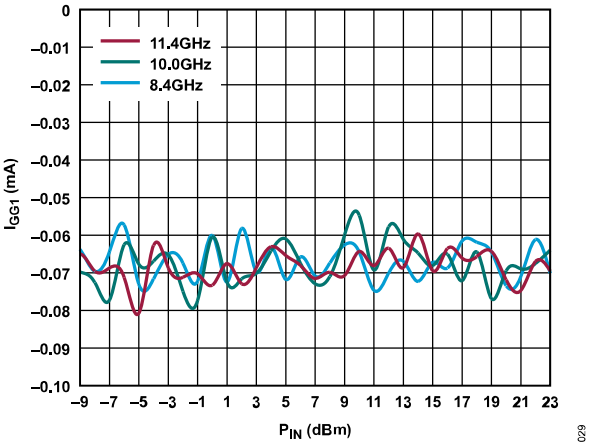

Figure 30. I_{GG1} vs. P_{IN} for Various Frequencies

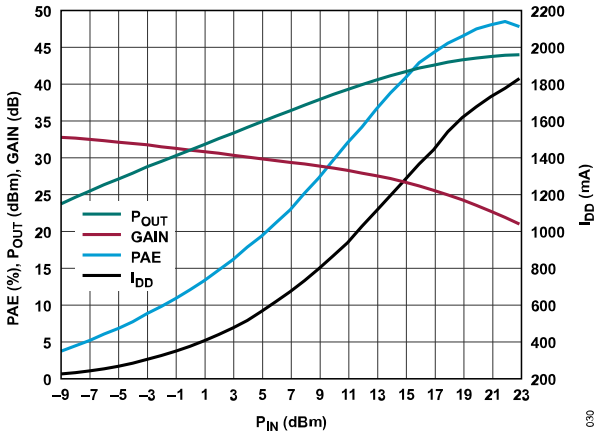

Figure 31. PAE, P_{OUT}, Gain, and Supply Current (I_{DD}) vs. P_{IN} at 8.4 GHz

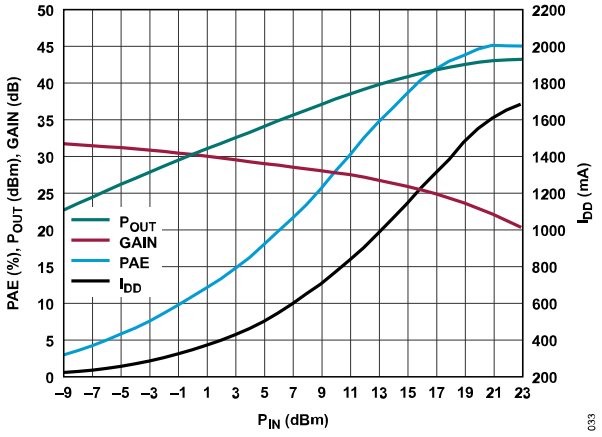

Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 10.0 GHz

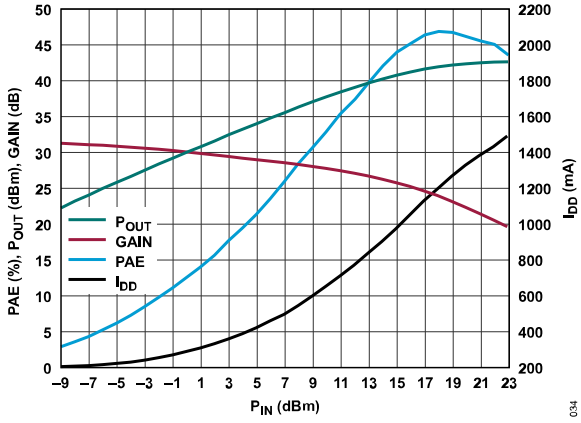

Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 11.4 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

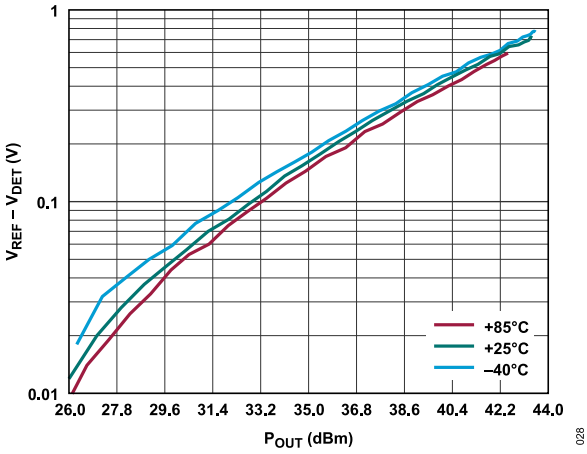

Figure 34. ($V_{REF} - V_{DET}$) vs. P_{OUT} for Various Temperatures at 10.0 GHz

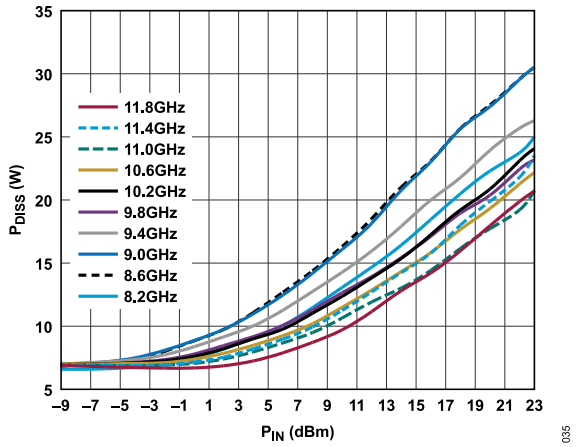

Figure 35. P_{DISS} vs. P_{IN} for Various Frequencies, Pulse Width = 10 µs at 10% Duty Cycle

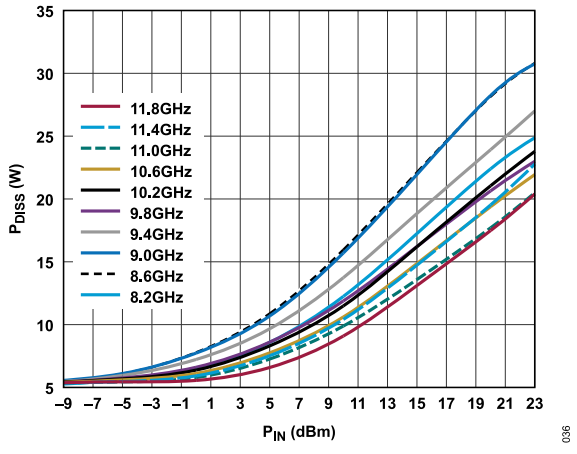

Figure 36. P_{DISS} vs. P_{IN} for Various Frequencies, Pulse Width = 100 µs at 5% Duty Cycle

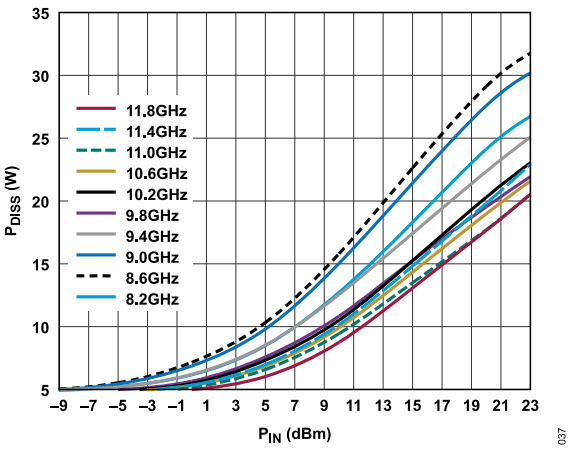

Figure 37. P_{DISS} vs. P_{IN} for Various Frequencies, Pulse Width = 100 µs at 10% Duty Cycle

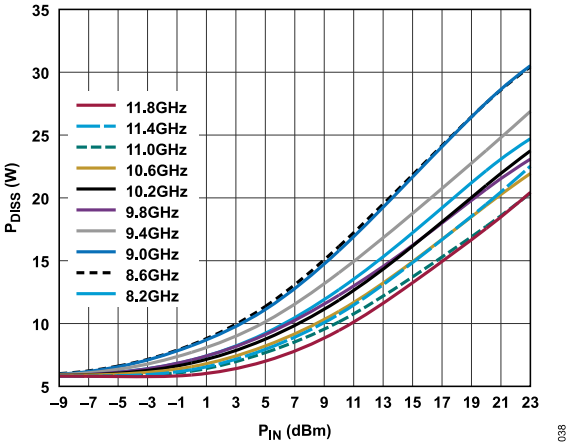

Figure 38. P_{DISS} vs. P_{IN} for Various Frequencies, Pulse Width = 100 µs at 20% Duty Cycle

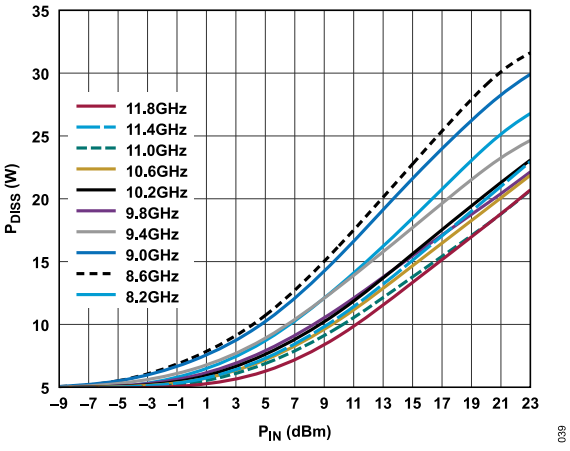

Figure 39. P_{DISS} vs. P_{IN} for Various Frequencies, Pulse Width = 300 µs at 10% Duty Cycle

TYPICAL PERFORMANCE CHARACTERISTICS

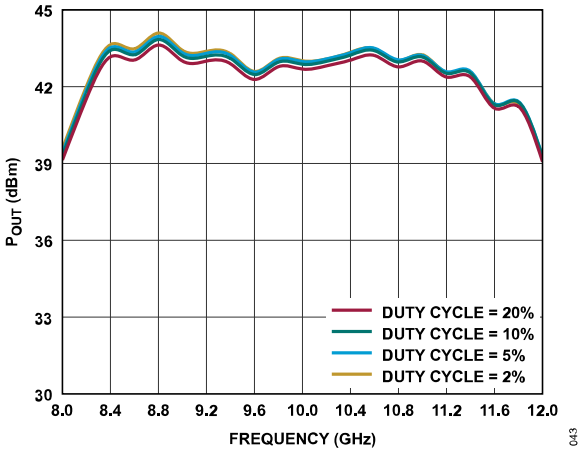

Figure 40. P_{OUT} vs. Frequency at P_{IN} = 22 dBm for Various Duty Cycles at Pulse Width = 100 µs

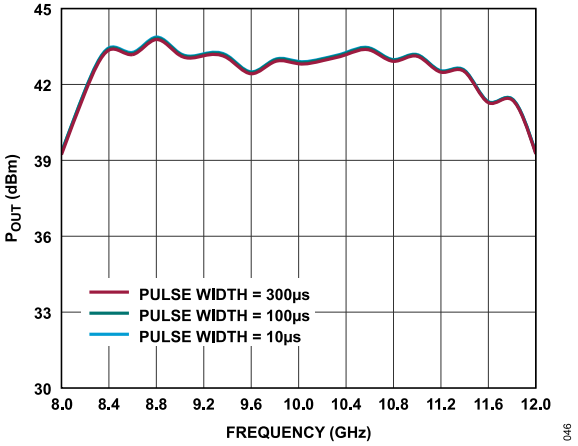

Figure 43. P_{OUT} vs. Frequency at P_{IN} = 22 dBm for Various Pulse Widths at Duty Cycle = 10%

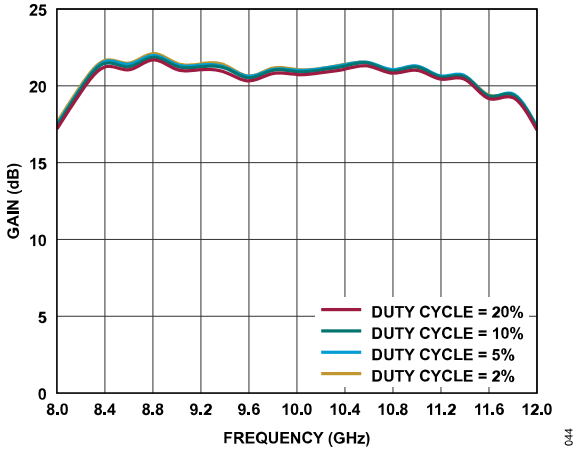

Figure 41. Gain vs. Frequency at P_{IN} = 22 dBm for Various Duty Cycles at Pulse Width = 100 µs

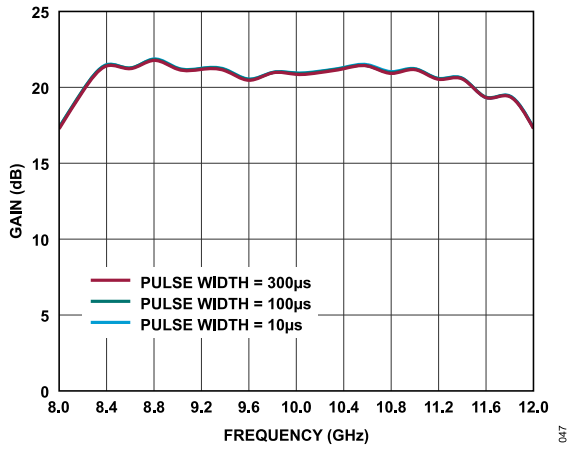

Figure 44. Gain vs. Frequency at P_{IN} = 22 dBm for Various Pulse Widths at Duty Cycle = 10%

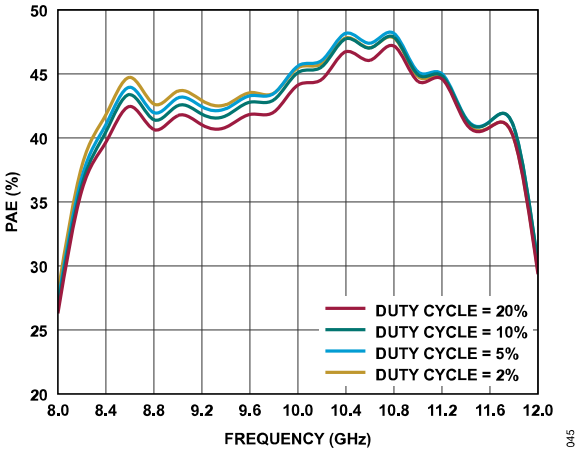

Figure 42. PAE vs. Frequency at P_{IN} = 22 dBm for Various Duty Cycles at Pulse Width = 100 µs

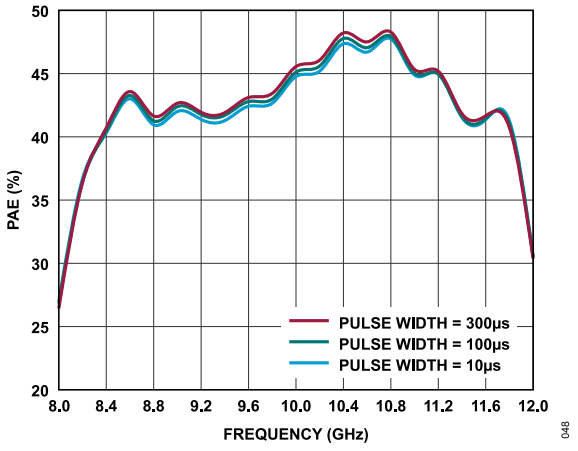

Figure 45. PAE vs. Frequency at P_{IN} = 22 dBm for Various Pulse Widths at Duty Cycle = 10%

THEORY OF OPERATION

The ADPA1122 is a GaN power amplifier that delivers 43 dBm (20 W) of pulsed power. The device consists of three cascaded gain stages. A simplified block diagram is shown in Figure 46.

The pulsed bias voltage that applied to the VDD1, VDD2A, and VDD3A pins provides bias to the drains of the first, second, and third gain stages, respectively (a single common supply voltage must be used). VDD2B and VDD3B are internally connected to VDD2A and VDD3A, respectively, and are used as decoupling nodes. The negative DC voltages applied to the VGG1 pin bias the gates of the first, second, and third gain stages, respectively, to allow control of the drain currents for each stage.

The recommended DC biasing results in a typical pulsed RF P_{OUT} and PAE of 43.5 dBm and 46%, respectively, across the band of 9.6 GHz to 11 GHz when the input power is 22 dBm.

The ADPA1122 has single-ended RFIN and RFOUT ports that are ac-coupled. The impedances of these ports are nominally 50 Ω over the 8.2 GHz to 11.8 GHz operating frequency range. Consequently, the ADPA1122 can be directly inserted into a 50 Ω system without the need for external impedance matching components or AC coupling capacitors.

A portion of the RF output signal (RFOUT) is directionally coupled to a diode to detect the RF P_{OUT}. When the diode is DC biased, it rectifies the RF power and makes it available as a DC voltage at VDET. To allow temperature compensation of VDET, the reference dc voltage detected through an identical diode that is not coupled to the RF power is available on the VREF pin. The difference of $V_{REF} - V_{DET}$ provides a temperature compensated detector voltage that is proportional to the RF P_{OUT}.

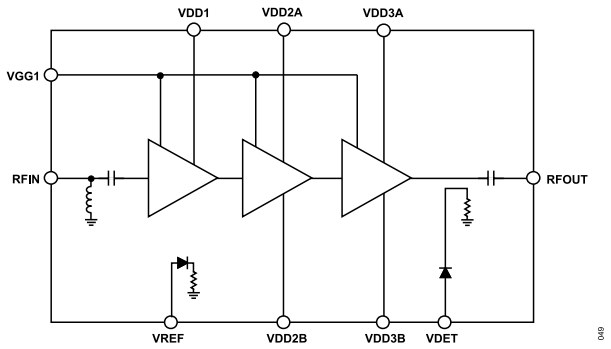

Figure 46. Basic Block Diagram

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The basic connections for operating the ADPA1122 are shown in Figure 47. Apply a power supply voltage between 24 V and 32 V to the VDD1, VDD2A, and VDD3A pins. Decouple the VDD1, VDD2A, VDD2B, VDD3A, and VDD3B pins with the capacitor and resistor values shown in Figure 47. A single VGG1 pin is used to bias the ADPA1122. Pin 5, Pin 9, Pin 11, and Pin 14 are designated as not internally connected (NIC) pins. Although these NIC pins are not internally connected, the NIC pins were all connected to ground during the characterization of the device.

Apply a voltage between −4 V and −2 V to the VGG1 line to set the bias level and drain current. Because the ADPA1122 cannot support continuous operation, the device must be operated in pulsed mode by pulsing either the gate voltage or the drain voltage.

In gate pulsed mode, V_{DD} is held at a fixed level (nominally +28 V) while the gate voltage is pulsed between −4 V (off) and approximately −2.6 V (on). The exact on level can be adjusted to achieve the desired quiescent drain current.

In drain pulsed mode, the V_{DD} voltage is pulsed on and off while the gate voltage is held at a fixed negative level between −4 V and −2 V. Because high currents and voltages are being switched on and off, a metal-oxide semiconductor field effect transistor (MOSFET) and a MOSFET switch driver are required in the circuit. Large capacitors are also required, which act as local reservoirs of charge and help provide the drain current required by the ADPA1122 while maintaining a steady drain voltage during the on time of the pulse.

The ADPA1122-EVALZ evaluation board package includes a plugin pulser board that contains the required circuitry to implement drain pulsed mode. See the ADPA1122-EVALZ user guide for more information.

To safely turn power on, V_{GG1} must be set to −4 V before the V_{DD} voltages are applied. After V_{GG1} is increased to achieve the desired drain bias current, the RF input can be applied. Trigger the RF source so that the RF is applied only during the time the drain pulse is high. To safely turn power off, remove the RF input signal and decrease V_{GG1} to −4 V. V_{DD} can then be decreased to 0 V before increasing V_{GG1} to 0 V.

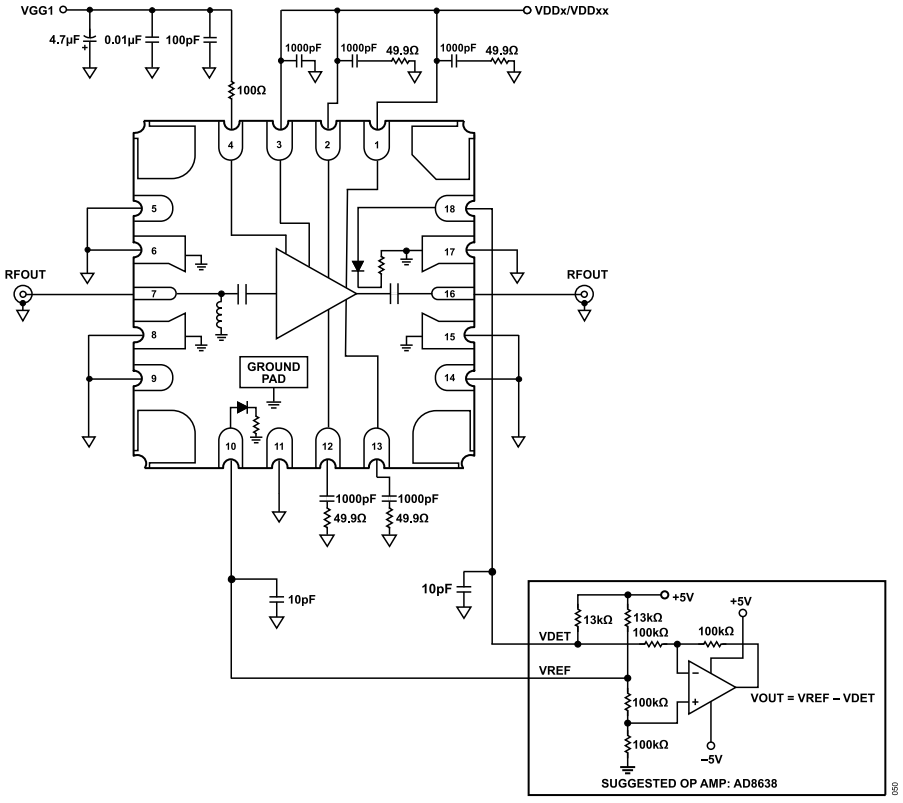

Figure 47. Basic Connections

APPLICATIONS INFORMATION

THERMAL MANAGEMENT

Proper thermal management is critical to achieve the specified performance and rated operating life. Pulsed biasing is required to limit the average power dissipated and to maintain a safe channel temperature. The channel (or die) temperature correlates closely with the mean time to failure.

Consider a continuous bias case (see Figure 48). When bias is applied, the channel temperature (T_{CHAN}) of the device rises through a turn on transient interval and eventually settles to a steady state value. Calculate the thermal resistance (θ_{JC}) of the device as the rise in T_{CHAN} above the starting T_{BASE} divided by the total device P_{DISS} with the following equation:

$$\theta_{JC} = t_{RISE}/P_{DISS}$$

where:
t_{RISE} is the rise in T_{CHAN} of the device above the T_{BASE} (°C).
P_{DISS} is the power dissipation (W) of the device.

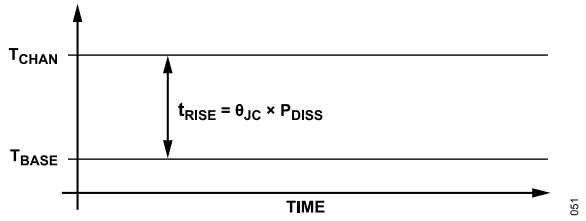

Figure 48. Channel Temperature Rise for Continuous Bias Condition

Next, consider a pulsed bias case at low duty cycle (see Figure 49). When bias is applied, the T_{CHAN} of the device can be described as a series of exponentially rising and decaying pulses. The peak channel temperature reached during consecutive pulses increases during the turn on transient interval and eventually settles to a steady state condition where peak channel temperatures from pulse to pulse stabilize.

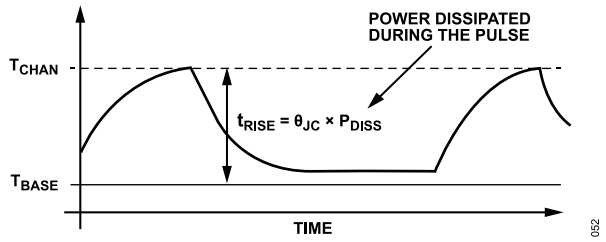

Figure 49. Pulsed Bias at Low Duty Cycle

OUTLINE DIMENSIONS

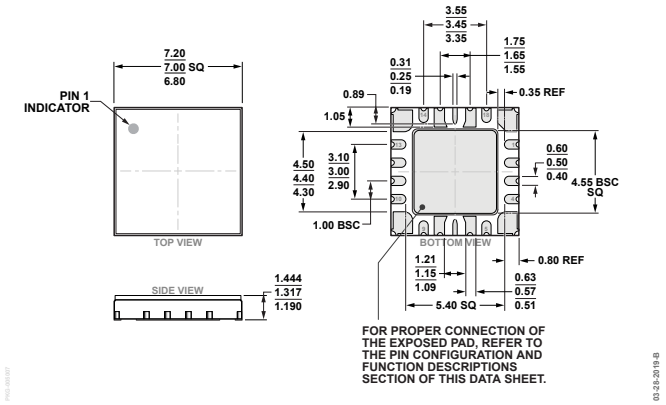

Figure 50. 18-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]
(EH-18-1)
Dimensions shown in millimeters

Updated: September 07, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADPA1122AEHZ	−40°C to +85°C	18-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]	Reel, 1	EH-18-1
ADPA1122AEHZ-R7	−40°C to +85°C	18-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]	Reel, 100	EH-18-1

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 8. Evaluation Boards

Models[1]	Description
ADPA1122-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.