GaAs, pHEMT, MMIC, Low Noise Amplifier, 23 GHz to 31 GHz

FEATURES

▶ Low noise figure: 1.8 dB typical at 27 GHz to 31 GHz
▶ Single positive supply (self biased)
▶ High gain: 26.5 dB typical at 27 GHz to 31 GHz
▶ High OIP3: 20 dBm typical at 27 GHz to 31 GHz
▶ Die size: 0.945 mm × 1.015 mm × 0.100 mm

APPLICATIONS

▶ Satellite communication
▶ Telecommunications
▶ Civilian radar

GENERAL DESCRIPTION

The ADL8142-2CHIP is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), low noise wideband amplifier that operates from 23 GHz to 31 GHz. The ADL8142-2CHIP provides a typical gain of 26.5 dB, a 1.8 dB typical noise figure, and a typical output third-order intercept (OIP3) of 20 dBm at 27 GHz to 31 GHz, requiring only 25 mA from a 2 V supply voltage. Note that the OIP3 can be improved with larger drain currents. The ADL8142-2CHIP also features inputs and outputs that are ac-coupled and internally matched to 50 Ω, making it ideal for high capacity microwave radio applications.

FUNCTIONAL BLOCK DIAGRAM

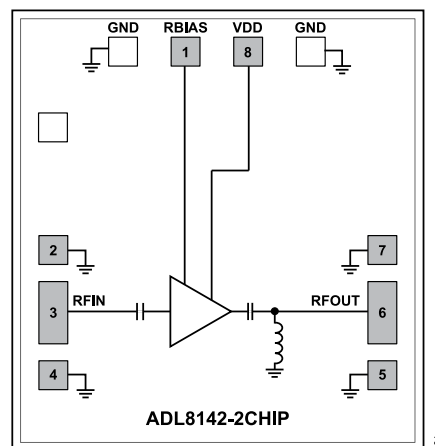Figure 1. Functional Block Diagram

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REVISION HISTORY

7/2022—Revision 0: Initial Version

SPECIFICATIONS

FREQUENCY RANGE: 23 GHz TO 27 GHz

T_{CASE} = 25°C, supply voltage (V_{DD}) = 2 V, and quiescent current (I_{DQ}) = 25 mA for nominal operation, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	23		27	GHz	
GAIN		28		dB	
Gain Variation over Temperature		0.023		dB/°C	
NOISE FIGURE		1.9		dB	
RETURN LOSS					
Input		11		dB	
Output		12		dB	
OUTPUT					
Power for 1 dB Compression (OP1dB)		7		dBm	
Saturated Output Power (P_{SAT})		9		dBm	
OIP3		16		dBm	Measurement taken at output power (P_{OUT}) per tone = –2 dBm
POWER ADDED EFFICIENCY (PAE)		14		%	Measured at P_{SAT}

FREQUENCY RANGE: 27 GHz TO 31 GHz

T_{CASE} = 25°C, V_{DD} = 2 V, and I_{DQ} = 25 mA for nominal operation, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	27		31	GHz	
GAIN	23.5	26.5		dB	
Gain Variation over Temperature		0.022		dB/°C	
NOISE FIGURE		1.8		dB	
RETURN LOSS					
Input		21		dB	
Output		8		dB	
OUTPUT					
OP1dB	6	8.5		dBm	
P_{SAT}		10		dBm	
OIP3		20		dBm	Measurement taken at P_{OUT} per tone = –2 dBm
POWER ADDED EFFICIENCY (PAE)		17		%	Measured at P_{SAT}

DC SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ}		25		mA
Amplifier Current (I_{DQ_AMP})		22.6		mA
RBIAS Current (I_{RBIAS})		2.4		mA
SUPPLY VOLTAGE				
V_{DD}	1.5	2	3.5	V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD}	4.0 V
RFIN	20 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 6 mW/°C Above 85°C)	0.54 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−55°C to +85°C
Nominal Channel (T_{CASE} = 85°C, V_{DD} = 2 V, I_{DQ} = 25 mA, Input Power (P_{IN}) = Off)	93.3°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Overall thermal performance is directly linked to the carrier or substrate on which the die is mounted. Careful attention is needed with each material used in the thermal path below the IC. With an epoxy layer of nominal thickness assumed under the die, θ_{JC} is the thermal resistance from the die channel to the bottom of the epoxy layer.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
C-8-28	166.5	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001.

ESD Ratings for the ADL8142-2CHIP

Table 6. ADL8142-2CHIP, 8-Pad CHIP

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
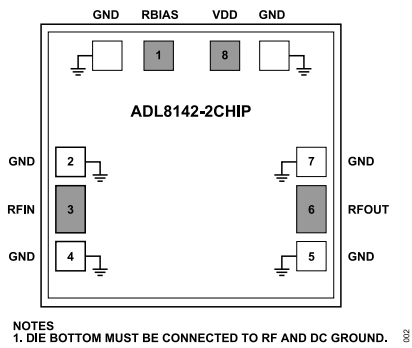
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

NOTES
1. DIE BOTTOM MUST BE CONNECTED TO RF AND DC GROUND.

Figure 2. Pad Configuration

Table 7. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD to set the I_{DQ}. See Figure 60 and Table 8 for more details. See Figure 3 for the interface schematic.
2, 4, 5, 7	GND	Ground. Connect the GND pins to a ground plane that has low electrical and thermal impedance. See Figure 6 for the interface schematic.
3	RFIN	RF Input. The RFIN pin is ac-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
6	RFOUT	RF Output. The RFOUT pin is ac-coupled and matched to 50 Ω. While the RF output path is ac-coupled, there is a dc path to ground on the RFOUT side of the ac coupling capacitor. See Figure 5 for the interface schematic.
8	VDD	Drain Bias. Connect the VDD pin to the supply voltage. See Figure 5 for the interface schematic.
Die Bottom	GND	Die bottom must be connected to RF and dc ground.

INTERFACE SCHEMATICS
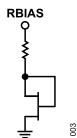
Figure 3. RBIAS Interface Schematic
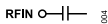
*Figure 4. RFIN Interface Schematic*
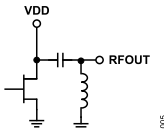
Figure 5. RFOUT/VDD Interface Schematic

Figure 6. GND Interface Schematic

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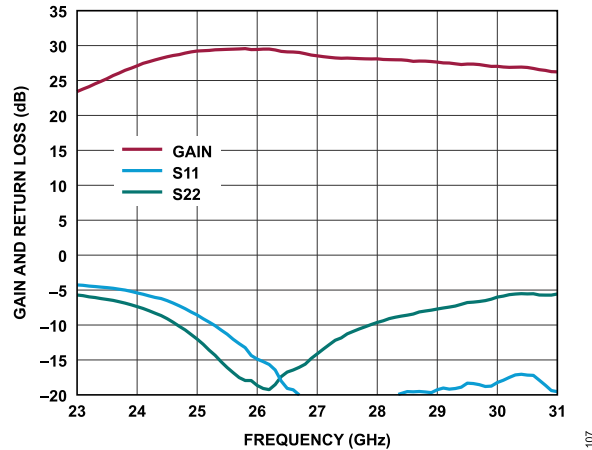
Figure 7. Gain and Return Loss vs. Frequency, V_{DD} = 2 V, I_{DQ} = 25 mA
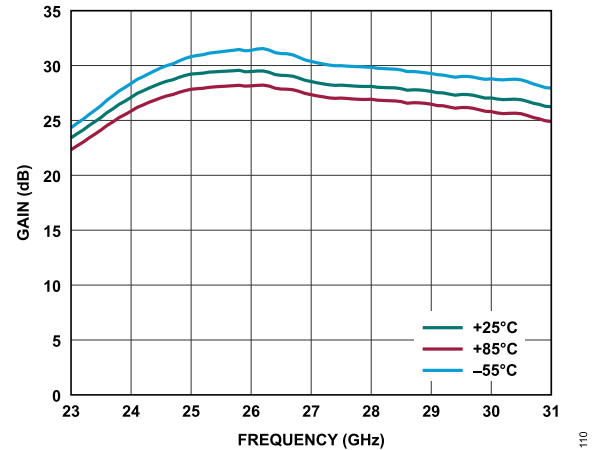
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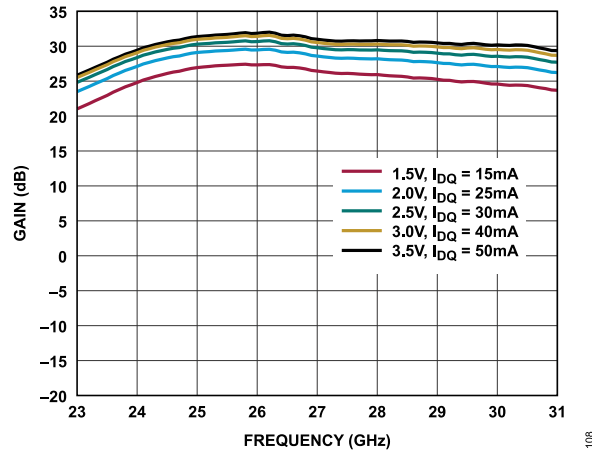
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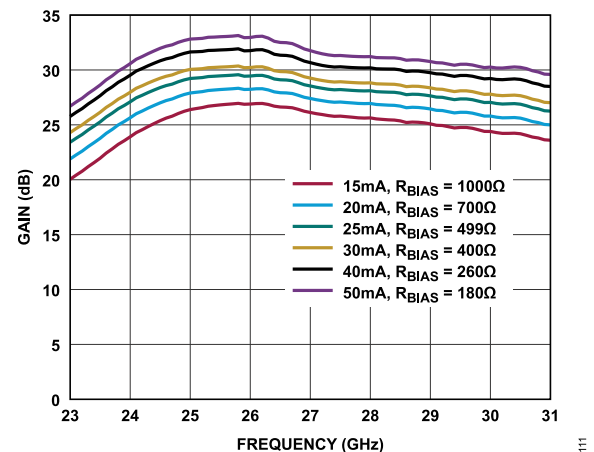
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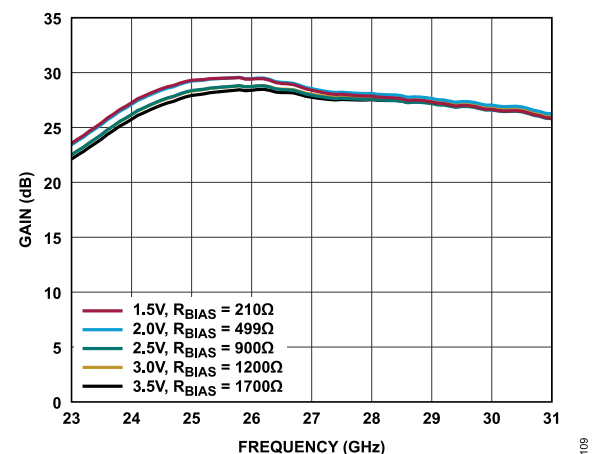
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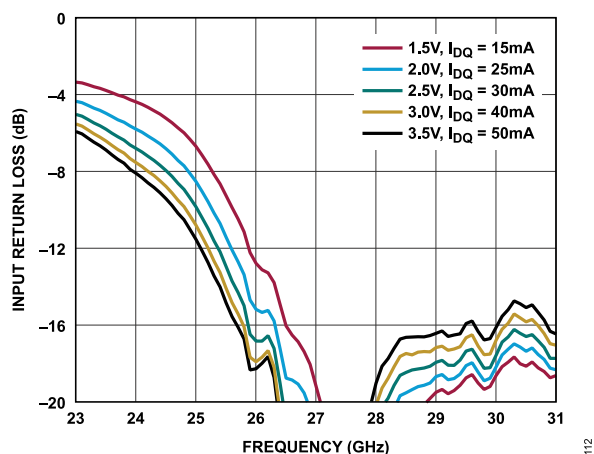
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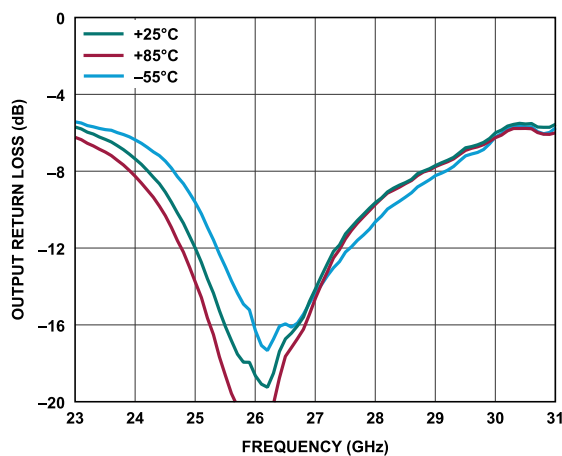# TYPICAL PERFORMANCE CHARACTERISTICS
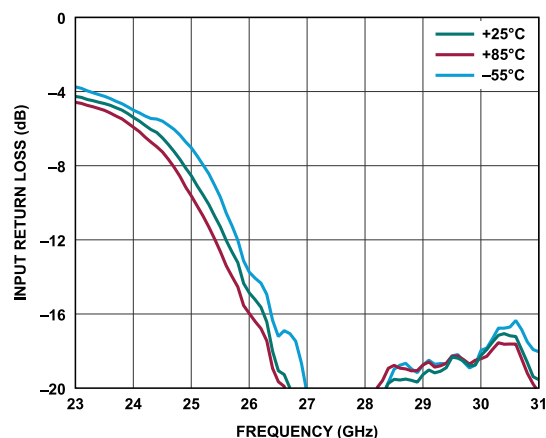
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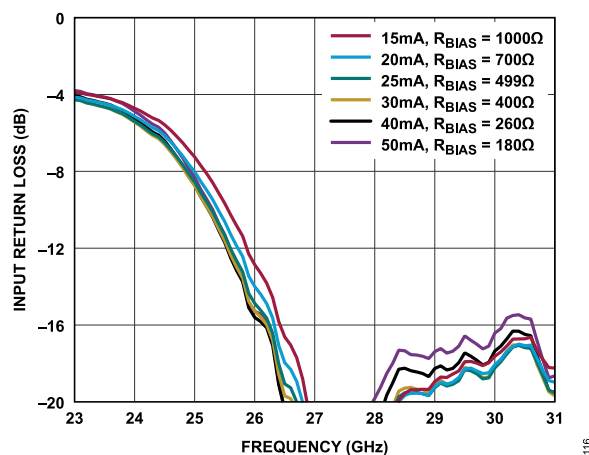
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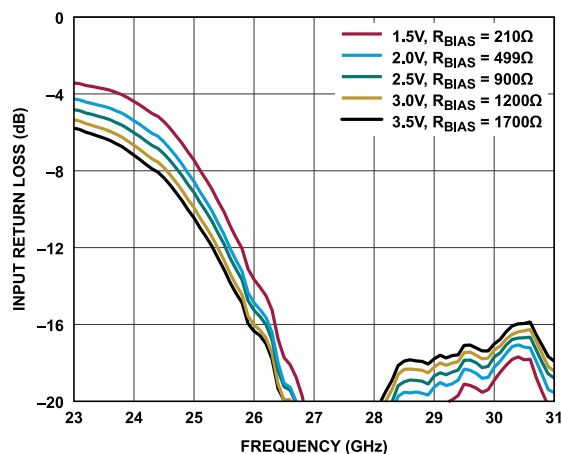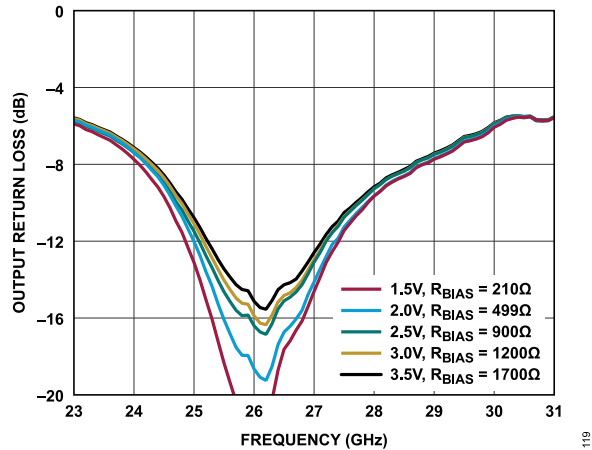

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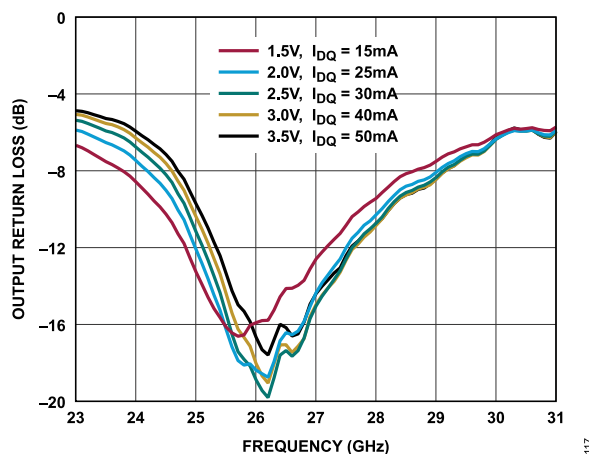
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Figure 15. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 499 Ω
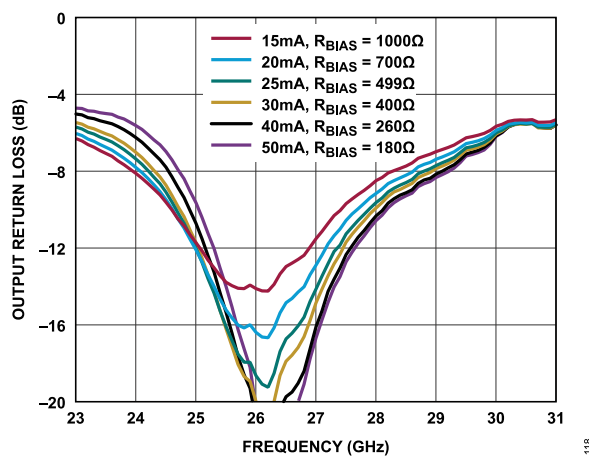
Figure 18. Output Return Loss vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

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Figure 19. Output Return Loss vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA
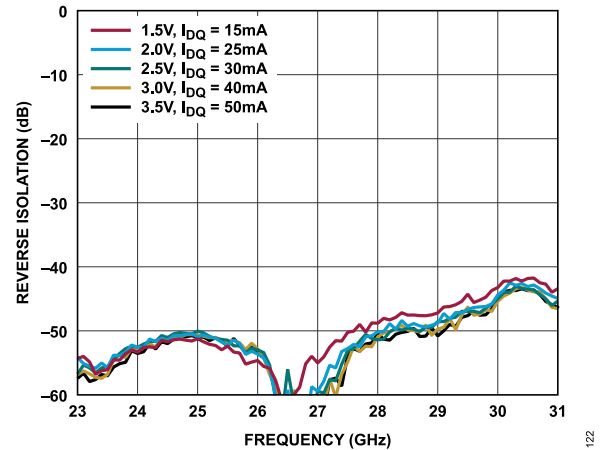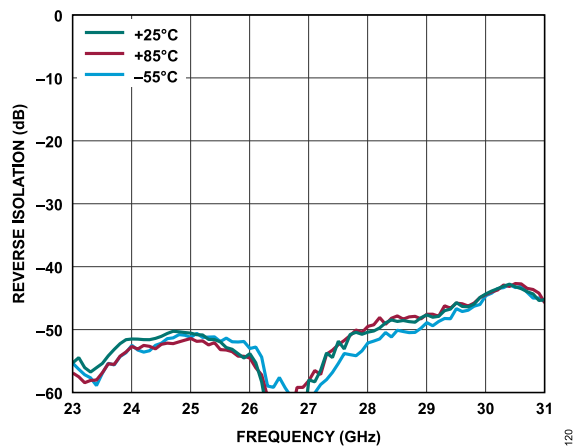

Figure 20. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 499 Ω
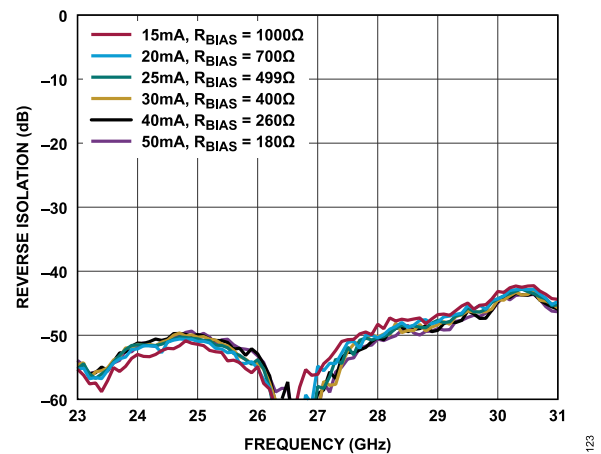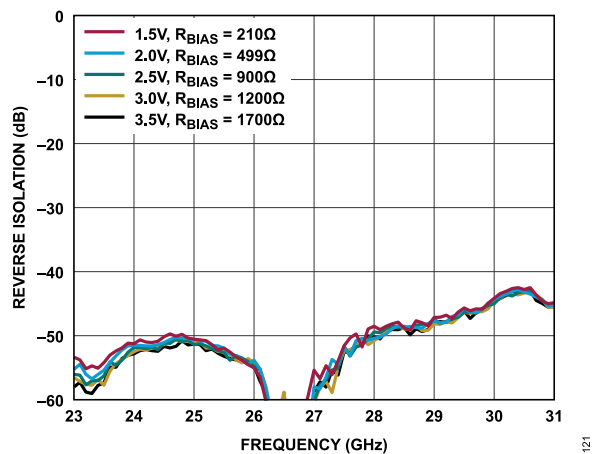

Figure 21. Reverse Isolation vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

Figure 22. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 499 Ω

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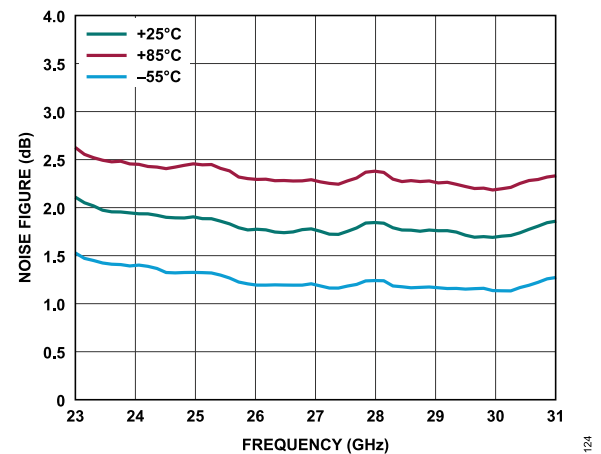

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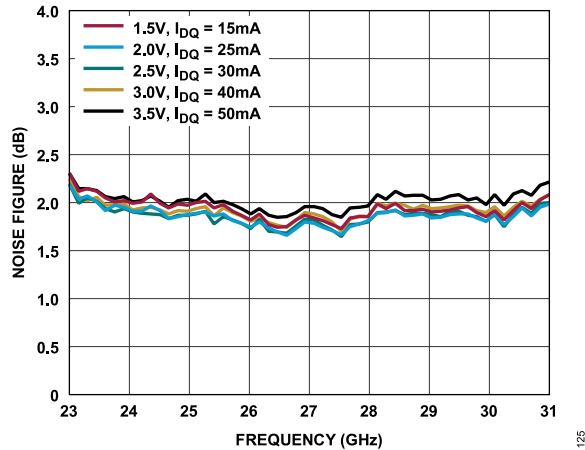

Figure 25. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 499 Ω
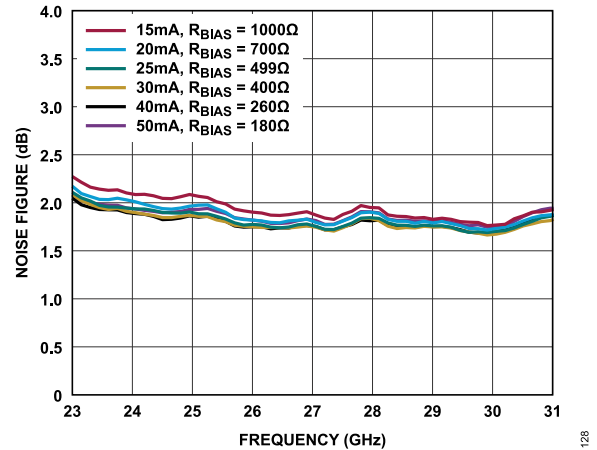

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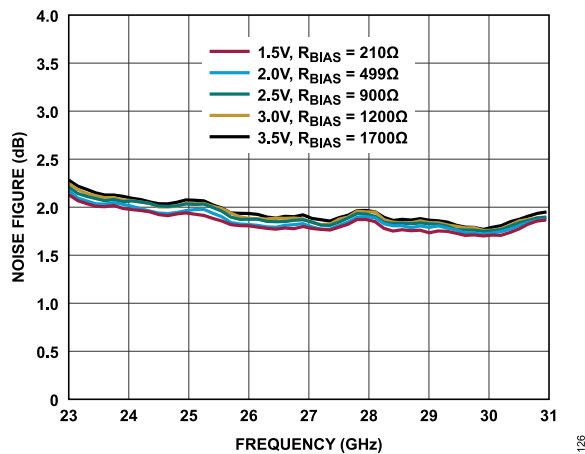

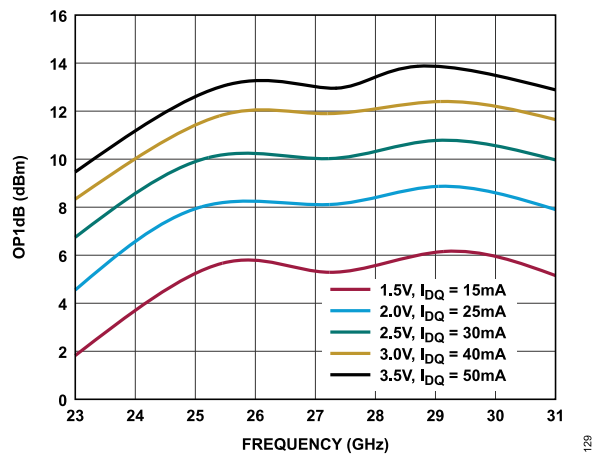Figure 26. Noise Figure vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

Figure 29. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 499 Ω

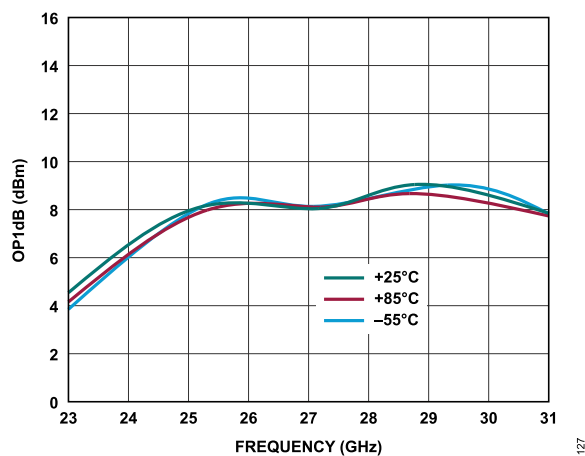Figure 27. OP1dB vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 499 Ω
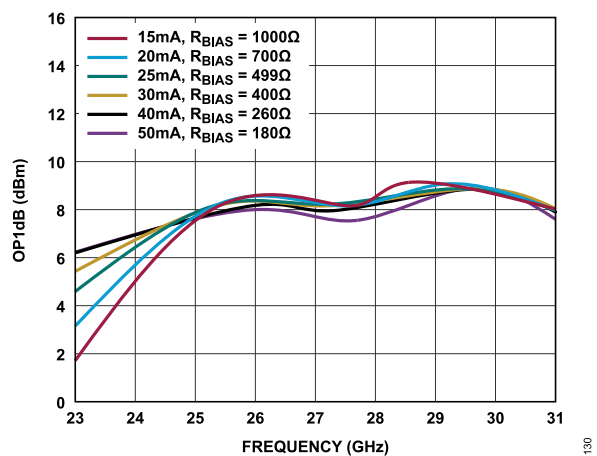

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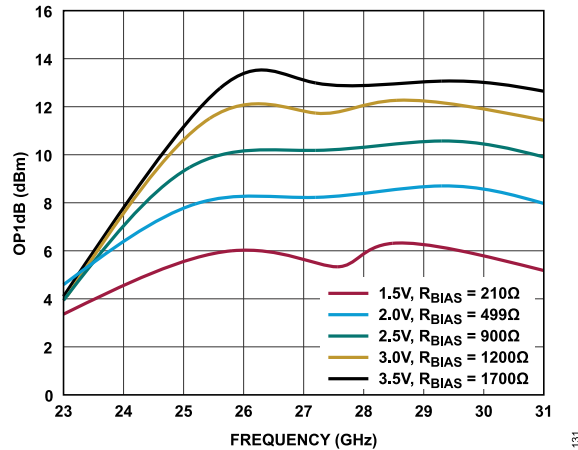
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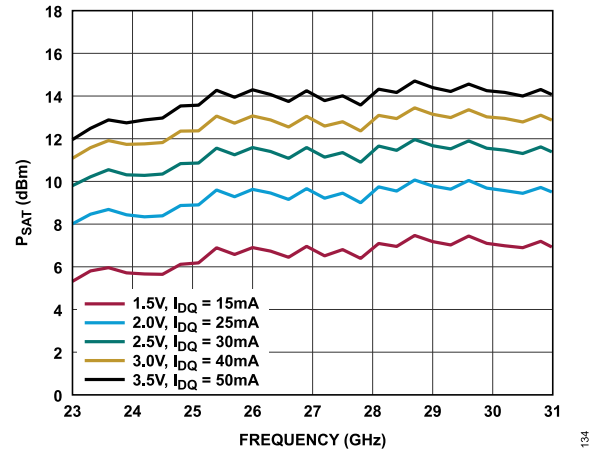*Figure 31. OP1dB vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA*

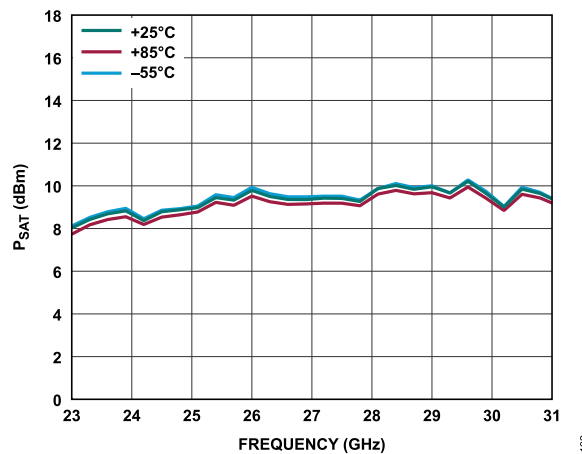*Figure 34. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 499 Ω*

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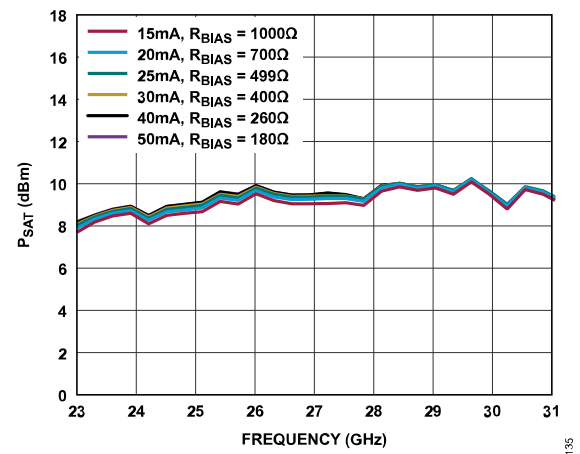

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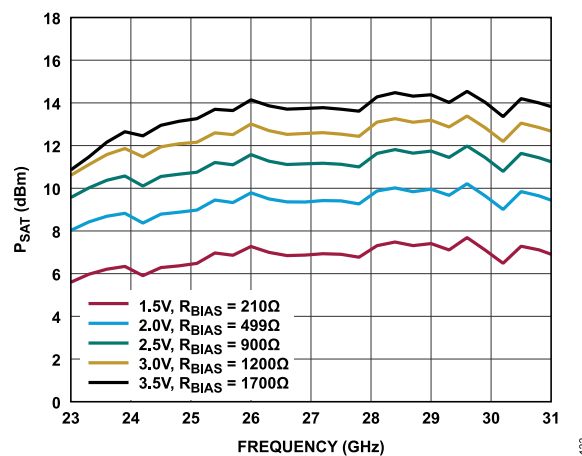

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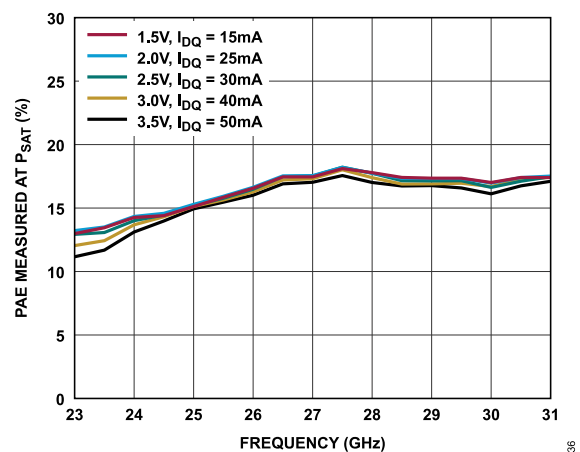

Figure 36. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 499 Ω
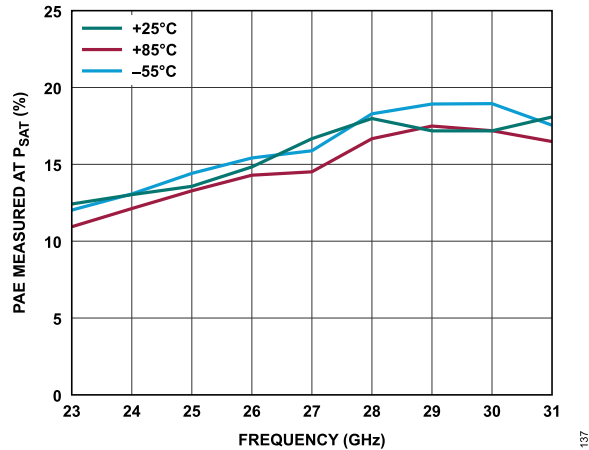
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Figure 37. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 2 V, I_{DQ} = 25 mA, R_{BIAS} = 499 Ω
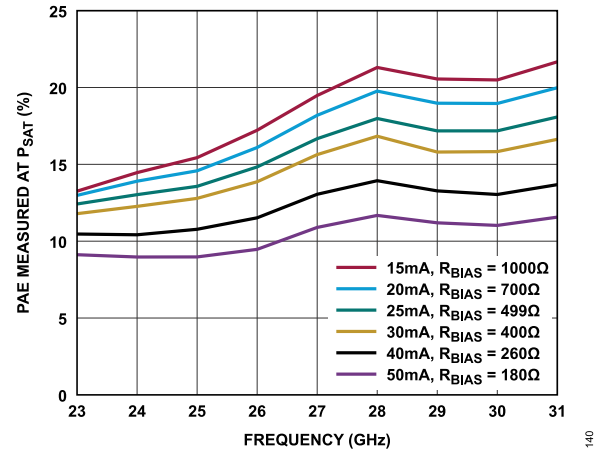

Figure 40. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V
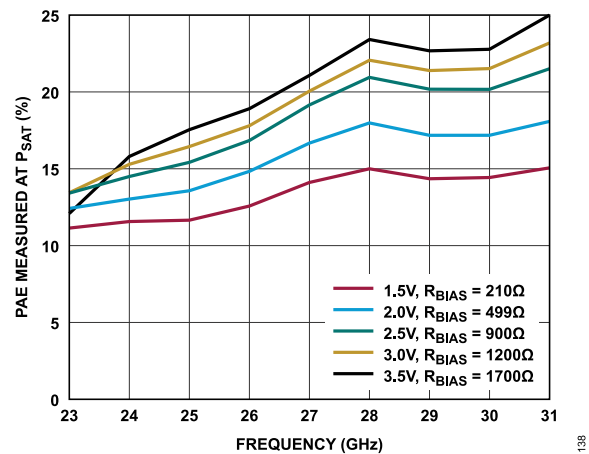

Figure 38. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA
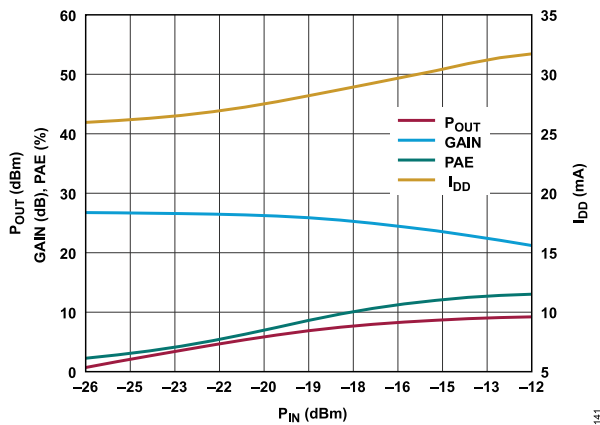

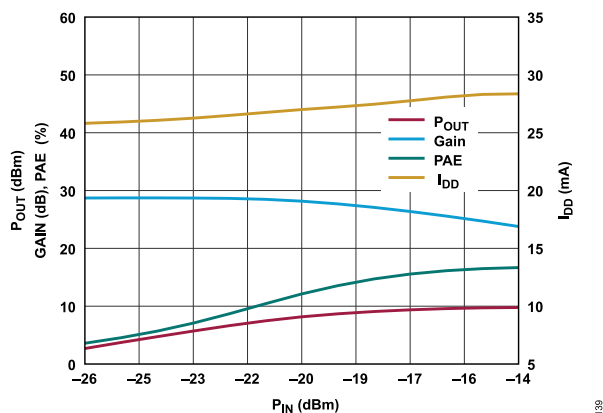Figure 41. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 24 GHz, V_{DD} = 2 V, R_{BIAS} = 499 Ω

Figure 39. P_{OUT}, Gain, PAE, and Power Supply Current (I_{DD}) vs. P_{IN} at 27 GHz, V_{DD} = 2 V, R_{BIAS} = 499 Ω
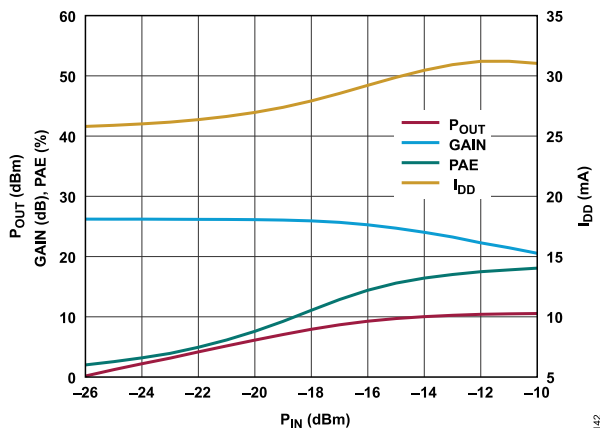

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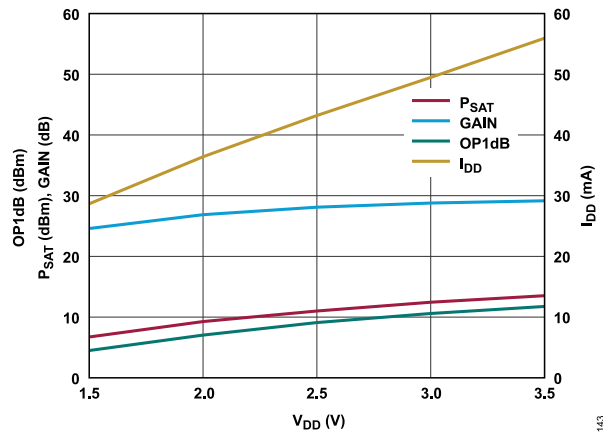
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Figure 44. OP1dB, P_{SAT}, Gain, and I_{DD} vs. Supply Voltage at 31 GHz, R_{BIAS} = 499 Ω

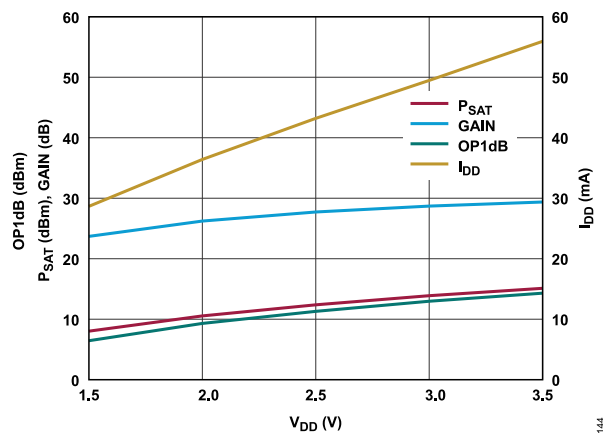Figure 45. I_{DD} vs. P_{IN} for Various Frequencies, V_{DD} = 2 V
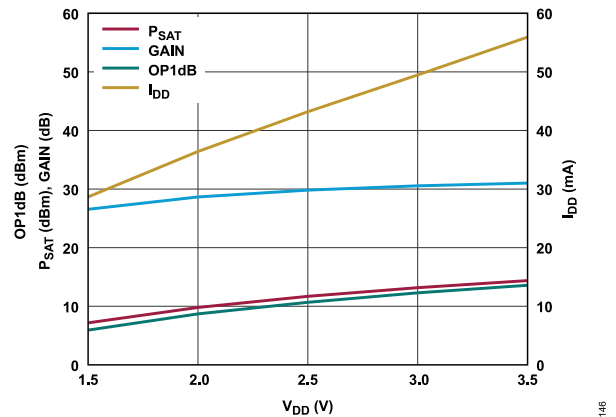
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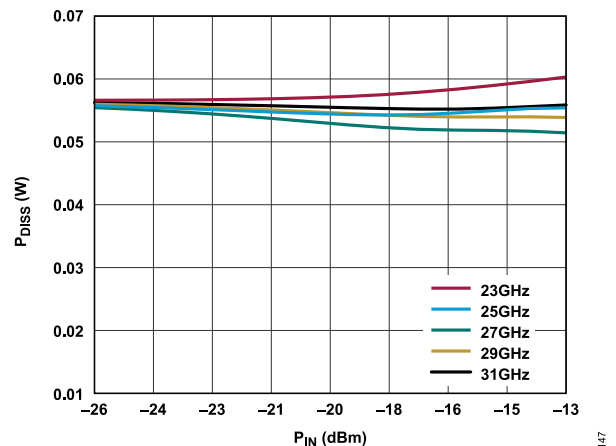
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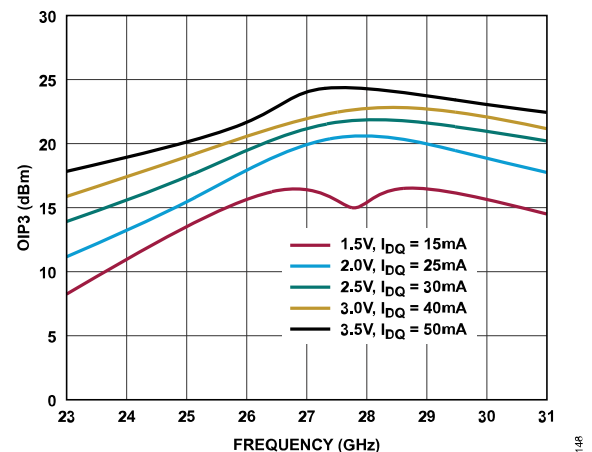
Figure 48. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ} Values, R_{BIAS} = 499 Ω

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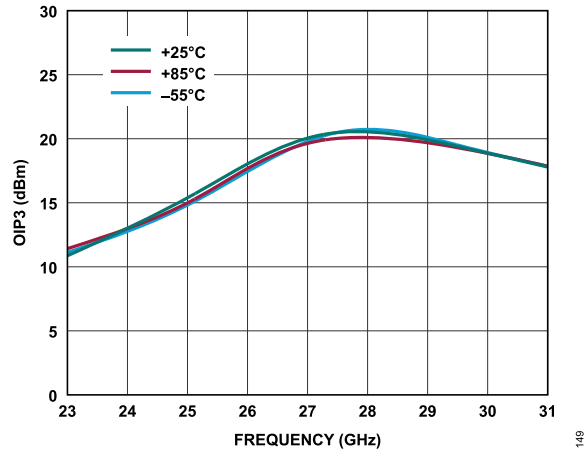
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Figure 50. OIP3 vs. Frequency for Various Supply Voltages and R_{BIAS} Values, I_{DQ} = 25 mA

Figure 51. Third-Order Intermodulation (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 2 V, R_{BIAS} = 499 Ω

Figure 52. OIP3 vs. Frequency for Various I_{DQ} and R_{BIAS} Values, V_{DD} = 2 V

Figure 53. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 1.5 V, R_{BIAS} = 499 Ω
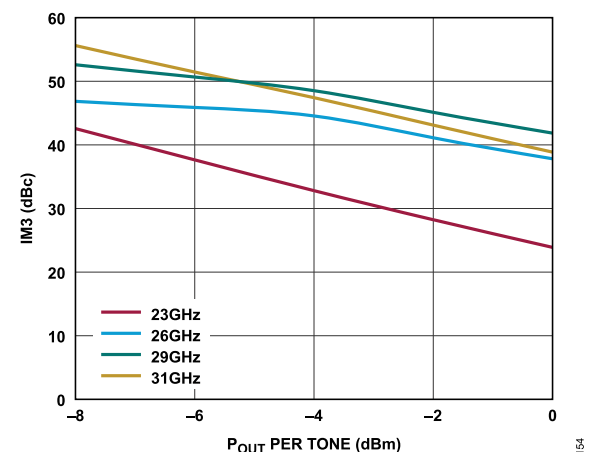
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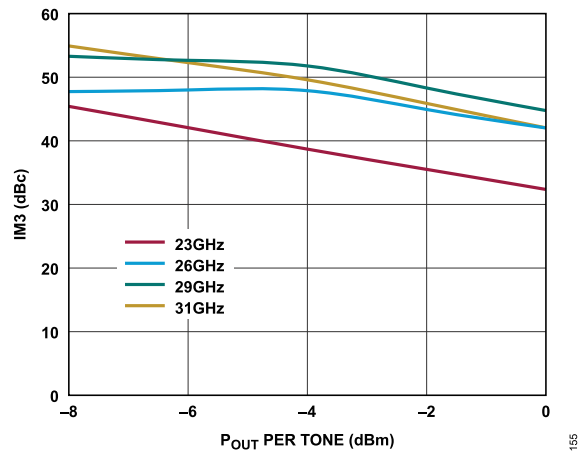
Figure 55. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3.0 V, R_{BIAS} = 499 Ω
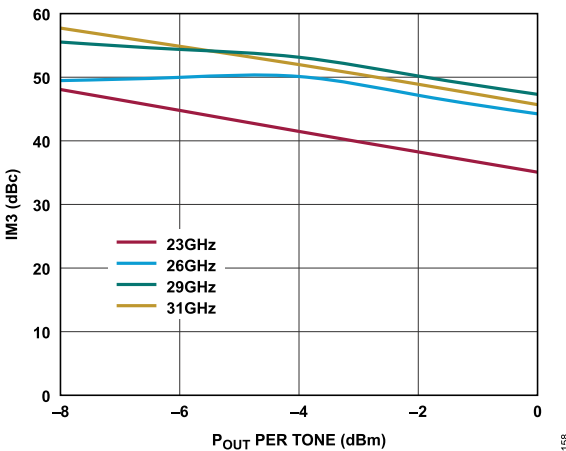
Figure 58. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 3.5 V, R_{BIAS} = 499 Ω
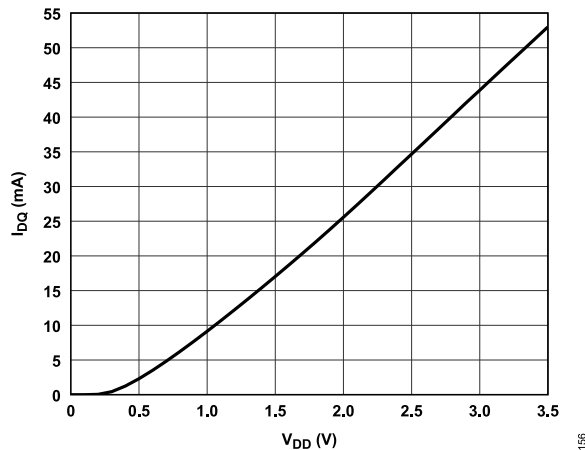
Figure 56. I_{DQ} vs. V_{DD}, R_{BIAS} = 499 Ω
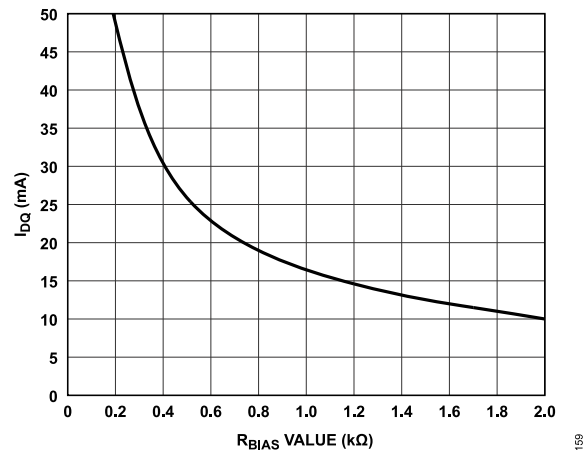
Figure 57. I_{DQ} vs. R_{BIAS} Value, V_{DD} = 2 V

THEORY OF OPERATION

The ADL8142-2CHIP is a GaAs, MMIC, pHEMT, low noise wide-band amplifier with an integrated bias inductor and ac-coupling capacitors. The simplified block diagram is shown in Figure 59.

To adjust the drain bias current, connect an external resistor between the RBIAS and VDD pins.

The ADL8142-2CHIP has ac-coupled, single-ended input and output ports with impedance that is nominally equal to 50 Ω over the 23 GHz to 31 GHz frequency range. No external matching components are required. While the RF output path is ac-coupled, there is a dc path to ground on the RFOUT side of the ac coupling capacitor.
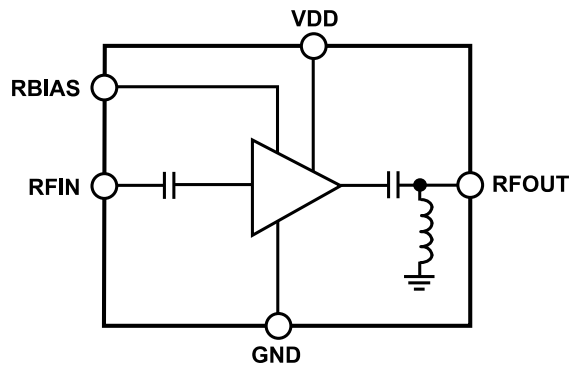
Figure 59. Simplified Block Diagram

APPLICATIONS INFORMATION

The basic connections for operating the ADL8142-2CHIP over the specified frequency range are shown in Figure 60. No external biasing inductor is required, allowing the 2 V supply to be connected to the VDD pin. It is recommended to use 0.1 µF and 100 pF power supply decoupling capacitors. The power supply decoupling capacitors shown in Figure 60 represent the configuration used to characterize and qualify the ADL8142-2CHIP.

To set I_{DQ}, connect a resistor (R2) between the RBIAS and VDD pins. A default value of 499 Ω is recommended, which results in a nominal I_{DQ} of 25 mA. The RBIAS pin also draws a current that varies with the value of RBIAS, and this current is typically a few mA. Do not leave the RBIAS pin open.

The RFIN and RFOUT pins are internally ac-coupled. If the RFOUT pin is connected to a dc bias level other than 0 V, ac-couple this pin because of the internal dc path to ground on RFOUT.

Figure 60. Basic Connections

RECOMMENDED BIAS SEQUENCING

During Power-Up

To power up the ADL8142-2CHIP, take the following bias sequencing steps:
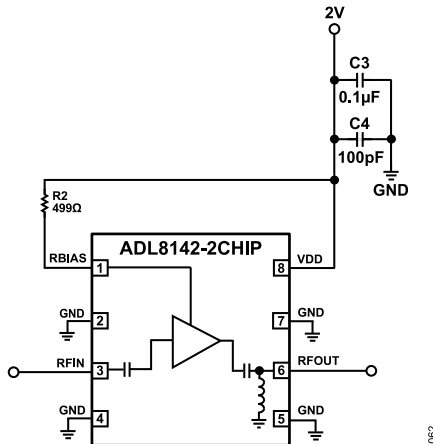
1. Connect the VDD power supply.
2. Set the VDD supply to 2 V.
3. Apply the RF input signal.

During Power-Down

To power down the ADL8142-2CHIP, take the following bias sequencing steps:

1. Turn off the RF input signal.
2. Set the VDD supply to 0 V.

Table 8. Recommended Bias Resistor Values for V_{DD} = 2 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
180	50	43.3	6.7
260	40	34.6	5.4
400	30	26.2	3.8
499	25	22.6	2.4
700	20	18	2.0
1000	15	14.2	0.8

ASSEMBLY DIAGRAM

Figure 61 shows the assembly diagram of the ADL8142-2CHIP.
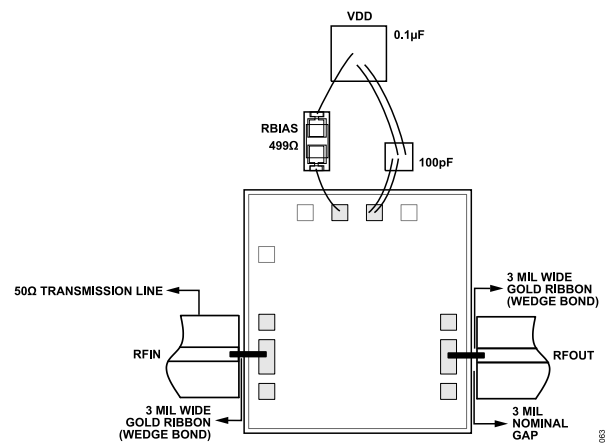
Figure 61. Assembly Diagram

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 62 shows a recommended power management circuit that uses the LT3083 low dropout (LDO) regulator that is available as a space-qualified die. With the IN and $V_{CONTROL}$ pins tied together, the minimum input voltage (V_{IN}) is 3.6 V when an output voltage (V_{OUT}) of 2 V and a current draw of up to 3 A are required. Assuming that the ADL8142-2CHIP is being used in a large array, a single LT3083 can provide power to the low noise amplifier in a 64-element array.

Table 9 provides recommended resistor values to set the other V_{DD} voltages. In each case, the minimum external supply is the minimum dropout voltage from the $V_{CONTROL}$ input to OUT.

APPLICATIONS INFORMATION
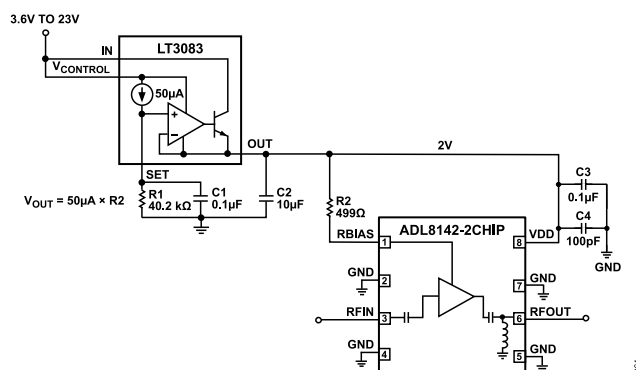
Figure 62. Recommended Power Management Circuit

Table 9. Recommended Resistor Values for Various LDO Output Voltages

V_{OUT} for the LT3083	R1 (kΩ)	Minimum Supply Voltage for the LT3083
1.5	30.1	3.1
2	40.2	3.6
2.5	49.9	4.1
3.3	66.5	4.9

APPLICATIONS INFORMATION

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICs

Figure 61 shows the recommend assembly diagram. Attach the die directly to the ground plane with conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section for additional information). Place the microstrip substrates as close to the die as possible to minimize ribbon bond length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

▶ Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. Once the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
▶ Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
▶ Follow ESD precautions to protect against ESD strikes.
▶ While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pick up.
▶ Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and must not be touched with vacuum collet, tweezers, or fingers.

Mounting

Before the epoxy die is attached, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Cure the epoxy per the schedule of the manufacturer.

Wire Bonding

RF wire bonds made with 0.076 mm × 0.0127 mm (3 mil × 0. 5 mil) gold ribbon is recommended for the RF ports. These bonds must be thermionically bonded with a force of 40 g to 60 g. Thermionically bonded dc wire bonds of 0.025 mm (1 mil) diameter are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply the minimum amount of ultrasonic energy (depending on the process and package being used) to achieve reliable bonds. Keep all bonds as short as possible, less than 0.203 mm (8 mil).

Alternatively, use short RF wire bonds that are 0.076 mm to 0.152 mm (3 mil to 6 mil) and made with three 0.025 mm (1 mil) diameter wires.

OUTLINE DIMENSIONS
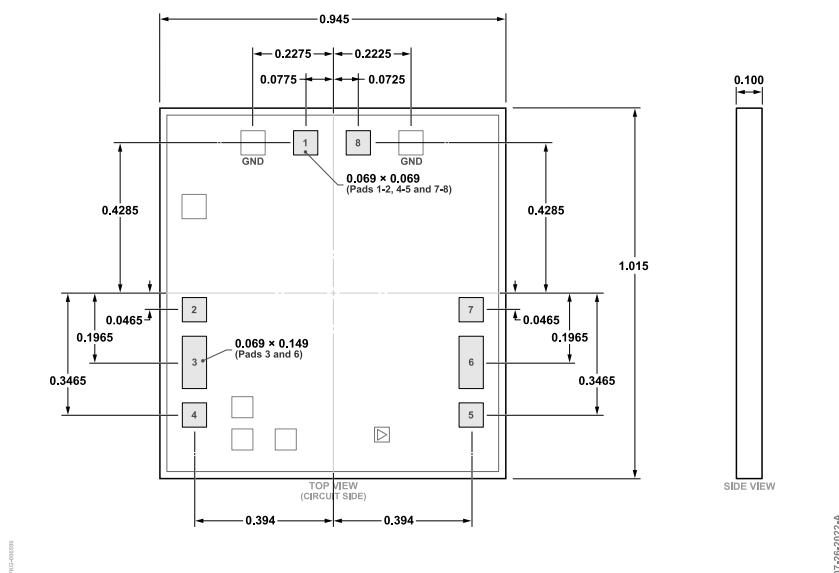
Figure 63. 8-Pad Bare Die [CHIP]
(C-8-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADL8142-2CHIP	−55°C to +85°C	8-Pad Bare Die [CHIP]	C-8-28
ADL8142-2C-SX	−55°C to +85°C	8-Pad Bare Die [CHIP]	C-8-28

[1] The ADL8142-2CHIP and ADL8142-2C-SX are RoHS compliant parts.

[2] The ADL8142-2C-SX is a sample order of two devices.