6ED2230S12C

1200 V Three Phase Gate Driver with Integrated Bootstrap Diode and OCP

Features

- Infineon Thin Film SOI technology
- Floating channel designed for bootstrap operation
- Fully operational to +1200 V
- Tolerant to negative transient voltage up to -100V (pulse widths up to 700ns)
- Gate drive supply range from 12 V to 20 V
- 25 V V_{CC} voltage supply (maximum)
- 3.3 V, 5 V, and 15 V input logic compatible
- Ultra-fast integrated bootstrap diodes
- Advanced input filter, inputs/outputs in phase
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Over current protection with ±5% ITRIP threshold
- Fault reporting, automatic Fault clear and Enable function on the same pin (RFE)
- Matched propagation delay for all channels
- Integrated 460 ns deadtime protection
- Shoot-through (cross-conduction) protection

Product Summary

V_{OFFSET}	≤ 1200 V
V_{OUT}	12 V – 20 V
I_{O+} & I_{O-} (typ.)	350 mA & 650 mA
t_{ON} & t_{OFF} (typ.)	700 ns & 650 ns
Dead time (typ.)	460 ns

Description

The 6ED2230S12C is a high voltage, high speed power MOSFET and IGBT with three independent high side and low side referenced output channels for three phase applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or TTL outputs, down to 3.3 V logic. A current trip function which terminates all six outputs can also be derived from this resistor. An open drain FAULT signal is provided to indicate that an over-current or under-voltage shutdown has occurred. Fault conditions are cleared automatically after a delay programmed externally via an RC network. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 1200 V. Propagation delays are matched to simplify the HVIC's use in high frequency applications.

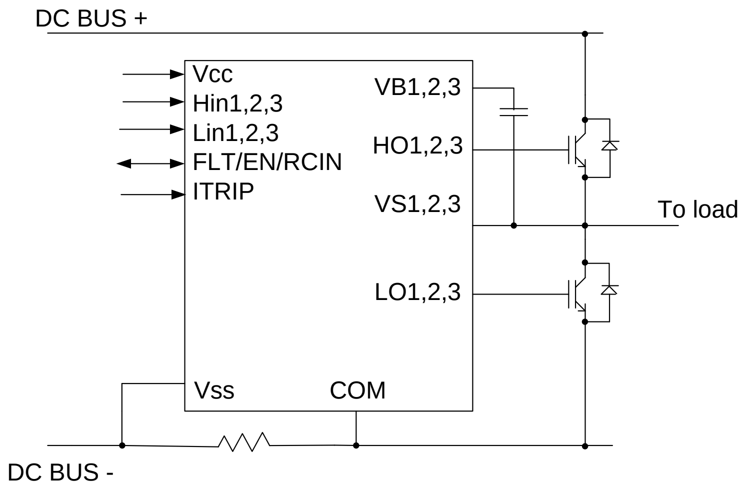
Typical Applications

- Industrial Drives
- Embedded inverters for Motor Control in Pumps, Fans, and other factory automation
- Commercial and Lite Commercial Air Conditioning
- Micro/Mini inverter drives
- General Purpose Inverters

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	MOQ*	
6ED2230S12C	Horizontal Frame Shipper	Wafer on Film	14,105	6ED2230S12CX7SA1

*Minimum Order Quantity equivalent to 5 wafers

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to Application Notes & Design Tips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_{CC}	Low side supply voltage	-0.3	25	
V_{IN}	Logic input voltage (LIN, HIN, RFE, ITRIP)	V_{SS} - 5	V_{CC} + 0.3	
$V_{B1,2,3}$	High-side floating well supply voltage	-0.3	1225	
$V_{S1,2,3}$	High-side floating well supply return voltage	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	V
$V_{HO1,2,3}$	Floating gate drive output voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
$V_{LO1,2,3}$	Low-side output voltage	- 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground	V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable V_S offset supply transient relative to COM	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ºC	—	1.3	W
Rth_{JA}	Thermal resistance, junction to ambient	—	75	ºC/W
T_J	Junction temperature	—	150	ºC
T_S	Storage temperature	-55	150	

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} - COM) = (V_B - V_S) = 15 V.

Symbol	Definition	Min	Max	Units
V_{CC}	Low-side supply voltage	13	20	
V_{IN}	Logic input voltage (LIN, HIN, ITRIP)	V_{SS}	V_{SS} + 5	
V_{RFE}	RFE logic input voltage	V_{SS}	V_{CC}	
$V_{B1,2,3}$	High-side floating well supply voltage	$V_{S1,2,3}$ + 12	$V_{S1,2,3}$ + 20	
$V_{S1,2,3}$	High-side floating well supply offset voltage	COM – 8 (Note 1)	900	V
V_{St}	Transient High-side floating well supply offset voltage	- 100 (Note 2)	1000	
$V_{HO1,2,3}$	Floating gate drive output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
$V_{LO1,2,3}$	Low-side output voltage	0	V_{CC}	
V_{SS}	Logic ground	- 5	5	
T_A	Ambient temperature	-40	125	ºC

Note 1 - Logic operation for VS of –8 V to 1200 V. Logic state held for V_S of –8 V to –V_{BS}.
Note 2 – In case of VCC > VB there is an additional power dissipation in the internal bootstrap diode between pins VCC and VBx. Insensitivity to bridge output to negative transient voltage up to -100 V is not subject to production test – verified by design and characterization.

Static Electrical Characteristics

(V_{CC} - COM) = (V_B - V_S) = 15 V. T_A = 25 °C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply under voltage positive threshold	9.2	10.4	11.6	V	
V_{BSUV-}	V_{BS} supply under voltage negative threshold	8.3	9.4	10.5		
V_{BSUVHY}	V_{BS} supply under voltage hysteresis	—	1	—		
V_{CCUV+}	V_{CC} supply under voltage positive threshold	10.2	11.4	12.6		
V_{CCUV-}	V_{CC} supply under voltage negative threshold	9.3	10.4	11.5		
V_{CCUVHY}	V_{CC} supply under voltage hysteresis	—	1	—		
V_{OH}	High level output voltage drop, V_{BIAS}-V_O	—	0.15	—		I_O = 20 mA
V_{OL}	Low level output voltage drop, V_O	—	0.35	—		
V_{IH}	Logic “1” input voltage	2.3	—	—		
V_{IL}	Logic “0” input voltage	—	—	0.7		
V_{RFE+}	RFE positive going threshold	1.7	1.9	2.3		
V_{RFE-}	RFE negative going threshold	0.7	0.9	1.1		
V_{ITRIP+}	ITRIP positive going threshold	0.475	0.500	0.525		
V_{ITRIP-}	ITRIP negative going threshold	0.425	0.450	0.475		
$V_{ITRIP\ HYS}$	ITRIP hysteresis	—	0.050	—		
I_{LK}	High-side floating well offset supply leakage	—	—	50	µA	V_B = V_S = 1200 V
I_{QBS}	Quiescent V_{BS} supply current	—	175	250		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	—	1000	1500		
$I_{O+\ mean}$	Mean Output current for load capacity charging from 3V (20%) to 6V (40%)	200	300	—		C = 22 nF
$I_{O-\ mean}$	Mean Output current for load capacity discharging from 10.5V (70%) to 7.5V (50%)	400	600	—		
I_{O+}	Output high short circuit pulsed current	—	350	—	mA	V_O = 0 V PW ≤ 1 µs
I_{O-}	Output low short circuit pulsed current	—	650	—		V_O = 15 V PW ≤ 1 µs
I_{RFE+}	Logic “1” Input bias current (RFE)	—	0	1	µA	V_{RFE} = 3.3 V
I_{RFE-}	Logic “0” Input bias current (RFE)	1	0	—		V_{RFE} = 0 V
I_{IN+}	Logic “1” Input bias current (LIN, HIN)	—	1000	1250		V_{IN} = 5 V
I_{IN-}	Logic “0” Input bias current (LIN, HIN)	—	—	1		V_{IN} = 0 V
I_{ITRIP+}	Logic “1” Input bias current (ITRIP)	—	15	25		V_{IN} = 5 V
I_{ITRIP-}	Logic “0” Input bias current (ITRIP)	—	—	1		V_{IN} = 0 V
R_{BS}	Bootstrap diode on resistance	—	120	150	Ω	

$V_{F\ BSD}$	Bootstrap diode forward voltage drop	—	0.9	—		I_O = 0.3 mA
$R_{ON,\ RFE}$	RFE mos resistance	—	40	60	Ω	

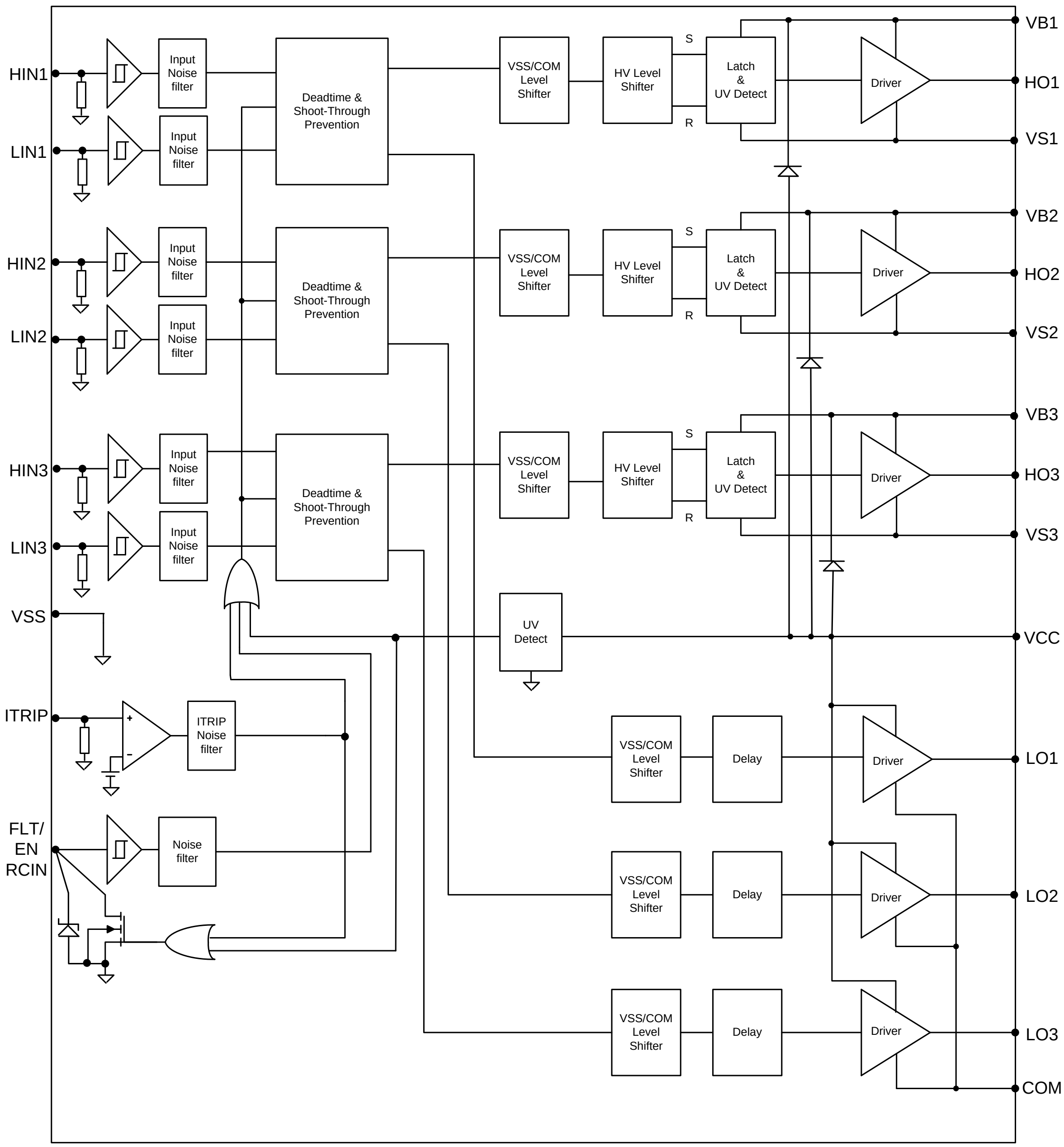
Please refer to Application Section for integrated bootstrap diode description.

Dynamic Electrical Characteristics

$V_{CC} = V_B$ = 15 V, V_S = COM, T_A = 25 ºC, and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	500	700	900	ns	V_S =0 V or 1200 V
t_{OFF}	Turn-off propagation delay	450	650	850		
t_R	Turn-on rise time	—	35	—		V_S = 0 V
t_F	Turn-off fall time	—	20	—		
DT	Dead time, LO turn-off to HO turn-on & HO turn-off to LO turn-on	300	460	700		
MT	Delay matching time (t_{ON}, t_{OFF})	—	—	130		
t_{EN}	Enable low to output shutdown propagation delay	—	600	—		
$T_{FIL,IN}$	Input filter time (LIN, HIN, EN)	200	350	500		
T_{FLTCLR}	FAULT clear time (R = 2 MΩ, C = 1 nF)	—	1.9	—	ms	VDD = 3.3V
T_{ITRIP}	ITRIP to output shutdown propagation delay	—	750	1100	ns	V_{ITRIP} = 1 V
T_{BL}	ITRIP blanking time	—	500	—		
T_{FLT}	ITRIP to FAULT propagation delay	450	650	900		

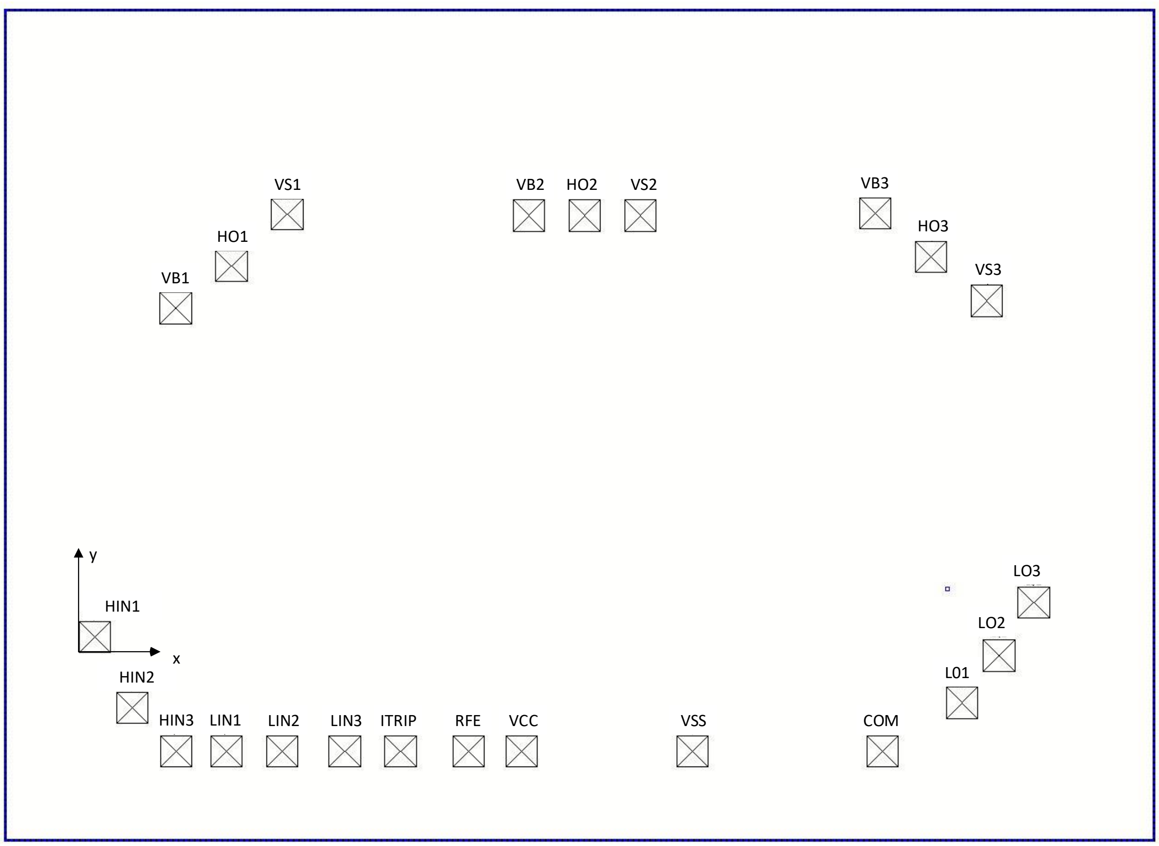
Functional Block Diagram



Pad Definitions

Symbol	Description
HIN1,2,3	Logic input for high side gate driver output (HO), in phase
LIN1,2,3	Logic input for low side gate driver output (LO), in phase
$V_{B1,2,3}$	High side floating supply
HO1,2,3	High side gate drive output
$V_{S1,2,3}$	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return
V_{SS}	Logic ground
ITRIP	Analog input for over-current shutdown. When active, ITRIP shuts down outputs and activates RFE low. When ITRIP becomes inactive, RFE stays active low for an externally set time tFLTCLR, then automatically becomes inactive (open-drain high impedance).
RFE	Integrated fault reporting function like over-current (ITRIP), or low-side undervoltage lockout and the fault clear timer. This pin has negative logic and an open-drain output. The use of over-current protection requires the use of external components.

Pad Assignments



	PAD #	x [µm]	y [µm]
HIN1	1	50	50
VB1	2	309.4	1108.2
HO1	3	487.4	1243.5
VS1	4	665.4	1411
VB2	5	1437.3	1406.4
HO2	6	1615.3	1406.4
VS2	7	1793.3	1406.4
VB3	8	2543.8	1414
HO3	9	2721.8	1273
VS3	10	2899.8	1132
LO3	11	3050.9	160.4
LO2	12	2939.7	-9.6
LO1	13	2820.6	-161.8
COM	14	2567.4	-317.3
Vss	15	1960.3	-317.3
Vcc	16	1414.7	-317.3
RFE	17	1244.7	-317.3
ITRIP	18	1027.5	-317.3
LIN3	19	849.7	-317.3
LIN2	20	648.9	-317.3
LIN1	21	471.1	-317.3
HIN3	22	311.2	-317.3
HIN2	23	171.2	-177.3

	[µm]	[µm]
pad size	100	100
die size	3742	2742

Parameter		**Unit**
Raster size of die	3742 x 2742	µm x µm
Area total / active	10.261	mm²
Thickness	280	µm
Wafer size	200	mm
Chips per wafer	2821	pcs
Passivation front side	Polyimide	
Backside (Note 2)	Grinded silicon	
Pad metal composition/thickness	Ti/TiN/AlCu 1.1	µm
Reject ink dot diameter	Min. 0.6 Max 1.2	mm
Sawing street	62	µm

Note1: Filler material inside the mould compound with sharp edges may harm the passivation.
Note2: Chip must be bonded onto an electrically insulated area

Application Information and Additional Details

Information regarding the following topics are included as subsections within this section of the datasheet.

- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Deadtime
- Matched Propagation Delays
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Shoot-Through Protection
- Enable Input
- Fault Reporting and Programmable Fault Clear Timer
- Over-Current Protection
- Truth Table: Undervoltage lockout, ITRIP, and ENABLE
- Advanced Input Filter
- Short-Pulse / Noise Rejection
- Integrated Bootstrap Diodes
- Negative V_S Transient SOA
- PCB Layout Tips
- Additional Documentation

IGBT/MOSFET Gate Drive

The 6ED2230S12C HVICs are designed to drive MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

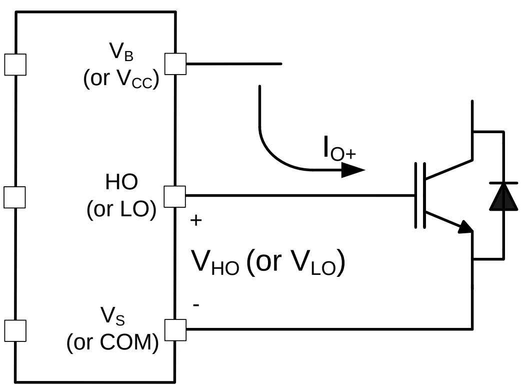


Figure 1: HVIC sourcing current

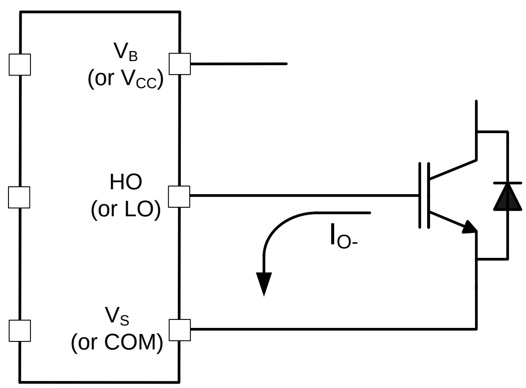


Figure 2: HVIC sinking current

Switching and Timing Relationships

The relationships between the input and output signals of the 6ED2230S12C are illustrated below in Figures 3. From these figures, we can see the definitions of several timing parameters (i.e., PW_{IN}, PW_{OUT}, t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

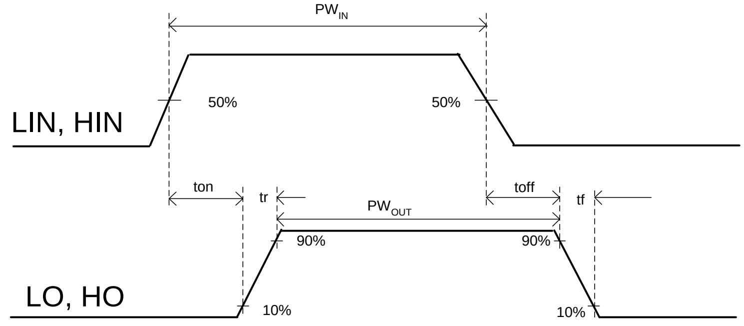


Figure 3: Switching time waveforms

The following two figures illustrate the timing relationships of some of the functionality of the 6ED2230S12C; this functionality is described in further detail later in this document.

During interval A of Figure 4, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has prevented this condition. HVIC is keeping on output channel that is already on ignoring the 2nd input signal.

Interval B of Figures 4 and 5 shows that the signal on the ITRIP input pin has gone from a low to a high state; as a result, all of the gate drive outputs have been disabled (i.e., see that HO has returned to the low state; LO is also held low), and a fault condition is reported on the RFE pin, which goes 0V. Once the ITRIP input has returned to the low state, the output will remain disabled and the fault condition reported until the voltage on the RFE pin charges up to VRFE+ threshold; the charging characteristics are dictated by the RC network attached to the RFE pin. After fault clear time HVIC is waiting for a new input signal on LIN/HIN before activate the output stage (LO/HO).

During interval C of Figure 4 and 6, we can see that the RFE pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); these results in the outputs (HO and LO) being held in the low state until the RFE pin is pulled high. After an enable event HVIC will wait for a new input signal on LIN/HIN before activate the output stage (LO/HO).

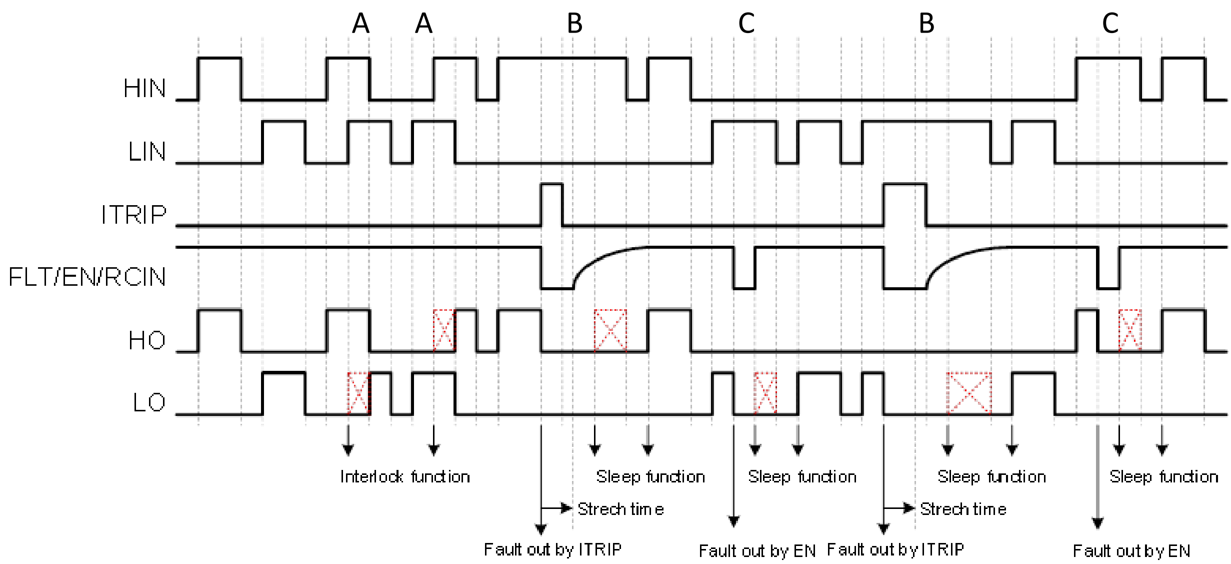


Figure 4: Input/output timing diagram

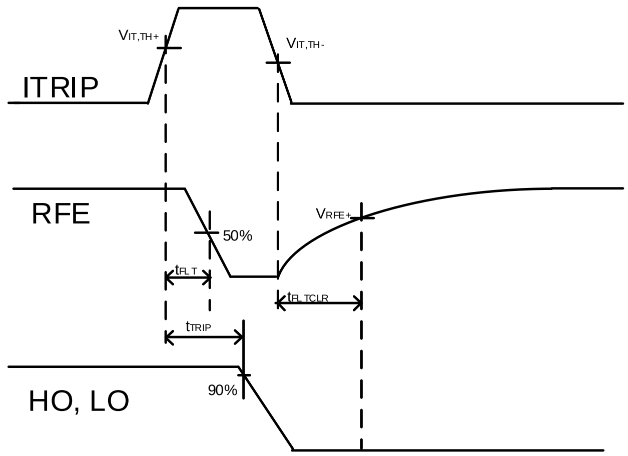


Figure 5: Detailed view of B interval

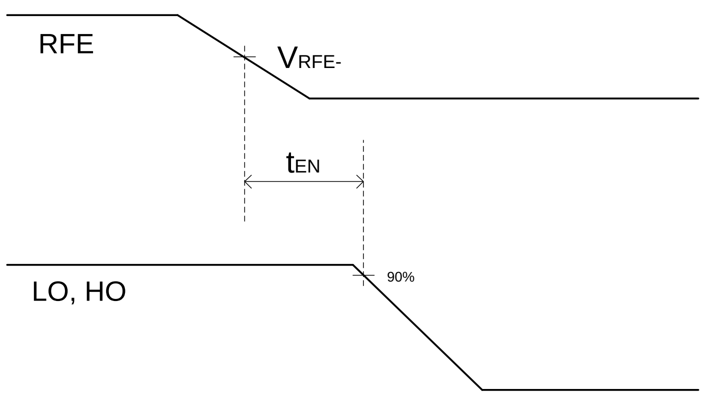


Figure 6: Detailed view of C interval

Deadtime

This HVIC features integrated deadtime protection circuitry. The deadtime for these ICs is fixed; other ICs within Infineon's HVIC portfolio feature programmable deadtime for greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver.

Matched Propagation Delays

The 6ED2230S12C HVIC is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the 6ED2230S12C is matched to the propagation turn-on delay (t_{OFF}).

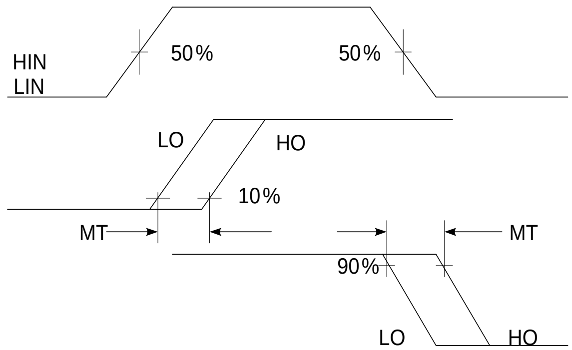


Figure 7: Delay Matching Waveform Definition

Input Logic Compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The 6ED2230S12C has been designed to be compatible with 3.3 V and 5 V logic-level signals. Figure 8 illustrates an input signal to the 6ED2230S12C, its input threshold values, and the logic state of the IC as a result of the input signal.

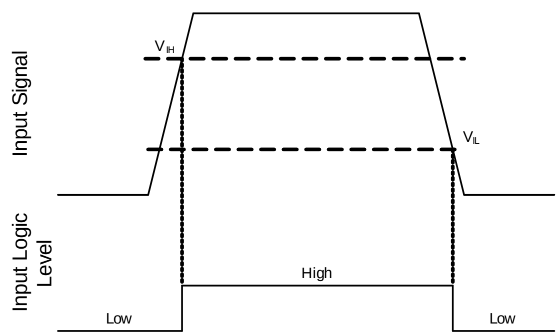


Figure 8: HIN & LIN input thresholds

Undervoltage Lockout Protection

This HVIC provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 9 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC will not turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the IC will not turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

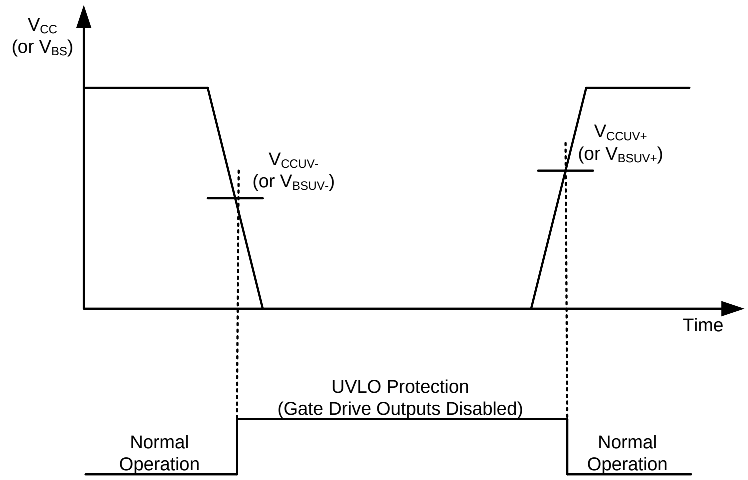


Figure 9: UVLO protection

Shoot-Through Protection

The 6ED2230S12C is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 10 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time.

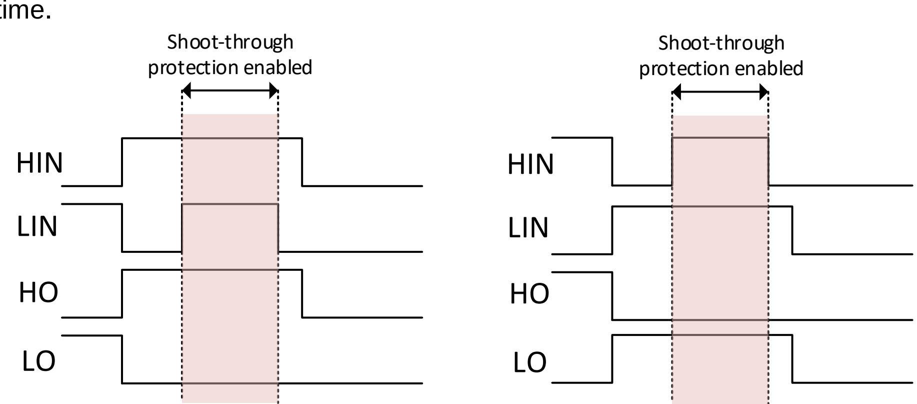


Figure 10: Illustration of shoot-through protection circuitry

Enable Input

The 6ED2230S12C provides an enable functionality that allows it to shutdown or enable the HVIC. When the RFE pin is in the high state the HVIC is able to operate normally (assuming no other under voltage fault conditions on Vcc). When the RFE pin is in a low state, the gate drive outputs are pulled low until the enable condition is restored. The enable circuitry of the 6ED2230S12C features an input filter; the minimum input duration is specified by $t_{FIL,EN}$. Please refer to the RFE pin parameters V_{RFE+}, V_{RFE-}, and I_{RFE} for the details of its use.

Fault Reporting and Programmable Fault Clear Timer

The 6ED2230S12C provides an integrated fault reporting output and an adjustable fault clear timer. There are two situations that would cause the HVIC to report a fault via the RFE pin. The first is an undervoltage condition of V_{CC} and the second is if the ITRIP pin recognizes a fault. Once the fault condition occurs, the RFE pin is internally pulled to Vss and the fault clear timer is activated. The RFE output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the RFE pin will return to its external pull-up voltage.

The length of the fault clear time period (t_{FLTCLR}) is determined by a fix time constant added to exponential charging characteristics of the capacitor where the time constant is set by R_{RFE} and C_{RFE}. Figure 11 shows that R_{RFE} is connected between the external supply (V_{DD}) and the RFE pin, while C_{RFE} is placed between the RFE and Vss pins.

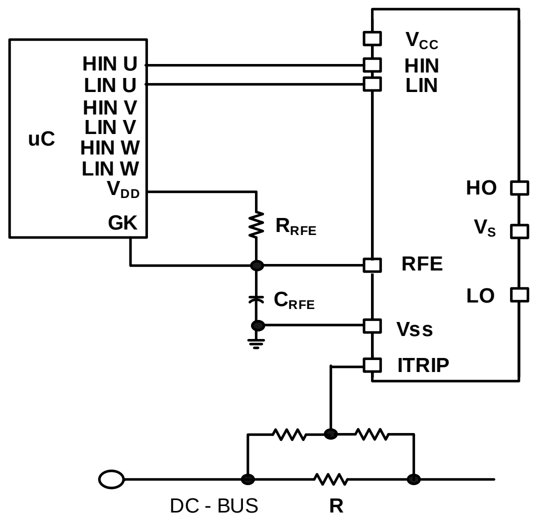


Figure 11 Programming the fault clear timer

The design guidelines for this network are shown in Table 3.

C_{RFE}	≤1 nF
	Ceramic
R_{RFE}	0.5 MΩ to 2 MΩ
	>> $R_{ON,RCIN}$

Table 3: Design guidelines

The length of the fault clear time period can be determined by using the formula below.

$$v_C(t) = V_f*(1-e^{-t/RC})$$

$$t_{FLTCLR} = -(R_{RFE}*C_{RFE})*\ln(1-V_{RFE+}/V_{DD}) + 160\mu s$$

The voltage on the RFE pin should not exceed the VDD of the uC power supply.

Over-Current Protection

The 6ED2230S12C HVICs are equipped with an ITRIP input pin. This functionality can be used to detect over-current events in the DC- bus. Once the HVIC detects an over-current event through the ITRIP pin, the outputs are shutdown, and RFE is pulled to Vss.

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as shown in Figure 12, and the ITRIP threshold (V_{ITRIP+}). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0, R_1, and R_2 such that the voltage at node V_X reaches the over-current threshold (V_{ITRIP+}) at that current level.

$$V_{ITRIP+} = R_0 * I_{DC-}(R_1/(R_1+R_2))$$

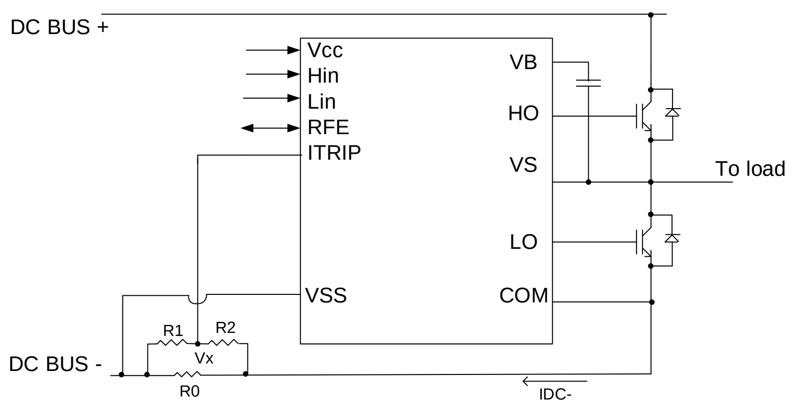


Figure 12 Programming the over-current protection

For example, a typical value for resistor R_0 could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

Truth Table: Undervoltage lockout, ITRIP, and ENABLE

Table 4 provides the truth table for the 6ED2230S12C. The first line shows that the UVLO for V_{CC} has been tripped; the RFE output has gone low and the gate drive outputs have been disabled. V_{CCUV} is not latched in this case and when V_{CC} is greater than V_{CCUV}, the FAULT output returns the driver is functional.

The second case shows that the UVLO for V_{BS} has been tripped and that the high-side gate drive outputs have been disabled. After V_{BS} exceeds the V_{BSUV} threshold, HO will stay low until the HVIC input receives a new rising transition of HIN. The third case shows the normal operation of the HVIC. The fourth case illustrates that the ITRIP trip threshold has been reached and that the gate drive outputs have been disabled. This condition is stored in the external RC network waiting for fault clear time. The last case shows when the HVIC has received an enable command through the RFE input to shutdown; as a result, the gate drive outputs have been disabled.

	VCC	VBS	ITRIP	RFE	LO	HO
UVLO V_{CC}	$<V_{CCUV}$	—	—	0	0	0
UVLO V_{BS}	15 V	$<V_{BSUV}$	0 V	HIGH	LIN	0
Normal operation	15 V	15 V	0 V	HIGH	LIN	HIN
ITRIP fault	15 V	15 V	$>V_{ITRIP+}$	0	0	0
Enable command	15 V	15 V	0 V	0	0	0

Table 4: 6ED2230S12C UVLO, ITRIP, FLT/EN/RCIN

Advanced Input Filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN ans LIN inputs. The working principle of the new filter is shown in Figures 13 and 14.

Figure 13 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.

Figure 14 shows the advanced input filter of the 6ED2230S12C and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

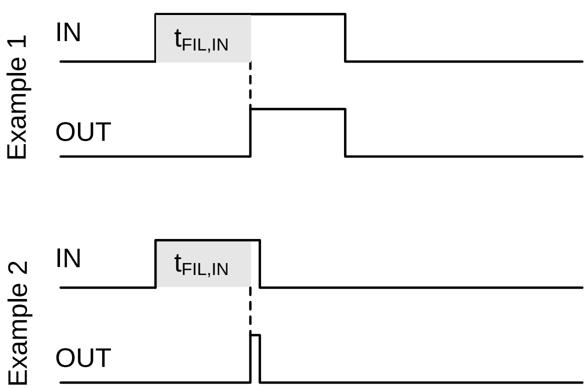


Figure 13: Typical input filter

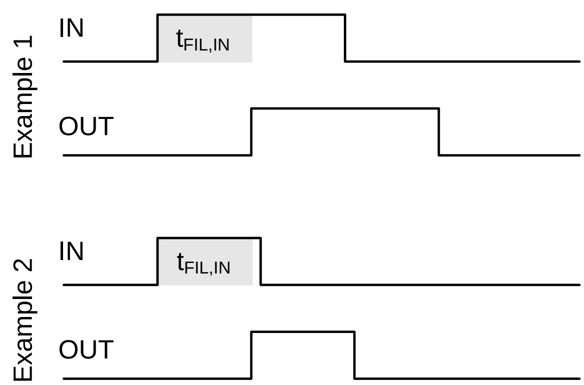


Figure 14: Advanced input filter

Short-Pulse / Noise Rejection

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than $t_{FIL,IN}$, the output will not change states. Example 1 of Figure 15 shows the input and output in the low state with positive noise spikes of durations less than $t_{FIL,IN}$; the output does not change states. Example 2 of Figure 15 shows the input and output in the high state with negative noise spikes of durations less than $t_{FIL,IN}$; the output does not change states.

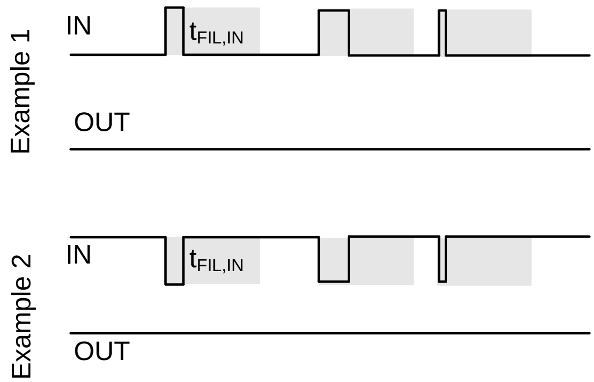


Figure 15: Noise rejecting input filters

Integrated Bootstrap Diodes

The 6ED2230S12C embeds three integrated ultra-fast bootstrap diodes that allow an alternative drive of the bootstrap supplies for a wide range of applications. The resistance of the diode (R_{BS}) helps to avoid high inrush currents when charging the bootstrap capacitance.

The bootstrap diode is connected between the floating supply V_B and V_{CC} (see Fig. 16).

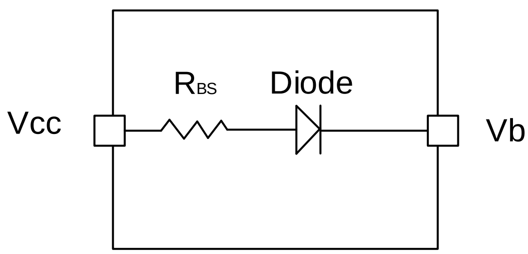


Figure 16: Simplified Bootstrap diode connection

The bootstrap diode is suitable for all PWM modulation schemes, including trapezoidal control, and can be used either in parallel with the external bootstrap network (diode+ resistor) or as a replacement of it.

Tolerant to Negative V_S Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical three phase inverter circuit is shown in Figure 17; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 18 and 19) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

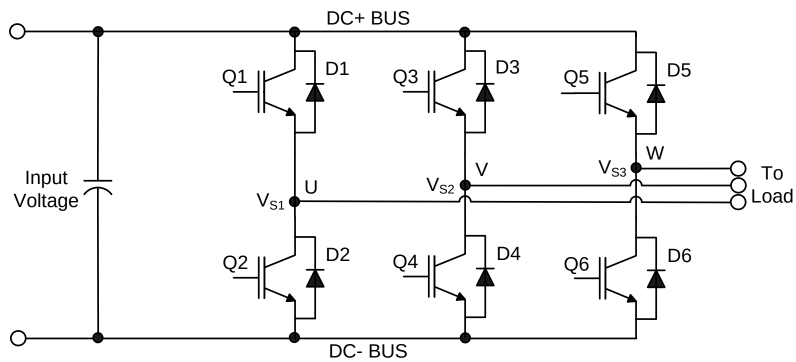


Figure 17: Three phase inverter

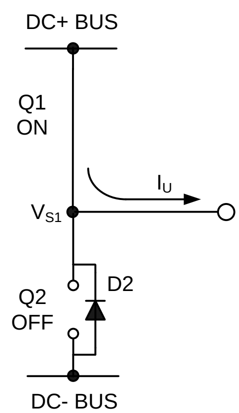


Figure 18: Q1 conducting

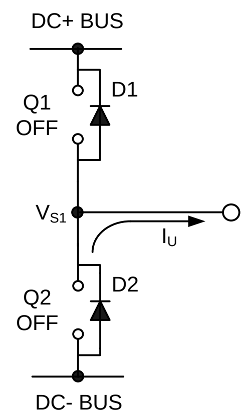


Figure 19: D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 20 and 21), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

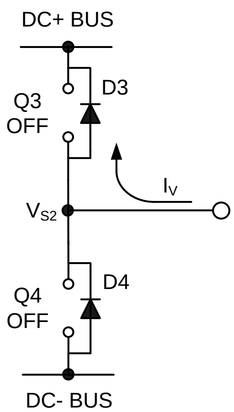


Figure 20: D3 conducting

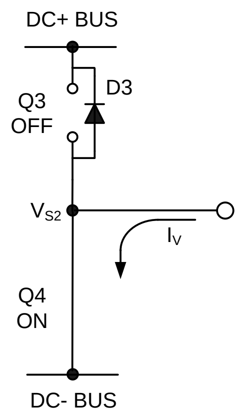


Figure 21: Q4 conducting

However, in a real inverter circuit the V_S voltage swing does not stop at the level of the negative DC bus but instead swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient".

The circuit shown in Figure 22 depicts one leg of the three phase inverter; Figures 23 and 24 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

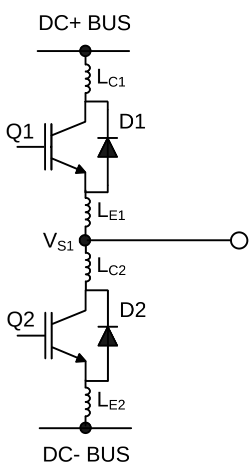


Figure 22: Parasitic Elements

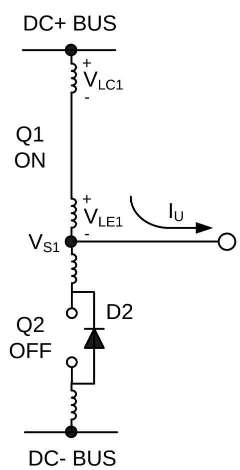


Figure 23: V_S positive

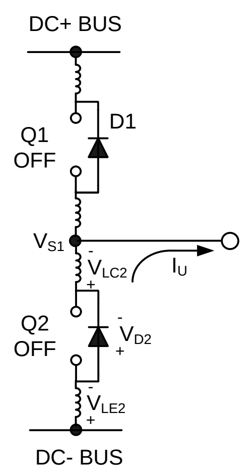


Figure 24: V_S negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the 6ED2230S12C's robustness can be seen in Figure 25, where the 6ED2230S12C Safe Operating Area is shown at V_{BS}=15V based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

TBD

Figure 25: **Negative V_S transient SOA for 6ED2230S12C @ VBS=15V**

Even though the 6ED2230S12C has been shown to be able to handle these large negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

PCB Layout Tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.
Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.
Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 26). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

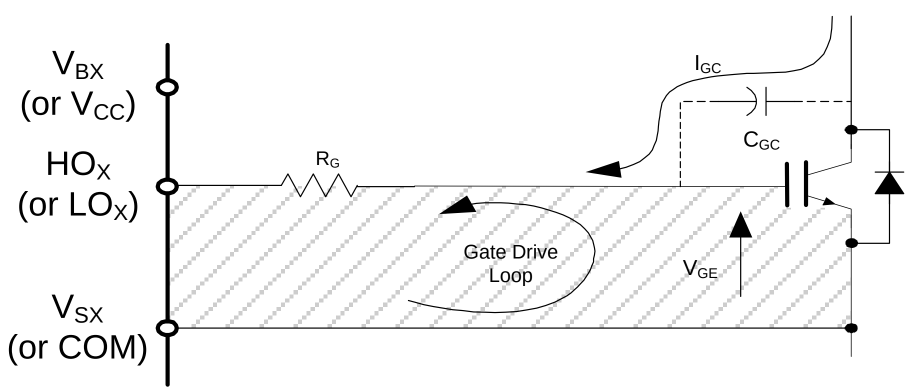


Figure 26: Antenna Loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and COM pins. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 27), and in some cases using a clamping diode between COM and V_S (see Figure 28). See DT04-4 at www.infineon.com for more detailed information.

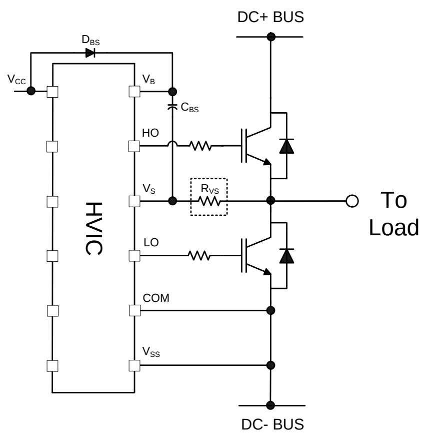


Figure 27: V_S resistor

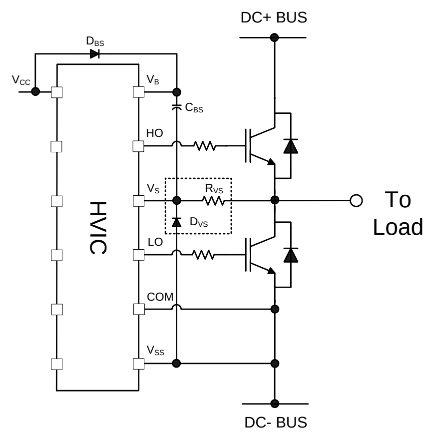


Figure 28: V_S clamping diode

Additional Documentation

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

Published by
Infineon Technologies AG
81726 München, Germany