High and Low Side Driver in Die form

Features

- Floating channel designed for bootstrap operation
- Fully operational to +1200 V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 12 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V logic compatible
- Separate logic supply range from 3.3 V to 20 V
- Logic and power ground ±5 V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET} (max)	1200 V
$I_{O+/-}$	1.7 A / 2 A
V_{OUT}	12 V – 20 V
$t_{on/off}$ (typical)	280 ns / 225 ns
Delay Matching	30 ns

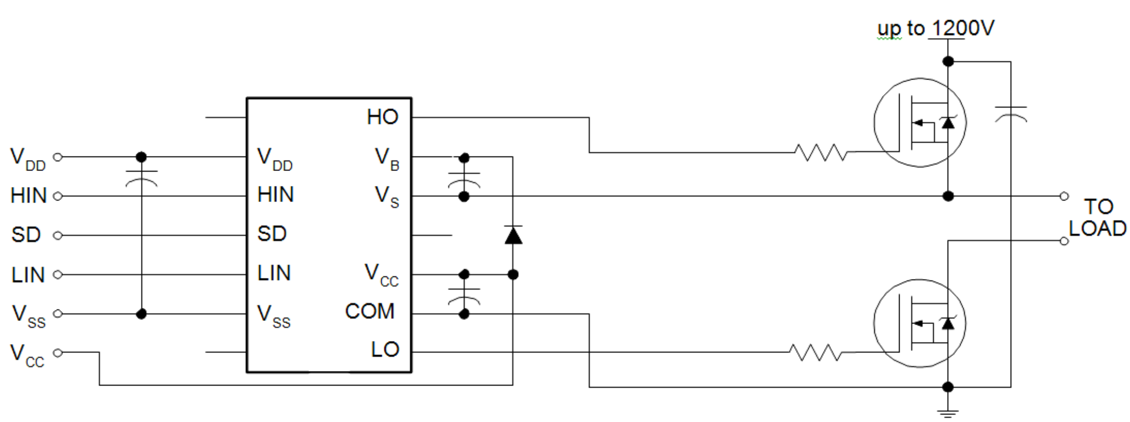
Description

The IR2213 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 1200 V.

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	MOQ*	
IR2213C_8	Bag of Non Dry	Wafer Unsawn	16,425 bare dies	IR2213C8X6SA1

*Minimum Order Quantity (MOQ) equivalent to 5 wafers

Typical Connection Diagram



Refer to Lead Assignments for correct pin configuration. This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Voltage	-0.3	1225	V
V_S	High Side Floating Supply Offset Voltage	V_B - 25	V_B + 0.3	
V_{HO}	High Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low Side Fixed Supply Voltage	-0.3	25	
V_{LO}	Low Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{DD}	Logic Supply Voltage	-0.3	V_{SS} + 25	
V_{SS}	Logic Supply Offset Voltage	V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS} - 0.3	V_{DD} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
T_J	Junction Temperature	—	125	°C
T_S	Storage Temperature	-55	150	

Recommended Operating Conditions

The Input / Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High Side Floating Supply Absolute Voltage	V_S + 12	V_S + 20	V
V_S	High Side Floating Supply Offset Voltage	†	1200	
V_{HO}	High Side Floating Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	12	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Voltage	V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic Supply Offset Voltage	-5 ††	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	

† Logic operational for V_S of -5 to +1200V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

†† When V_{DD}<5V, the minimum V_{SS} offset is limited to $-V_{DD}$

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V, C_L = 1000 pF, T_A = 25 °C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

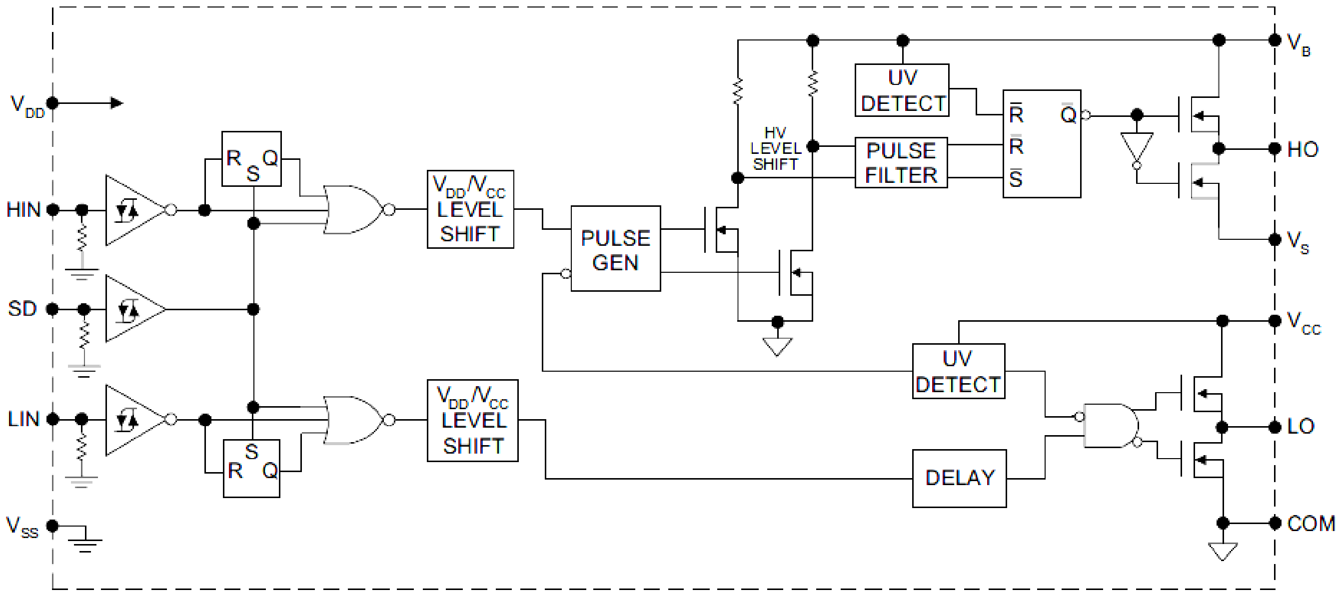
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	—	280	—	ns	V_S = 0V
t_{off}	Turn-Off Propagation Delay	—	225	—		V_S = 1200V
t_{sd}	Shutdown Propagation Delay	—	230	—		V_S = 1200V
t_r	Turn-On Rise Time	—	25	—		
t_f	Turn-Off Fall Time	—	17	—		
MT	Delay Matching, HS & LS Turn-On/Off	—	—	30		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V, T_A = 25 °C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	9.5	—	—	V	
V_{IL}	Logic "0" Input Voltage	—	—	6.0		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset Supply Leakage Current	—	—	50	µA	V_B = V_S = 1200V
I_{QBS}	Quiescent V_{BS} Supply Current	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} Supply Current	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} Supply Current	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic "1" Input Bias Current	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic "0" Input Bias Current	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.7	10.2	11.7	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.9	9.3	10.7		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	8.7	10.2	11.7		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.9	9.3	10.7		
I_{O+}	Output High Short Circuit Pulsed Current	1.7	2.0	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

Functional Block Diagram



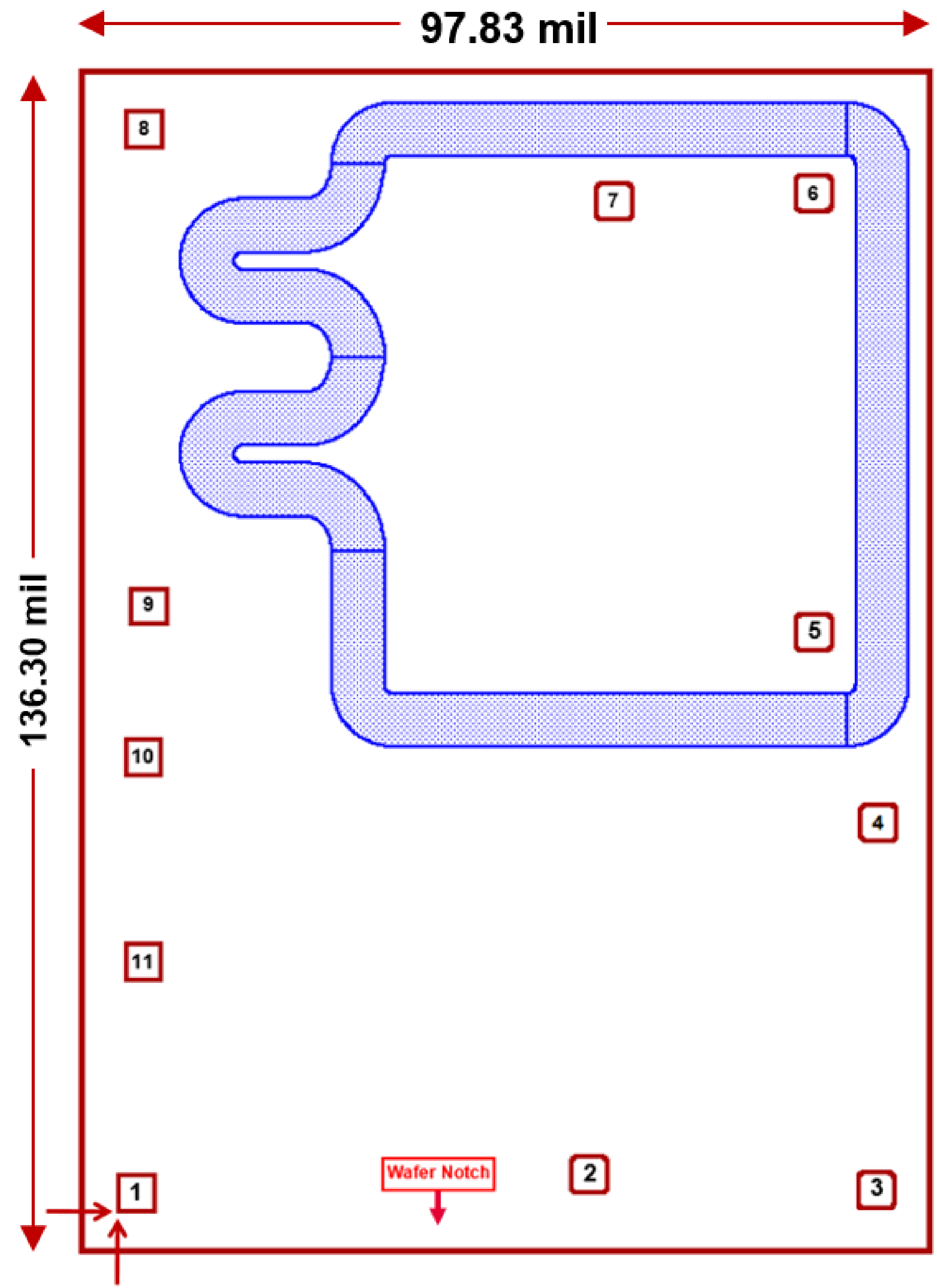
Pad Definitions

Symbol	Description
V_{DD}	Logic Supply
HIN	Logic Input for High Side Gate Driver Output (HO), In Phase
SD	Logic Input for Shutdown
LIN	Logic Input for Low Side Gate Driver Output (LO), In Phase
V_{SS}	Logic Ground
V_B	High Side Floating Supply
HO	High Side Gate Drive Output
V_S	High Side Floating Supply Return
V_{CC}	Low Side Supply
LO	Low Side Gate Drive Output
COM	Low Side Return

Device Information

Process & Design Rule		HVDCMOS 1200 V (HV1201)
Die Size		97.83 mil x 136.30 mil
Nominal Front Metal Composition, Thickness		Al-Si (Si: 1.0 % ± 0.1 %), 1 µm
Wafer Size		200 mm
Wafer Thickness		750±20 µm
Passivation Thickness		1.6 µm
Passivation Material		PSG + SiON
SiON		0.6 µm
Minimum Street Width:	Vertical	100 µm
	Horizontal	170 µm
Reject Ink Dot Size		0.38 mm
Pad Size		100 µm x 100 µm
Thickness		1 µm
Backside Composition		Silicon
Method of Saw		Full Cut
Method of Die Bond		-
Gross die per wafer		3285
Wafer fab		Vanguard (VIS), Taiwan
Remarks:		Store in original container, in dessicated nitrogen, with no contamination.

Die Outline:
(in mils)



PAD#	FUNCTION	DATUM X	DATUM Y	PAD SIZE
1	VSS	0.0000	0.0000	0.0040x0.0040
2	LOUT	0.0050	0.0020	0.0040x0.0040
3	COM	0.0817	0.0003	0.0040x0.0040
4	VCC	0.0819	0.0408	0.0040x0.0040
5	VS	0.0748	0.0619	0.0040x0.0040
6	VB	0.0748	0.1104	0.0040x0.0040
7	HOUT	0.0528	0.0937	0.0040x0.0040
8	VDD	0.0009	0.1174	0.0040x0.0039
9	HIN	0.0015	0.0648	0.0039x0.0039
10	DS	0.0008	0.0481	0.0039x0.0039
11	LIN	0.0008	0.0256	0.0039x0.0039
Tolerance		+/−0.0002	+/−0.0002	+/−0.0002

Application Information and Additional Information

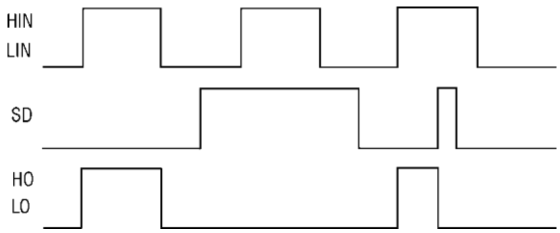


Figure 1. Input / Output Timing Diagram

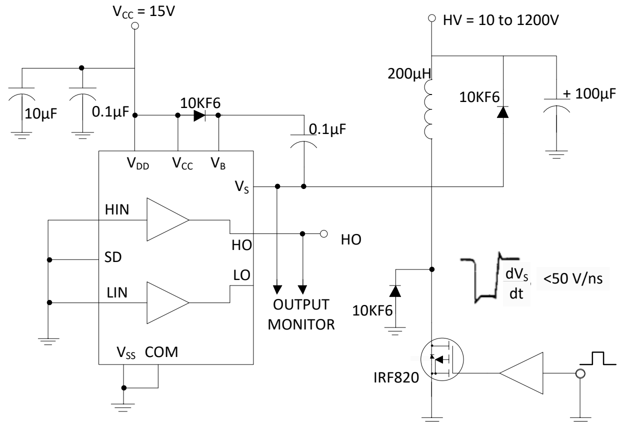


Figure 2. Floating Supply Voltage Transient Test Circuit

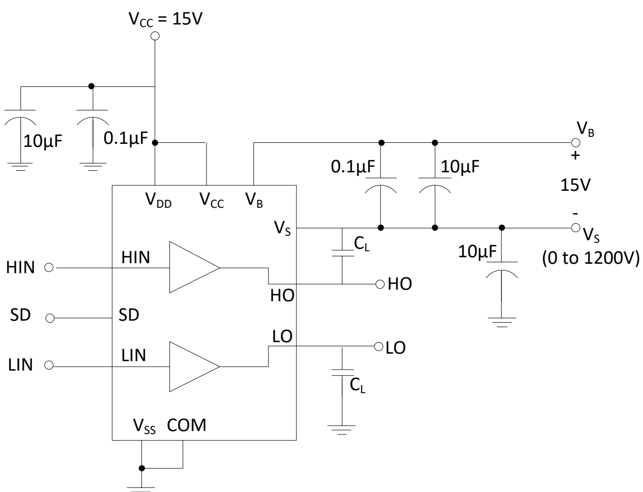


Figure 3. Switching Time Test Circuit

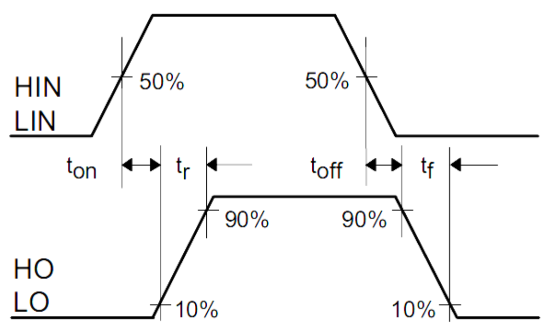


Figure 4. Switching Time Waveform Definition

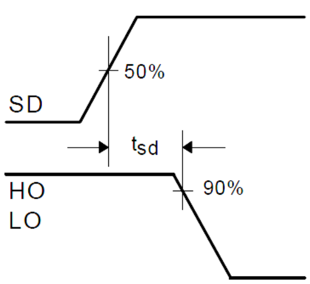


Figure 5. Shutdown Waveform Definitions

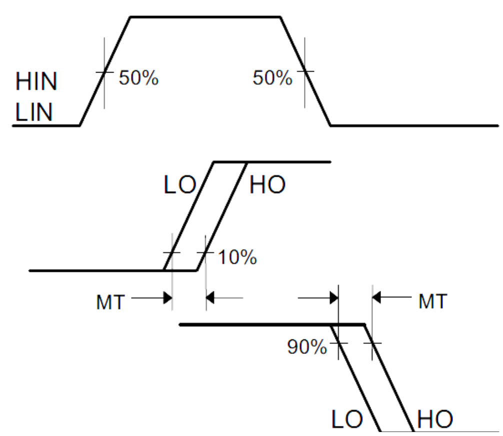


Figure 6. Delay Matching Waveform Definitions

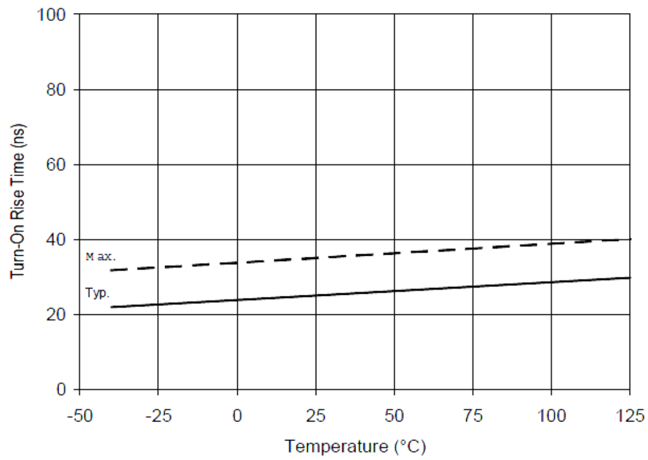


Figure 7A. Turn-On Rise Time vs. Temperature

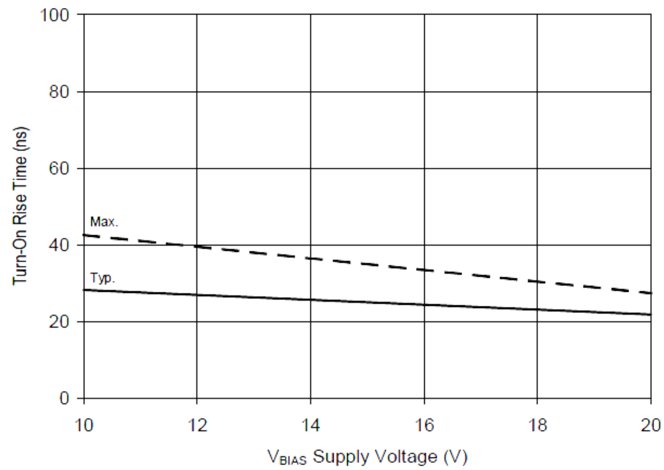


Figure 7B. Turn-On Rise Time vs. Voltage

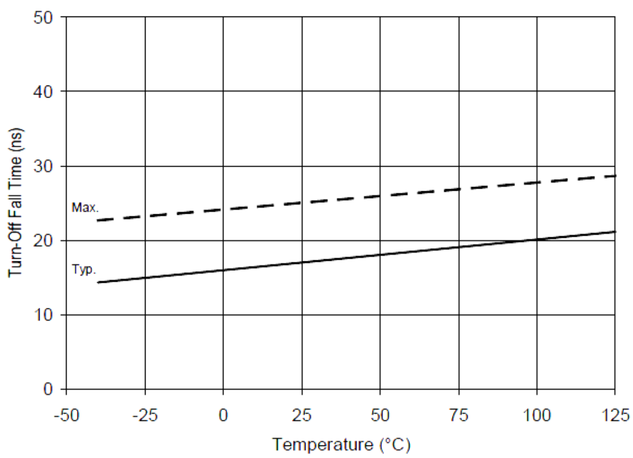


Figure 8A. Turn-Off Fall Time vs. Temperature

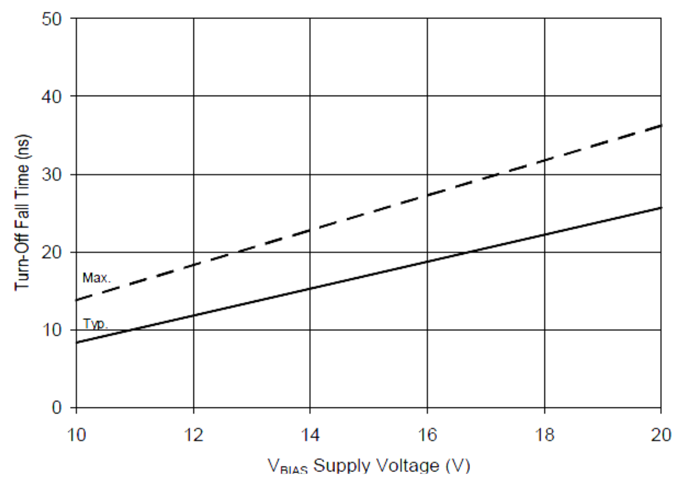


Figure 8B. Turn-Off Fall Time vs. Voltage

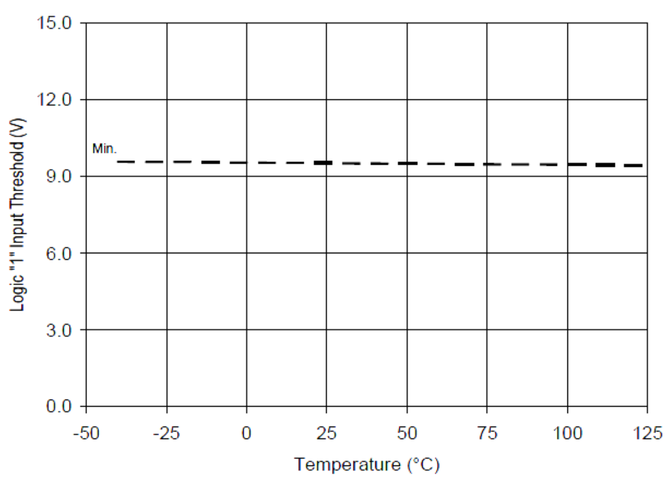


Figure 9A. Logic “1” Input Threshold vs. Temperature

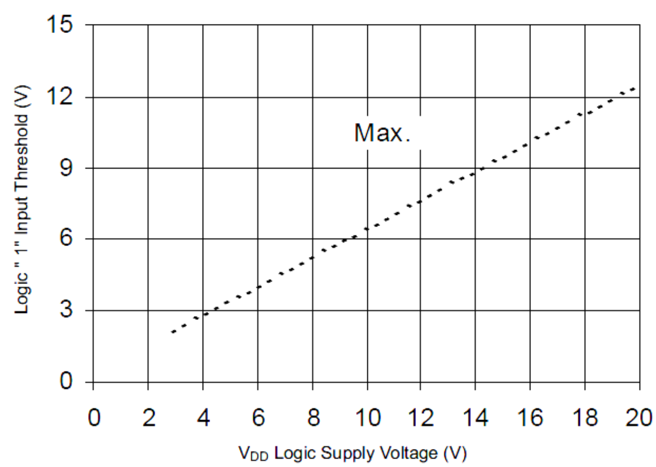


Figure 9B. Logic “1” Input Threshold vs. Voltage

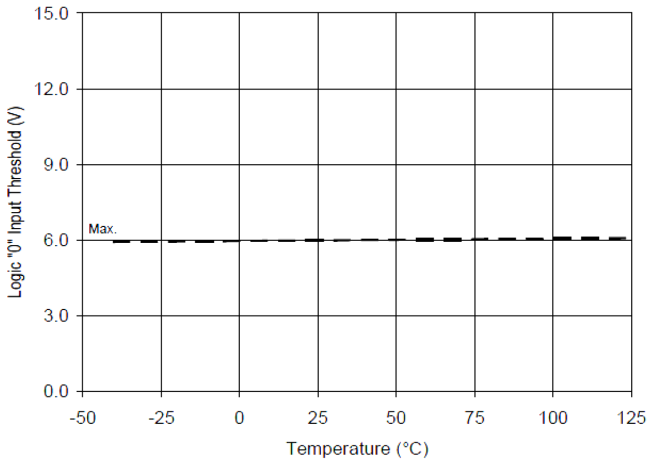


Figure 10A. Logic "0" Input Threshold vs. Temperature

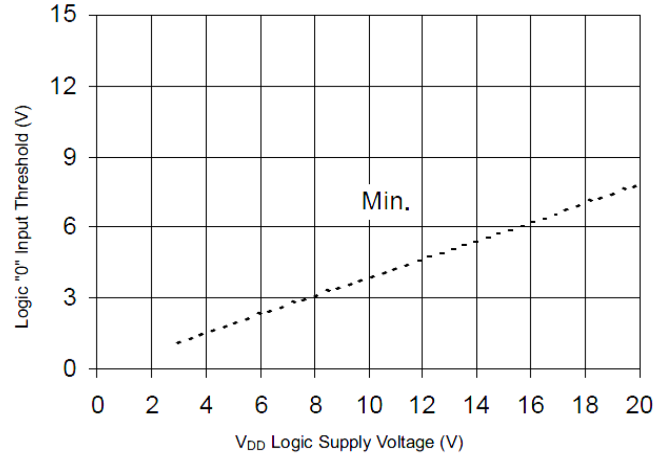


Figure 10B. Logic "0" Input Threshold vs. Voltage

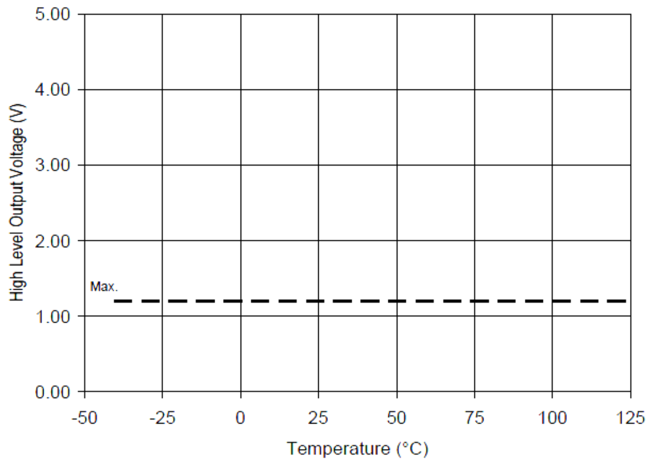


Figure 11A. High Level Output vs. Temperature

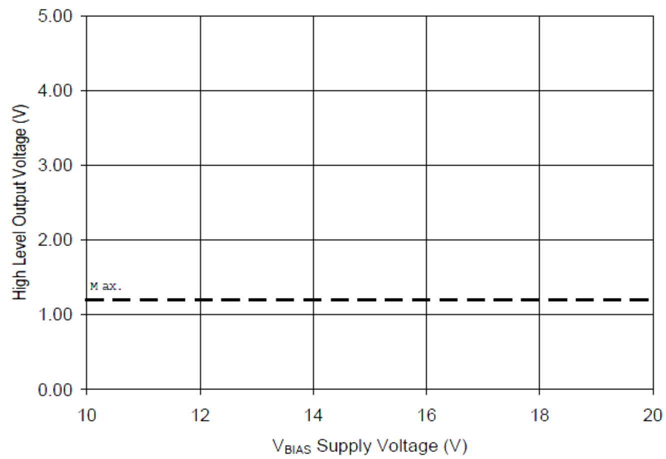


Figure 11B. High Level Outputs vs. Voltage

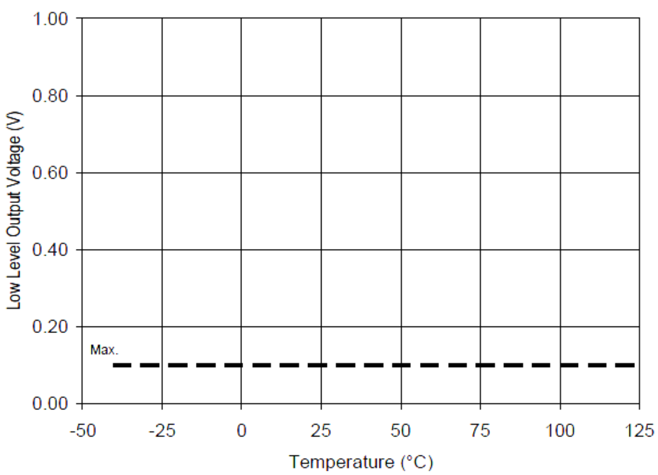


Figure 12A. Low Level Output vs. Temperature

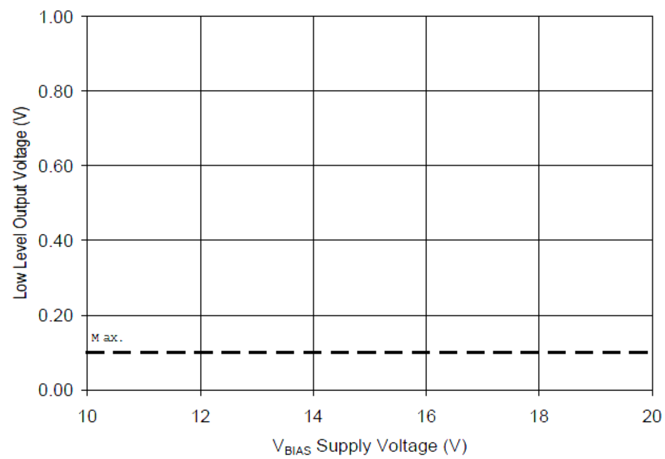


Figure 12B. Low Level Output vs. Voltage

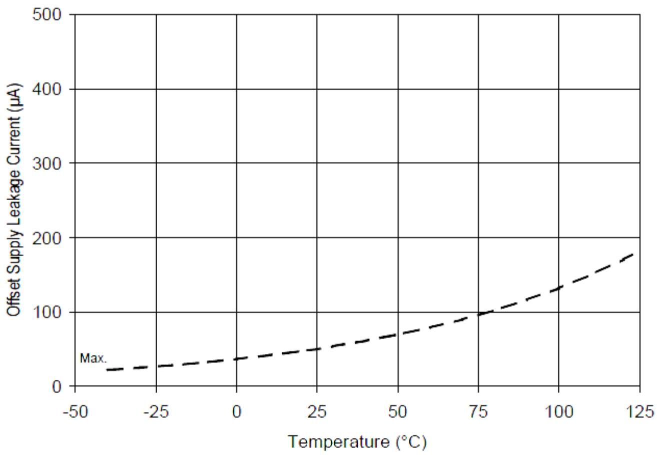


Figure 13A. Offset Supply Current vs. Temperature

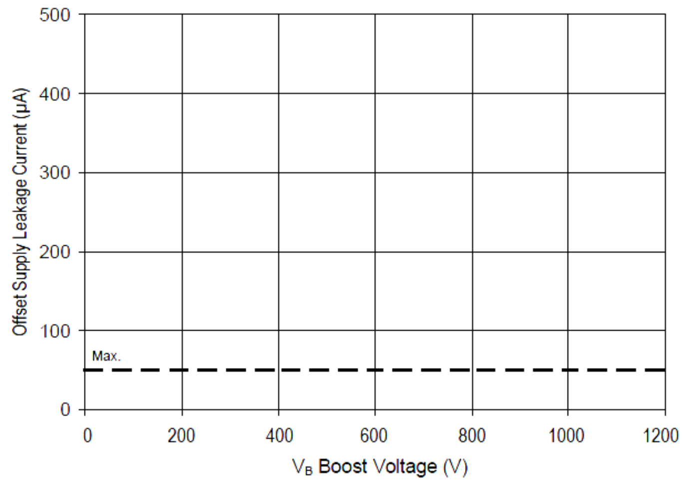


Figure 13B. Offset Supply Current vs. Voltage

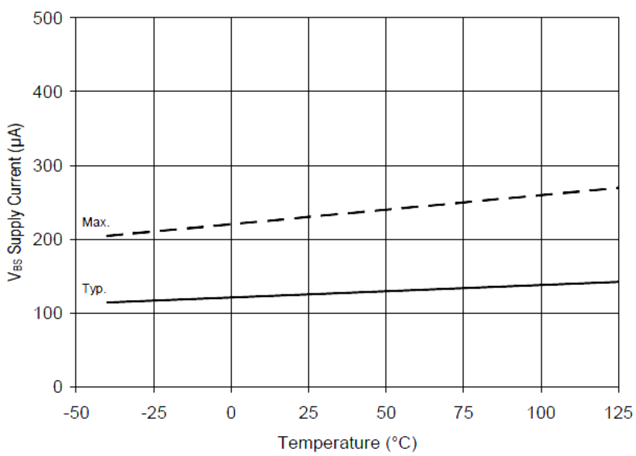


Figure 14A. V_{BS} Supply Current vs. Temperature

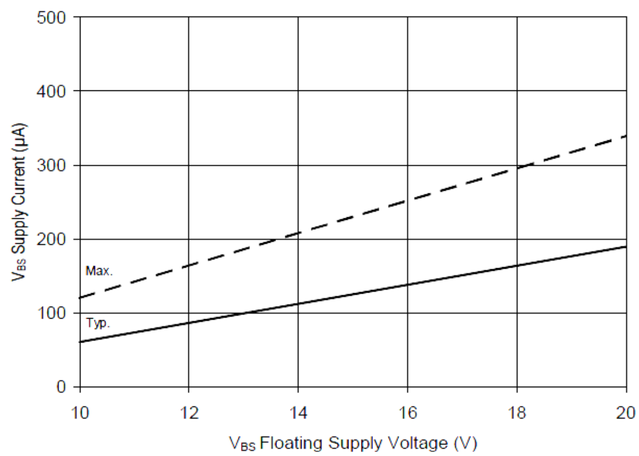


Figure 14B. V_{BS} Supply Current vs. Voltage

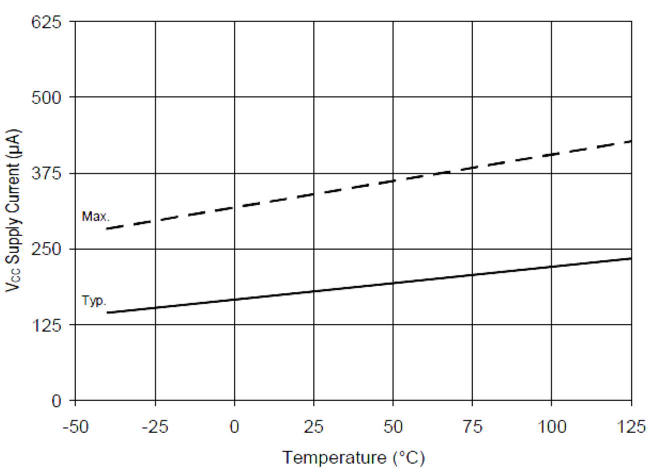


Figure 15A. V_{CC} Supply Current vs. Temperature

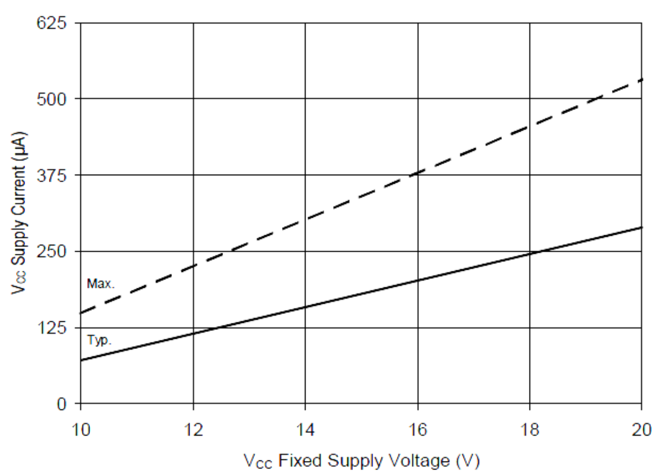


Figure 15B. V_{CC} Supply Current vs. Voltage

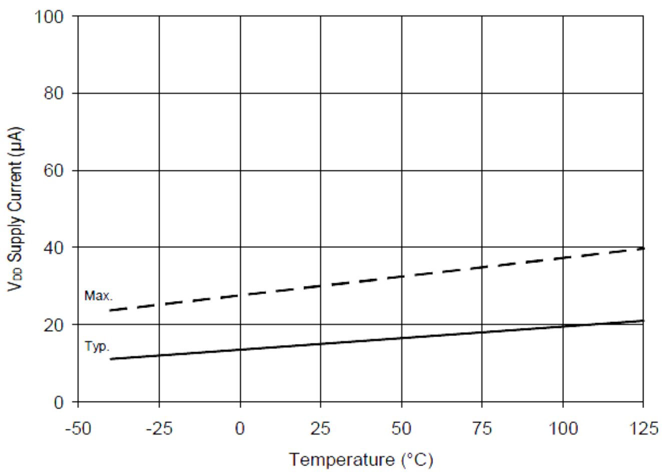


Figure 16A. V_{DD} Supply Current vs. Temperature

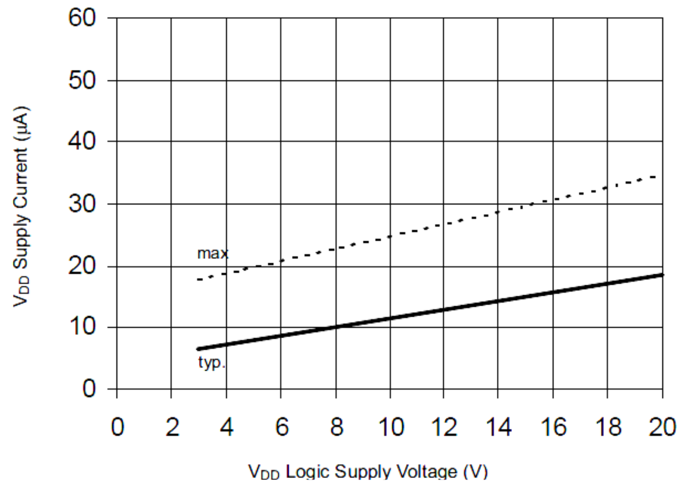


Figure 16B. V_{DD} Supply Current vs. V_{DD} Voltage

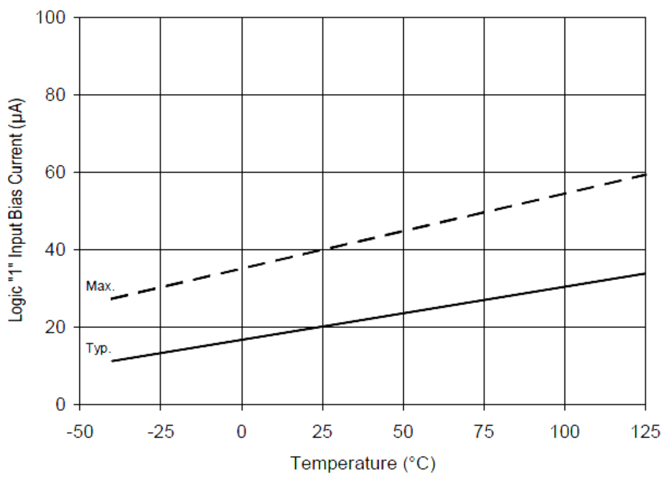


Figure 17A. Logic “1” Input Current vs. Temperature

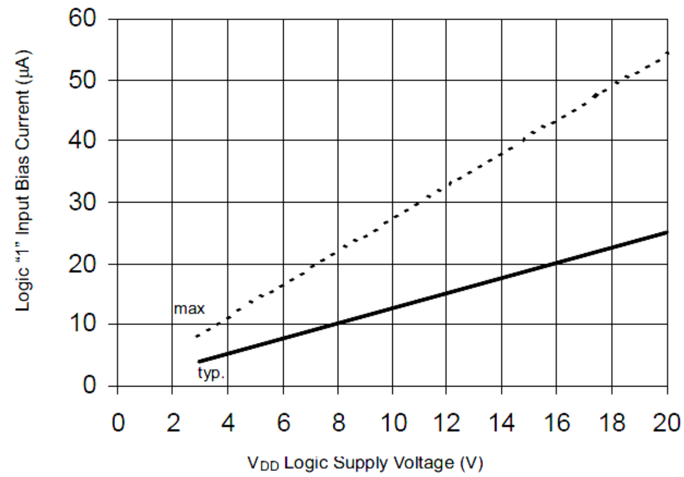


Figure 17B. Logic “1” Input Current vs. V_{DD} Voltage

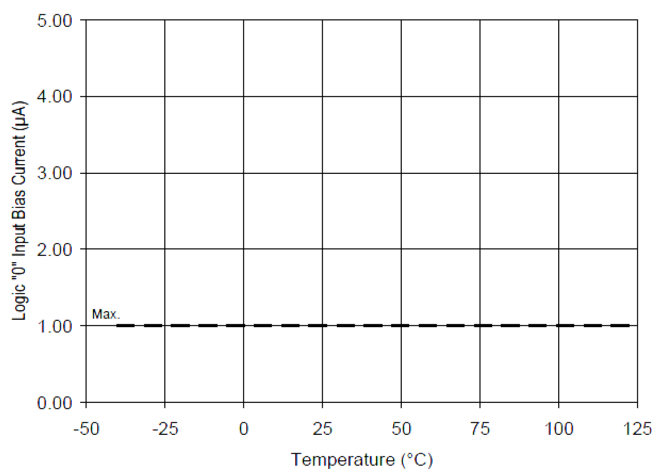


Figure 18A. Logic “0” Input Current vs. Temperature

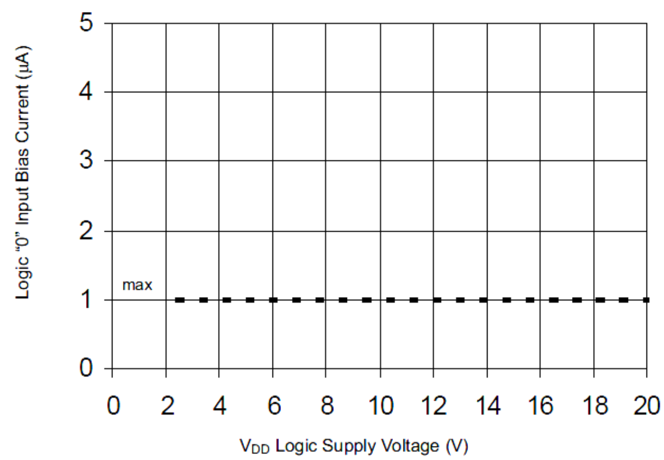


Figure 18B. Logic “0” Input Current vs. V_{DD} Voltage

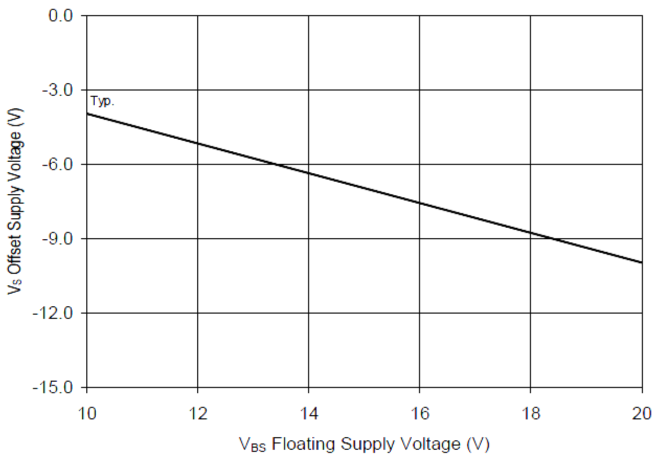


Figure 19. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

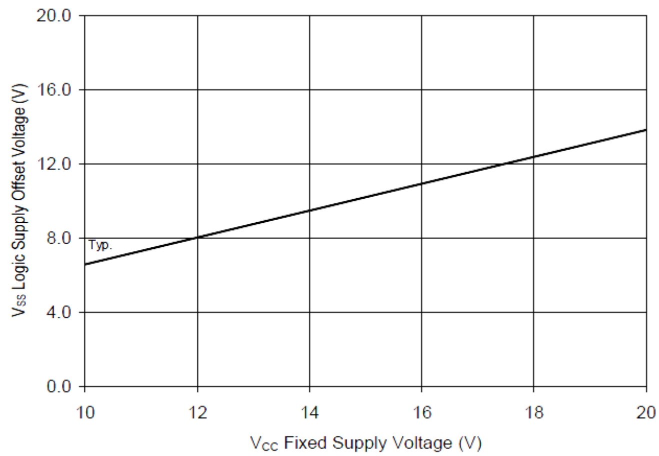


Figure 20. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

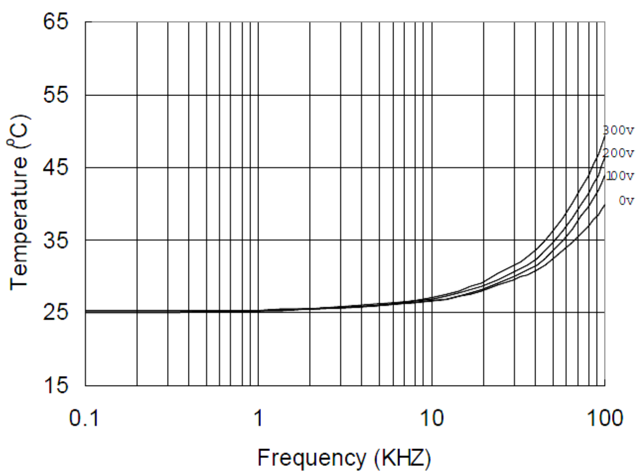


Figure 21. IR2213S vs. Frequency (IRFBC20) R_{gate}=33Ω, V_{CC}=15V

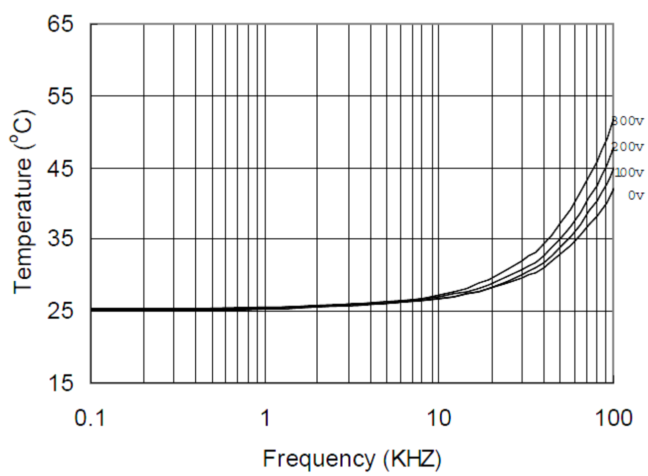


Figure 22. IR2213S vs. Frequency (IRFBC30) R_{gate}=22Ω, V_{CC}=15V

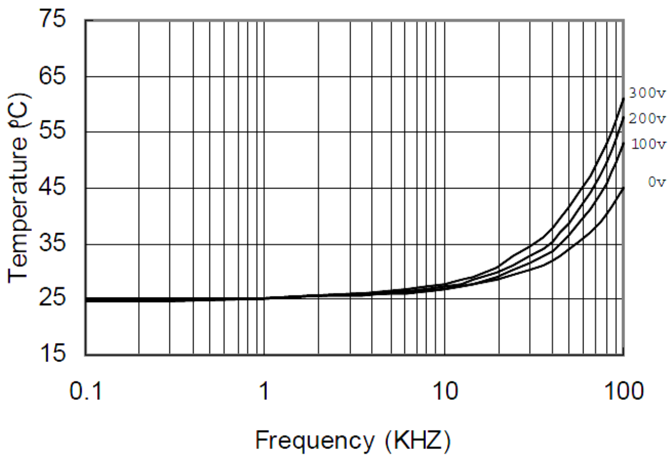


Figure 23. IR2213S vs. Frequency (IRFBC40)
R_{gate}=15Ω, V_{CC}=15V

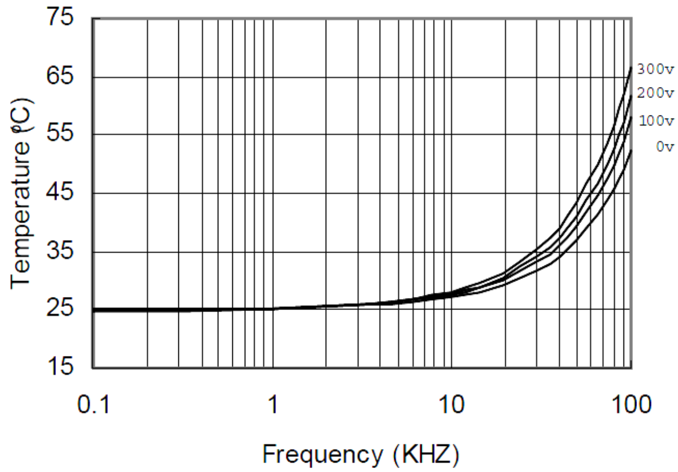


Figure 24. IR2213S vs. Frequency (IRFBC50)
R_{gate}=10Ω, V_{CC}=15V

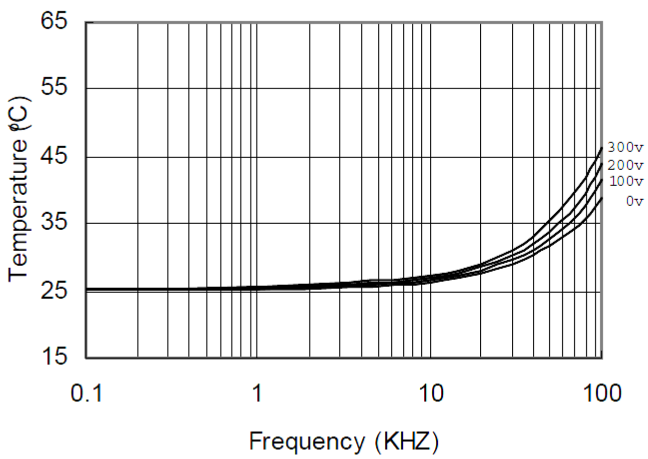


Figure 25. IR2213 vs. Frequency (IRFBC20)
R_{gate}=33Ω, V_{CC}=15V

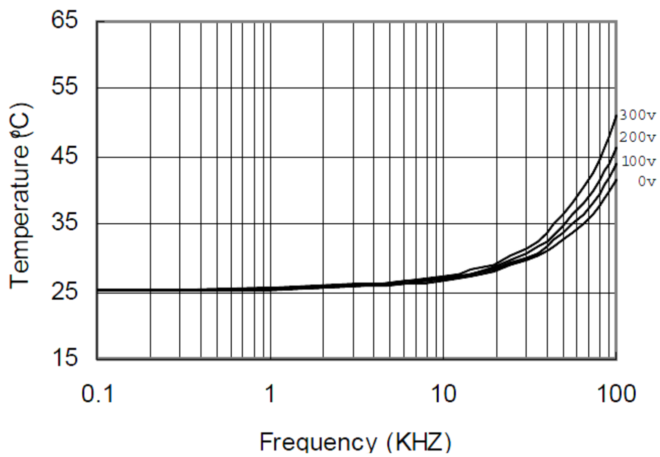


Figure 26. IR2213 vs. Frequency (IRFBC30)
R_{gate}=22Ω, V_{CC}=15V

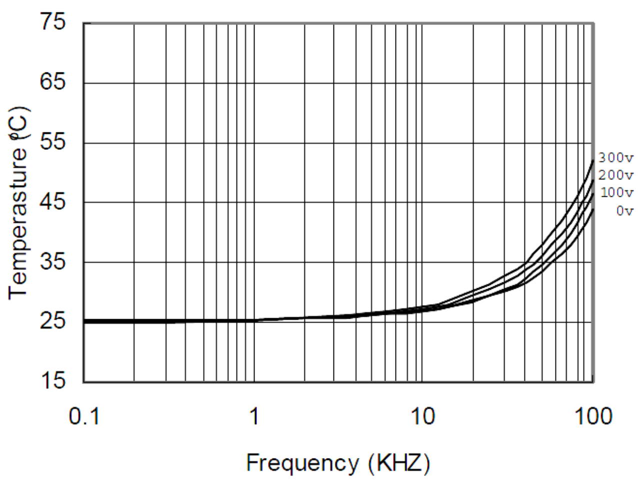


Figure 27. IR2213 vs. Frequency (IRFBC40)
R_{gate}=15Ω, V_{CC}=15V

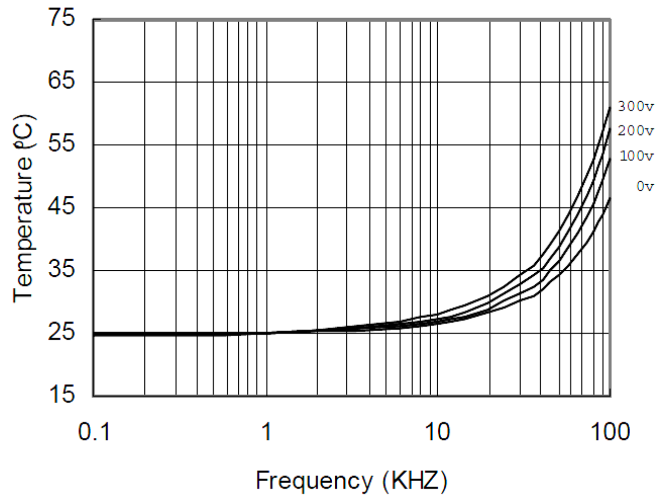


Figure 28. IR2213 vs. Frequency (IRFBC50)
R_{gate}=10Ω, V_{CC}=15V

Shipping

Three shipping options are offered as standard.

- Un-sawn wafer

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Un-sawn wafers and singulated die can be stored for up to 12 months when in the original sealed packaging at room temperature (45% ± 15% RH controlled environment).
- Un-sawn wafers and singulated die that have been opened can be stored when returned to their containers and placed in a nitrogen purged cabinet, at room temperature (45% ± 15% RH controlled environment).
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.
- Die in surf tape type carrier tape are intended for immediate use and have a limited shelf life. This is primarily due to the nature of the adhesive tape used to hold the product in the carrier tape cavity. This product can be stored for up to 30 days. This applies whether or not the material has remained in its original sealed container.