2Gb/4Gb SEMPER™ Flash

Octal interface, 1.8V/3.0V

Device overview

- **Architecture**
  - Infineon® 45-nm MIRRORBIT™ technology that stores two data bits in each memory array cell
  - Multi-chip package (MCP)
    - 02GT Dual die package (DDP) 2 × 1 Gb die
    - 04GT Quad die package (QDP) 4 × 1 Gb die
  - Sector architecture options
    - Uniform: Address space consists of all 256 KB sectors
    - Hybrid:
      Configuration 1: Address space consists of thirty-two 4 KB sectors grouped either on the top or the bottom while the remaining sectors are all 256 KB
      Configuration 2: Address space consists of thirty-two 4 KB sectors at the top and bottom while the remaining sectors are all 256 KB
  - Page programming buffer of 256 or 512 bytes
  - OTP secure silicon array of 1024-bytes (32 × 32 bytes)

- **Interface**
  - Octal interface (8S-8S-8S, 8D-8D-8D)
    - JEDEC eXpanded SPI (JESD251) compliant
    - SDR option runs up to 166 MBps (166 MHz clock speed)
    - DDR option runs up to 332 MBps (166 MHz clock speed)
    - Supports data strobe (DS) to simplify the read data capture in high-speed systems
  - SPI(1S-1S-1S)
    - JEDEC eXpanded SPI (JESD251) compliant
    - SDR option runs up to 21 MBps (166 MHz clock speed)

- **Highlights**
  - Safety features
    - Functional safety with the industry's first ISO26262 ASIL B compliant and ASIL D ready NOR Flash
    - Infineon Endurance flex architecture provides high-endurance and long retention partitions
    - Data integrity CRC detects errors in memory array
    - SafeBoot reports device initialization failures, detects configuration corruption, and provides recovery options
    - Built-in error correcting code (ECC) corrects single-bit error and detects double-bit error (SECDED) on memory array data
    - Sector erase status indicator for power loss during erase
  - Protection features
    - Legacy block protection for memory array and device configuration
    - Advanced sector protection for individual memory array sector based protection
  - Hardware reset through CS# signaling method (JEDEC) or individual RESET# pin

- **Identification**
  - Serial flash discoverable parameters (SFDP) describing device functions and features
  - Device identification, manufacturer identification, and unique identification

- **Data integrity**
  - Minimum 2,560,000 program-erase cycles for the main array
  - Minimum 300,000 program-erase cycles for the 4 KB sectors
  - Minimum 25 years data retention

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- **Supply voltage**
  - 1.7-V to 2.0-V (HS-T)
  - 2.7-V to 3.6-V (HL-T)

- **Grade / Temperature range**
  - Industrial (-40 °C to +85 °C)
  - Industrial Plus (-40 °C to +105 °C)
  - Automotive AEC-Q100 grade 3 (-40 °C to +85 °C)
  - Automotive AEC-Q100 grade 2 (-40 °C to +105 °C)
  - Automotive AEC-Q100 grade 1 (-40 °C to +125 °C)

- **Packages**
  - 24-ball BGA 8 × 8 mm

Performance summary

Maximum read rates

Transaction	Initial access latency (Cycles)	Clock rate (MHz)	MBps
SPI read	0	50	6.25
SPI read fast (HS-T)	10	166	20.75
SPI read fast (HL-T)	7	133	16.62
Octal read SDR (HS-T)	14	166	166
Octal read SDR (HL-T)	12	133	133
Octal read DDR (HS-T)	20	166	332
Octal read DDR (HL-T)	14	133	266

Typical program and erase rates

Operation	KBps
Page programming 256 bytes page buffer (4 KB sector / 256 KB sector)	595 / 533
Page programming 512 bytes page buffer (4 KB sector / 256 KB sector)	753 / 898
256 KB sector erase	331
4 KB sector erase	95

Typical current consumption DDP

Operation	HL-T current (mA)	HS-T current (mA)
SDR read 50 MHz	10	10
SDR read (Octal)	96 (133 MHz)	110 (166 MHz)
DDR read (Octal)	96 (133 MHz)	110 (166 MHz)
Program	50	50
Erase	50	50
Standby	0.028	0.022
Deep power down	0.0044	0.0026

Typical current consumption QDP

Operation	HL-T current (mA)	HS-T current (mA)
SDR read 50 MHz	10	10
SDR read 166 MHz (SPI)	40	40
SDR read (Octal)	96 (133 MHz)	110 (166 MHz)
DDR read (Octal)	96 (133 MHz)	110 (166 MHz)
Program	50	50
Erase	50	50
Standby	0.056	0.044
Deep power down	0.0088	0.0052

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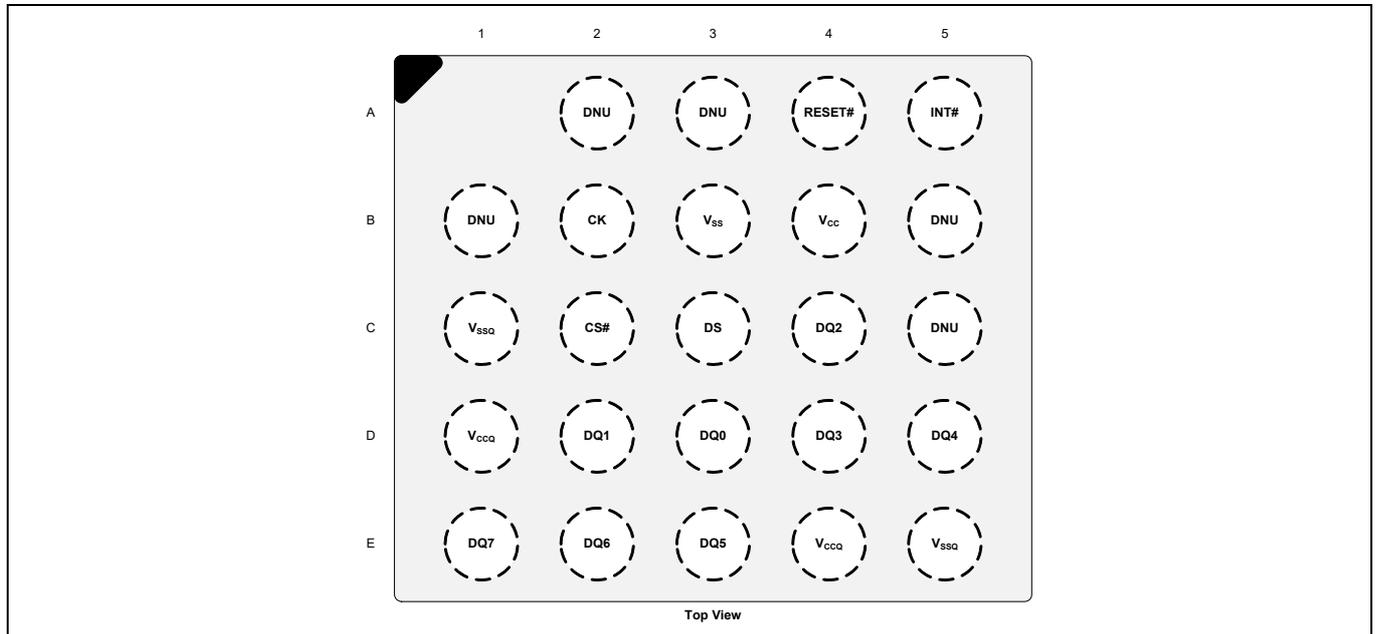# 1 Pinout and signal description

Figure 1   24-ball BGA pinout configuration[1]

Note
1. Flash memory devices in BGA packages can be damaged if exposed to ultrasonic cleaning methods. The package, data integrity, or both may be compromised if the package body is exposed to temperatures above 150 °C for prolonged periods of time.

Pinout and signal description

Table 1 **Signal description**

Symbol	Type	Mandatory / optional	Description
CS#	Input	Mandatory	**Chip Select (CS#).** All bus transactions are initiated with a HIGH to LOW transition on CS# and terminated with a LOW to HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the active mode. When CS# is driven HIGH, the device enters standby mode, unless an internal embedded operation is in progress. All other input pins are ignored and the output pins are put in high impedance state. On parts where the pin configuration offers a dedicated RESET# pin, it remains active when CS# is HIGH.
CK	Input	Mandatory	**Clock (CK)**. Clock provides the timing of the serial interface. Transactions are latched on the rising edge of the clock. In SDR protocol, command, address, and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DDR protocol, command, address, and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.
DS	Output	Mandatory	**Read Data Strobe (DS)**. DS is used for data read operations only and indicates output data valid for SDR/DDR modes. During a read transaction while CS# is LOW, DS toggles to synchronize data output until CS# goes high.
DQ[7:0]	Input/Output	Mandatory	**Serial Data (DQ[7:0])**. Bidirectional signals that transfer command, address, and data information. **Legacy (×1) SPI interface**: DQ[0] is an input (SI) and DQ[1] is an output (SO). **Octal (×8) Interface**: DQ[7:0] are input and output.
RESET#	Input (Weak pullup)	Optional	**Hardware Reset (RESET#)**. When LOW, the device will self initialize and return to the array read state. DS and DQ[7:0] are placed into the high impedance state when RESET# is LOW. RESET# includes a weak pull up, meaning, if RESET# is left unconnected it will be pulled up to the HIGH state on its own.
INT#	Output (Open drain)	Optional	**System Interrupt (INT#)**. When LOW, the device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output. The recommended pull-up resistor for the INT# outputs is 5 kΩ to 10 kΩ.
V_{CC}	Power supply	Mandatory	**Core Power Supply**
V_{CCQ}	Power supply	Mandatory	**Input/Output Power Supply**
V_{SS}	Ground supply	Mandatory	**Core Ground**
V_{SSQ}	Ground supply	Mandatory	**Input/Output Ground**
DNU	–	–	**Do Not Use**

2 Interface overview

2.1 General description

The Infineon® SEMPER™ Flash Octal family of products are high-speed CMOS, MIRRORBIT™ NOR Flash devices that are compliant with the JEDEC JESD251eXpanded SPI (xSPI) specification. SEMPER™ Flash is designed for functional safety with development according to ISO 26262 standard to achieve ASIL-B compliance and ASIL-D readiness.

SEMPER™ Flash with Octal interface devices support both the octal peripheral interface (OPI) as well as legacy ×1 SPI. Both interfaces serially transfer transactions reducing the number of interface connection signals. SPI supports SDR, whereas OPI supports both SDR and DDR.

Read operations from the device are burst oriented. Read transactions can be configured to use either a wrapped or linear burst. Wrapped bursts read from a single page, whereas linear bursts can read the whole memory array.

The erased state of each memory bit is a logic 1. Programming changes a logic 1 (HIGH) to a logic 0 (LOW). Only an erase operation can change a memory bit from a 0 to a 1. An erase operation must be performed on a complete sector (4 KBs or 256 KBs).

SEMPER™ Flash provides a flexible sector architecture. The address space can be configured as either a uniform 256 KB sector array or a hybrid grouped array where thirty-two 4 KB sectors are either grouped at the top or at the bottom while the remaining sectors are all 256 KB, or a hybrid split array where the thirty-two 4 KB sectors are at both the top and the bottom while the remaining sectors are all 256 KB.

The page programming buffer used during a single programming operation is configurable to either 256 bytes or 512 bytes. The 512 byte option provides the highest programming throughput.

This device is an MCP with DDP or QDP stacked die, with the control signals for all dies tied together internally in the package.
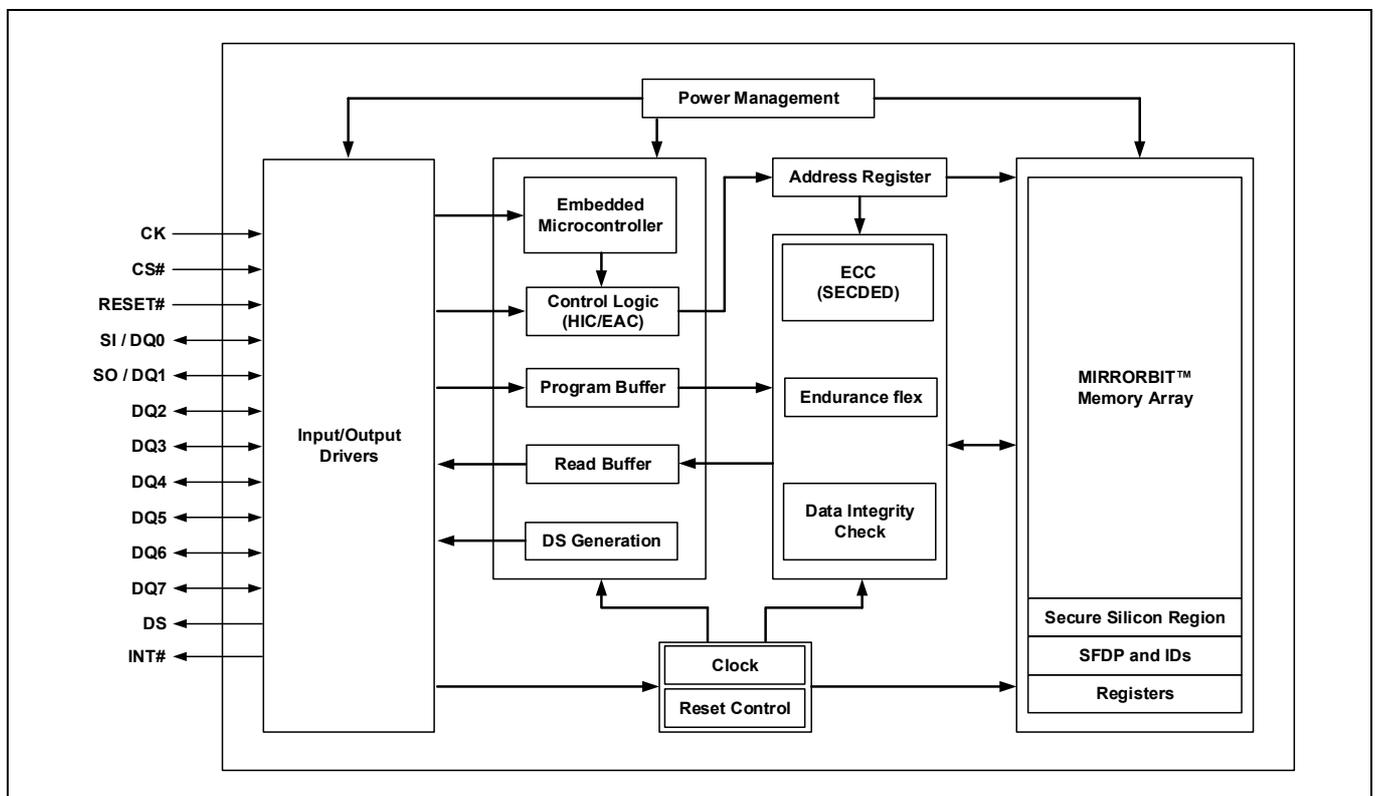

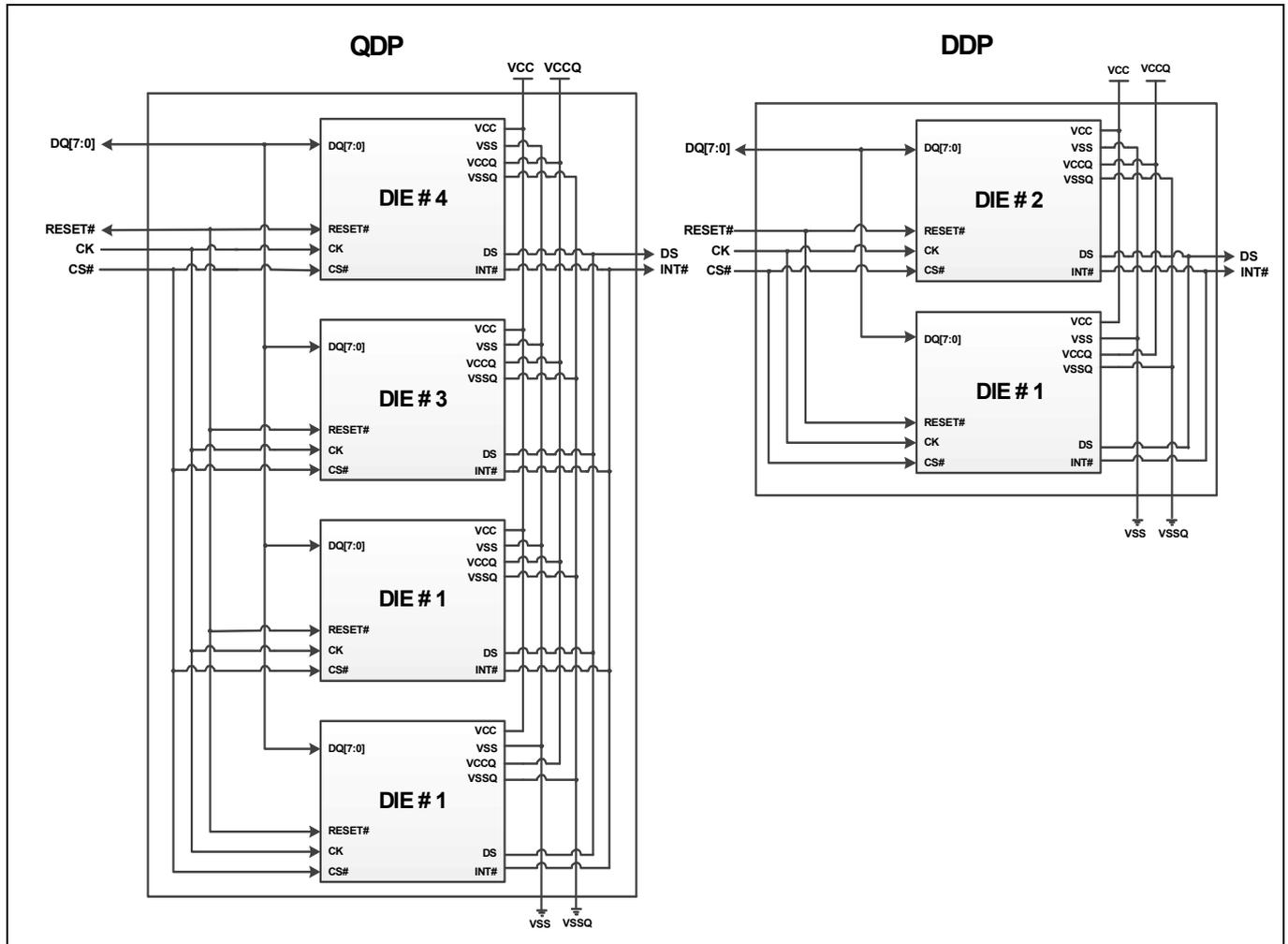**Figure 2   Logic block diagram monolithic die**

Figure 3   MCP diagram

The SEMPER™ Flash with Octal interface family consists of multiple densities with 1.8 V and 3.0 V core and I/O voltage options.

The device control logic is subdivided into two parallel operating sections: the host interface controller (HIC) and the embedded algorithm controller (EAC).

The HIC monitors signal levels on the device inputs and drives outputs as needed to complete read, program, and write data transfers with the host system. The HIC delivers data from the currently entered address map on read transfers; places write transfer address and data information into the EAC command memory, and notifies the EAC of power transition, and write transfers. The EAC interrogates the command memory, after a program or write transfer, for legal command sequences and performs the related embedded algorithms.

Changing the nonvolatile data in the memory array requires a sequence of operations that are part of embedded algorithms (EA). The algorithms are managed entirely by the internal EAC. The main algorithms perform programming and erase of the main flash array data. The host system writes command codes to the flash device. The EAC receives the command, performs all the necessary steps to complete the transaction, and provides status information during the progress of an EA.

In addition to the mandatory SPI signals CK, CS#, SI/DQ0, SO/DQ1, and DQ[7:2], the SEMPER™ Flash with octal interface device also includes RESET#, DS, and INT# signals. The RESET# transition from LOW to HIGH returns the device to the default state that occurs after an internal power-on reset (POR). The data strobe (DS) is synchronized with the output data during read transactions enabling host system to capture data at high clock frequency operation. The INT# is an open-drain output that can provide an interrupt to the device master to indicate when the device transitions from busy to ready at the end of a program or erase operation or to indicate the detection of an error (ECC) during read.

Endurance flex architecture provides system designers the ability to customize the NOR Flash endurance and retention for their specific application. The host defines partitions for high endurance or long retention, providing up to 1+ million cycles or 25 years of data retention.

The SEMPER™ Flash with Octal interface device supports error detection and correction by generating an embedded hamming error correction code (ECC) during memory array programming. This ECC code is then used for single-bit and double-bit error detection and single-bit correction during read.
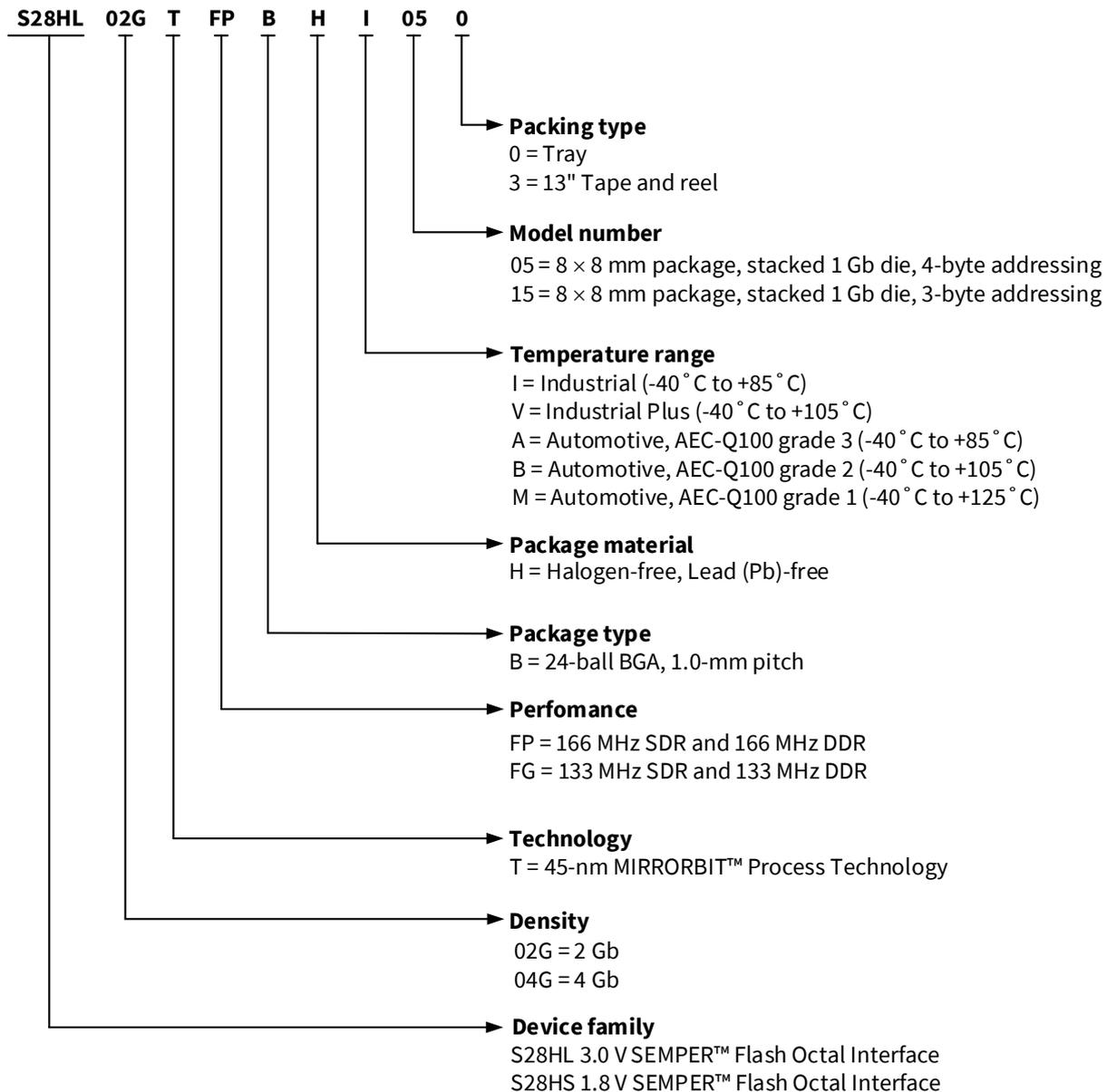
The SEMPER™ Flash with octal interface device has built-in diagnostic features providing the host system with the device status.

• Program and erase operation: Reporting of program or erase success, failure, and suspend statuses

• ECC: 1-bit and/or 2-bit error status with address trapping and error count

• Data integrity check: Error detection over memory array contents

• SafeBoot: Reporting of proper flash device initialization and configuration corruption recovery

• Sector erase status: Reporting of erase success or failure status per sector

• Sector erase counter: Counts the number of erase cycles per sector

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3 Ordering information

Register for the SEMPER™ Access Program and get access to Software and Evaluation kits, models, datasheets, and application notes.

The ordering part number is formed by a valid combination of the following:

S28HL   02G   T   FP   B   H   I   05   0

Packing type
0 = Tray
3 = 13" Tape and reel

Model number
05 = 8 × 8 mm package, stacked 1 Gb die, 4-byte addressing
15 = 8 × 8 mm package, stacked 1 Gb die, 3-byte addressing

Temperature range
I = Industrial (-40 ˚C to +85 ˚C)
V = Industrial Plus (-40 ˚C to +105 ˚C)
A = Automotive, AEC-Q100 grade 3 (-40 ˚C to +85 ˚C)
B = Automotive, AEC-Q100 grade 2 (-40 ˚C to +105 ˚C)
M = Automotive, AEC-Q100 grade 1 (-40 ˚C to +125 ˚C)

Package material
H = Halogen-free, Lead (Pb)-free

Package type
B = 24-ball BGA, 1.0-mm pitch

Perfomance
FP = 166 MHz SDR and 166 MHz DDR
FG = 133 MHz SDR and 133 MHz DDR

Technology
T = 45-nm MIRRORBIT™ Process Technology

Density
02G = 2 Gb
04G = 4 Gb

Device family
S28HL 3.0 V SEMPER™ Flash Octal Interface
S28HS 1.8 V SEMPER™ Flash Octal Interface

Revision history

Document version	Date of release	Description of changes
**	2022-02-09	Initial release.

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