TEXAS INSTRUMENTS
LMP7704-SP
ZHCSN30C – DECEMBER 2020 – REVISED MARCH 2022

LMP7704-SP 具有低输入偏置和宽电源电压范围的耐辐射加固保障 (RHA)、精密 RRIO 放大器

1 特性

- QML V 类 (QMLV)、RHA、SMD 5962-19206
- 辐射性能
  - RHA 高达 TID = 100krad(Si)
  - 无低剂量率辐射损伤增强 (ELDRS)，最高 TID = 100krad(Si)
  - SEL 对于 LET 的抗扰度 = 85MeV-cm^2/mg
  - SEE 对于 LET 的额定值 = 85MeV cm^2/mg
- 超低输入偏置电流：±500fA
- 输入失调电压：±60μV
- 单位带宽增益积：2.5MHz
- 电源电压范围：2.7 V 至 12 V
- 轨至轨输入和输出
- 军用温度范围-55°C 至 +125°C
- 采用 14 引线 CFP，具有业界通用四路放大器引脚分配

2 应用

- 卫星运行状况监控和遥测
- 科学勘探有效载荷
- 姿态和轨道控制系统 (AOCS)
- 卫星电力系统 (EPS)
- 通信负载
- 雷达成像有效载荷

3 说明

LMP7704-SP 是一款精密放大器，具有低输入偏置、低失调电压、2.5 MHz 增益带宽积和宽电源电压。该器件耐辐射，可在 -55°C 至 +125°C 的军用级温度范围内运行。

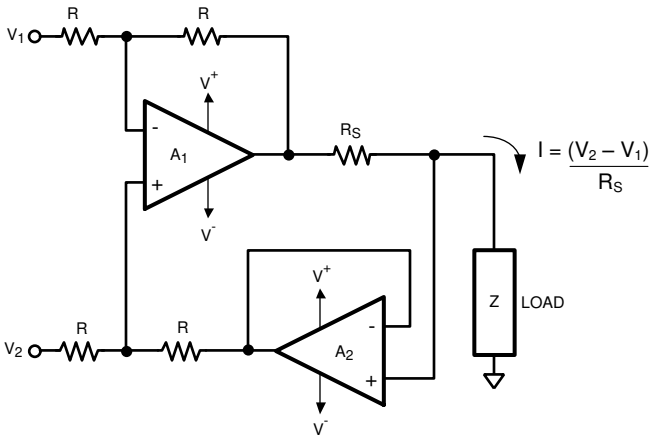
该放大器拥有高直流精度等特性，特别是 ±60 μV 的低失调电压和 ±500 fA 的超低输入偏置，因此非常适合具有高输出阻抗的精密传感器接口。该放大器可配置为换能器/传感器、电桥、应变仪和跨阻放大。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
5962R1920601VXC，飞行模型 (QMLV)，RHA 达 100 krad	CFP (14)	9.73mm x 6.47mm
LMP7704HBH/EM，工程模型(2)		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 这些器件仅适用于工程评估。按非合规性流程对其进行了处理（即未进行老化处理等操作）并且仅在 25°C 的额定温度下进行了测试。这些部件不适用于质检、量产、辐射测试或飞行。这些零件无法在 –55°C 至 +125°C 的完整 MIL 额定温度范围内或运行寿命中保证其性能。有关工程模型的更多信息，请参阅 *德州仪器 (TI) 工程评估单元与 MIL-PRF-38535 QML V 类处理概述*。



典型应用原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (September 2021) to Revision C (March 2022)	Page
• 将 5962R1920601VXC 飞行模型从预发布更改为量产数据（正在供货）	1
• 删除了*器件信息*表中已淘汰的 5962-1920601VXC 飞行模型	1

Changes from Revision A (January 2021) to Revision B (September 2021)	Page
• 将器件状态从“预告信息（预发布）”更改为“量产数据（正在供货）”	1

5 Pin Configuration and Functions

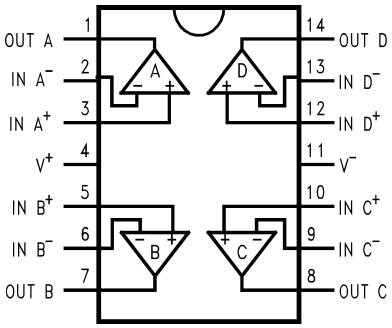


图 5-1. HBH Package, 14-Pin CFP, Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN A+	3	I	Noninverting input for amplifier A
IN A−	2	I	Inverting input for amplifier A
IN B+	5	I	Noninverting input for amplifier B
IN B−	6	I	Inverting input for amplifier B
IN C+	10	I	Noninverting input for amplifier C
IN C−	9	I	Inverting input for amplifier C
IN D+	12	I	Noninverting input for amplifier D
IN D−	13	I	Inverting input for amplifier D
OUT A	1	O	Output for amplifier A
OUT B	7	O	Output for amplifier B
OUT C	8	O	Output for amplifier C
OUT D	14	O	Output for amplifier D
V+	4	P	Positive supply
V−	11	P	Negative supply
LID	—	—	The metal lid is internally connected to V−

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)			13.2	V
	Voltage	Common-mode	(V–) – 0.3	(V+) + 0.3	V
		Differential		(V+) – (V–) + 0.3	
	Current			±10	mA
	Output short circuit(2)		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	2.7		12	V
T_A	Specified temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMP7704-SP HBH (CFP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	20.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics: V_S = 5 V

at T_A = +25°C, V_S = (V+) – (V–) = 5 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±60	±260	µV
		T_A = –55°C to +125°C				±520	
dV_{OS}/dT	Input offset voltage drift(1)	T_A = –55°C to +125°C			±1	±5	µV/°C
PSRR	Power-supply rejection ratio	2.7 V < V_S < 12 V		86	100		dB
			T_A = –55°C to +125°C	82			dB
INPUT BIAS CURRENT							
I_B	Input bias current				±0.5	±10	pA
		T_A = –55°C to +125°C				±400	pA
I_{OS}	Input offset current				±40		fA
NOISE							
e_n	Input voltage noise density	f = 1 kHz			9		nV/√Hz
i_n	Input current noise density	f = 100 kHz			1		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	T_A = –55°C to +125°C		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+)		85	130		dB
			T_A = –55°C to +125°C	81			
			Flight model post-HDR exposure, T_A = –55°C to +125°C	76			
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V < V_{OUT} < (V+) – 0.3 V, R_L = 2 kΩ		100	119		dB
			T_A = –55°C to +125°C	94			
			Flight model post-HDR exposure, T_A = –55°C to +125°C	84			
		(V–) + 0.2 V < V_{OUT} < (V+) – 0.2 V		100	130		
			T_A = –55°C to +125°C	96			
FREQUENCY RESPONSE							
GBW	Gain bandwidth				2.5		MHz
SR	Slew rate	G = 1, 4-V step, 10% to 90% rising			1		V/µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz			0.02%		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	R_L = 2 kΩ to V_S / 2		60	120	mV
			R_L = 2 kΩ to V_S / 2, T_A = –55°C to +125°C			200	
					40	60	
			T_A = –55°C to +125°C			120	
		Negative rail	R_L = 2 kΩ to V_S / 2		50	120	
			R_L = 2 kΩ to V_S / 2, T_A = –55°C to +125°C			190	
					30	50	
			T_A = –55°C to +125°C			100	
I_{SC}	Short-circuit current	V_{OUT} = V_S / 2, V_{IN} = ±100 mV			+66 / –76		mA
POWER SUPPLY							

6.5 Electrical Characteristics: V_S = 5 V (continued)

at T_A = +25°C, V_S = (V+) – (V –) = 5 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Total quiescent current	I_O = 0 A			2.9	3.7	mA
			T_A = –55°C to +125°C			5.1	

(1) Specification set by device characterization, not tested in final production.

6.6 Electrical Characteristics: V_S = 10 V

at T_A = +25°C, V_S = (V+) – (V–) = 10 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±60	±260	µV
		T_A = –55°C to +125°C				±520	
dV_{OS}/dT	Input offset voltage drift(1)	T_A = –55°C to +125°C			±1	±5	µV/°C
PSRR	Power-supply rejection ratio	2.7 V < V_S < 12 V		86	100		dB
			T_A = –55°C to +125°C	82			dB
INPUT BIAS CURRENT							
I_B	Input bias current				±1	±10	pA
		T_A = –55°C to +125°C				±400	pA
I_{OS}	Input offset current				±40		fA
NOISE							
e_n	Input voltage noise density	f = 1 kHz			9		nV/√Hz
i_n	Input current noise density	f = 100 kHz			1		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+)		90	130		dB
			T_A = –55°C to +125°C	86			
			Flight model post-HDR exposure, T_A = –55°C to +125°C	83			
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V < V_{OUT} < (V+) – 0.3 V, R_L = 2 kΩ		100	121		dB
			T_A = –55°C to +125°C	94			
		(V–) + 0.2 V < V_{OUT} < (V+) – 0.2 V		100	134		
			T_A = –55°C to +125°C	97			
FREQUENCY RESPONSE							
GBW	Gain bandwidth				2.5		MHz
SR	Slew rate	G = 1, 9-V step, 10% to 90% rising			0.8		V/µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz			0.02%		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	R_L = 2 kΩ to V_S / 2		60	120	mV
			R_L = 2 kΩ to V_S / 2, T_A = –55°C to +125°C			200	
					40	60	
			T_A = –55°C to +125°C			120	
		Negative rail	R_L = 2 kΩ to V_S / 2		50	120	
			R_L = 2 kΩ to V_S / 2, T_A = –55°C to +125°C			190	
					30	50	
			T_A = –55°C to +125°C			100	
I_{SC}	Short-circuit current	V_{OUT} = V_S / 2, V_{IN} = ±100 mV			+86 / –84		mA
POWER SUPPLY							

6.6 Electrical Characteristics: V_S = 10 V (continued)

at T_A = +25°C, V_S = (V+) – (V –) = 10 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Total quiescent current	I_O = 0 A			3.2	4.2	mA
			T_A = –55°C to +125°C			5.7	

(1) Specification set by device characterization, not tested in final production.

6.7 Typical Characteristics

at T_A = 25°C, V_{CM} = V_S/2, and R_L > 10 kΩ (unless otherwise noted)

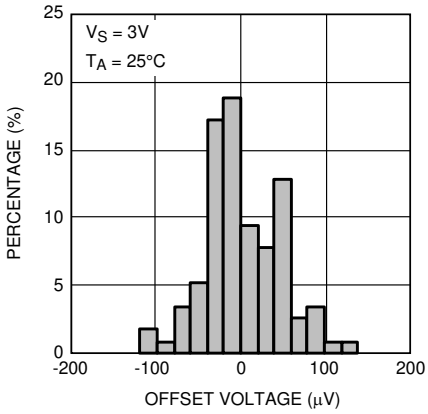


图 6-1. Offset Voltage Distribution

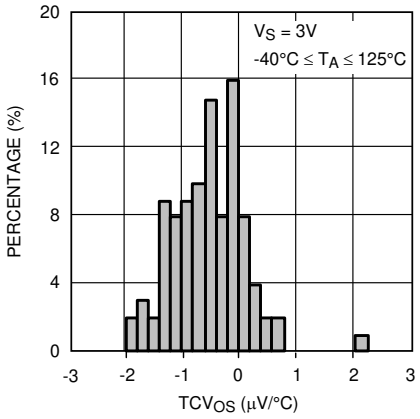


图 6-2. TCV_{OS} Distribution

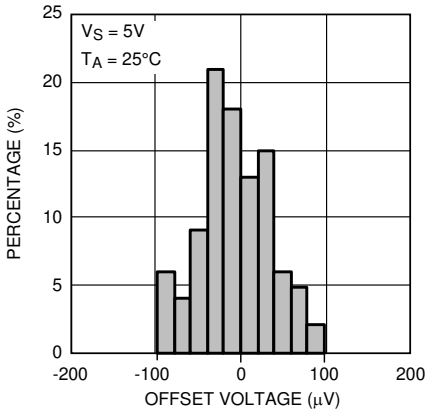


图 6-3. Offset Voltage Distribution

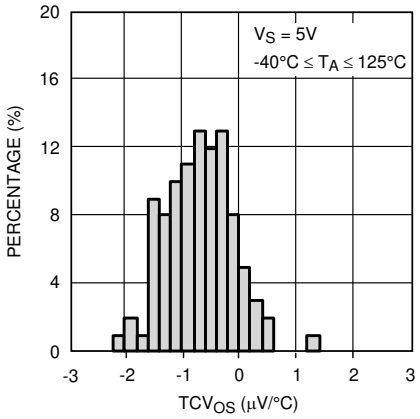


图 6-4. TCV_{OS} Distribution

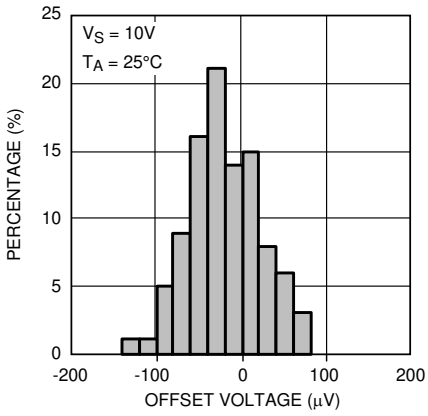


图 6-5. Offset Voltage Distribution

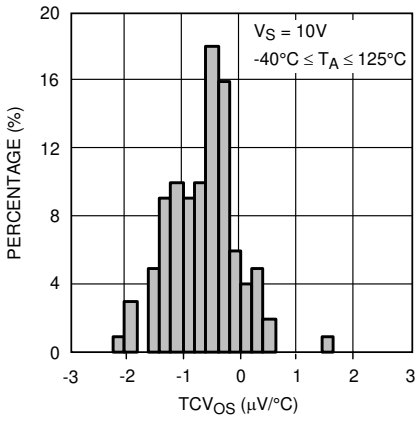


图 6-6. TCV_{OS} Distribution

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_S/2, and R_L > 10 kΩ (unless otherwise noted)

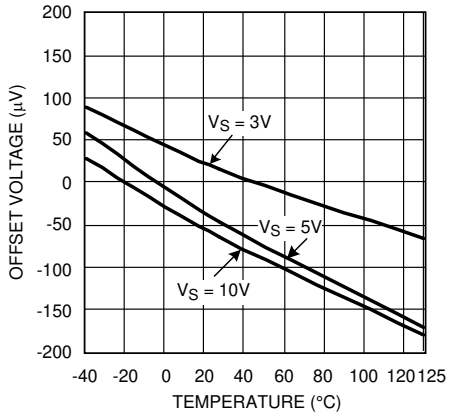


图 6-7. Offset Voltage vs Temperature

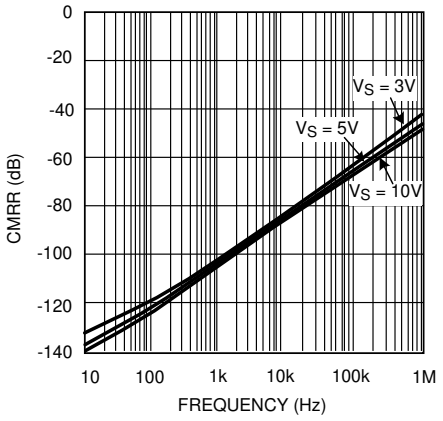


图 6-8. CMRR vs Frequency

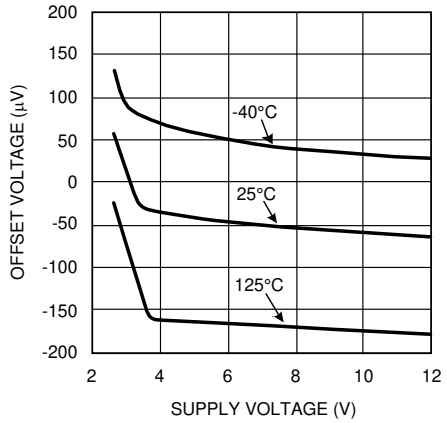


图 6-9. Offset Voltage vs Supply Voltage

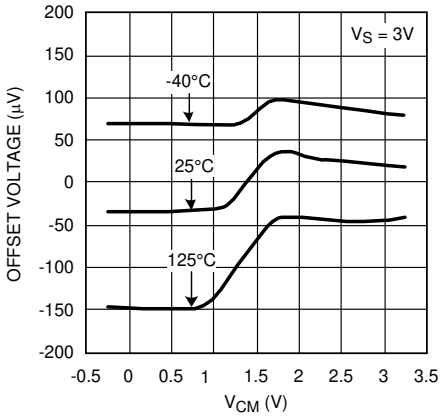


图 6-10. Offset Voltage vs V_{CM}

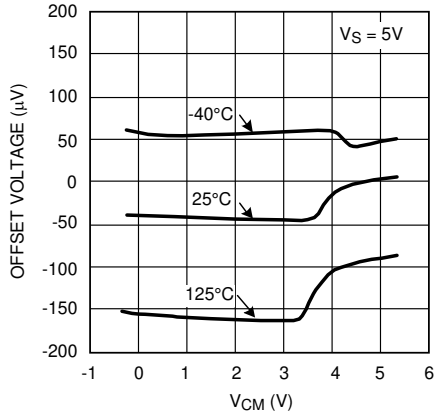


图 6-11. Offset Voltage vs V_{CM}

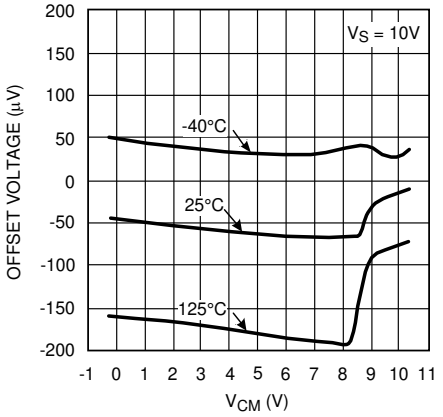


图 6-12. Offset Voltage vs V_{CM}

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_S/2, and R_L > 10 kΩ (unless otherwise noted)

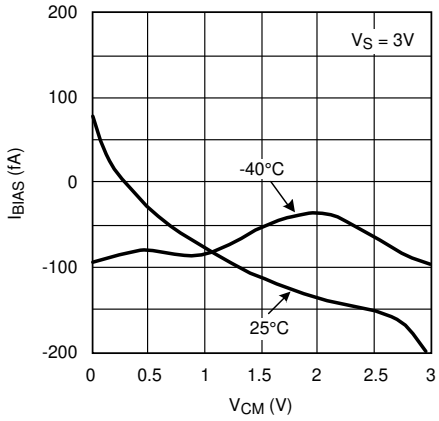


图 6-13. Input Bias Current vs V_{CM}

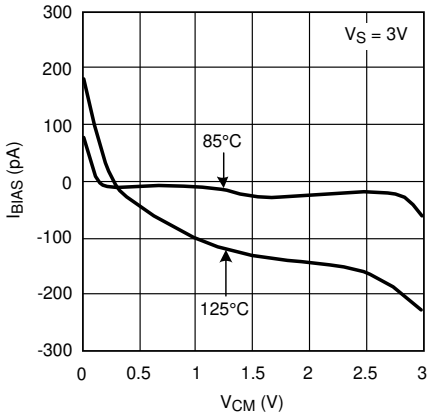


图 6-14. Input Bias Current vs V_{CM}

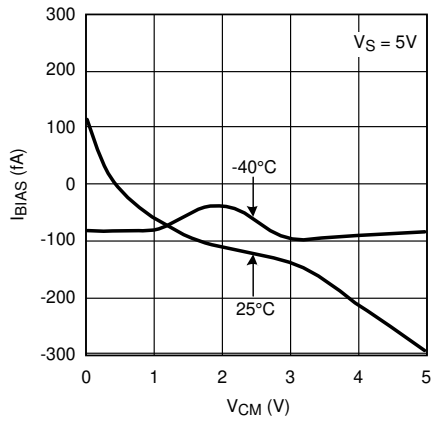


图 6-15. Input Bias Current vs V_{CM}

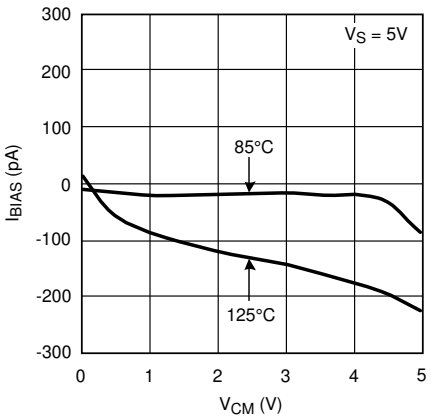


图 6-16. Input Bias Current vs V_{CM}

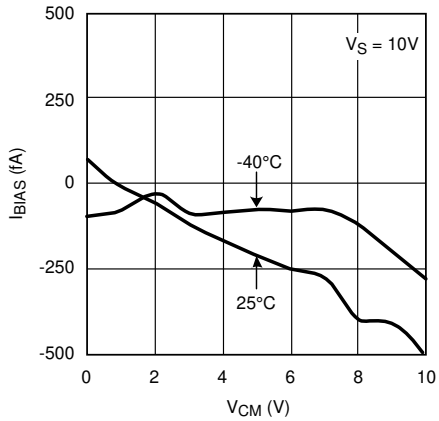


图 6-17. Input Bias Current vs V_{CM}

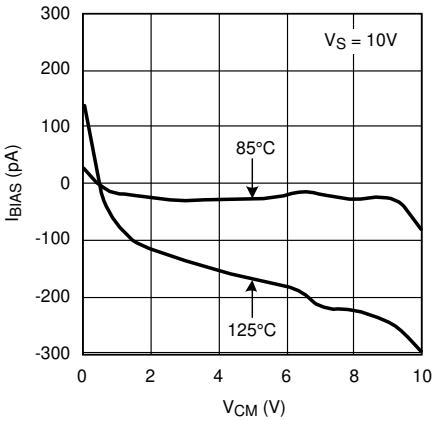


图 6-18. Input Bias Current vs V_{CM}

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_S/2, and R_L > 10 kΩ (unless otherwise noted)

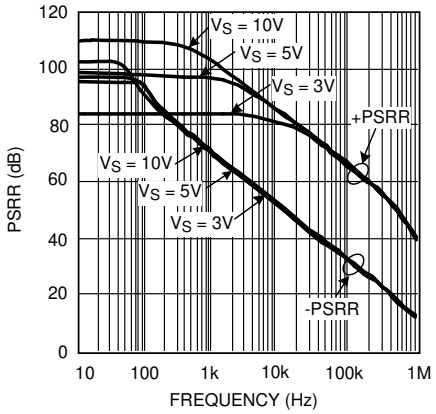


图 6-19. PSRR vs Frequency

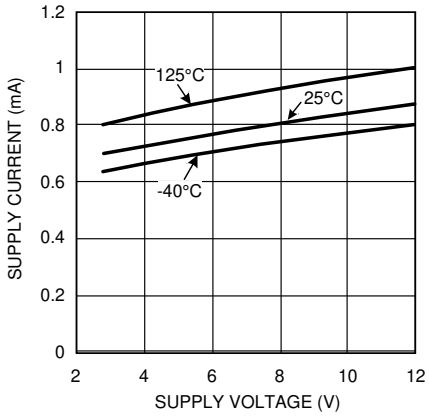


图 6-20. Supply Current vs Supply Voltage (Per Channel)

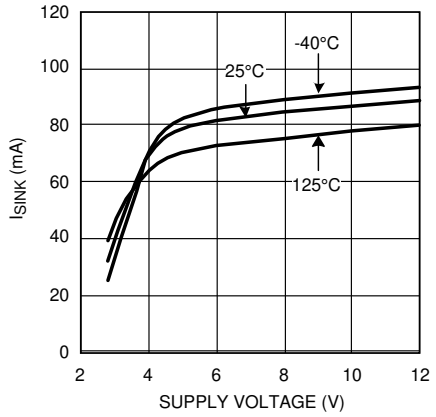


图 6-21. Sinking Current vs Supply Voltage

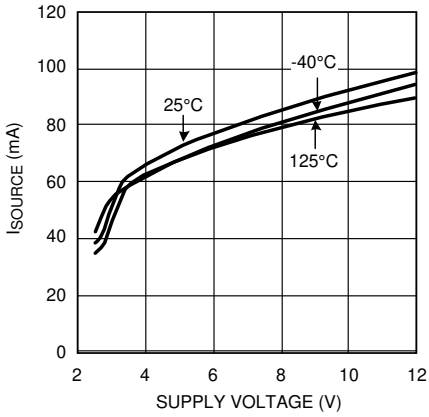


图 6-22. Sourcing Current vs Supply Voltage

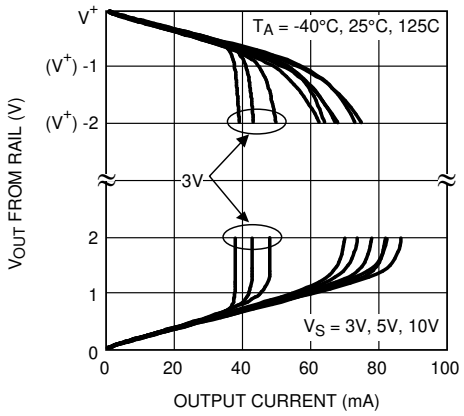


图 6-23. Output Voltage vs Output Current

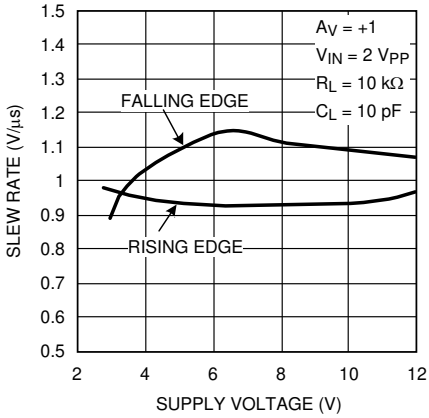


图 6-24. Slew Rate vs Supply Voltage

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_S/2, and R_L > 10 kΩ (unless otherwise noted)

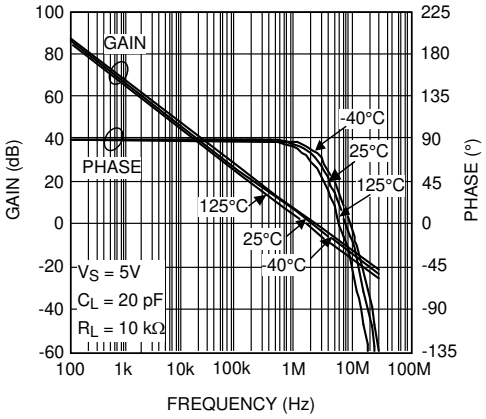


图 6-25. Open-Loop Frequency Response

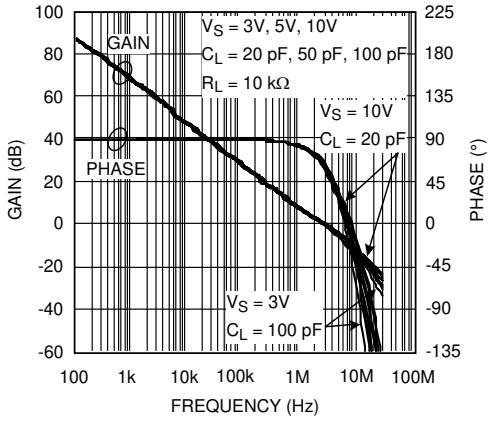


图 6-26. Open-Loop Frequency Response

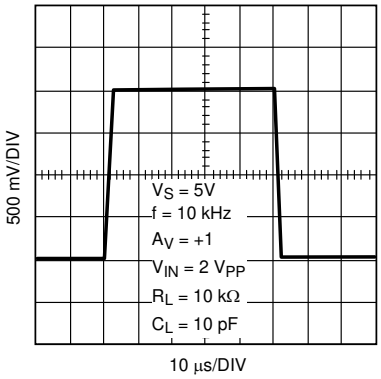


图 6-27. Large Signal Step Response

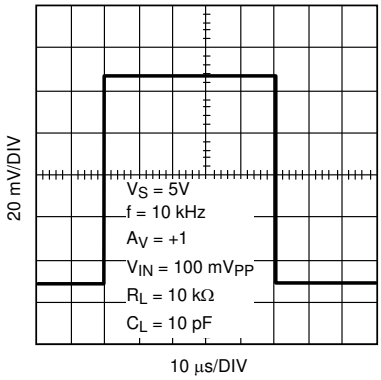


图 6-28. Small Signal Step Response

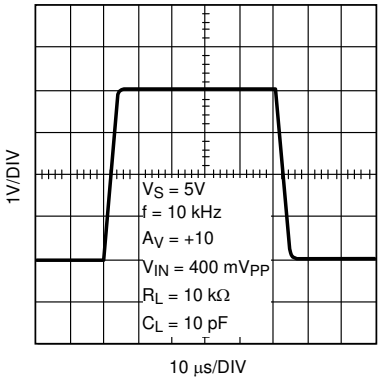


图 6-29. Large Signal Step Response

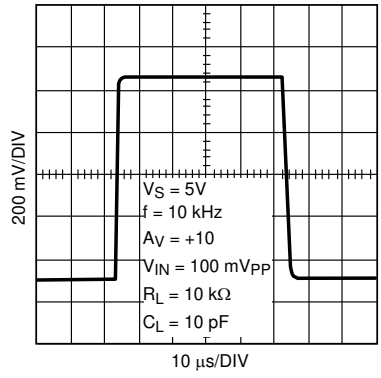


图 6-30. Small Signal Step Response

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_S/2, and R_L > 10 kΩ (unless otherwise noted)

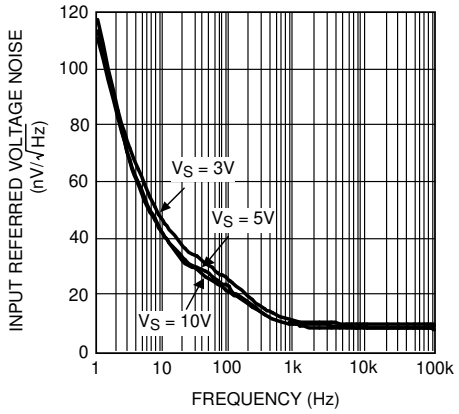


图 6-31. Input Voltage Noise vs Frequency

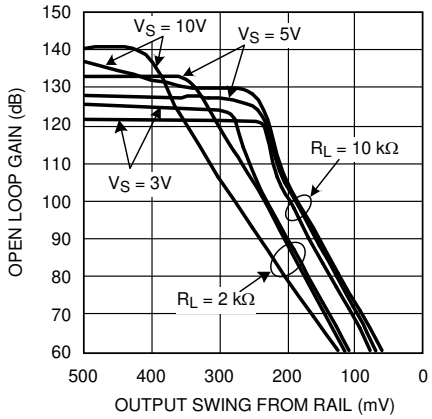


图 6-32. Open Loop Gain vs Output Voltage Swing

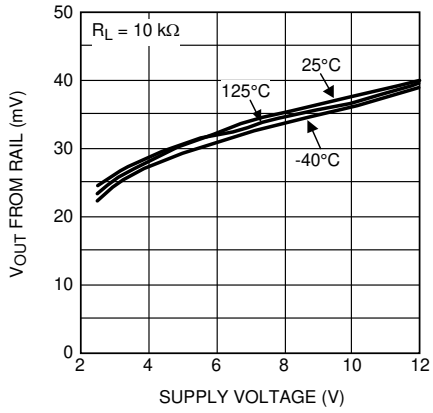


图 6-33. Output Swing High vs Supply Voltage

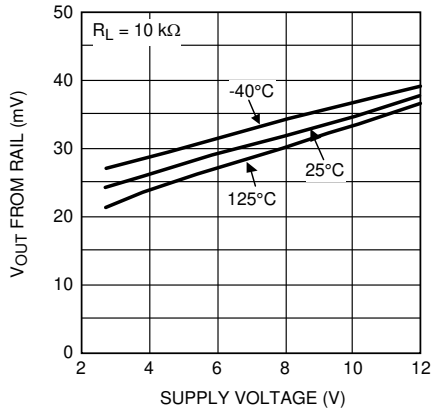


图 6-34. Output Swing Low vs Supply Voltage

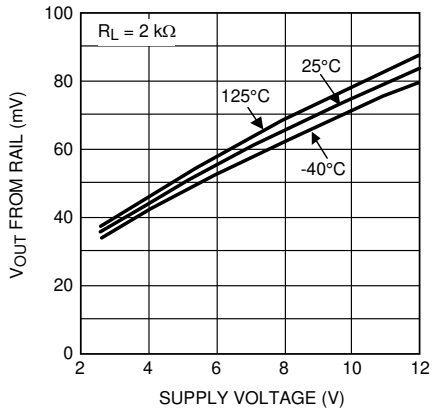


图 6-35. Output Swing High vs Supply Voltage

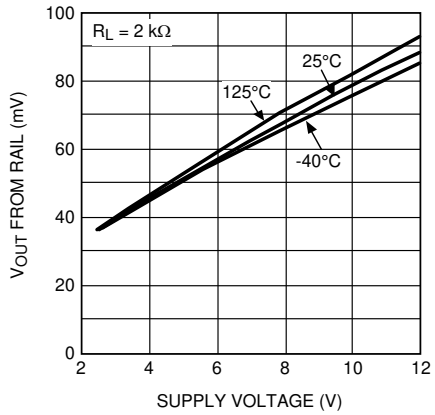


图 6-36. Output Swing Low vs Supply Voltage

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_S/2, and R_L > 10 kΩ (unless otherwise noted)

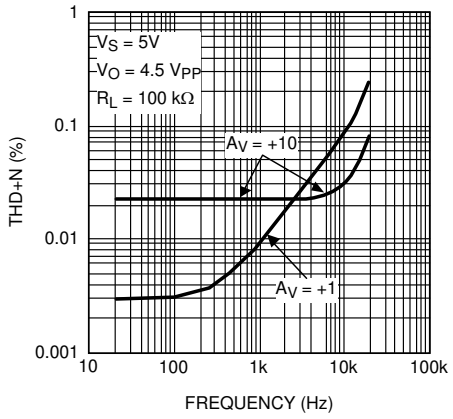


图 6-37. THD+N vs Frequency

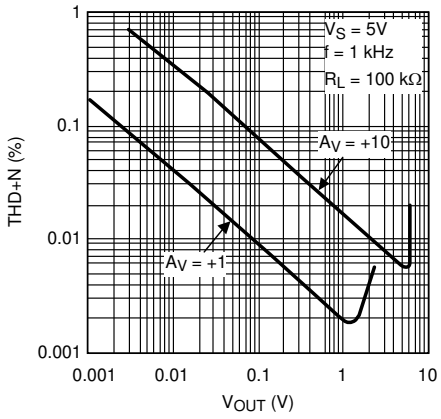


图 6-38. THD+N vs Output Voltage

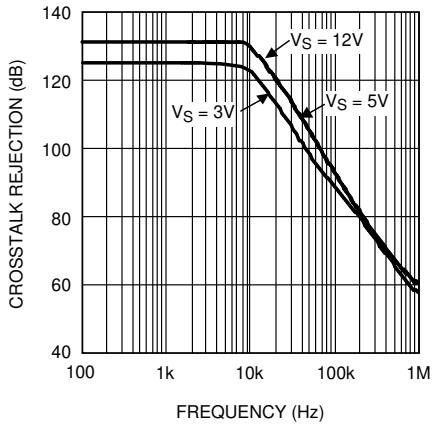


图 6-39. Crosstalk Rejection Ratio vs Frequency (LMP7702/LMP7704)

7 Detailed Description

7.1 Overview

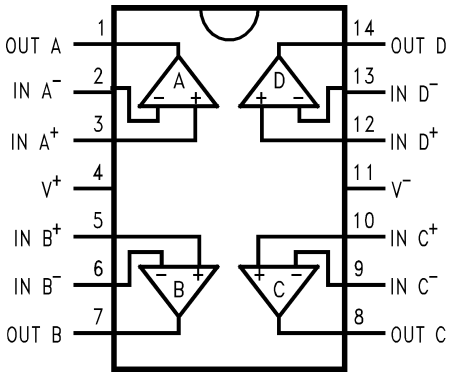
The LMP7704-SP is a radiation-hardened, quad, low offset voltage, rail-to-rail input and output precision amplifier with a CMOS input stage. The LMP7704-SP has a wide supply voltage range of 2.7 V to 12 V and a very low input bias current of only ±500 fA at room temperature.

The wide supply voltage range of 2.7 V to 12 V over the extensive temperature range of −55°C to +125°C makes the LMP7704-SP an excellent choice for low-voltage, precision applications with extensive temperature requirements.

The LMP7704-SP has only ±60 μV of input-referred offset voltage. This offset voltage allows for more accurate signal detection and amplification in precision applications.

The low input bias current of only ±500 fA along with the low input-referred voltage noise of 9 nV/ $\sqrt{\text{Hz}}$ give the LMP7704-SP superiority for use in sensor applications. Lower levels of noise from the LMP7704-SP mean better signal fidelity and a higher signal-to-noise ratio.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Radiation Hardened Performance

Total Ionizing Dose (TID)—The LMP7704-SP is a radiation-hardness-assured (RHA) QML class V (QMLV) product, with a total ionizing dose (TID) level specified in the *Device Information* table on the front page of this data sheet. Testing and qualification of these products is done on a wafer level according to MIL-STD-883, Test Method 1019. Radiation lot acceptance testing (RLAT) is performed at 30-krad, 50-krad, and 100-krad TID levels.

Group E TID RLAT data are available with lot shipments as part of the QCI summary reports; for information on finding QCI summary reports, see *QML Flow, Its Importance, and Obtaining Lot Information*.

Neutron Displacement Damage (NDD)—The LMP7704-SP was irradiated up to 1 × 10^{12} n/cm^2. A sample size of 15 units was exposed to radiation testing per MILSTD-883, Method 1017 for Neutron Irradiation.

Single-Event Effects (SEE)—One-time SEE characterization was performed according to EIA/JEDEC standard, EIA/JEDEC57 to linear energy transfer (LET) = 85 MeV·cm^2/mg. During testing, no single-event latch-up (SEL) was observed.

7.3.2 Engineering Model (Devices With /EM Suffix)

Engineering evaluation or engineering model (EM) devices are available for order and are identified by the */EM* in the orderable device name (see the *Ordering Information* table on the front page of the data sheet). These devices meet the performance specifications of the data sheet at room temperature only and have not received the full space production flow or testing. Engineering samples may be QCI rejects that failed tests that would not impact the performance at room temperature, such as radiation or reliability testing.

7.3.3 Capacitive Load

The LMP7704-SP can be connected as a noninverting unity gain follower. This configuration is the most sensitive to capacitive loading.

The combination of a capacitive load placed on the output of an amplifier along with the amplifier output impedance creates a phase lag, which in turn reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response is either underdamped or oscillated.

To drive heavier capacitive loads, use an isolation resistor, labeled as R_{ISO} in 图 7-1. By using this isolation resistor, the capacitive load is isolated from the amplifier output, and thus, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the output voltage. If values of R_{ISO} are sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

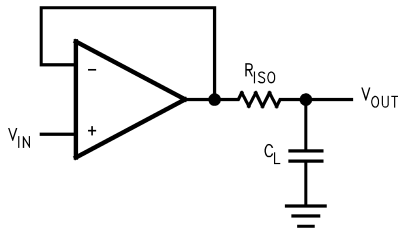


图 7-1. Isolating Capacitive Load

7.3.4 Input Capacitance

CMOS input stages inherently have low input bias current and higher input-referred voltage noise. The LMP7704-SP enhances this performance by having a low input bias current of only ±500 fA, as well as a very low input-referred voltage noise of 9 nV/ √Hz. To achieve these specifications, a larger input stage is used. This larger input stage increases the input capacitance of the LMP7704-SP. The typical value of this input capacitance, C_{IN}, for the LMP7704-SP is 25 pF. The input capacitance interacts with other impedances, such as gain and feedback resistors, which are seen on the inputs of the amplifier, to form a pole. This pole has little or no effect on the output of the amplifier at low frequencies and dc conditions, but plays a bigger role as the frequency increases. At higher frequencies, the presence of this pole decreases phase margin and also causes gain peaking. To compensate for the input capacitance, choose the feedback resistors carefully. In addition to being selective in picking values for the feedback resistor, add a capacitor to the feedback path to increase stability.

The dc gain of the circuit shown in 图 7-2 is simply $-R_2/R_1$.

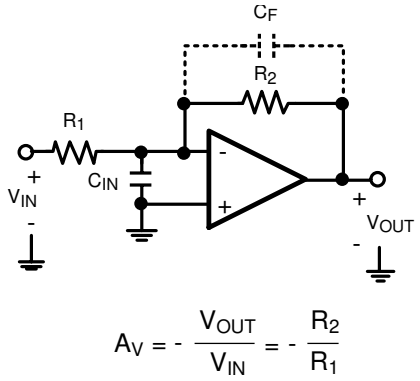


图 7-2. Compensating for Input Capacitance

For the time being, ignore C_F. The ac gain of the circuit in 图 7-2 can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}\right]} \quad (1)$$

This equation is rearranged to find the location of the two poles:

$$P_{1,2} = \frac{-1}{2C_{IN}}\left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4\,A_0 C_{IN}}{R_2}}\right] \quad (2)$$

方程式 2 shows that as values of R_1 and R_2 are increased, the magnitude of the poles is reduced, which in turn decreases the bandwidth of the amplifier. Whenever possible, the best practice is to choose smaller feedback resistors. 图 7-3 shows the effect of the feedback resistor on the bandwidth of the LMP7704-SP.

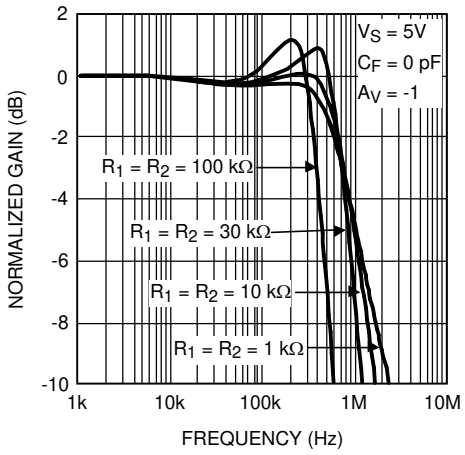


图 7-3. Closed-Loop Gain vs Frequency

方程式 2 has two poles. In most cases, the presence of pairs of poles causes gain peaking. To eliminate this effect, place the poles in a Butterworth position, because poles in a Butterworth position do not cause gain peaking. To achieve a Butterworth pair, set the quantity under the square root in 方程式 2 to equal −1. Using this fact and the relation between R_1 and R_2 ($R_2 = -A_V R_1$), the optimum value for R_1 is found. Use 方程式 3 to calculate the value of R1. If R_1 is larger than this optimum value, gain peaking occurs.

$$R_1 < \frac{(1 - A_V)^2}{2A_0A_VC_{IN}} \tag{3}$$

In 图 7-2, C_F is added to compensate for input capacitance and to increase stability. Additionally, C_F reduces or eliminates the gain peaking that can be caused by having a larger feedback resistor. 图 7-4 shows how C_F reduces gain peaking.

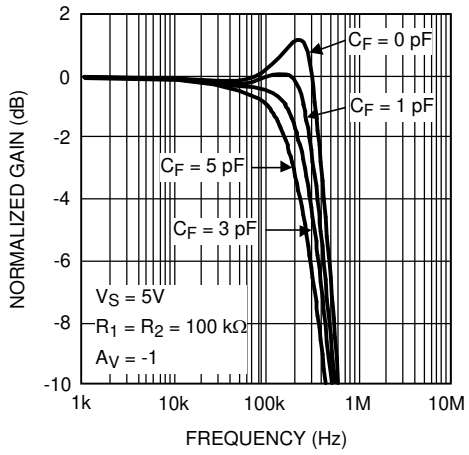


图 7-4. Closed-Loop Gain vs Frequency With Compensation

7.3.5 Diodes Between the Inputs

The LMP7704-SP have a set of anti-parallel diodes between the input pins, as shown in 图 7-5. These diodes are present to protect the input stage of the amplifier. At the same time, the diodes limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than one diode voltage drop might damage the diodes. The differential signal between the inputs must be limited to ±300 mV or the input current must be limited to ±10 mA.

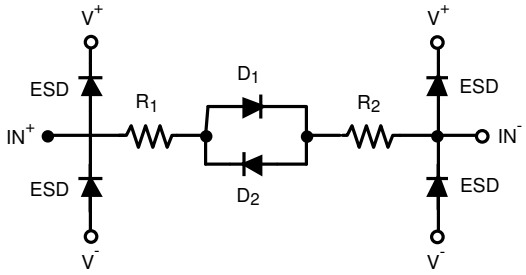


图 7-5. Input of LMP7704-SP

7.4 Device Functional Modes

7.4.1 Precision Current Source

The LMP7704-SP can be used as a precision current source in many different applications. 图 7-6 shows a typical precision current source. This circuit implements a precision, voltage-controlled current source. Amplifier A1 is a differential amplifier that uses the voltage drop across R_S as the feedback signal. Amplifier A2 is a buffer that eliminates the error current from the load side of the R_S resistor. In general, the circuit is stable as long as the closed-loop bandwidth of amplifier A2 is greater then the closed-loop bandwidth of amplifier A1. If A1 and A2 are the same type of amplifiers, then the feedback around A1 reduces bandwidth compared to A2.

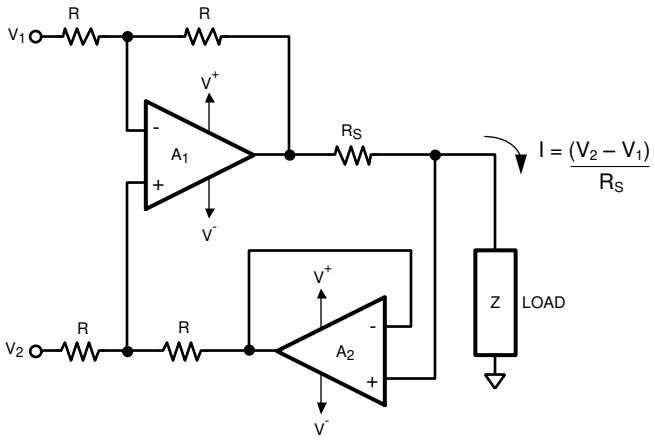


图 7-6. Precision Current Source

The equation for output current is derived as shown in 方程式 4:

$$\frac{V_2 R}{R+R} + \frac{(V_0 - IR_S)R}{R+R} = \frac{V_1 R}{R+R} + \frac{V_0 R}{R+R} \tag{4}$$

Solving for current I results in 方程式 5:

$$I = \frac{V_2 - V_1}{R_S} \tag{5}$$

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 Low Input Voltage Noise

The LMP7704-SP has a very low input voltage noise of 9 nV/ √Hz. This input voltage noise is further reduced by placing N amplifiers in parallel, as shown in 图 8-1. The total voltage noise on the output of this circuit is divided by the square root of the number of amplifiers used in this parallel combination. The reason is because each individual amplifier acts as an independent noise source, and the average noise of independent sources is the quadrature sum of the independent sources divided by the number of sources. For N identical amplifiers:

$$\text{REDUCED INPUT VOLTAGE NOISE} = \frac{1}{N}\sqrt{e_{n1}^2+e_{n2}^2+\cdots+e_{nN}^2}$$

$$= \frac{1}{N}\sqrt{Ne_n^2} = \frac{\sqrt{N}}{N}\ e_n$$

$$= \frac{1}{\sqrt{N}}\ e_n \tag{6}$$

图 8-1 shows a schematic of this input voltage noise reduction circuit. Typical resistor values are:

R_G = 10 Ω, R_F = 1 kΩ, and R_O = 1 kΩ.

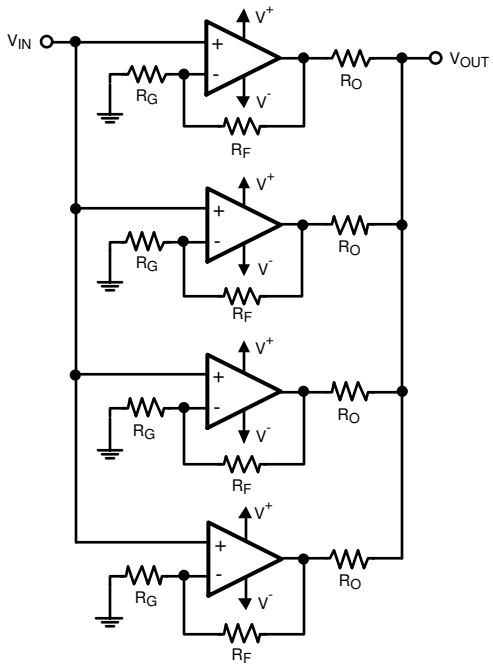


图 8-1. Noise Reduction Circuit

8.1.2 Total Noise Contribution

The LMP7704-SP has a very-low input bias current, very-low input current noise, and very-low input voltage noise. As a result, this amplifier is an excellent choice for circuits with high-impedance sensor applications.

图 8-2 shows the typical input noise of the LMP7704-SP as a function of source resistance where:

- e_n denotes the input-referred voltage noise.
- e_i is the voltage drop across source resistance due to input-referred current noise or $e_i = R_S * i_n$.
- e_t shows the thermal noise of the source resistance.
- e_{ni} shows the total noise on the input, where:

$$e_{ni} = \sqrt{e_n^2 + e_i^2 + e_t^2}$$

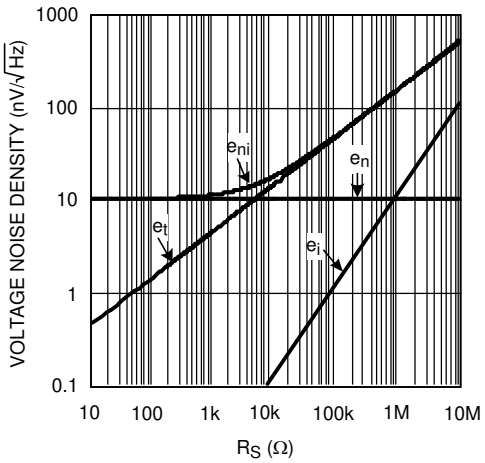


图 8-2. Total Input Noise

The input current noise of the LMP7704-SP is so low that this noise does not become the dominant factor in the total noise unless the source resistance exceeds 300 MΩ, which is an unrealistically high value.

As is evident in 图 8-2, at lower R_S values, total noise is dominated by the amplifier input voltage noise. If R_S is larger than a few kilo-ohms, then the dominant noise factor becomes the thermal noise of R_S. As mentioned previously, the current noise will not be the dominant noise factor for any practical application.

8.2 Typical Application

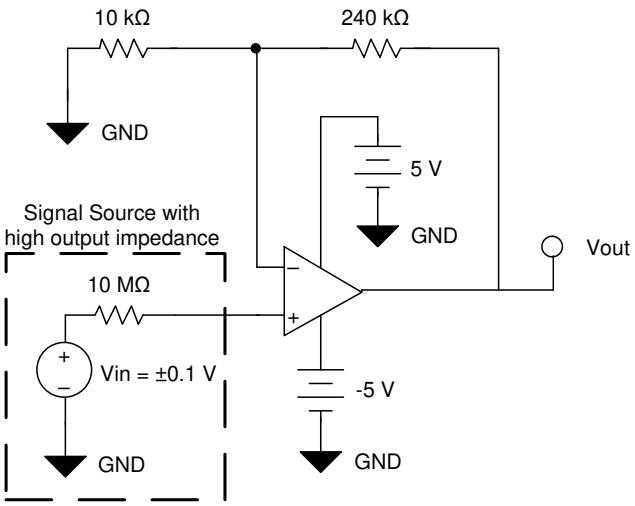


图 8-3. LMP7704-SP Configured for 25x Gain With High Signal Source Impedance

8.2.1 Design Requirements

Many precision analog sensors, such as temperature or pressure (bridge) sensors, require a high-precision amplifier with low input bias to condition the signal before the analog-to-digital converter. The LMP7704-SP is an excellent amplifier choice for a voltage gain stage thanks to the low offset voltage, offset voltage drift, and ultra-low input bias current.

8.2.2 Detailed Design Procedure

Many sensors have high source impedances that may range up to 10 MΩ. The output signal of sensors must often be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in 图 8-4, where $V_{IN+} = V_S - I_{BIAS} * R_S$.

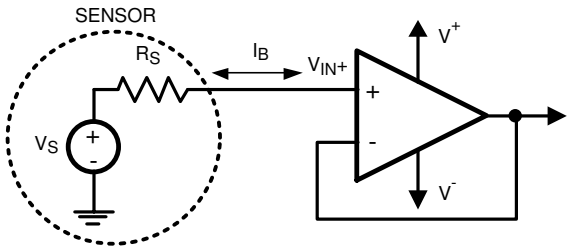


图 8-4. Offset Error Due to I_{BIAS}

The last term, $I_{BIAS} * R_S$, shows the voltage drop across R_S. To prevent errors introduced to the system due to this voltage, an op amp with very low input bias current must be used with high impedance sensors. An amplifier with low input bias also has low input current noise, further improving the accuracy of systems with high source resistance.

图 8-3 shows one channel of the LMP7704-SP configured for a gain of 25. A high source impedance is placed between the input signal and the noninverting input of the amplifier to represent the output impedance of the sensor.

With the ultra-low input bias current of the LMP7704-SP, even with a signal source that has high output impedance, the system output maintains very good linearity to the ideal output voltage (that is, the output of an ideal amplifier in the same configuration). 图 8-5 shows the output voltage vs input voltage of the LMP7704-SP with a 10-MΩ source impedance. 图 8-6 shows the output voltage vs input voltage for an ideal amplifier with no

input bias current. Comparing the two graphs shows that the LMP7704-SP maintains high accuracy even with a large source impedance connected to an input.

8.2.3 Application Curves

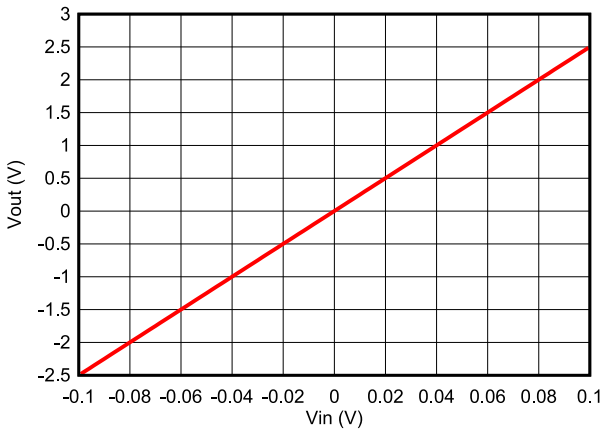


图 8-5. LMP7704-SP Output Voltage vs Input Voltage

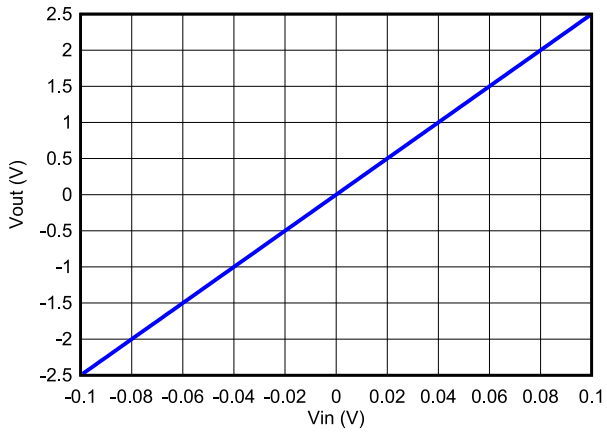


图 8-6. LMP7704-SP Ideal Output Voltage vs Input Voltage

9 Power Supply Recommendations

For proper operation, the power supplies must be decoupled. To decouple the supply, place 10-nF to 1-µF capacitors as close as possible to the operational-amplifier power-supply pins. For single-supply configurations, place a capacitor between the V^+ and V^- supply pins. For dual-supply configurations, place one capacitor between V^+ and ground, and place a second capacitor between V^- and ground. Bypass capacitors must have a low ESR of less than 0.1 Ω.

10 Layout

10.1 Layout Guidelines

Take care to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. Use a ground plane underneath the device; best practice is for any bypass components to ground to have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins lowers the power-supply inductance and provides a more stable power supply.

To minimize stray parasitics, place the feedback components as close as possible to the device.

10.2 Layout Example

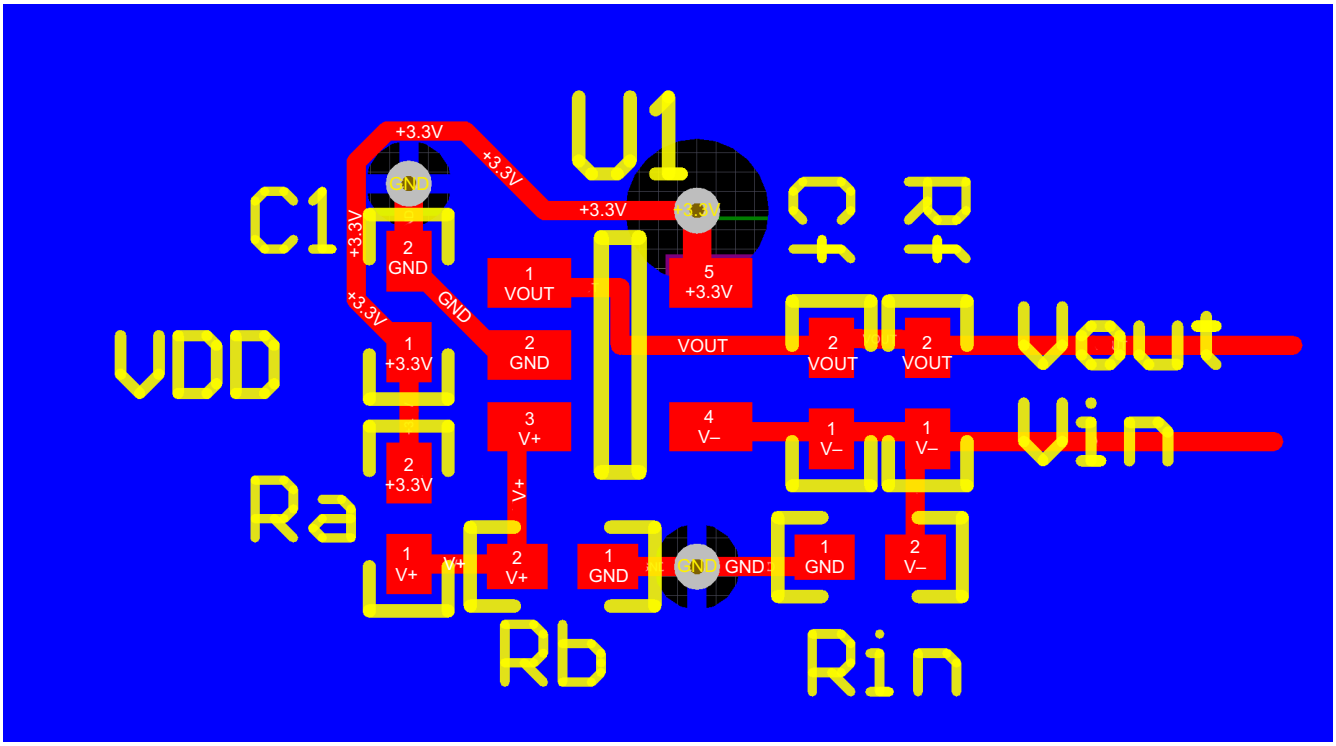


图 10-1. LMP7704-SP Example Layout for a Single Channel

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

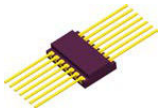
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

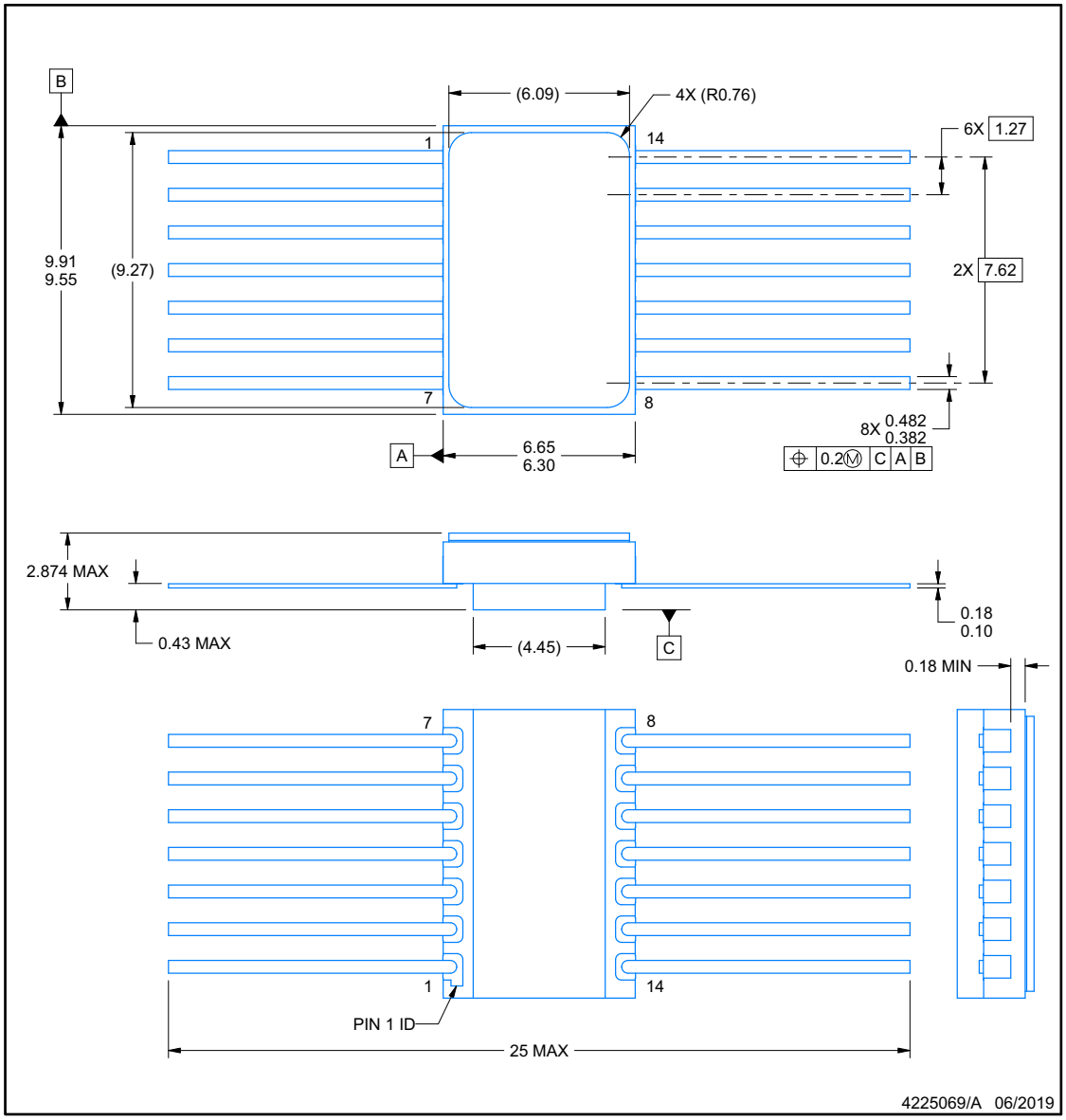


PACKAGE OUTLINE

HBH0014A

CFP - 2.874 mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R1920601VXC	ACTIVE	CFP	HBH	14	25	RoHS & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R1920601VXC LMP7704	Samples
LMP7704HBH/EM	ACTIVE	CFP	HBH	14	25	RoHS & Green	NIAU	N / A for Pkg Type	-55 to 125	LMP7704HBH/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

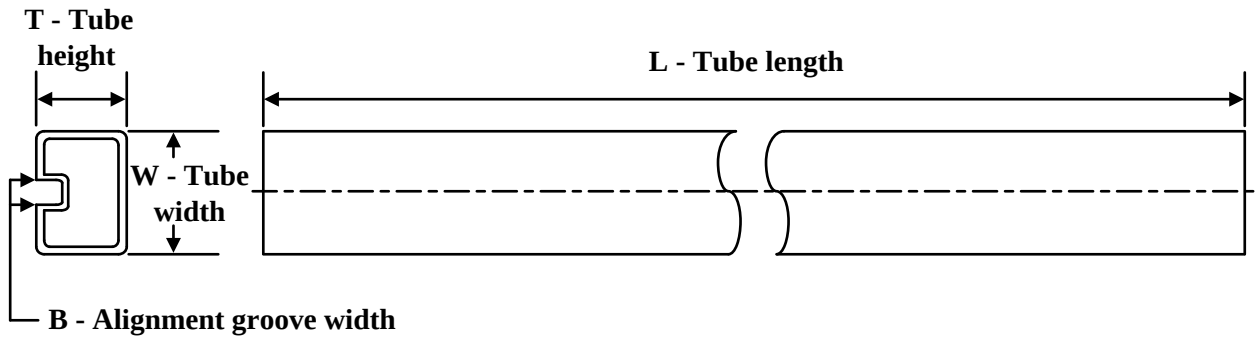
OTHER QUALIFIED VERSIONS OF LMP7704-SP :

- Catalog : LMP7704

NOTE: Qualified Version Definitions:

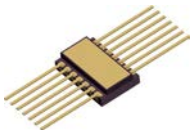
- Catalog - TI's standard catalog product

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R1920601VXC	HBH	CFP	14	25	506.98	26.16	6220	NA
LMP7704HBH/EM	HBH	CFP	14	25	506.98	26.16	6220	NA

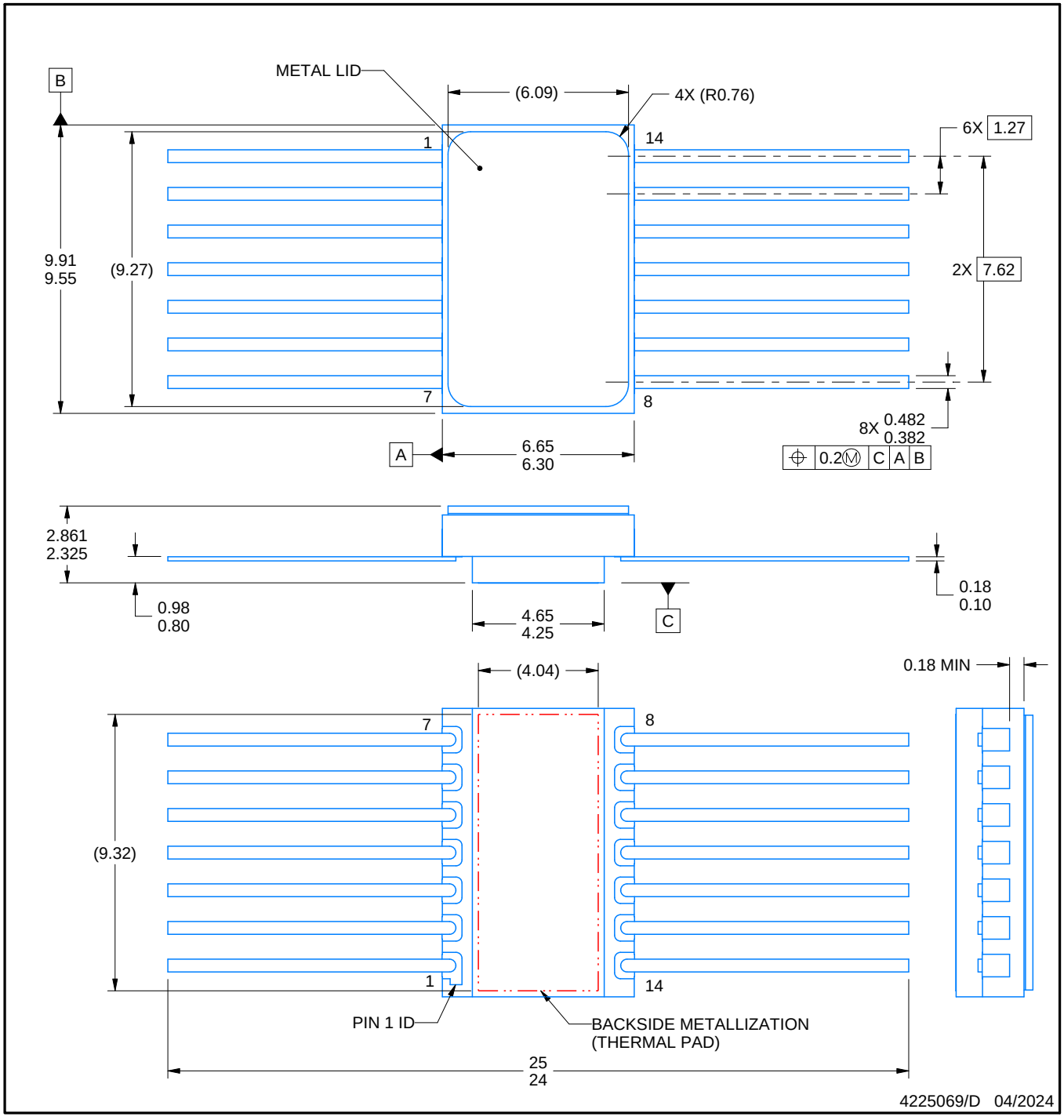


PACKAGE OUTLINE

HBH0014A

CFP - 2.861 mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metalization.

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