

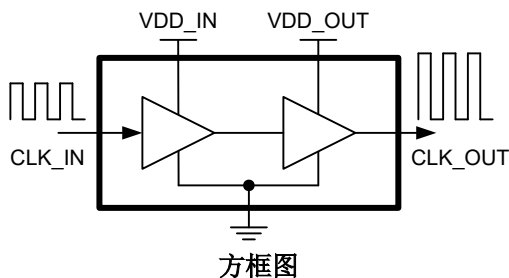
## CDCBT1001 1.2V 至 1.8V 时钟缓冲器和电平转换器

## 1 特性

- 时钟频率范围：DC 到 24 MHz
- 1.2V 至 1.8V LVCMOS 时钟电平转换：
  - $VDD\_IN = 1.2V \pm 10\%$
  - $VDD\_OUT = 1.8V \pm 10\%$
- 低附加抖动和低相位噪声：
  - 最大 0.8ps 的 12kHz 至 5MHz 附加 RMS 抖动 ( $f_{out} = 24MHz$ )
  - 发生 1kHz 偏移时的最大相位噪声为 -120dBc/Hz ( $f_{out} = 24MHz$ )
  - 最大相位本底噪声为 -148dBc/Hz ( $f_{out} = 24MHz$ ,  $f_{offset} \geq 1MHz$ )
- 在 20% 至 80% 条件下具有 5ns 的上升/下降时间
- 10ns 传播延迟
- 低电流消耗
- 工作温度范围：-40°C 至 85°C

## 2 应用

- 个人电子产品中的 FPGA/处理器时钟缓冲/电平转换
- 服务器和附加卡中的 1.2V 时钟缓冲器和电平转换器



## 3 说明

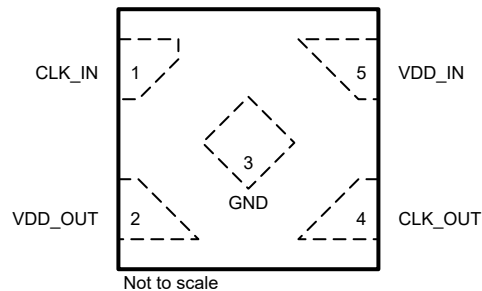
CDCBT1001 是 1.2V 至 1.8V 时钟缓冲器和电平转换器。VDD\_IN 引脚电源电压定义了输入 LVCMOS 时钟的电平。VDD\_OUT 引脚电源电压定义了输出 LVCMOS 时钟的电平。VDD\_IN = 1.2V  $\pm$  10%。VDD\_OUT = 1.8V  $\pm$  10%。

24MHz 下的 12kHz 至 5MHz 附加 RMS 抖动小于 0.8ps。

## 器件信息

| 器件型号      | 封装 <sup>(1)</sup> | 封装尺寸 (标称值)             |
|-----------|-------------------|------------------------|
| CDCBT1001 | X2SON (5)         | 0.80mm $\times$ 0.80mm |

- (1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| DATE     | REVISION | NOTES           |
|----------|----------|-----------------|
| May 2022 | *        | Initial Release |

## 5 Pin Configuration and Functions

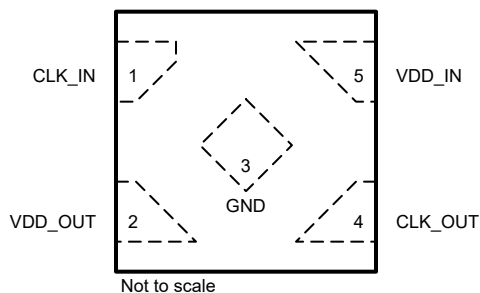


图 5-1. DPW Package 5-Pin X2SON Transparent Top View

表 5-1. Pin Functions

| PIN     |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                          |
|---------|-----|---------------------|----------------------------------------------------------------------------------------------------------------------|
| NAME    | NO. |                     |                                                                                                                      |
| CLK_IN  | 1   | I                   | Clock input. LVCMOS input clock is injected into this pin. The acceptable LVCMOS voltage level is defined by VDD_IN. |
| CLK_OUT | 4   | O                   | Clock output. This pin outputs LVCMOS clock. The output LVCMOS voltage level is defined by VDD_OUT                   |
| VDD_IN  | 5   | P                   | Input supply voltage. $1.08\text{ V} \leq \text{VDD\_IN} \leq 1.32\text{ V}$ .                                       |
| VDD_OUT | 2   | P                   | Output supply voltage. $1.62\text{ V} \leq \text{VDD\_OUT} \leq 1.98\text{ V}$ .                                     |
| GND     | 3   | G                   | Ground                                                                                                               |

(1) I = Input, O = Output, P = Power, G = Ground

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                                                       | MIN   | MAX           | UNIT |
|------------------|---------------------------------------------------------------------------------------|-------|---------------|------|
| VDD_IN           | VDD_IN supply voltage                                                                 | – 0.5 | 1.5           | V    |
| VDD_OUT          | VDD_OUT supply voltage                                                                | – 0.5 | 2.25          | V    |
| V <sub>I</sub>   | Input voltage <sup>(2)</sup>                                                          | – 0.5 | 1.5           | V    |
| V <sub>O</sub>   | Voltage applied to the output in the high-impedance or power-off state <sup>(2)</sup> | – 0.5 | 2.25          | V    |
|                  | Voltage applied to the output in the high or low state <sup>(2) (3)</sup>             | – 0.5 | VDD_OUT + 0.2 | V    |
| I <sub>IK</sub>  | Input clamp current, V <sub>I</sub> < 0                                               |       | – 50          | mA   |
| I <sub>OK</sub>  | Output clamp current, V <sub>O</sub> < 0                                              |       | – 50          | mA   |
| I <sub>O</sub>   | Continuous output current                                                             | – 50  | 50            | mA   |
|                  | Continuous current through VDD_OUT or GND                                             | – 50  | 50            | mA   |
| I <sub>O</sub>   | Continuous current through VDD_IN                                                     | – 10  | 10            | mA   |
| T <sub>J</sub>   | Junction temperature                                                                  | – 40  | 150           | °C   |
| T <sub>stg</sub> | Storage temperature                                                                   | – 65  | 150           | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 2.25 V maximum if the output current ratings are observed.

### 6.2 ESD Ratings

|                    |                         |                                                                                     | VALUE | UNIT | OWNER |
|--------------------|-------------------------|-------------------------------------------------------------------------------------|-------|------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>         | ±2000 | V    |       |
|                    |                         | Charged device model (CDM), per JEDEC specification JS-002, all pins <sup>(2)</sup> | ±1000 | V    |       |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                |                       | MIN  | NOM | MAX  | UNIT |
|----------------|-----------------------|------|-----|------|------|
| VDD_IN         | Input supply voltage  | 1.08 |     | 1.32 | V    |
| VDD_OUT        | Output supply voltage | 1.62 |     | 1.98 | V    |
| T <sub>A</sub> | Ambient temperature   | – 40 |     | 85   | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                           | CDCBT1001   | UNIT |
|-------------------------------|-------------------------------------------|-------------|------|
|                               |                                           | DPW (X2SON) |      |
|                               |                                           | 5 PINS      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance    | 462.7       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance | 227.7       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance      | 326.5       | °C/W |

| THERMAL METRIC <sup>(1)</sup> |                                              | CDCBT1001   | UNIT |
|-------------------------------|----------------------------------------------|-------------|------|
|                               |                                              | DPW (X2SON) |      |
|                               |                                              | 5 PINS      |      |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 33.8        | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 325.1       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

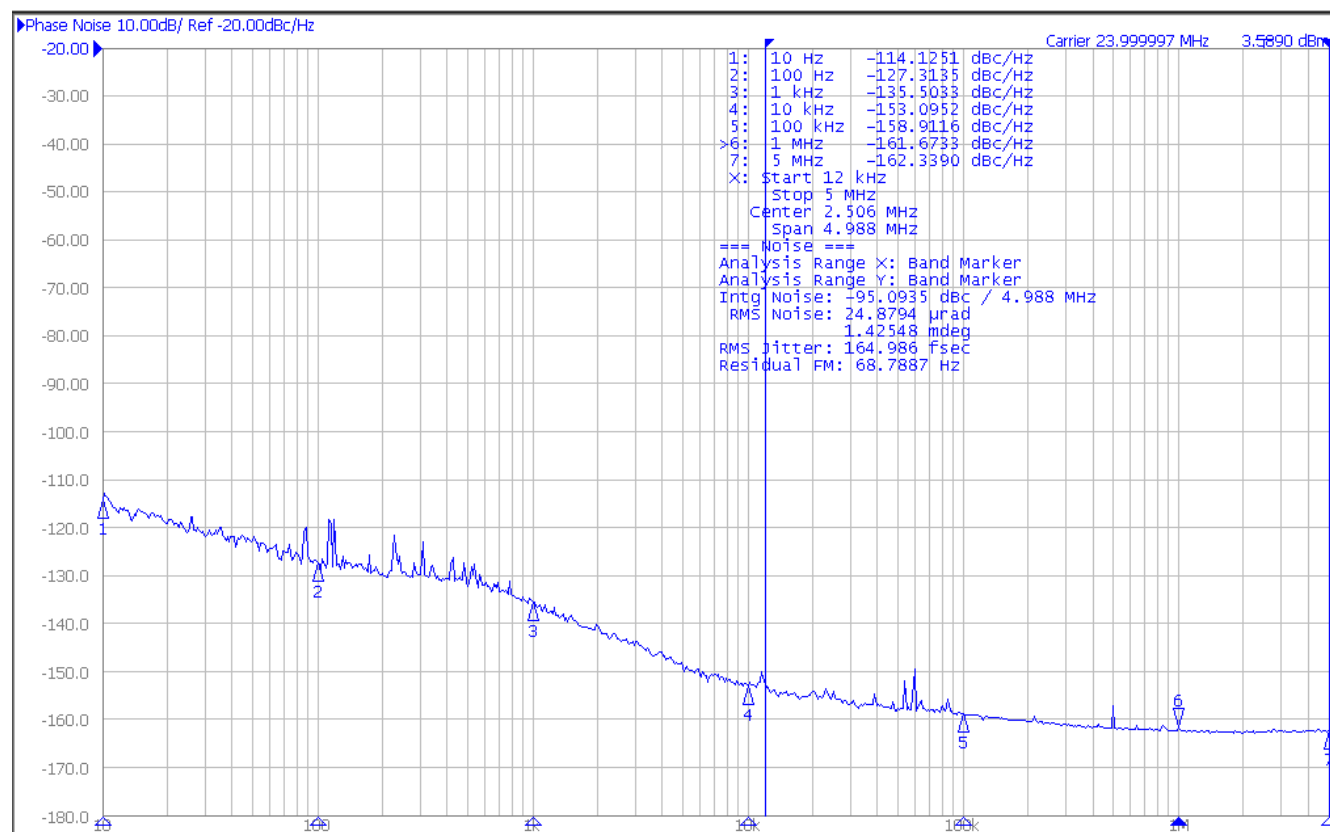
over operating free-air temperature range (unless otherwise noted)

| PARAMETER                       |                                                                                                | TEST CONDITIONS                                                                                                                                                          | MIN           | TYP | MAX  | UNIT |
|---------------------------------|------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-----|------|------|
| POWER SUPPLY CHARACTERISTICS    |                                                                                                |                                                                                                                                                                          |               |     |      |      |
| IDD_IN                          | Current consumption on VDD_IN                                                                  | Both input and output clocks are toggling. 2 pF load termination. f <sub>0</sub> = 12 MHz.                                                                               |               |     | 35   | μA   |
|                                 |                                                                                                | Both input and output clocks are toggling. 2 pF load termination. f <sub>0</sub> = 24 MHz.                                                                               |               |     | 60   | μA   |
| IDD_OUT                         | Current consumption on VDD_OUT                                                                 | Both input and output clocks are toggling. 2 pF load termination. f <sub>0</sub> = 12 MHz.                                                                               |               |     | 500  | μA   |
|                                 |                                                                                                | Both input and output clocks are toggling. 2 pF load termination. f <sub>0</sub> = 24 MHz.                                                                               |               |     | 1000 | μA   |
| CLOCK INPUT CHARACTERISTICS     |                                                                                                |                                                                                                                                                                          |               |     |      |      |
| f <sub>0</sub>                  | Operating frequency                                                                            |                                                                                                                                                                          | DC            |     | 24   | MHz  |
| I <sub>IN_LEAK</sub>            | Input leakage current                                                                          |                                                                                                                                                                          | - 8           |     | 8    | μA   |
| V <sub>IH</sub>                 | Input voltage high                                                                             |                                                                                                                                                                          | VDD_IN x 0.8  |     |      | V    |
| V <sub>IL</sub>                 | Input voltage low                                                                              |                                                                                                                                                                          | VDD_IN x 0.2  |     |      | V    |
| Δv/Δt                           | Input edge rate                                                                                |                                                                                                                                                                          | 0.01          |     |      | V/ns |
| C <sub>I</sub>                  | Input capacitance                                                                              |                                                                                                                                                                          |               |     | 2    | pF   |
| t <sub>startup</sub>            | Time after power supply exceeds 0.5 V before applying input clock, to ensure glitchless output |                                                                                                                                                                          |               |     | 225  | us   |
| CLOCK OUTPUT CHARACTERISTICS    |                                                                                                |                                                                                                                                                                          |               |     |      |      |
| V <sub>OH</sub>                 | Output voltage high                                                                            | V <sub>I</sub> = V <sub>IH</sub> , I <sub>OH</sub> = -100 μA, VDD_OUT = 1.62-1.98 V                                                                                      | VDD_OUT - 0.1 |     |      | V    |
| V <sub>OH</sub>                 | Output voltage high                                                                            | V <sub>I</sub> = V <sub>IH</sub> , I <sub>OH</sub> = -8 mA, VDD_OUT = 1.62 V                                                                                             | 1.2           |     |      | V    |
| V <sub>OL</sub>                 | Output voltage low                                                                             | V <sub>I</sub> = V <sub>IL</sub> , I <sub>OL</sub> = 100 μA, VDD_OUT = 1.62-1.98 V                                                                                       |               |     | 0.1  | V    |
| V <sub>OL</sub>                 | Output voltage low                                                                             | V <sub>I</sub> = V <sub>IL</sub> , I <sub>OL</sub> = 8 mA, VDD_OUT = 1.62 V                                                                                              |               |     | 0.45 | V    |
| ODC                             | Output duty cycle                                                                              | Input duty cycle = 45% - 55%, input slew rate ≥ 0.2 V/ns, V <sub>IL</sub> ≤ 0.15 * VDD_IN, V <sub>IH</sub> ≥ 0.85 * VDD_IN, V <sub>IH</sub> - V <sub>IL</sub> ≥ 850 mVpp | 40            |     | 60   | %    |
|                                 |                                                                                                | Input duty cycle = 45% - 55%, input slew rate ≥ 0.2 V/ns, V <sub>IL</sub> ≤ 0.2 * VDD_IN, V <sub>IH</sub> ≥ 0.8 * VDD_IN, V <sub>IH</sub> - V <sub>IL</sub> ≥ 850 mVpp   | 37            |     | 63   | %    |
| t <sub>R</sub> , t <sub>F</sub> | Clock output rise/fall time                                                                    | 20% to 80%, 2 pF load capacitance                                                                                                                                        |               |     | 3    | ns   |
| t <sub>PD</sub>                 | Input-to-output propagation delay                                                              | Input slew rate ≥ 0.2 V/ns, V <sub>IL</sub> ≤ 0.2 * VDD_IN, V <sub>IH</sub> ≥ 0.8 * VDD_IN, V <sub>IH</sub> - V <sub>IL</sub> ≥ 850 mVpp                                 |               |     | 10   | ns   |
| R <sub>out</sub>                | Output impedance                                                                               |                                                                                                                                                                          | 34            |     |      | Ω    |
| CLOCK OUTPUT PERFORMANCE        |                                                                                                |                                                                                                                                                                          |               |     |      |      |

over operating free-air temperature range (unless otherwise noted)

| PARAMETER             |                                            | TEST CONDITIONS                                                                                                   | MIN | TYP | MAX   | UNIT   |
|-----------------------|--------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-----|-----|-------|--------|
| RJ <sub>RMS-ADD</sub> | 12 kHz to 5 MHz additive RMS random jitter | $f_0 = 24$ MHz, input slew rate $\geq 0.2$ V/ns, $V_{IH} - V_{IL} \geq 850$ mVpp                                  |     |     | 0.8   | ps     |
| PN <sub>10</sub>      | Output phase noise @10 Hz                  | $f_0 = 24$ MHz, input phase noise = -104 dBc/Hz, input slew rate $\geq 0.2$ V/ns, $V_{IH} - V_{IL} \geq 850$ mVpp |     |     | - 100 | dBc/Hz |
| PN <sub>100</sub>     | Output phase noise @100 Hz                 | $f_0 = 24$ MHz, input phase noise = -127 dBc/Hz, input slew rate $\geq 0.2$ V/ns, $V_{IH} - V_{IL} \geq 850$ mVpp |     |     | - 110 | dBc/Hz |
| PN <sub>1k</sub>      | Output phase noise @1 kHz                  | $f_0 = 24$ MHz, input phase noise = -137 dBc/Hz, input slew rate $\geq 0.2$ V/ns, $V_{IH} - V_{IL} \geq 850$ mVpp |     |     | - 120 | dBc/Hz |
| PN <sub>10k</sub>     | Output phase noise @10 kHz                 | $f_0 = 24$ MHz, input phase noise = -159 dBc/Hz, input slew rate $\geq 0.2$ V/ns, $V_{IH} - V_{IL} \geq 850$ mVpp |     |     | - 130 | dBc/Hz |
| PN <sub>100k</sub>    | Output phase noise @100 kHz                | $f_0 = 24$ MHz, input phase noise = -164 dBc/Hz, input slew rate $\geq 0.2$ V/ns, $V_{IH} - V_{IL} \geq 850$ mVpp |     |     | - 140 | dBc/Hz |
| PN <sub>1M</sub>      | Output phase noise @1 MHz                  | $f_0 = 24$ MHz, input phase noise = -166 dBc/Hz, input slew rate $\geq 0.2$ V/ns, $V_{IH} - V_{IL} \geq 850$ mVpp |     |     | - 148 | dBc/Hz |
| PN <sub>5M</sub>      | Output phase noise @5 MHz                  | $f_0 = 24$ MHz, input phase noise = -165 dBc/Hz, input slew rate $\geq 0.2$ V/ns, $V_{IH} - V_{IL} \geq 850$ mVpp |     |     | - 148 | dBc/Hz |

## 6.6 Typical Characteristics



VDD\_IN = 1.2 V, VDD\_OUT = 1.8 V, T<sub>A</sub> = 25 °C,

Input phase noise as specified in *Electrical Characteristics* table

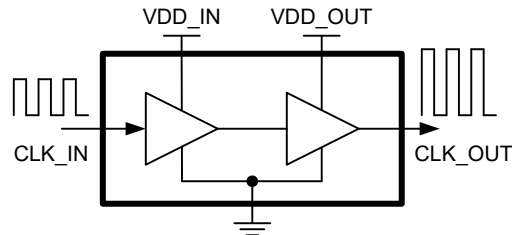
图 6-1. 24-MHz Phase Noise

## 7 Detailed Description

### 7.1 Overview

The CDCBT1001 is a single-channel, 1.2-V to 1.8-V clock buffer and level translator. VDD\_IN defines input LVCMOS clock level and VDD\_OUT defines output LVCMOS clock level.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Power Down Tolerant Input

The device can have a clock signal on the input pin when the chip is powered down.

#### 7.3.2 Up Conversion

The device supports 1.2-V to 1.8-V up conversion.

### 7.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

## 8 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The CDCBT1001 device can be used in level-translation applications for interfacing between devices or systems that are operating at different interface voltages.

### 8.2 Typical Applications

#### 8.2.1 Processor Clock Up Translation

图 8-1 shows an example of CDCBT1001 being used in a clock level shifting application.

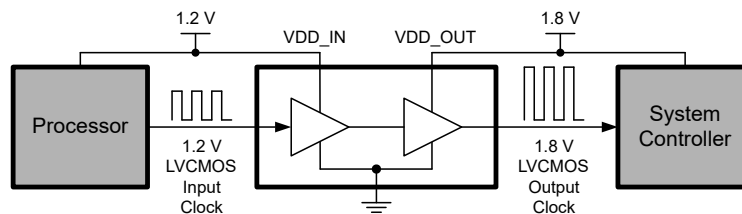


图 8-1. Processor Clock Up Translation Application

##### 8.2.1.1 Design Requirements

For this design example, use the parameters shown in 表 8-1.

表 8-1. Design Parameters

| DESIGN PARAMETER      | EXAMPLE VALUE |
|-----------------------|---------------|
| Input voltage supply  | 1.2 V         |
| Output voltage supply | 1.8 V         |

##### 8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input clock
  - The supply voltage on VDD\_IN will determine the input clock voltage range.
  - For a valid logic-high, the high level clock input must exceed  $V_{IH}$  spec. For a valid logic-low, the low level clock input must be below  $V_{IL}$ .
  - Some specifications such as duty cycle and phase noise have additional requirements for  $V_{IH}$ ,  $V_{IL}$ , input swing and input slew rate. Refer to the test conditions column in the *Electrical Characteristics* table.
- Output clock
  - The supply voltage on VDD\_OUT will determine the output clock voltage range.

##### 8.2.1.3 Application Curve

图 6-1 listed in the *Typical Characteristics* section can also be used as an application curve for the *Processor Clock Up Translation* application example.

表 8-2. Table of Graphs

| TITLE              | FIGURE                |
|--------------------|-----------------------|
| 24-MHz Phase Noise | <a href="#">图 6-1</a> |

## 9 Power Supply Recommendations

TI recommends to place a 0.1- $\mu$ F bypass capacitor on each VDD pin.

## 10 Layout

### 10.1 Layout Guidelines

To ensure reliability of the device, follow the common printed-circuit board layout guidelines listed below:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.

图 10-1 shows an example layout for the DPW (X2SON-5) package. This example layout includes two 0402 (metric) capacitors, and uses the measurements listed in the package outline drawing appended to the end of this data sheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or the via can be left out of the layout.

### 10.2 Layout Example

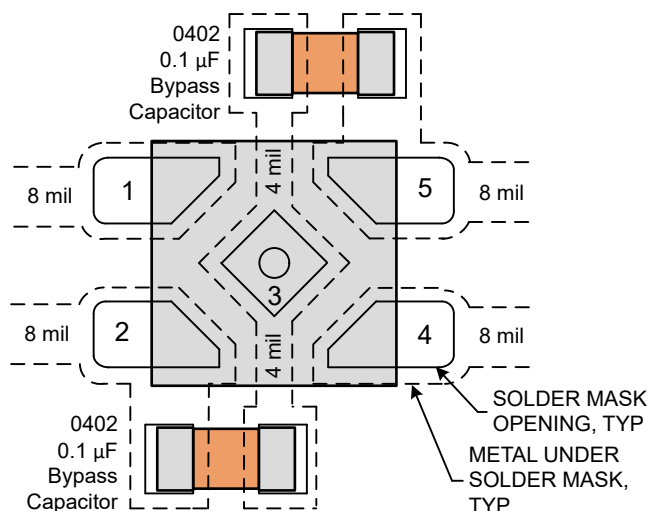


图 10-1. Example Layout for the DPW (X2SON-5) Package

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#) application report
- Texas Instruments, [Designing and Manufacturing with TI's X2SON Packages](#) application report

#### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

#### 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

#### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CDCBT1001DPWR    | ACTIVE        | X2SON        | DPW                | 5    | 3000           | RoHS & Green    | NIPDAUAG                             | Level-1-260C-UNLIM   | -40 to 85    | BT                      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## GENERIC PACKAGE VIEW

**DPW 5**

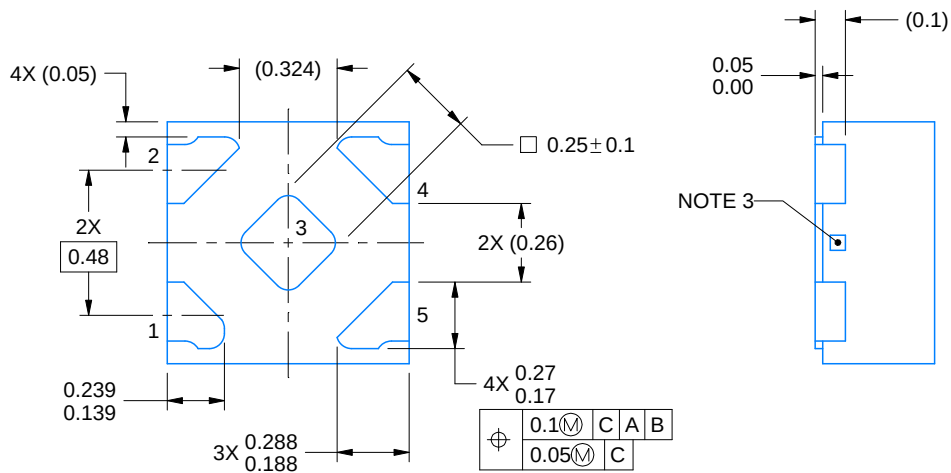
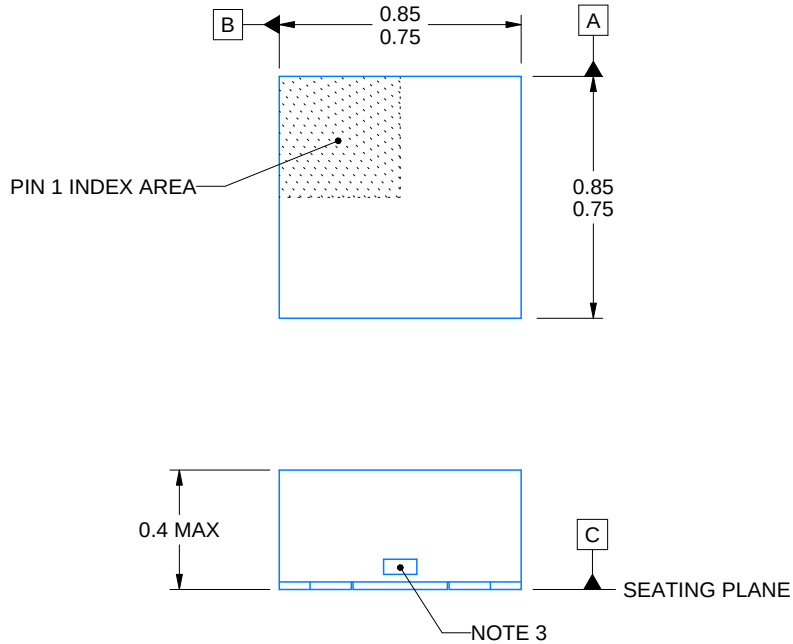
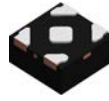
**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211218-3/D



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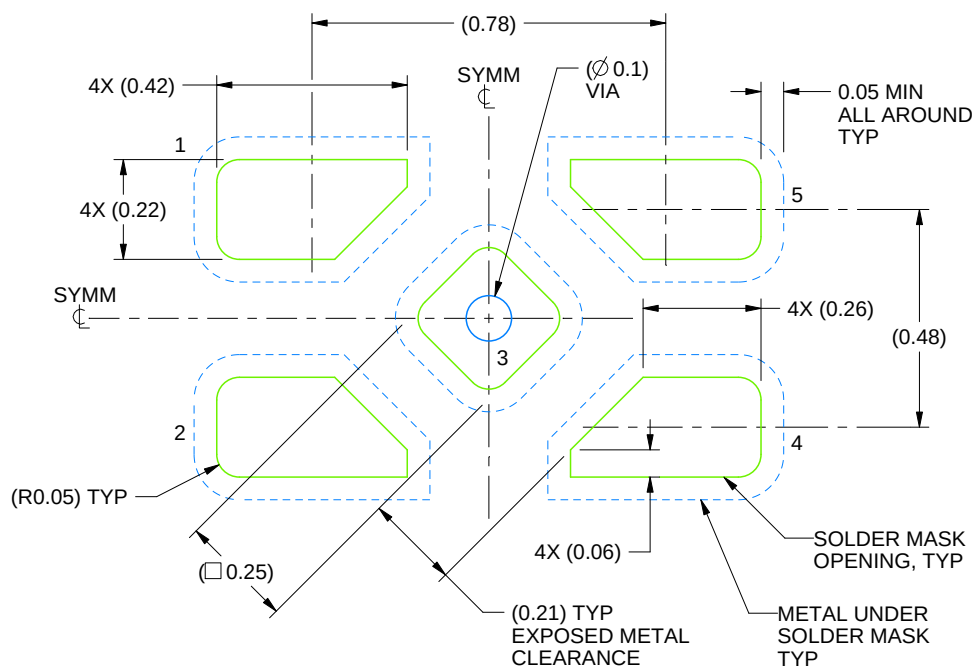
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

**DPW0005A**

**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:60X

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NOTES: (continued)

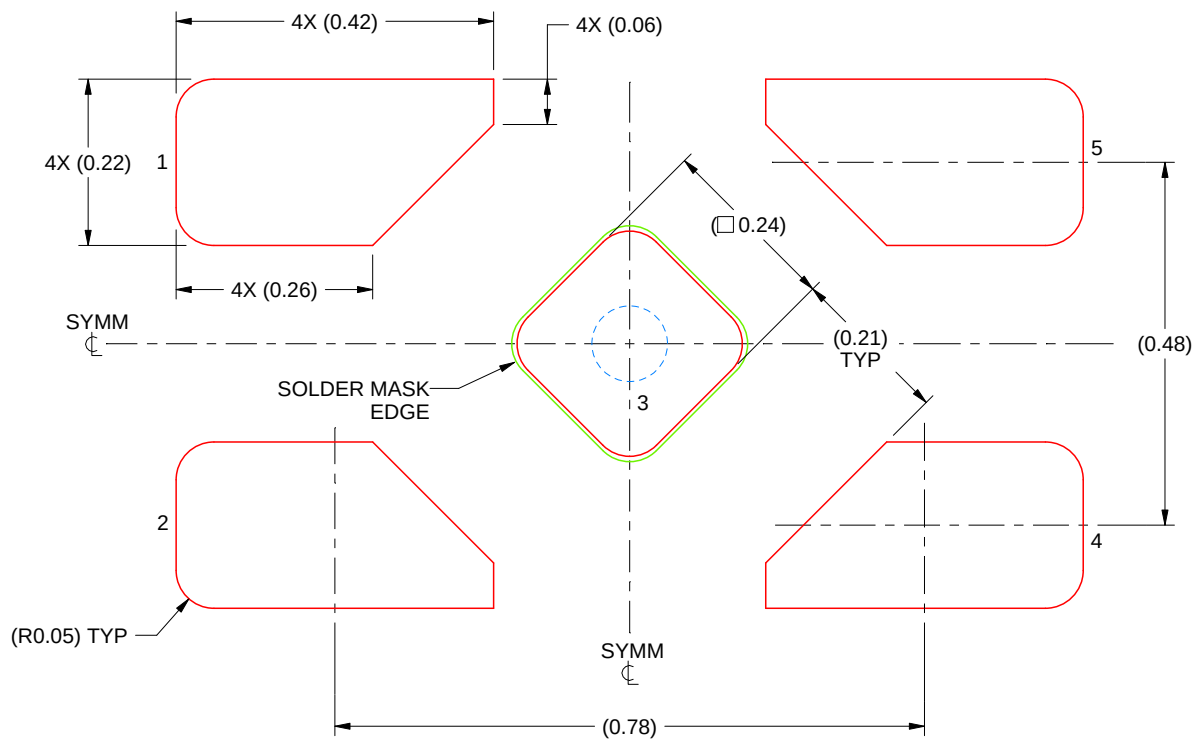
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3  
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:100X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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