

TPSI2072-Q1 适用于绝缘监测和高压测量且具有 2mA 雪崩额定值的双通道 600V、50mA 汽车类隔离开关

1 特性

- 符合汽车应用要求
 - AEC-Q100 等级 1: -40°C 至 125°C, T_A
- 集成雪崩额定 MOSFET
 - 针对电介质耐压测试 (Hi-Pot) 可靠性进行设计和认证
 - $I_{AVA} = 2\text{mA}$ (5s 脉冲), 1mA (60s 脉冲)
 - $V_{HIPOT, 5-s} = 4300\text{V}$, $R_{series} > 1.83\text{M}\Omega$
 - $V_{HIPOT, 5-s} = 2850\text{V}$, $R_{series} > 1.1\text{M}\Omega$
 - 600V 关断电压
 - $R_{ON} = 65\Omega$ ($T_J = 25^\circ\text{C}$)
 - 当电压为 500V ($T_J = 105^\circ\text{C}$) 时, $I_{OFF} = 1\mu\text{A}$
- 低初级侧电源电流
 - 5mA 单通道、9mA 双通道导通状态电流
- 功能安全型
 - 可帮助进行 ISO 26262 和 IEC 61508 系统设计的文档
- 稳健可靠的隔离栅:
 - 在 1000V_{RMS}/1500V_{DC} 工作电压下预计寿命超过 26 年
 - 隔离额定值 V_{ISO} 高达 3750V_{RMS}/5300V_{DC}
- SOIC 11 引脚 (DWQ) 封装, 具有宽引脚, 可提高热性能
 - 爬电距离和间隙 $\geq 8\text{mm}$ (初级-次级)
 - 爬电距离和间隙 $\geq 3\text{mm}$ (开关端子之间)
- 安全相关认证
 - (计划) DIN VDE V 0884-11:2017-01
 - (计划) UL 1577 组件认证计划

2 应用

- 固态继电器
- 混合动力、电动和动力传动系统
- 电池管理系统 (BMS)
- 能量存储系统 (ESS)
- 太阳能
- 车载充电器
- 电动汽车充电基础设施
- 另请参阅与这些应用相关的 TI 参考设计。

3 说明

TPSI2072-Q1 是一款双通道隔离式固态继电器, 专为高电压汽车和工业应用而设计。TPSI2072-Q1 与 TI 具有高可靠性的电容隔离技术和内部背对背 MOSFET 整合在一起, 形成了一款完全集成式解决方案, 无需次级侧电源。TPSI2072-Q1 可提高系统可靠性, 因为 TI 的

电容隔离技术不会受到机械继电器和光继电器元件中常见的机械损耗或光退化故障模式的影响。

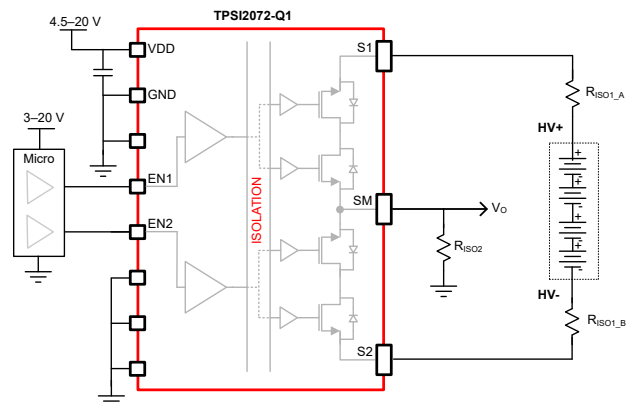
该器件的初级侧仅由 9mA 的输入电流供电, 并集成了失效防护引脚 EN1 和 EN2, 可防止对 VDD 电源反向供电的任何可能性。在大多数应用中, 器件的 VDD 引脚应连接到 4.5V 至 20V 的系统电源, 并且器件的 EN1 和 EN2 引脚应由逻辑高电平介于 2.1V 至 20V 之间的 GPIO 输出驱动。在其他应用中, VDD、EN1 和 EN2 引脚可直接由系统电源或 GPIO 输出驱动。

次级侧的每个通道都包含背对背 MOSFET, 从 SM 至 S1 以及 SM 至 S2 的关断电压为 +/-600 V。TPSI2072-Q1 MOSFET 的雪崩稳健性和热敏感封装设计使其能够可靠地支持系统级电介质耐压测试 (HiPot), 并且无需任何外部元件即可承受高达 2mA 的直流快速充电器浪涌电流。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
TPSI2072-Q1	SOIC 11 引脚 (DWQ)	10.3mm × 7.5mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



TPSI2072-Q1 简化版应用原理图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
June 2023	*	Initial Release

5 Pin Configuration and Functions

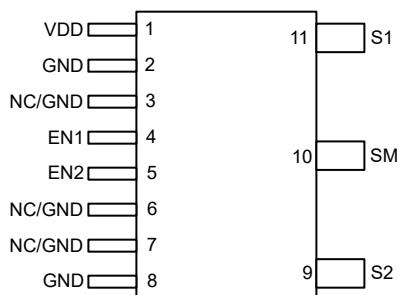


图 5-1. TPSI2072-Q1 DWQ Package, 11-Pin SOIC (Top View)

5.1 Pin Functions

PIN NO.	PIN NAME	TYPE ⁽¹⁾	DESCRIPTION
1	VDD	P	Power supply for primary side
2	GND	GND	Ground supply for primary side
3	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
4	EN1	I	Active high switch enable signal, S1-SM
5	EN2	I	Active high switch enable signal, SM-S2
6	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
7	NC/GND	NC/GND	Internally connected, connect externally to ground or leave floating
8	GND	GND	Internally connected to GND, connect externally to ground or leave floating
9	S2	I/O	Switch input
10	SM	I/O	Shared switch input, see Layout Guidelines for more information
11	S1	I/O	Switch input

(1) P = power, I = input, O = output, GND = ground, NC = no connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		MIN	MAX	UNIT
V _{VDD}	Primary side supply voltage ⁽²⁾	– 0.3	20.7	V
V _{EN1}	Enable1 voltage ⁽²⁾	– 0.3	20.7	V
V _{EN2}	Enable2 voltage ⁽²⁾	– 0.3	20.7	V
I _{S1,S2}	Switch current, S1/S2	– 55	55	mA
I _{SM}	Switch current, SM	– 110	110	mA
I _{AVA,S1,S2}	Repetitive avalanche rating, 5s pulse, S1/S2 ⁽³⁾	– 2	2	mA
	Repetitive avalanche rating, 60s pulse, S1/S2 ⁽⁴⁾	– 1	1	mA
I _{AVA,SM}	Repetitive avalanche rating, 5s pulse, SM ⁽³⁾	– 4	4	mA
	Repetitive avalanche rating, 60s pulse, SM ⁽⁴⁾	– 2	2	mA
T _J	Junction temperature	– 40	150	°C
T _{stg}	Storage temperature	– 65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Voltage values are with respect to GND.
- (3) 5 minutes accumulated over lifetime in increments of no longer than 5 second periods, duty cycle < 33%
- (4) 5 minutes accumulated over lifetime in increments of no longer than 60 second periods, duty cycle < 10%

6.2 ESD Ratings

				VALUE	UNIT
HBM _{Prim}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	Primary Side Pins No. 1-8	±2000	V
HBM _{Sec}		Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 1C	Secondary Side Pins No. 9-11	±1500	V
CDM	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4	All pins	±750	V

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V _{VDD}	Primary side supply voltage ⁽¹⁾	4.5		20	V
V _{EN1}	Enable1 voltage ⁽¹⁾	0		20	V
V _{EN2}	Enable2 voltage ⁽¹⁾	0		20	V
V _{SM-S1} , V _{SM-S2}	Switch input voltage	– 600		600	V
I _{S1,S2}	Switch current	– 50		50	mA
I _{SM}	Switch current	– 100		100	mA
T _A	Ambient operating temperature	– 40		125	°C
T _J	Junction operating temperature	– 40		150	°C

(1) Voltage values are with respect to GND.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DEVICE	UNIT
		DWQ (SOIC)	
		11 PINS	
R _{ΘJA}	Junction-to-ambient thermal resistance	70	°C/W
R _{ΘJA} , EVM, 60S	Junction-to-ambient thermal resistance ^{(2) (3)}	52	°C/W
R _{ΘJA} , EVM, 5S	Junction-to-ambient thermal resistance ^{(2) (4)}	30	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	22	°C/W
R _{ΘJC(top)}	Junction-to-case (top) thermal resistance	26	°C/W
ψ _{JT}	Junction-to-top characterization parameter	14	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	21	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) EVM PCB dimensions are 70mm x 70mm x 1.58mm. 4 layer PCB with 2oz Cu on layers 1,4 and 1oz Cu on layer 2,3.

(3) Performance of EVM with power applied for 60s.

(4) Performance of EVM with power applied for 5s.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _D	Maximum power dissipation, total	V _{VDD} = 5 V, V _{EN1,EN2} = 5 V peak to peak, V _{S1-SM} = 600V, R _{S1} = 500kΩ, V _{S2-SM} = 600V, R _{S2} = 500kΩ, f _{EN1,EN2} = 1Hz square wave			30.2	mW
P _{D_P}	Maximum power dissipation (primary)				30	mW
P _{D_S}	Maximum power dissipation (secondary)				0.2	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
IEC 60664-1				
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External Creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>10.5	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-III	
		Rated mains voltage ≤ 1000 V _{RMS}	I-II	
DIN V VDE 0884-11:2017-01 ⁽²⁾ , IEC 60747-17:2020				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V _{PK}
V _{IOWM}	Maximum isolation working voltage	AC voltage (sine wave)	1000	V _{RMS}
		DC voltage	1500	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification)	5300	V _{PK}
		V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production)	6360	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Tested in oil per IEC 62638-1, 1.2/50 μs waveform, V _{TEST} = 1.3 × V _{IOSM} = 6500 V _{PK} (qualification)	5000	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} = 1800 V _{PK} , t _m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.3 × V _{IORM} = 1950 V _{PK} , t _m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.5 × V _{IORM} = 2250 V _{PK} , t _m = 1 s	≤5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.4 × sin (2 π ft), f = 1 MHz	4	pF
R _{IO}	Insulation resistance, input to output ⁽⁵⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
	Climatic category		40/150/21	
UL 1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification) V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production)	3750	V _{RMS}
Misc.				
V _{ISO}	Withstand isolation voltage		5300	V _{DC}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN V VDE V 0884-11:2017-01	Not Planned, contact TI to request.	Plan to certify according to UL 1577 Component Recognition Program	Not Planned, contact TI to request.	Not Planned, contact TI to request.
Maximum transient isolation voltage, 5300 V _{PK} ; Maximum repetitive peak isolation voltage, 1500 V _{PK} ; Maximum surge isolation voltage, 6000 V _{PK}		Single protection, 3750 V _{RMS}		
Certificate planned		Certificate planned		

6.8 Safety Limiting Values

PARAMETER ^{(1) (2)}		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S	Safety VDD Current	R _{θJA} = 70°C/W, V _{VDD} = 20 V, T _J = 150°C, T _A = 25°C			77	mA
	Safety Switch Current, S1 or S2 (On State)	R _{θJA} = 70°C/W, V _{VDD} = 20 V, T _J = 150°C, T _A = 25°C			71	
	Safety Switch Current, S1 or S2 (Off State, 5 second)	R _{θJA, EVM, 5S} ⁽³⁾ = 30°C/W, V _{VDD} = 0 V, T _J = 150°C, T _A = 25°C			2.7	
	Safety Switch Current, S1 or S2 (Off State, 60 second)	R _{θJA, EVM, 60S} ⁽³⁾ = 52°C/W, V _{VDD} = 0 V, T _J = 150°C, T _A = 25°C			1.5	
P _S	Safety input, output, or total power	R _{θJA} = 70°C/W, T _J = 150°C, T _A = 25°C.			1.78	W
T _S	Maximum safety temperature				150	°C

- (1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.
- (2) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.
- (3) Assuming PCB layout similar to EVM in Layout Guideline section

6.9 Electrical Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at $T_J = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $V_{EN1,EN2} = 5\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PRIMARY SIDE SUPPLY (VDD)						
V _{UVLO_R}	VDD undervoltage threshold rising	VDD rising	4	4.2	4.4	V
V _{UVLO_F}	VDD undervoltage threshold falling	VDD falling	3.9	4.1	4.3	V
V _{UVLO_HYS}	VDD undervoltage threshold hysteresis		40	100	150	mV
I _{VDD_ON_S}	VDD current, single channel powered on	V _{EN1} = 5 V, V _{EN2} = 0 V OR V _{EN 1} = 0 V, V _{EN2} = 5 V, T _J = 25°C		5	6	mA
		V _{EN1} = 5 V, V _{EN2} = 0 V OR V _{EN 1} = 0 V, V _{EN2} = 5 V, - 40°C ≤ T _J ≤ 150°C		5	6.5	mA
I _{VDD_ON}	VDD current, both channels powered on	V _{EN1,EN2} = 5 V, T _J = 25°C		9	11	mA
		V _{EN1,EN2} = 5 V, - 40°C ≤ T _J ≤ 150°C		9	12	mA
I _{VDD_OFF}	VDD current, 5 V, device powered off	V _{VDD} = 5 V, V _{EN1,EN2} = 0 V, T _J = 25°C		3.5	8	μA
		V _{VDD} = 5 V, V _{EN1,EN2} = 0 V, T _J = 105°C		4.5	11	μA
		V _{VDD} = 5 V, V _{EN1,EN2} = 0 V, T _J = 125°C		5.2	16	μA
		V _{VDD} = 5 V, V _{EN1,EN2} = 0 V, - 40°C ≤ T _J ≤ 150°C			30	μA
	VDD current, 20 V, device powered off	V _{VDD} = 20 V, V _{EN1,EN2} = 0 V, T _J = 25°C		8	10.5	μA
		V _{VDD} = 20 V, V _{EN1,EN2} = 0 V, T _J = 105°C		10	17	
		V _{VDD} = 20 V, V _{EN1,EN2} = 0 V, T _J = 125°C		11	25	
		V _{VDD} = 20 V, V _{EN1,EN2} = 0 V, - 40°C ≤ T _J ≤ 150°C			40	
FET CHARACTERISTICS (S1, S2, SM)						
R _{DSON}	On resistance, S1-SM or SM-S2	I _{S1,S2} = 2 mA, T _J = 25°C		65	90	Ω
		I _{S1,S2} = 2 mA, T _J = 85°C		88	120	
		I _{S1,S2} = 2 mA, T _J = 105°C		96	125	
		I _{S1,S2} = 2 mA, T _J = 125°C		105	140	
		I _{S1,S2} = 2 mA, - 40°C ≤ T _J ≤ 150°C			150	
I _{OFF}	Off leakage, S1-SM or SM-S2, 500 V	V = +/- 500 V, T _J = 25°C		.02	0.1	μA
		V = +/- 500 V, T _J = 85°C			0.3	
		V = +/- 500 V, T _J = 105°C			1	
		V = +/- 500 V, T _J = 125°C			4	
		V = +/- 500 V, - 40°C ≤ T _J ≤ 150°C			20	
	Off leakage, S1-SM or SM-S2, 600 V	V = +/- 600 V, T _J = 25°C		.02	0.1	μA
		V = +/- 600 V, T _J = 85°C			0.5	
		V = +/- 600 V, T _J = 105°C			1.5	
		V = +/- 600 V, T _J = 125°C			6	
		V = +/- 600 V, - 40°C ≤ T _J ≤ 150°C			50	

6.9 Electrical Characteristics (continued)

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at $T_J = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $V_{EN1,EN2} = 5\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVA}	Avalanche voltage	$I_O = 10\text{ }\mu\text{A}$, $T_J = 25^\circ\text{C}$	650	770		V
		$I_O = 100\text{ }\mu\text{A}$, $T_J = 150^\circ\text{C}$	650	770		
C_{OSS}	S1, S2 capacitance	$V_{S1,S2,SM} = 0\text{ V}$, $F = 1\text{ MHz}$		150		pF
C_{OSS_SM}	SM capacitance	$V_{SM,S1,S2} = 0\text{ V}$, $F = 1\text{ MHz}$		300		pF
LOGIC-LEVEL INPUT (EN1, EN2)						
V_{IL}	Input logic low voltage		0.0		0.8	V
V_{IH}	Input logic high voltage		2.1		20.0	V
V_{HYS}	Input logic hysteresis		100	250	300	mV
I_{IL}	Input logic low current	$V_{EN1,EN2} = 0\text{ V}$	– 1		1	μA
		$V_{EN1,EN2} = 0.8\text{ V}$	2	4	6.5	μA
I_{IH}	Input logic high current	$V_{EN1,EN2} = 5\text{ V}$	10	25	50	μA
		$V_{EN1,EN2} = 20\text{ V}$	100	175	350	μA
I_{VDD_FS}	VDD fail-safe current	$V_{EN1,EN2} = 20\text{ V}$, $V_{DD} = 0\text{ V}$	– 0.1	0	0.1	μA
R_{PD}	Pulldown resistance	Two point measurement, $V_{EN1,EN2} = 0.5\text{ V}$ and $V_{EN1,EN2} = 0.8\text{ V}$	100	200	350	$\text{k}\Omega$
NOISE IMMUNITY						
CMTI	Common-mode transient immunity	$ V_{CM} = 1000\text{ V}$			100.0	V/ns

6.10 Switching Characteristics

Unless otherwise noted, all minimum/maximum specifications are over recommended operating conditions. All typical values are measured at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $V_{EN1,EN2} = 5\text{ V}$.

MODE	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching Characteristics						
EN switching	t_{PD_ON}	Input HI to Output voltage falling propagation delay			300	μs
	t_F	Output fall time		20	100	
	t_{ON}	Input HI to Output LO delay			400	
	t_{PD_OFF}	Input LO to Output voltage rising propagation delay			200	
	t_R	Output rise time			600	
	t_{OFF}	Input LO to Output HI delay			700	
		$V_{IN} = 600\text{ V } R_L = 1\text{ M}\Omega$				
EN and VDD switching	t_{PD_ON}	Input HI to Output voltage falling propagation delay			400	μs
	t_F	Output fall time		20	100	
	t_{ON}	Input HI to Output LO delay			500	
	t_{PD_OFF}	Input LO to Output voltage rising propagation delay			200	
	t_R	Output rise time			600	
	t_{OFF}	Input LO to Output HI delay			700	
		$V_{IN} = 600\text{ V } R_L = 1\text{ M}\Omega$				

7 Parameter Measurement Information

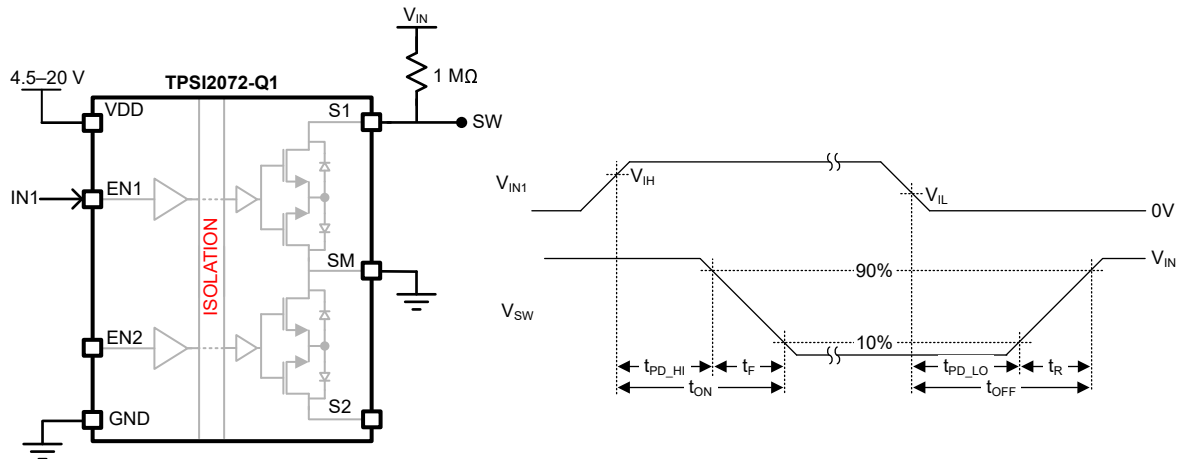


图 7-1. Timing Diagram, EN1 Switching

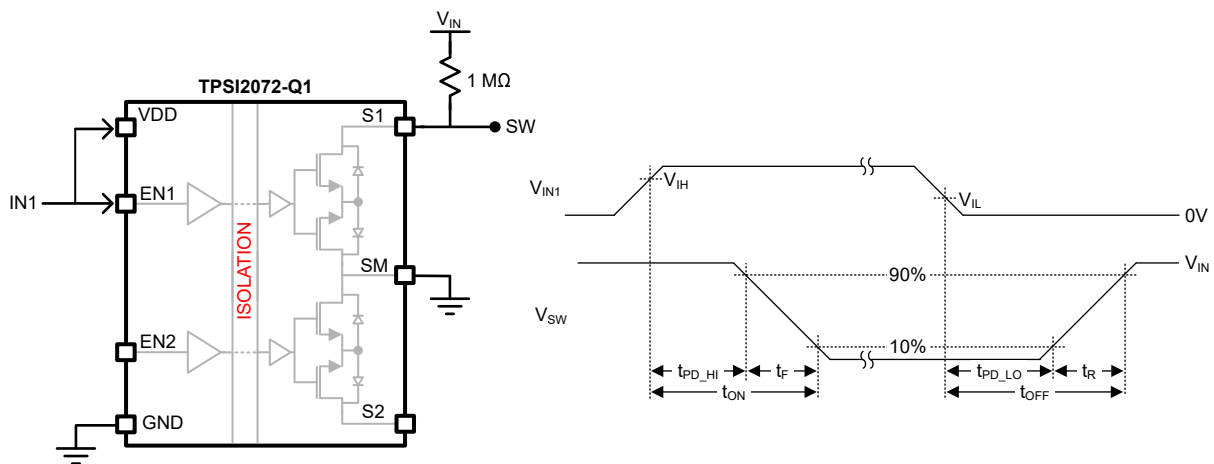


图 7-2. Timing Diagram, EN1 and VDD Switching

8 Detailed Description

8.1 Overview

The TPSI2072-Q1 is a two channel isolated solid state relay designed for high voltage automotive and industrial applications. TI's high reliability capacitive isolation technology in combination with back-to-back MOSFETs form a completely integrated solution requiring no secondary side power supply.

As seen in the [Functional Block Diagram](#), the primary side consists of two drivers which deliver power and enable logic information to each of the internal MOSFETs on the secondary side. The on-board oscillator controls the frequency of the drivers' operation and the Spread Spectrum Modulation (SSM) controller varies the driver frequency to improve system EMI performance. When one or both of the enable pins are brought HI and the VDD voltage is above the UVLO threshold, the oscillator starts and the drivers send power and a logic HI across the barrier. When one or both of the enable pins are brought LO or the VDD voltage falls below the UVLO threshold, the corresponding driver or drivers are disabled. The lack of activity communicates a logic LO to the secondary side and the MOSFETs are disabled.

Each MOSFET on the secondary side has a dedicated full-bridge rectifier to form its local power supply and a receiver. The receiver determines the logic state delivered from the primary side through the capacitive isolation barrier and uses a slew rate controlled driver to drive the MOSFET's gate. Each receiver performs signal conditioning on the signals received across the barrier in order to filter common mode interference and ensure that the MOSFETs are controlled according to the logic sent by the primary side driver and the system.

The avalanche robust MOSFETs and the thermal benefits of the widened pins on the 11 DWQ package enable the TPSI2072-Q1 to support dielectric withstand testing (HiPot) and DC fast charger surge currents of up to 2 mA without requiring any external protection components.

8.2 Functional Block Diagram

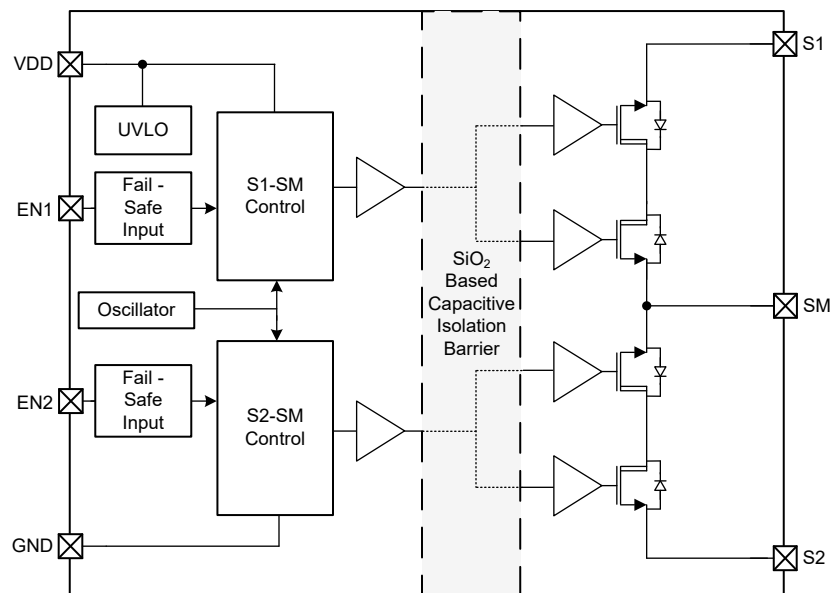


图 8-1. TPSI2072-Q1 Block Diagram

8.3 Feature Description

8.3.1 Avalanche Robustness

When the voltage between the S1 and SM pins or the voltage between SM and S2 pins exceeds ± 600 V the secondary side MOSFETs could enter an avalanche mode of operation. The MOSFETs and the 11 DWQ package have been designed and qualified to be robust in this mode of operation to support [Dielectric Withstand Testing \(HiPot\)](#). To help ensure the thermal performance of the the system in this mode of operation, refer to the [PCB Layout Guidelines](#).

8.4 Device Functional Modes

表 8-1. Device Functional Modes

VDD	EN1	EN2	S1-SM State	S2-SM State	COMMENTS
Powered Up ⁽¹⁾	L	L	OFF	OFF	VDD current is in OFF state range.
	H	L	ON	OFF	VDD current is in ON state range.
	L	H	OFF	ON	VDD current is in ON state range.
	H	H	ON	ON	VDD current is in ON state range.
Powered Down ⁽²⁾	L	L	OFF	OFF	VDD current is in OFF state range.
	H	X ⁽³⁾	OFF	OFF	Primary side analog is powered on, VDD current is between off state and ON state ranges.
	X ⁽³⁾	H	OFF	OFF	Primary side analog is powered on, VDD current is between off state and ON state ranges.

(1) $VDD \geq VDD$ undervoltage rising threshold.

(2) $VDD \leq VDD$ undervoltage falling threshold.

(3) X: do not care

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TPSI2072-Q1 is a two channel 600-V, 50-mA automotive isolated switch optimized for high voltage switching in measurement applications, especially those that require switching across an isolation barrier or galvanically isolated domain. Common end equipments include energy storage systems (ESS), solar panel arrays, EV chargers, and EV battery management systems. The device enables the system designer to reduce cost and improve reliability by replacing mechanical relays and optically isolated devices.

The TPSI2072-Q1's enable inputs are fail safe and do not need to be driven from the same domain as the VDD pin supply.

The TPSI2072-Q1 supports an input voltage range of 4.5 V to 20 V on the VDD primary supply pin and a logic high of 2.1 V to 20 V on the enable pins. The secondary side supports high voltage switching from – 600 V to 600V.

TI Reference Designs

The TI reference designs linked below are a helpful introduction to high voltage applications using the TPSI2072-Q1. To maximize the thermal performance of the TPSI2072-Q1 for dielectric withstand testing (HiPot), please follow the [Layout Guidelines](#) contained within this datasheet.

- [TIDA-010232: High Voltage Insulation Monitoring](#)
- [TIDA-01513: Automotive High Voltage and Isolation Leakage Measurements](#)

9.2 Typical Application

Insulation Resistance Monitoring

In high voltage applications such as electric vehicle systems, the high voltage battery pack is intentionally isolated from the chassis domain of the car to protect the driver and prevent damage to electrical components. These systems actively monitor the integrity of this insulation to ensure the safety of the system throughout its lifetime. This active monitoring is referred to as insulation resistance monitoring (also known as isolation check, insulation check, isolation monitoring, insulation monitoring, and residual current monitoring (RCM)) and is performed by measuring the resistances from each of the battery terminals to the chassis ground, illustrated below as R_{ISOP} and R_{ISON} .

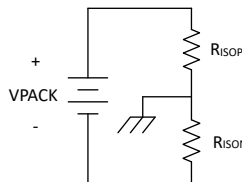


图 9-1. Insulation Resistance Model

There are multiple design architectures using the TPSI2072-Q1 to measure these insulation resistances, R_{ISOP} and R_{ISON} . Some architectures employ a microcontroller that performs measurements from the high voltage domain, which will be referred to in this document as the Battery V- Reference architecture. Others use a

microcontroller in the low voltage domain, which will be referred to in this document as the Chassis Ground Reference architecture. The primary difference between the two architectures is the node that the MCU uses as its GND reference. An example of a Battery V- MCU is the [BQ79631-Q1 UIR sensor](#).

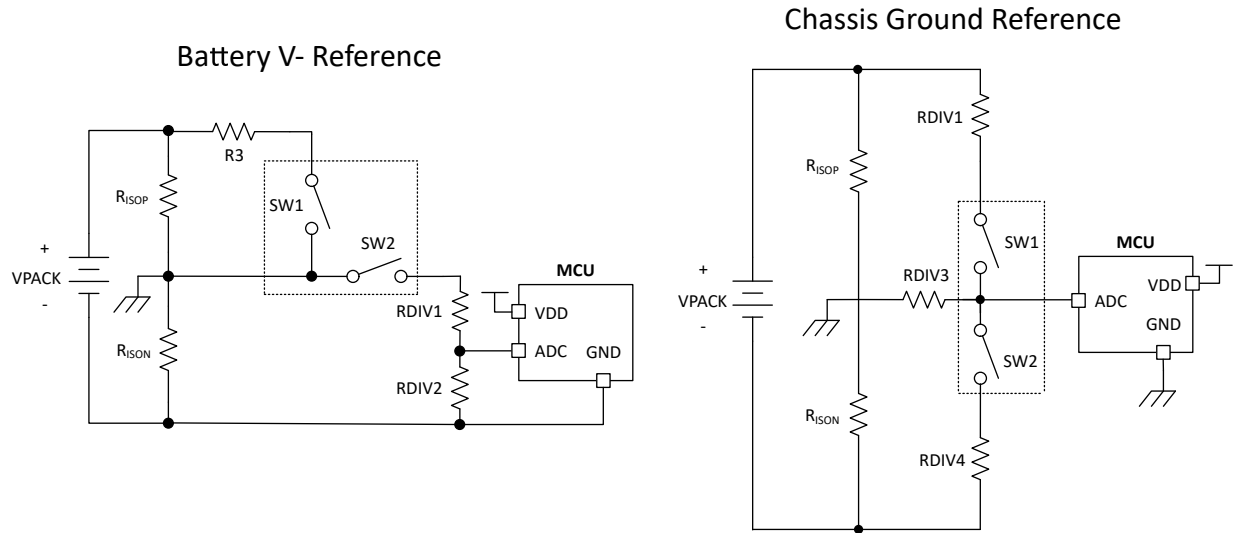


图 9-2. Different MCU ADC Reference Examples

The two following sections demonstrate the measurement algorithms and the systems of equations used to calculate the isolation resistances using each architecture.

Battery V- Reference Example

A Battery V- Reference architecture is shown below with the TPSI2072-Q1 illustrated as a switch (SW1 and SW2). SW2 initiates a connection between the chassis and PACK- and enables the measurement path to the ADC. SW1 initiates a connection between the chassis and the PACK+. RDIV1 and RDIV2 form a divider which scales the measured voltages down to the appropriate ADC range.

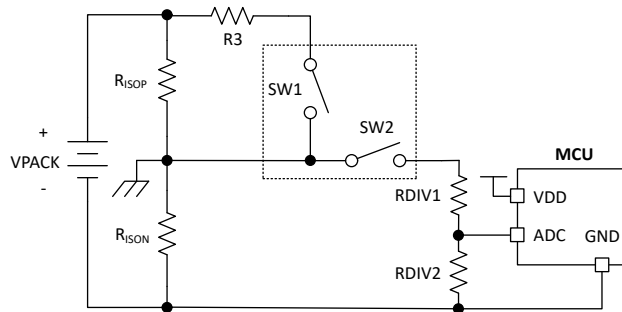


图 9-3. Battery V- Reference Architecture

Two ADC measurements must be taken in order to obtain enough information to calculate the two unknown isolation resistances. The first measurement is taken with SW1 open and SW2 closed. The second measurement is taken with SW1 closed and SW2 closed. With these two measurements it is possible to solve the system of equations and calculate R_{ISOP} and R_{ISON} .

In the following example the voltage on the chassis ground is arbitrarily referred to as V_{RISONx} .

For the first ADC measurement SW2 is closed as shown below and the following equations relate the ADC voltage to the other parameters in the system in this condition:

- V_{ADC1} measurement 1: SW1 open, SW2 closed

$$V_{RISON1} = V_{PACK} \times \frac{R_{ISON} || (R_{DIV1} + R_{DIV2})}{R_{ISOP} + (R_{ISON} || (R_{DIV1} + R_{DIV2}))} \quad (1)$$

$$V_{ADC1} = V_{RISON1} \times \frac{R_{DIV2}}{R_{DIV1} + R_{DIV2}} \quad (2)$$

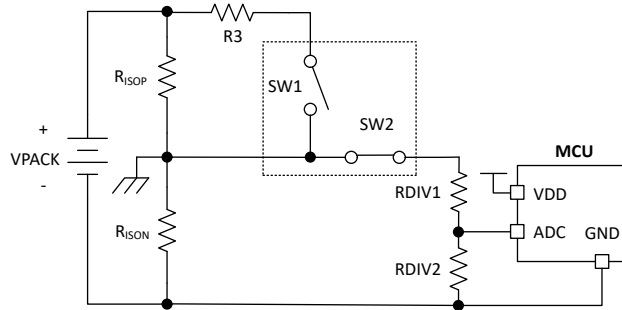


图 9-4. Battery V- Reference Switch Positions for ADC1 Measurement

For the second ADC measurement SW1 and SW2 are closed as shown below and the following equations relate the ADC voltage to the other parameters in the system in this condition:

- V_{ADC2} measurement 2: SW1 closed, SW2 closed

$$V_{RISON2} = V_{PACK} \times \frac{R_{ISON} || (R_{DIV1} + R_{DIV2})}{(R_{ISOP} || R_3) + (R_{ISON} || (R_{DIV1} + R_{DIV2}))} \quad (3)$$

$$V_{ADC2} = V_{RISON2} \times \frac{R_{DIV2}}{R_{DIV1} + R_{DIV2}} \quad (4)$$

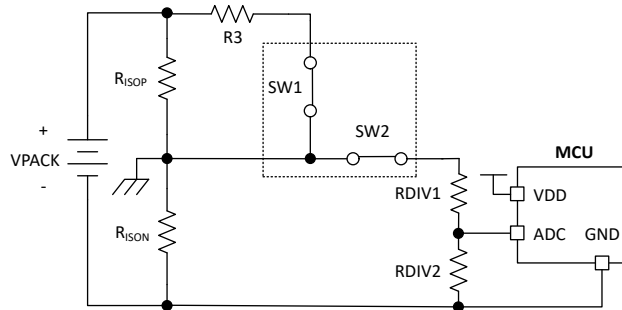


图 9-5. Battery V- Reference Switch Positions for ADC2 Measurement

Chassis Ground Reference Example

A Chassis Ground Reference architecture is shown below. SW1 and SW2 initiate connections to the PACK+ and PACK- and enable the measurement paths to the ADC. RDIV1, RDIV3, and RDIV4 scale the measured voltages down to the appropriate ADC ranges.

This first measurement is taken with SW1 closed and SW2 open and the second measurement is taken with SW1 open and SW2 closed.

- V_{ADC1} : SW1 closed, SW2 open

$$V_{ADC1} = V_{RDIV3} = V_{PACK} \frac{(R_{ISOP} || (R_{DIV1} + R_{DIV3}))}{(R_{ISOP} || (R_{DIV1} + R_{DIV3}) + R_{ISON})} \times \frac{R_{DIV3}}{R_{DIV1} + R_{DIV3}} \quad (5)$$

- V_{ADC2} : SW1 open, SW2 closed

$$V_{ADC2} = V_{RDIV3} = -V_{PACK} \frac{(R_{ISON} || (R_{DIV3} + R_{DIV4}))}{(R_{ISON} || (R_{DIV3} + R_{DIV4})) + R_{ISOP}} \times \frac{R_{DIV3}}{R_{DIV3} + R_{DIV4}} \quad (6)$$

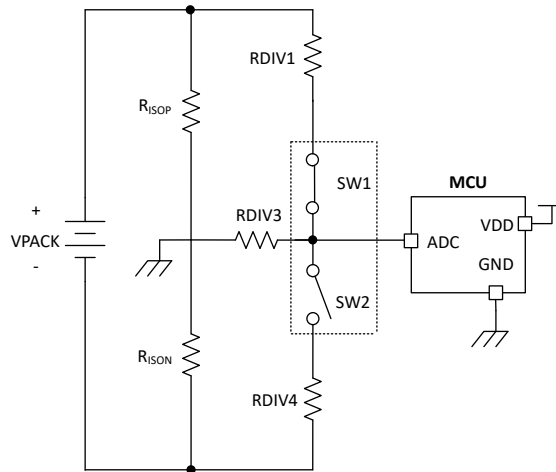


图 9-6. Chassis Ground Reference Switch Positions for ADC1 Measurement

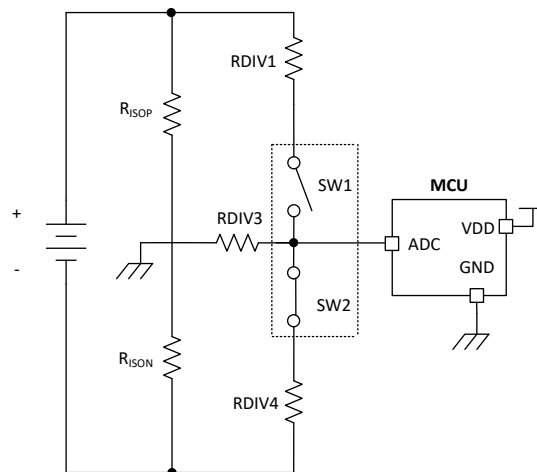


图 9-7. Chassis Ground Reference Switch Positions for ADC2 Measurement

Battery V- Reference and Chassis Ground Reference Architectures with the TPSI2072-Q1

The circuits in 图 9-8 and 图 9-9 demonstrate how to connect the TPSI2072-Q1 as a switch in each of the architectures above.

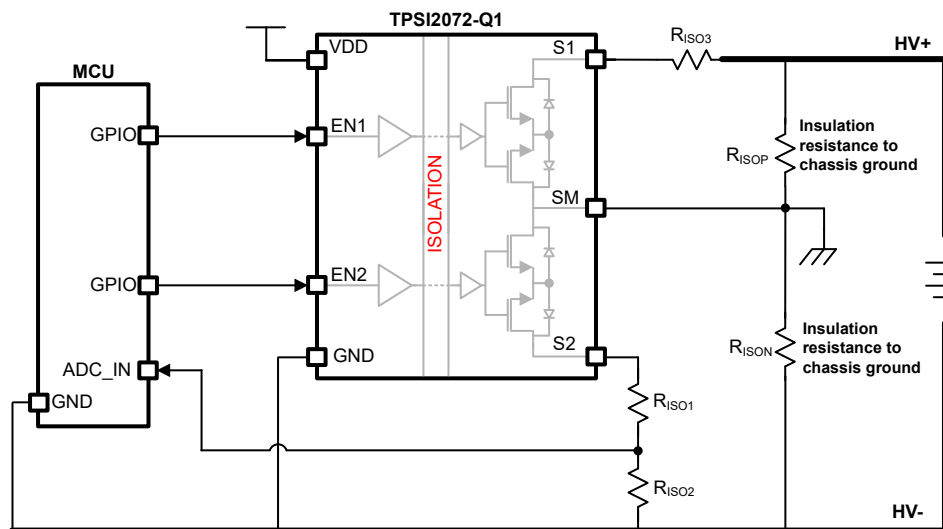


图 9-8. TPSI2072-Q1 Insulation Resistance Monitoring - Battery V- Reference

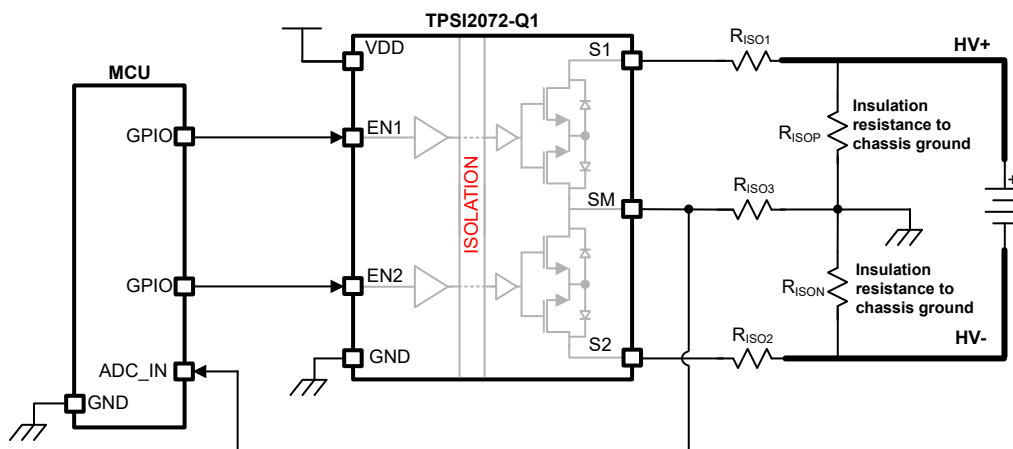


图 9-9. TPSI2072-Q1 Insulation Resistance Monitoring - Chassis Ground Reference

9.2.1 Dielectric Withstand Testing (HiPot)

The TPSI2072-Q1 is specifically designed to support dielectric withstand testing. In a high voltage system, a dielectric withstand test (HiPot) may be administered during the characterization, production or maintenance of the system to validate the reliability of the insulation barriers and galvanically isolated domains it contains. These withstand voltage tests intentionally stress the components spanning these domains and put them in an overvoltage condition. MOSFETs that are placed under these overvoltage conditions will enter avalanche mode and begin conducting current at a high voltage, dissipating high power and heating up. The design and qualification of the TPSI2072-Q1 was completed with this state in mind and supports up to 2 mA I_{AVA} for 5 seconds intervals and 1 mA I_{AVA} for 60 second intervals.

The dielectric withstand test voltage (V_{HiPot}), the TPSI2072-Q1's avalanche voltage (V_{AVA}), and the resistance (R) in series with the TPSI2072-Q1 should be chosen to limit the avalanche current (I_{AVA}) to the corresponding current limit depending on the test duration. In addition, the PCB design should follow the recommendations in the [Layout Guidelines](#) section to ensure adequate thermal performance to keep the junction temperature (T_J) below the absolute maximum rating of the TPSI2072-Q1.

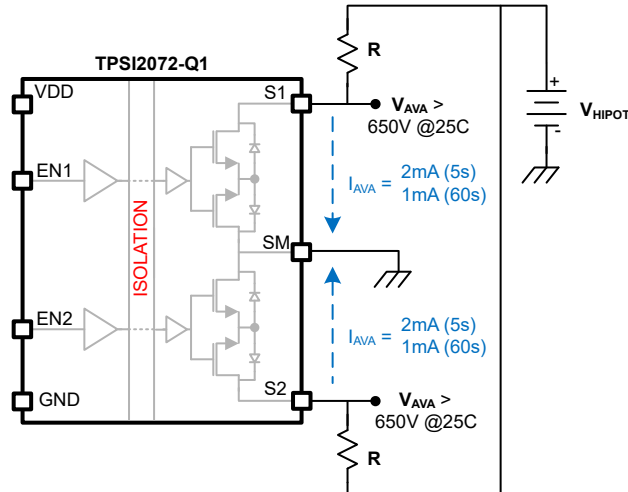


图 9-10. Dielectric Withstand Test (HiPot) - Simplified Schematic

9.2.2 Design Requirements

表 9-1 lists the Design Requirements for a typical insulation resistance monitoring application using the Chassis Ground Reference architecture and the TPSI2072-Q1 for switching.

表 9-1. Typical Design Parameters For Insulation Resistance Monitoring Using the TPSI2072-Q1 - Chassis Ground Reference Architecture

PARAMETER	VALUE
V _{PACK} Voltage (maximum)	500 V
Primary side supply (V _{VDD})	5 V ±10 %
Dielectric withstand voltage test	2850 V
	5 s
Surge voltage (IEC61000-3-5)	2500 V

9.2.3 Design Procedure - Chassis Ground Reference

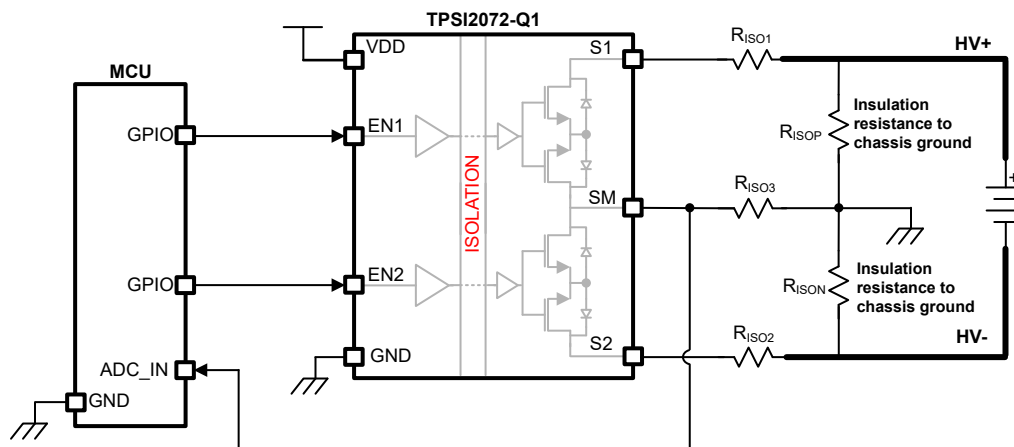


图 9-11. Chassis Ground Reference

R_{ISO1}, R_{ISO2} Selection

In order to protect the TPSI2072-Q1, R_{ISO1} and R_{ISO2} must be sized to limit the current in an overvoltage condition. The amount of resistance required to protect the TPSI2072-Q1 depends on the amount of overvoltage applied. For example, during a dielectric withstand voltage test (HiPot) of 2850 V for 5 seconds, the S1 to SM

voltage and the SM to S2 voltage will be clamped to 650 V (V_{AVA} minimum) by the TPSI2072-Q1 and the R_{ISO1} , R_{ISO2} resistances required to keep the current under 2 mA would be $1.1\text{ M}\Omega$.

$$I_{AVA} = \frac{V_{HIPOT} - V_{AVA}}{R_{ISO1}} = \frac{2850V - 650V}{1.1\text{ M}\Omega} = 2.0mA \quad (7)$$

If the high potential test lasts for 60 seconds, the R_{ISO1} , R_{ISO2} resistances must be doubled to $2.2\text{ M}\Omega$ to keep the current below 1 mA.

DC Overvoltage	$R_{ISO1, ISO2}$ Minimum (5 second intervals)	$R_{ISO1, ISO2}$ Minimum (60 second intervals)
2000 V	675 k Ω	1350 k Ω
2850 V	1100 k Ω	2200 k Ω
3500 V	1425 k Ω	2850 k Ω
4300 V	1825 k Ω	3650 k Ω

9.3 Power Supply Recommendations

To ensure a reliable supply voltage, TI recommends that a 100-nF ceramic capacitor be placed between the VDD pin and the GND pin of the TPSI2072-Q1. The capacitor should be placed as close to the device's VDD pin as possible < 10 mm.

9.4 Layout

9.4.1 Layout Guidelines

Component placement:

Decoupling capacitors for the primary side VDD supply must be placed as close as possible to the device pins.

EMI considerations:

The TPSI2072-Q1 employs spread spectrum modulation (SSM) and in some systems, no additional system design considerations are required to meet the EMI performance needs.

However, the system designer may choose to take additional measures to minimize EMI depending on the system requirements and safety preferences of the system designer. The measures listed below reduce emissions by providing a capacitive return path from the secondary side to the primary side or by increasing the common mode loop impedance with an inductive component on the primary side.

• Capacitive Return Paths:

- An interlayer stitching capacitance in the range of 10-20 pF can be implemented on the PCB. This zero-cost implementation is typically preferred as it also serves the purpose of thermal performance improvement if placed directly underneath the TPSI2072-Q1. Please see the [Layout Example](#) for more details.
- Most system designs already employ discrete Y capacitors or contain an amount of parasitic Y capacitance between the high voltage and low voltage domains. If this Y capacitance is located on the same board as the TPSI2072-Q1, it will act as a capacitive return path.
- A discrete high voltage capacitor could be placed between the GND pin and the SM pin. Or discrete capacitors could be placed between the GND pin and S1 and S2 pins.

• Inductive Components:

- A pair of ferrite beads or a common mode choke with a high frequency impedance in the range of 10 k Ω may be placed in series with the system VDD pin and GND pin supply on the primary side of the TPSI2072-Q1.

High-voltage considerations:

The creepage from the primary side to the secondary side, the creepage from the S1 pin to SM pin, and the creepage from the SM pin to S2 pin of the TPSI2072-Q1 should be maintained according to system requirements. It is most likely that the system designer will avoid any top layer PCB routing underneath the body of the package or between the S1, SM and S2 pins.

Thermal considerations:

If the system designer plans to use the TPSI2072-Q1 in avalanche mode, it is important for the PCB layout to be designed with thermal performance in mind. Proper PCB layout can help dissipate heat from the device to the PCB and keep the junction temperature (T_J) under the absolute maximum rating. Floating inner layer planes or the planes used to implement a stitch capacitor can be drawn beneath the secondary side pins or directly beneath the TPSI2072-Q1 for improved heat dissipation. An example of this can be seen in the [Layout Example](#).

9.4.2 Layout Example

Varying PCB implementations are possible depending on both the system EMI requirements and the system dielectric withstand testing (HiPot) parameters. The following sections detail the [TPSI2072-Q1 EVM with Thermal Optimization](#) with secondary side metallization for optimized thermal performance and the [Interlayer Stitch Capacitance Option for EMI and Thermal Optimization](#).

TPSI2072-Q1 EVM with Thermal Optimization

The TPSI2072-Q1 EVM images below demonstrate a secondary side thermal metallization pattern and internal floating metal that provides thermal relief to the TPSI2072-Q1 during system dielectric withstand testing (HiPot). The [TPSI2072-Q1 Secondary Side Layout Recommendation for Optimized Thermal Performance: Top Layer 1](#) shows the top side creepage and clearance considerations.

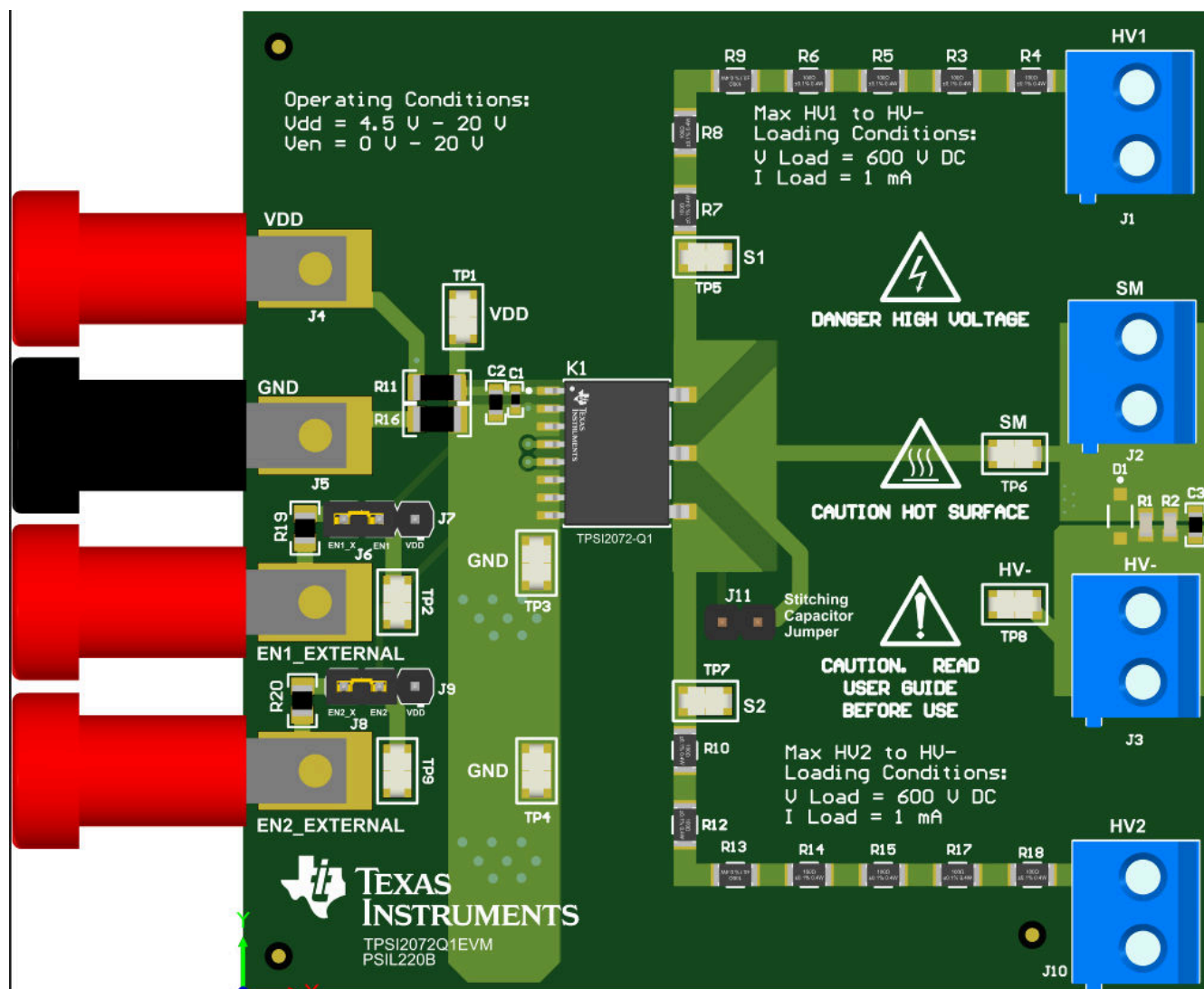
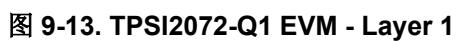


图 9-12. TPSI2072-Q1 EVM - Component View



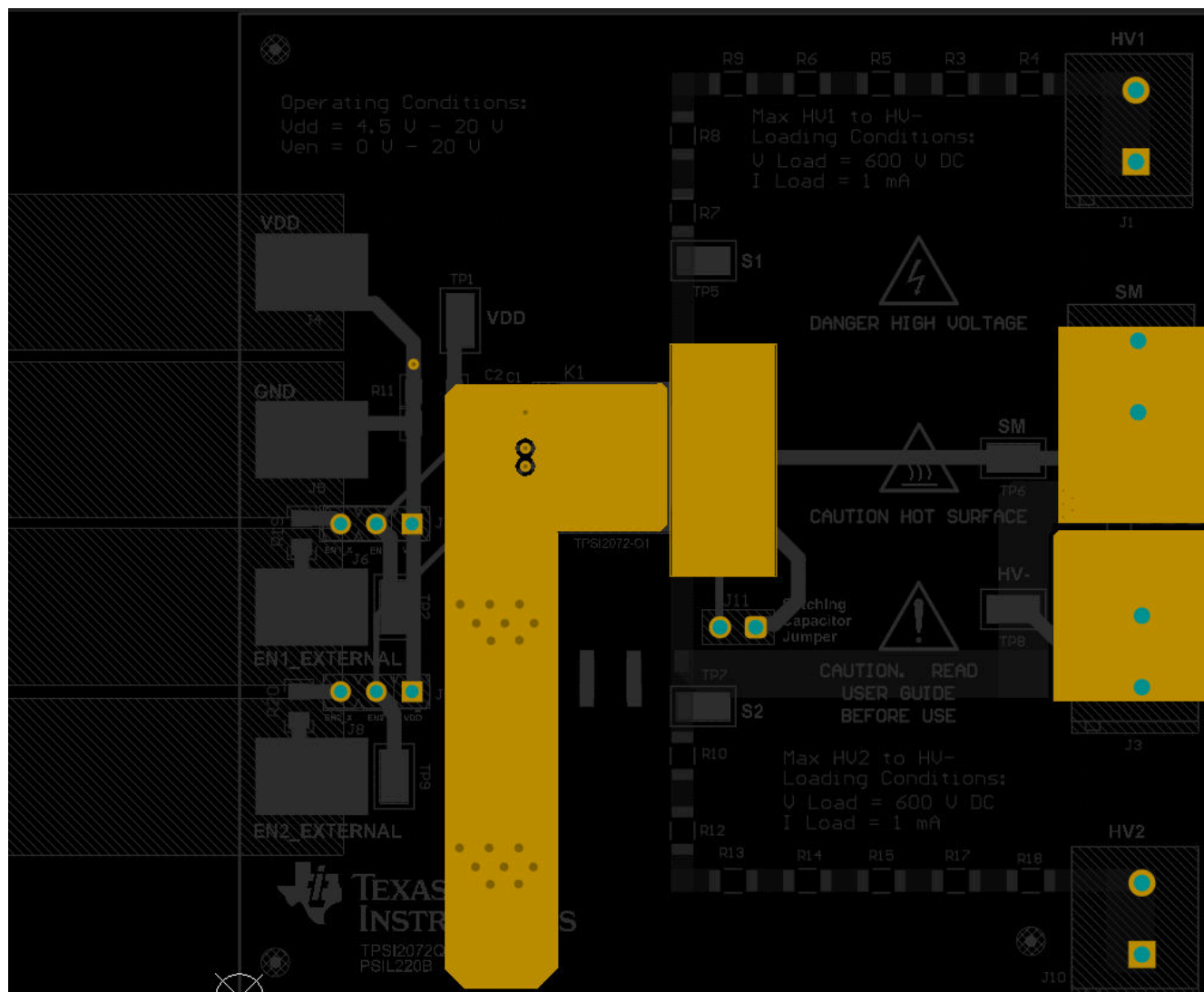


图 9-14. TPSI2072-Q1 EVM - Layer 2

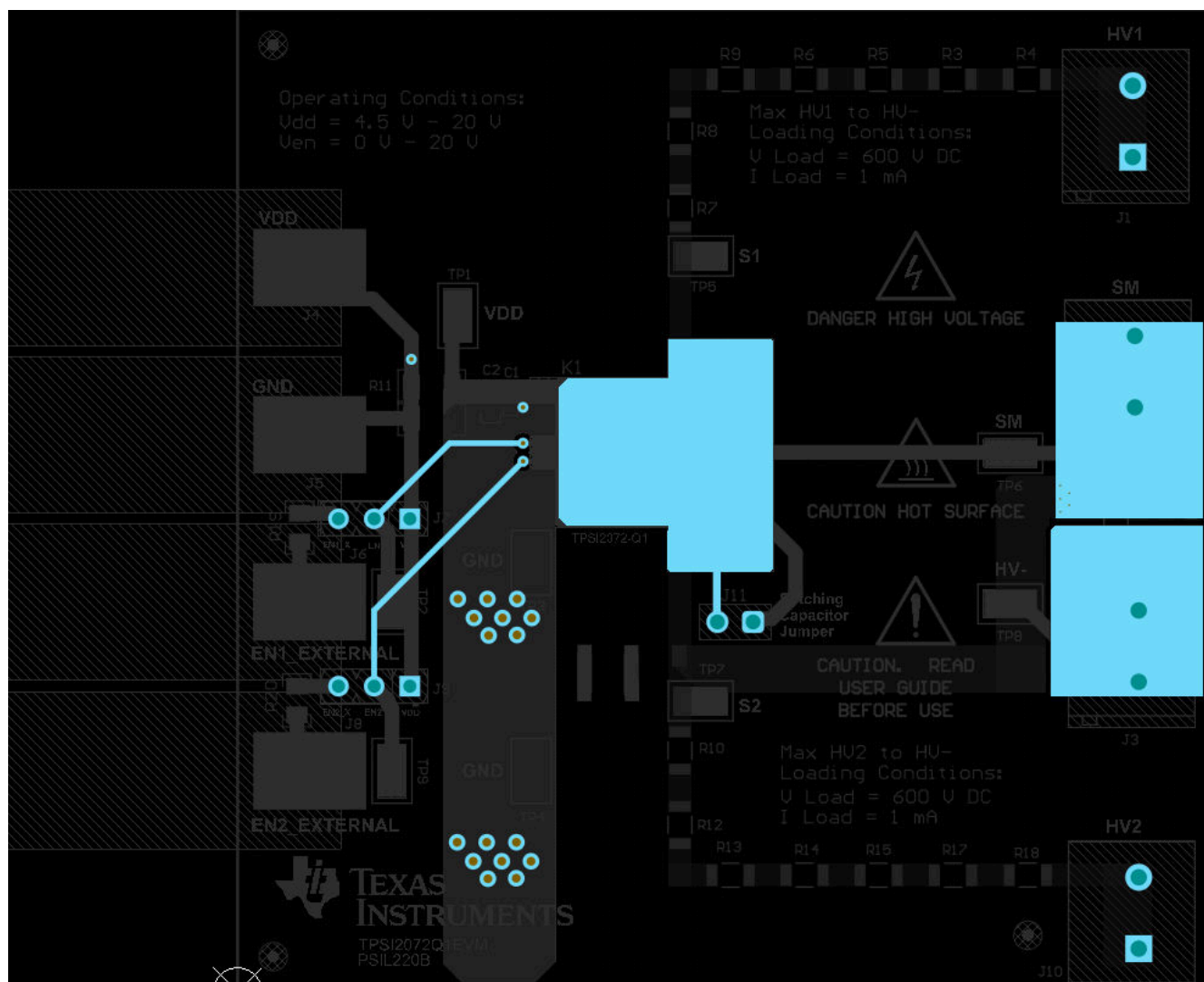


图 9-15. TPSI2072-Q1 EVM - Layer 3

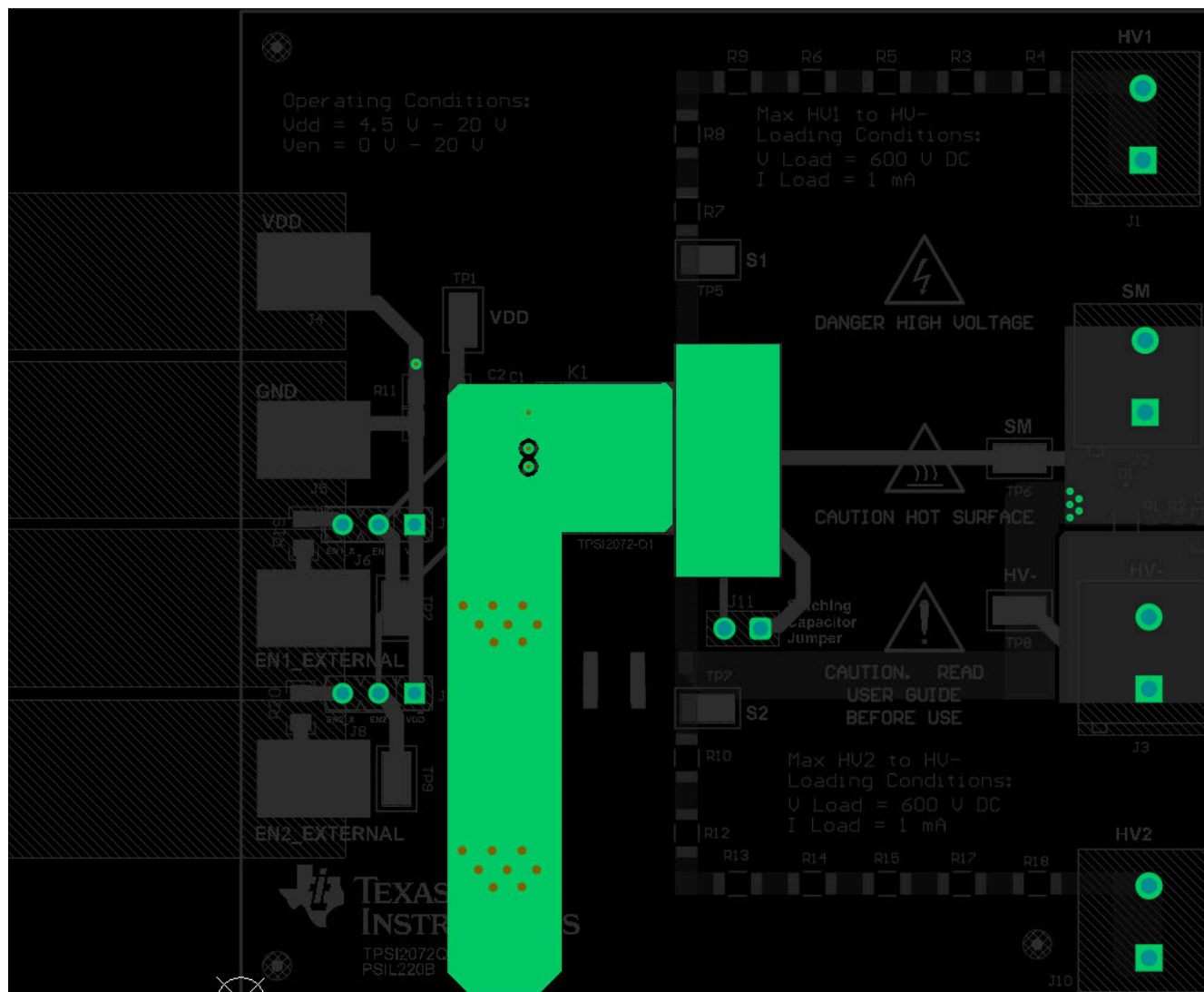


图 9-16. TPSI2072-Q1 EVM - Layer 4

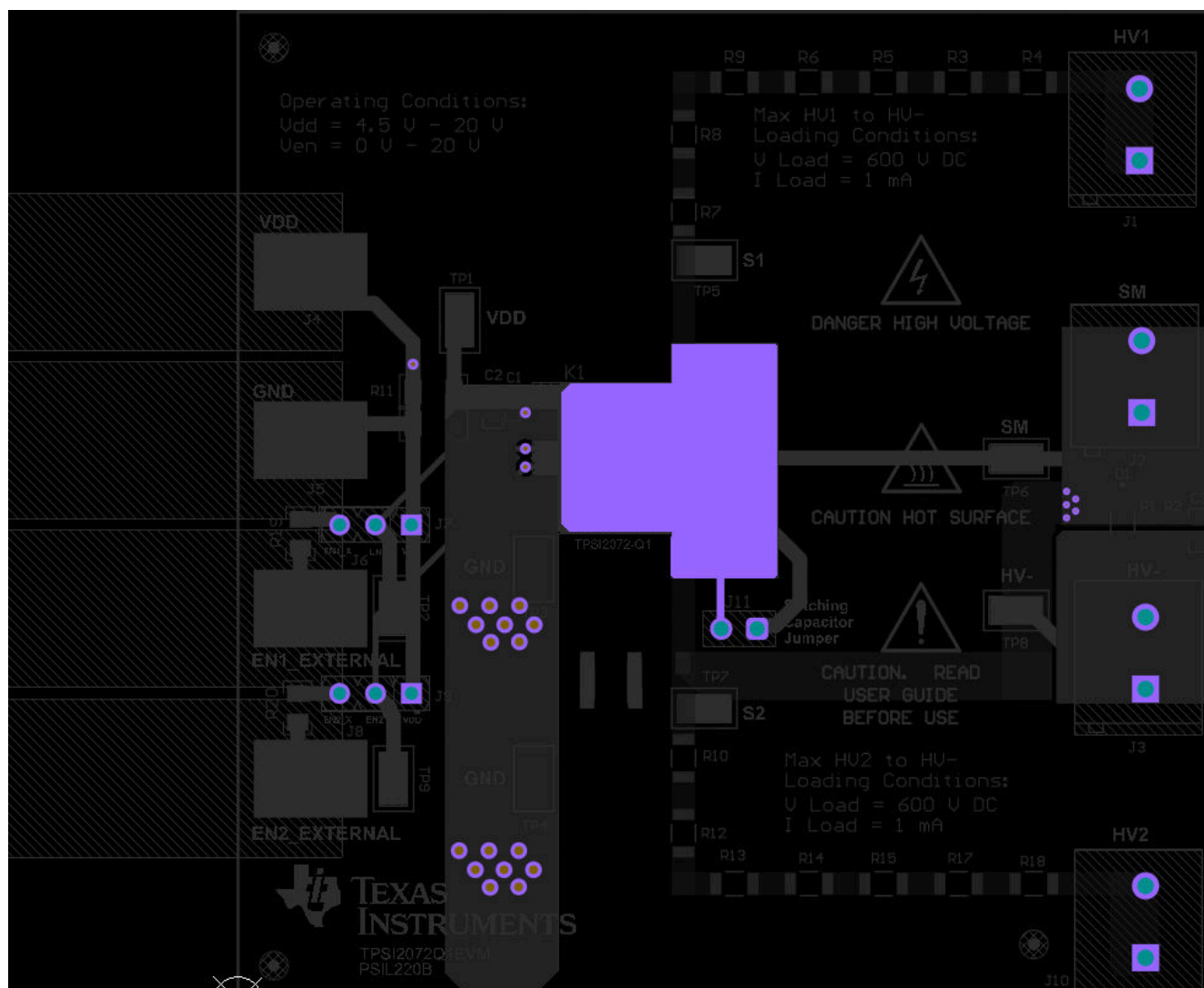


图 9-17. TPSI2072-Q1 EVM - Layer 5

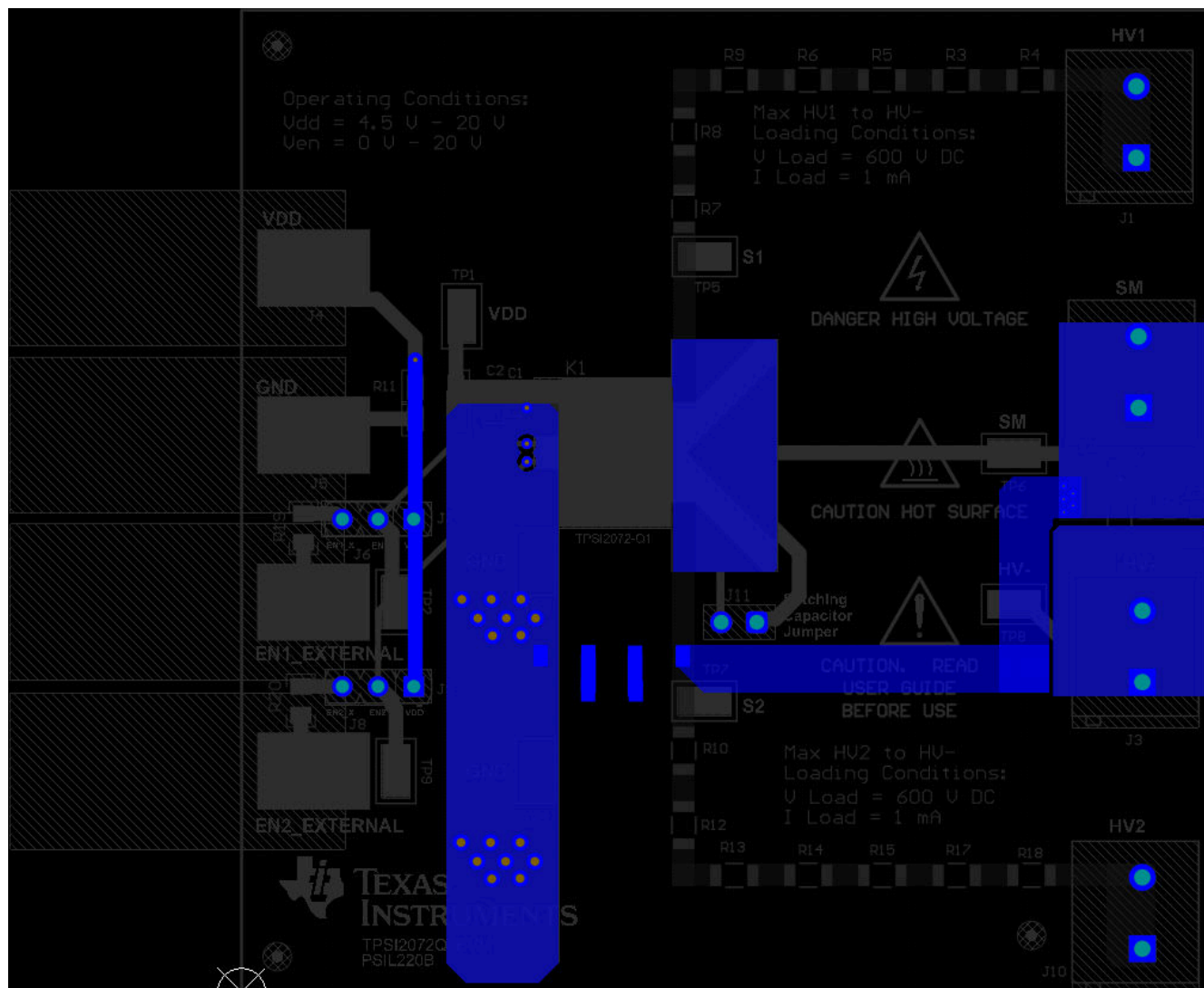


图 9-18. TPSI2072-Q1 EVM - Layer 6

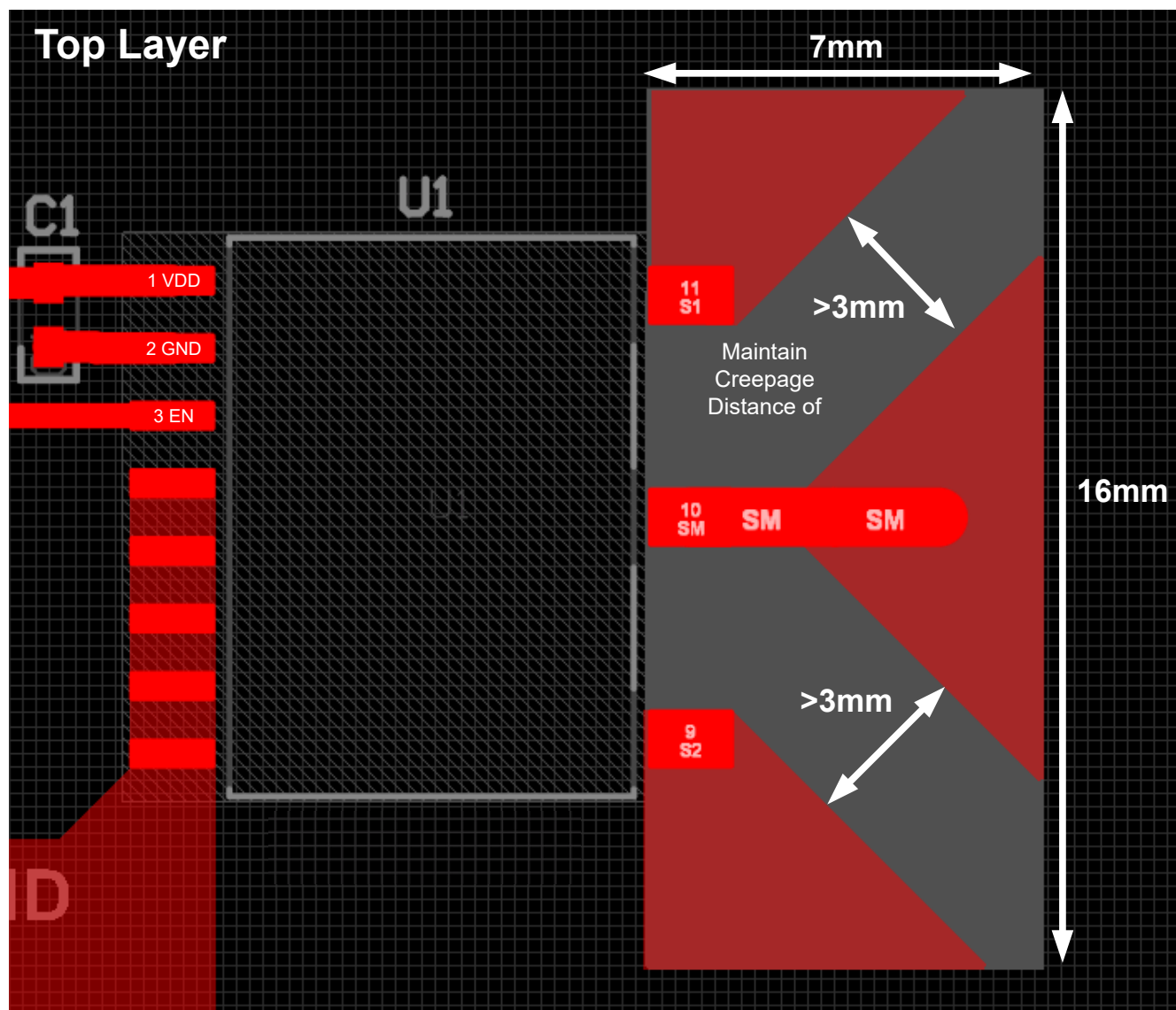


图 9-19. TPSI2072-Q1 Secondary Side Layout Recommendation for Optimized Thermal Performance: Top Layer 1

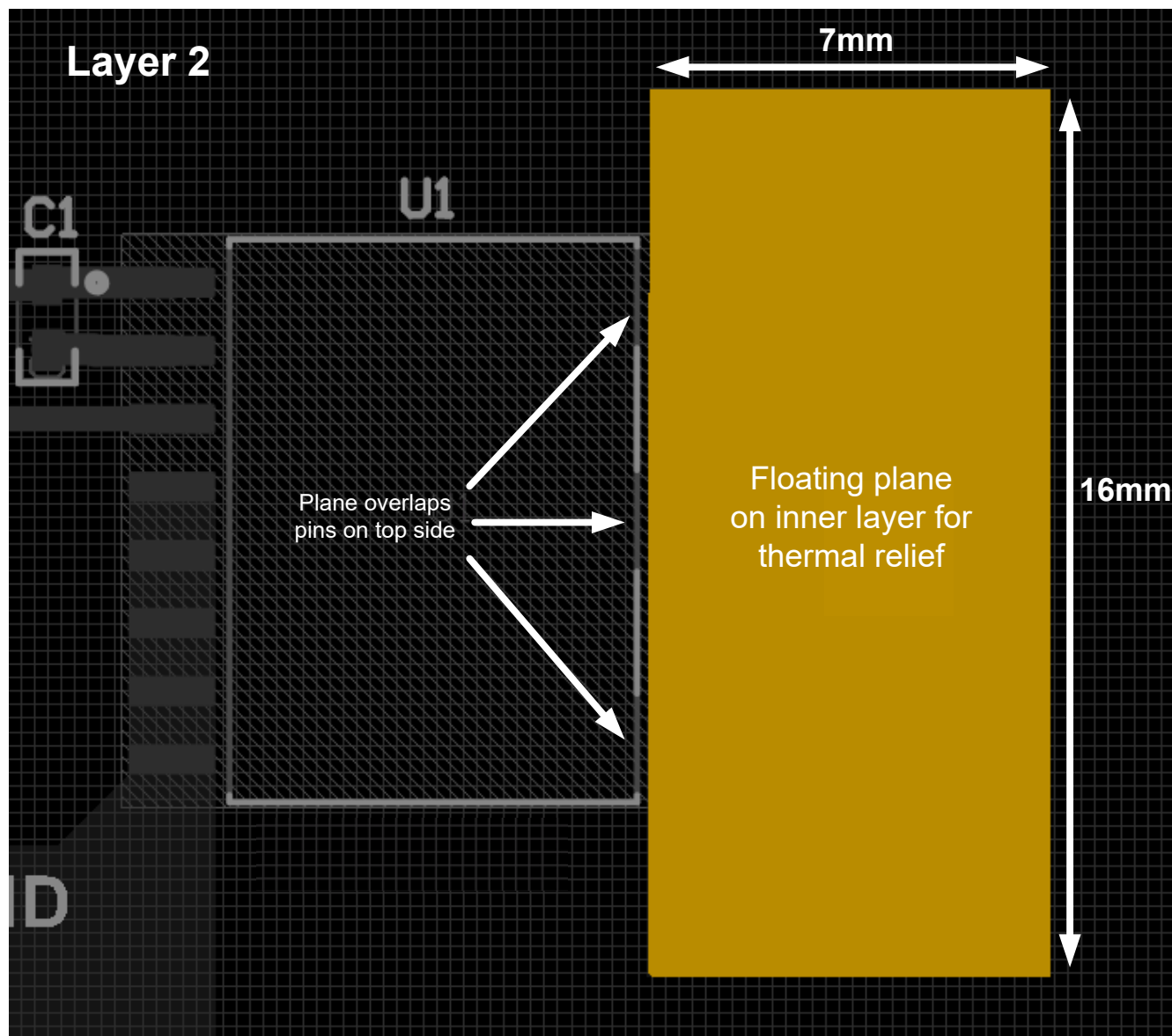


图 9-20. TPSI2072-Q1 Secondary Side Layout Recommendation for Optimized Thermal Performance:
 Inner Layer 2

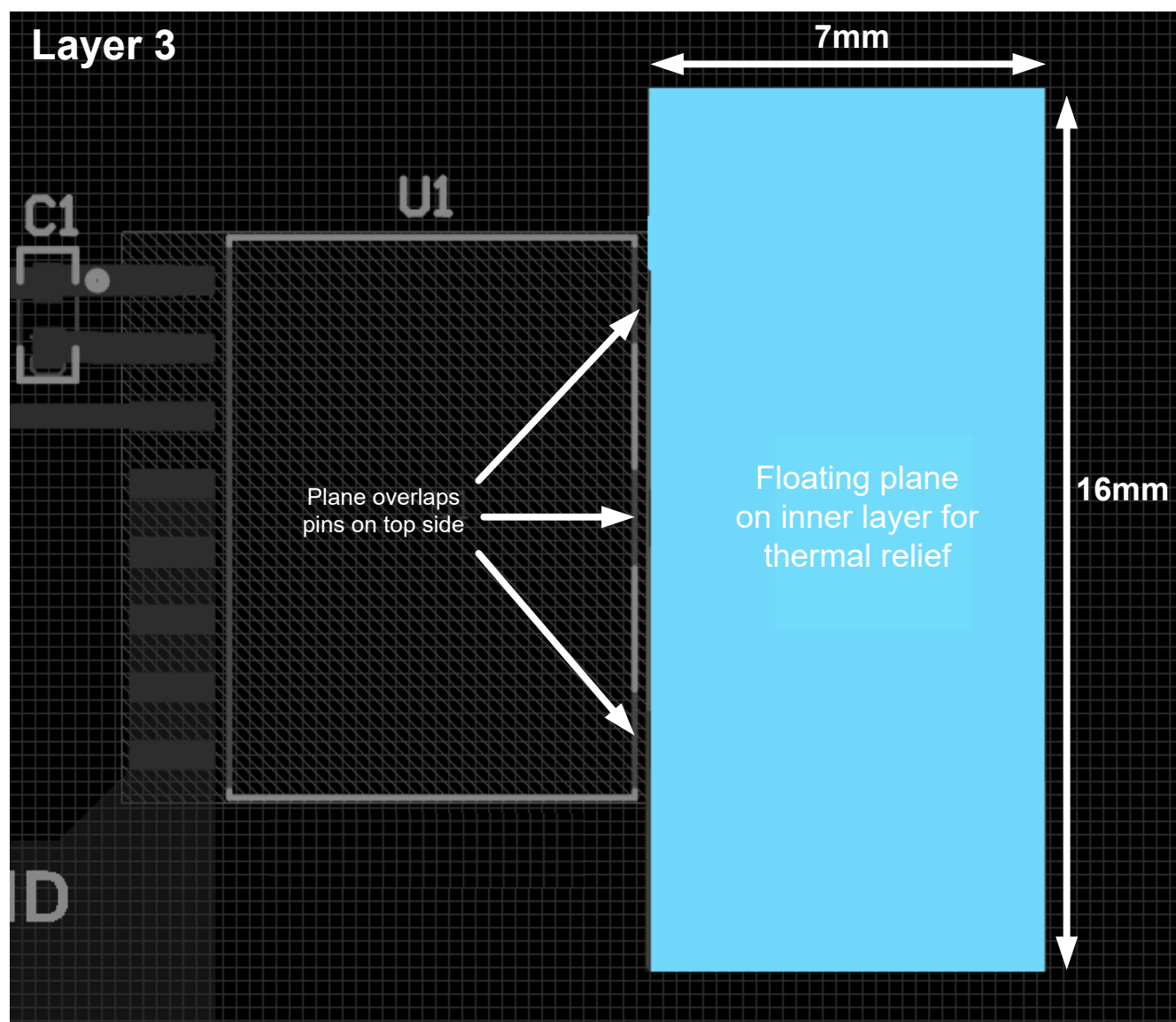


图 9-21. TPSI2072-Q1 Secondary Side Layout Recommendation for Optimized Thermal Performance:
Inner Layer 3

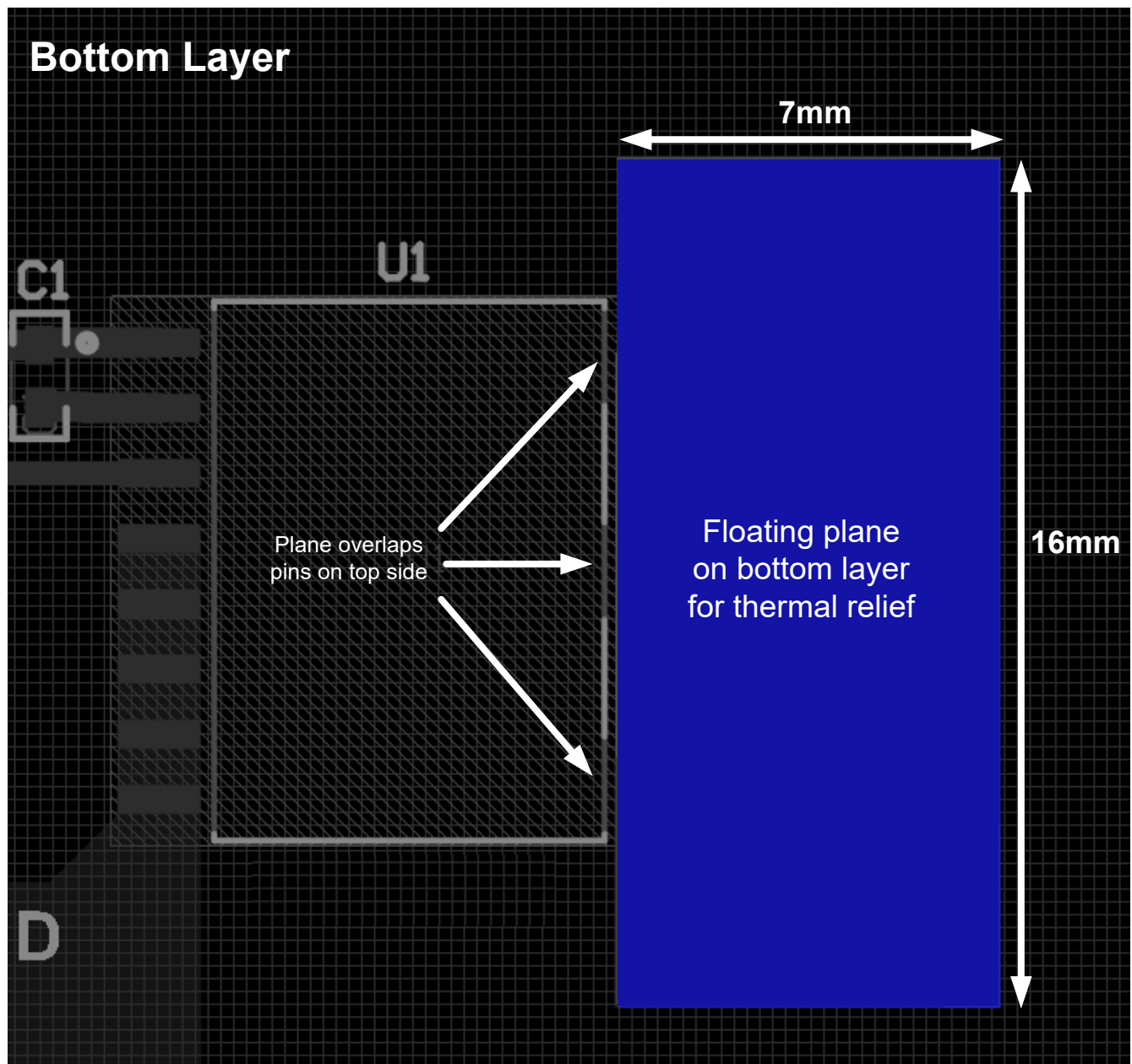


图 9-22. TPSI2072-Q1 Secondary Side Layout Recommendation for Optimized Thermal Performance: Bottom Layer 4

Interlayer Stitch Capacitance Option for EMI and Thermal Optimization

The layout example below demonstrates an EMI optimized and thermally optimized PCB Design for high voltage switching applications. The overlapping metal layers beneath the TPSI2072-Q1 form an interlayer stitching capacitance between the primary side ground and the SM pin and increase the board copper content, improving the thermal performance for dielectric withstand testing (HiPot). Metal islands on the S1, SM, and S2 pins on the top side and inner layers further improve the thermal performance. Care should be taken to maintain both the vertical and horizontal interlayer dielectric (ILD) spacings between high voltage terminals required by the system.

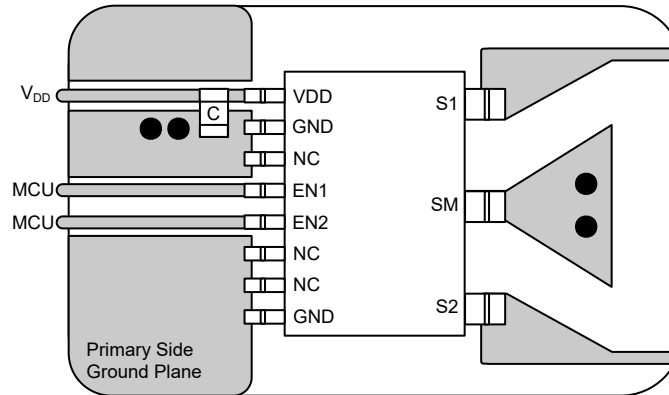


图 9-23. TPSI2072-Q1 Layout with Interlayer Stitch Capacitance: Top Layer (1)

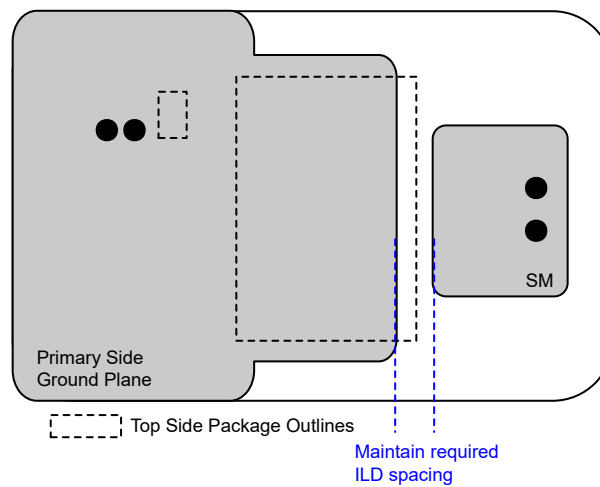


图 9-24. TPSI2072-Q1 Layout with Interlayer Stitch Capacitance: Inner Layer (2,4)

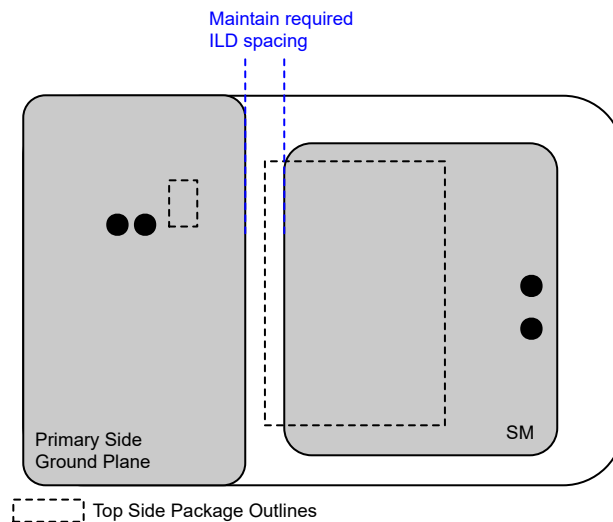


图 9-25. TPSI2072-Q1 Layout with Interlayer Stitch Capacitance: Inner Layer (3)

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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10.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSI2072QDWQRQ1	ACTIVE	SOIC	DWQ	11	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	2072Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

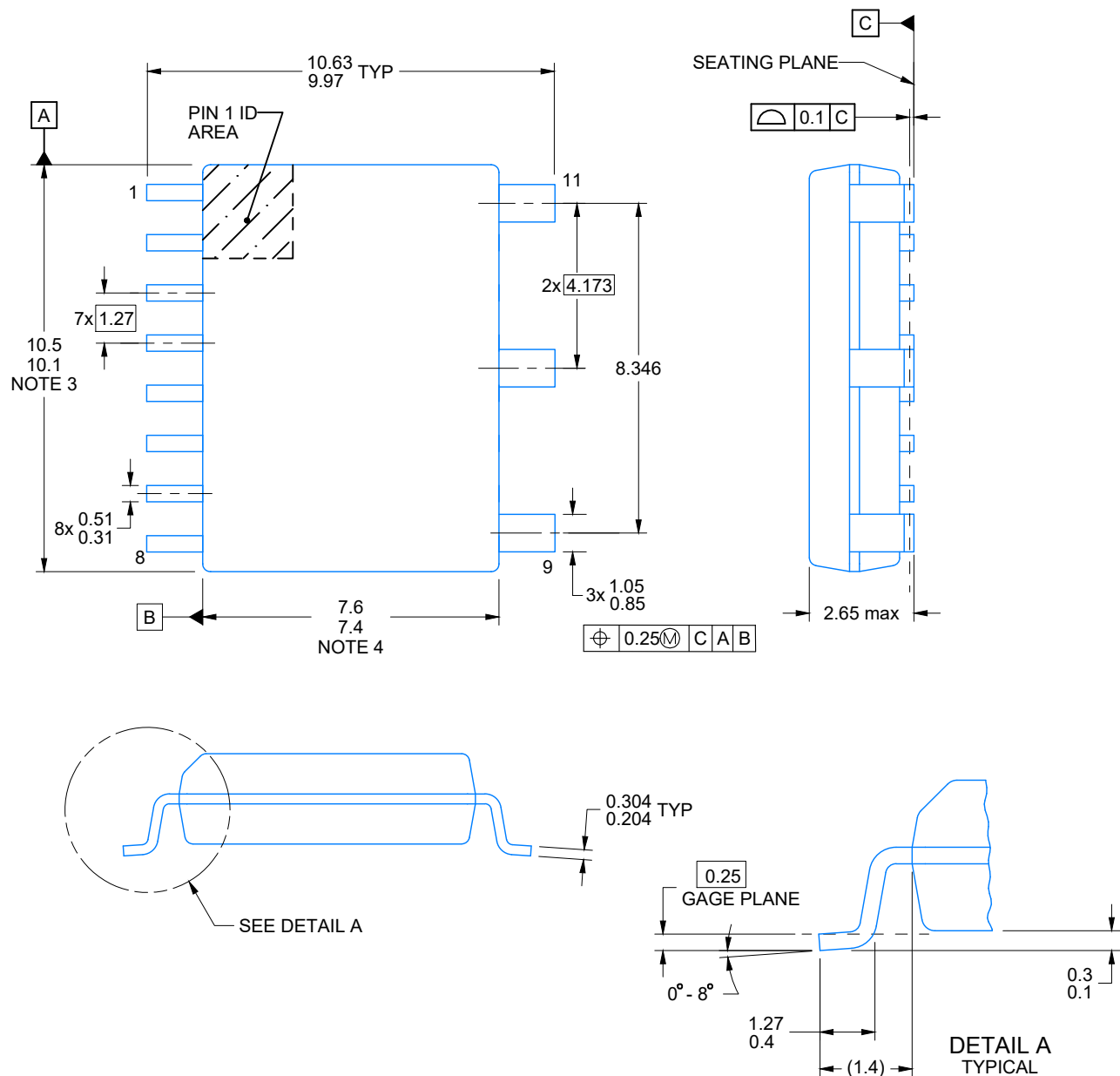
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DWQ0011A

SOIC - 2.65 mm max height

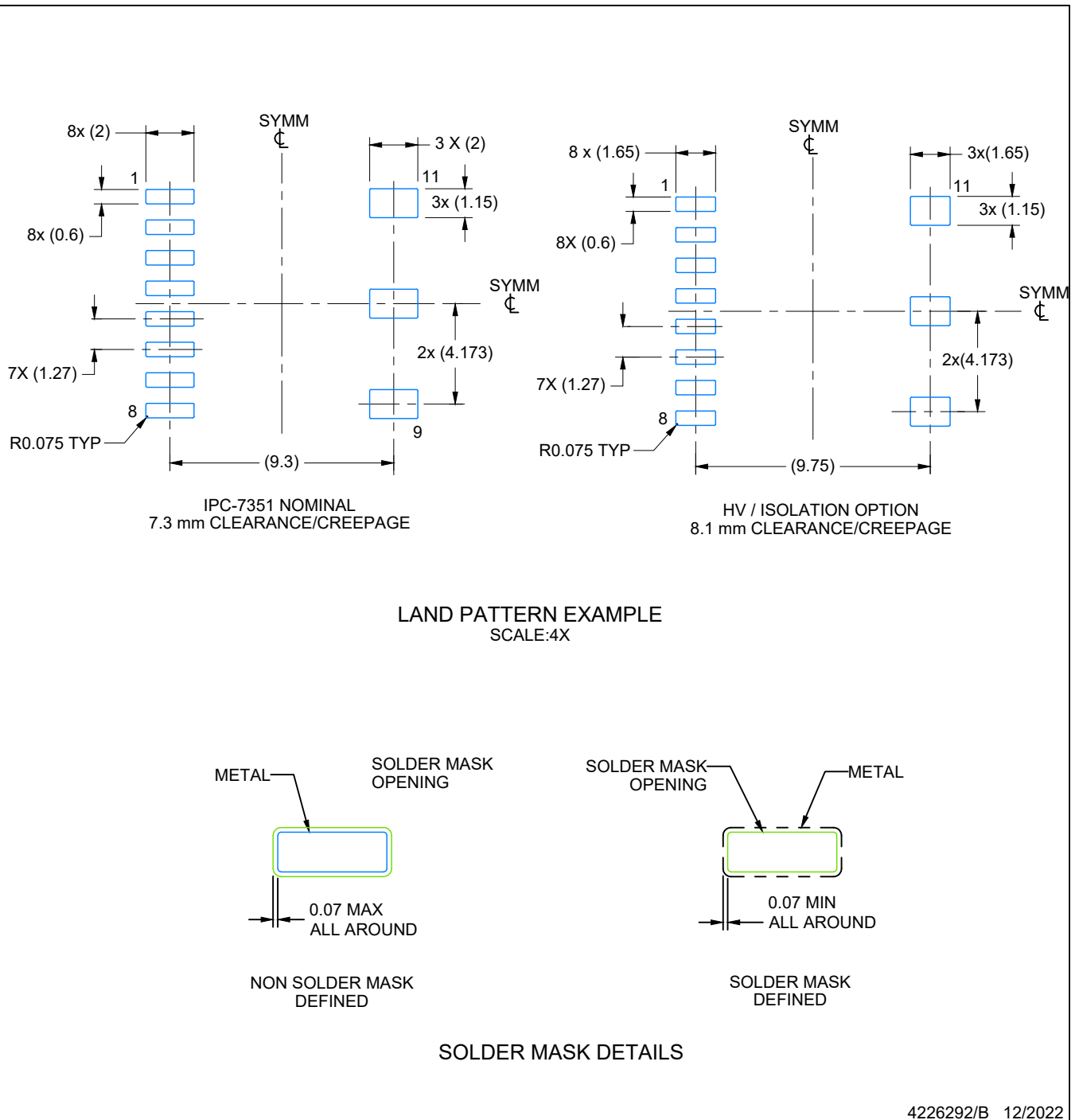
SMALL OUTLINE PACKAGE



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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

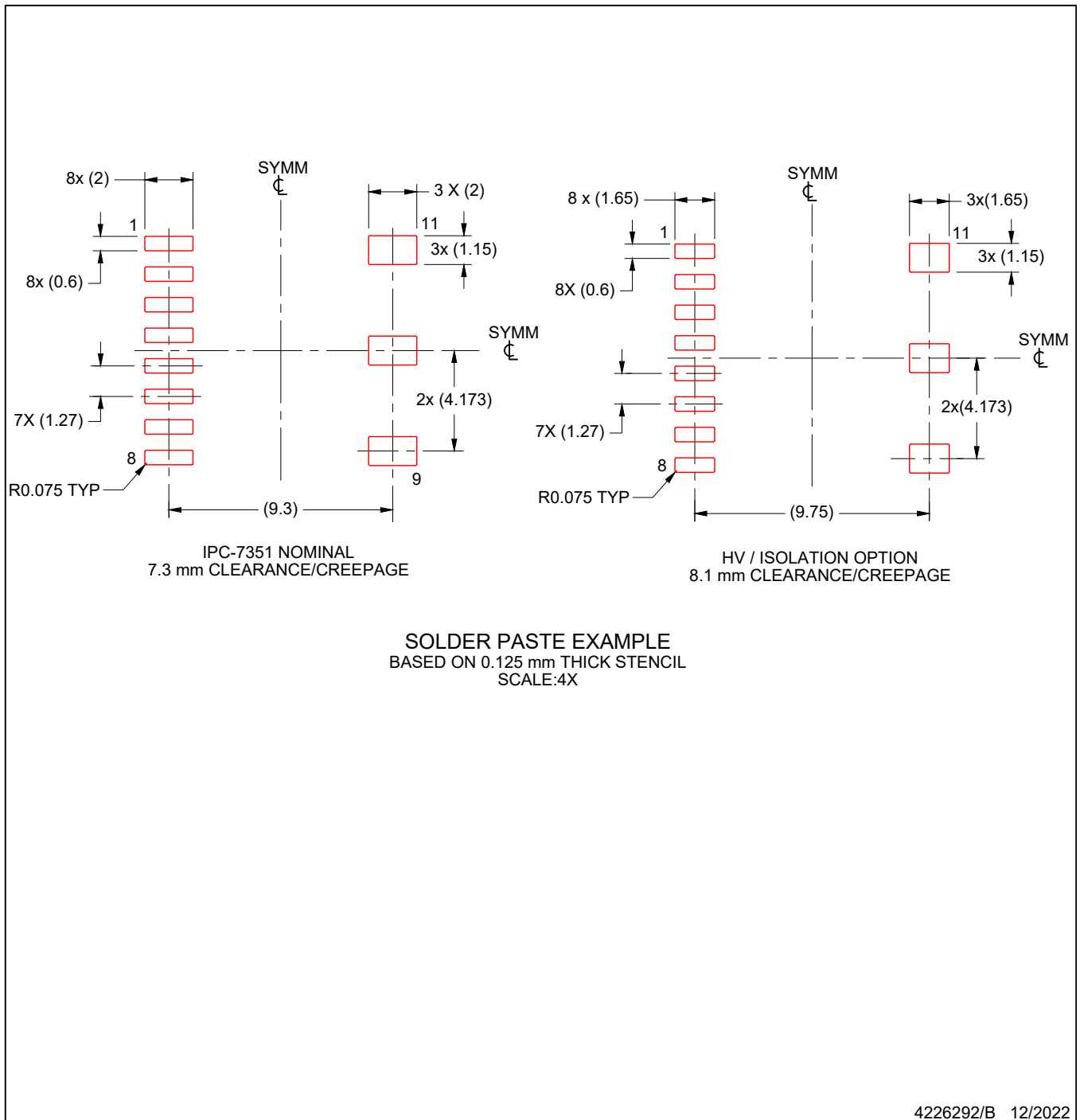


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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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