

# 2N6052

Preferred Device

## Darlington Complementary Silicon Power Transistors

This package is designed for general-purpose amplifier and low frequency switching applications.

### Features

- High DC Current Gain —  $h_{FE} = 3500$  (Typ) @  $I_C = 5.0$  Adc
- Collector-Emitter Sustaining Voltage — @ 100 mA  
 $V_{CEO(sus)} = 100$  Vdc (Min)
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- This is a Pb-Free Device\*

### MAXIMUM RATINGS (Note 1)

| Rating                                                                                | Symbol         | Value        | Unit                     |
|---------------------------------------------------------------------------------------|----------------|--------------|--------------------------|
| Collector-Emitter Voltage                                                             | $V_{CEO}$      | 100          | Vdc                      |
| Collector-Base Voltage                                                                | $V_{CB}$       | 100          | Vdc                      |
| Emitter-Base Voltage                                                                  | $V_{EB}$       | 5.0          | Vdc                      |
| Collector Current – Continuous Peak                                                   | $I_C$          | 12<br>20     | Adc                      |
| Base Current                                                                          | $I_B$          | 0.2          | Adc                      |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$          | 150<br>0.857 | W<br>W/ $^\circ\text{C}$ |
| Operating and Storage Temperature Range                                               | $T_J, T_{stg}$ | -65 to +200  | $^\circ\text{C}$         |

### THERMAL CHARACTERISTICS

| Characteristic                       | Symbol          | Max  | Unit               |
|--------------------------------------|-----------------|------|--------------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 1.17 | $^\circ\text{C/W}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates JEDEC Registered Data.

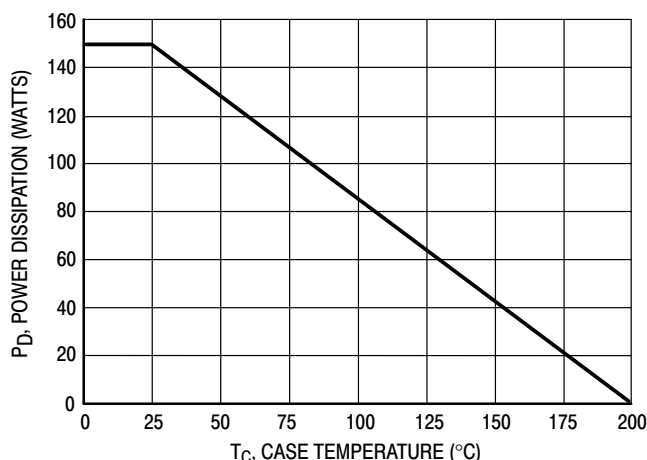


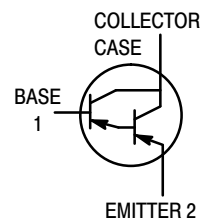
Figure 1. Power Derating



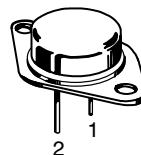
ON Semiconductor®

<http://onsemi.com>

## 12 AMPERE COMPLEMENTARY SILICON POWER TRANSISTOR 100 VOLTS, 150 WATTS



### MARKING DIAGRAM



TO-204AA (TO-3)  
CASE 1-07  
STYLE 1

2N6052 = Device Code  
G = Pb-Free Package  
A = Location Code  
YY = Year  
WW = Work Week  
MEX = Country of Origin

### ORDERING INFORMATION

| Device  | Package           | Shipping       |
|---------|-------------------|----------------|
| 2N6052G | TO-3<br>(Pb-Free) | 100 Units/Tray |

Preferred devices are recommended choices for future use and best overall value.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted) (Note 2)

| Characteristic                                                                                                                                                                                         | Symbol         | Min    | Max        | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|--------|------------|------|
| <b>OFF CHARACTERISTICS</b>                                                                                                                                                                             |                |        |            |      |
| Collector-Emitter Sustaining Voltage (Note 3) ( $I_C = 100\text{ mAdc}$ , $I_B = 0$ )                                                                                                                  | $V_{CEO(sus)}$ | 100    | —          | Vdc  |
| Collector Cutoff Current ( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )                                                                                                                                      | $I_{CEO}$      | —      | 1.0        | mAdc |
| Collector Cutoff Current<br>( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ )<br>( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) | $I_{CEX}$      | —<br>— | 0.5<br>5.0 | mAdc |
| Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )                                                                                                                                       | $I_{EBO}$      | —      | 2.0        | mAdc |

**ON CHARACTERISTICS** (Note 3)

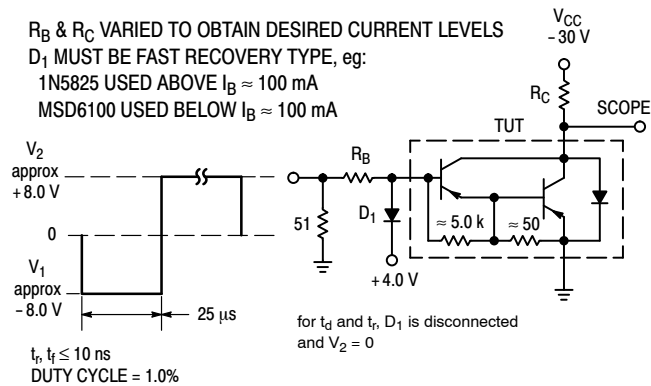
|                                                                                                                                                    |               |            |             |     |
|----------------------------------------------------------------------------------------------------------------------------------------------------|---------------|------------|-------------|-----|
| DC Current Gain<br>( $I_C = 6.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )<br>( $I_C = 12\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )                 | $h_{FE}$      | 750<br>100 | 18,000<br>— | —   |
| Collector-Emitter Saturation Voltage<br>( $I_C = 6.0\text{ Adc}$ , $I_B = 24\text{ mAdc}$ )<br>( $I_C = 12\text{ Adc}$ , $I_B = 120\text{ mAdc}$ ) | $V_{CE(sat)}$ | —<br>—     | 2.0<br>3.0  | Vdc |
| Base-Emitter Saturation Voltage ( $I_C = 12\text{ Adc}$ , $I_B = 120\text{ mAdc}$ )                                                                | $V_{BE(sat)}$ | —          | 4.0         | Vdc |
| Base-Emitter On Voltage ( $I_C = 6.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )                                                                     | $V_{BE(on)}$  | —          | 2.8         | Vdc |

**DYNAMIC CHARACTERISTICS**

|                                                                                                                                                                        |            |     |     |     |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|-----|-----|
| Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio<br>( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ ) | $ h_{fe} $ | 4.0 | —   | MHz |
| Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )                                                                                     | $C_{ob}$   | —   | 500 | pF  |
| Small-Signal Current Gain ( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )                                                                | $h_{fe}$   | 300 | —   | —   |

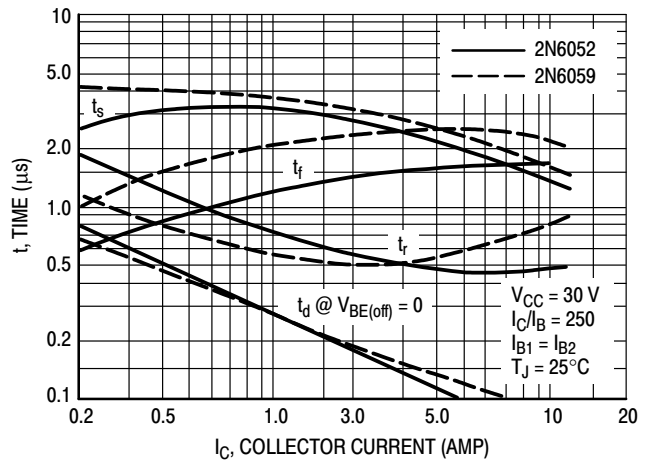
2. Indicates JEDEC Registered Data.

3. Pulse test: Pulse Width =  $300\text{ }\mu\text{s}$ , Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.

**Figure 2. Switching Times Test Circuit**



**Figure 3. Switching Times**

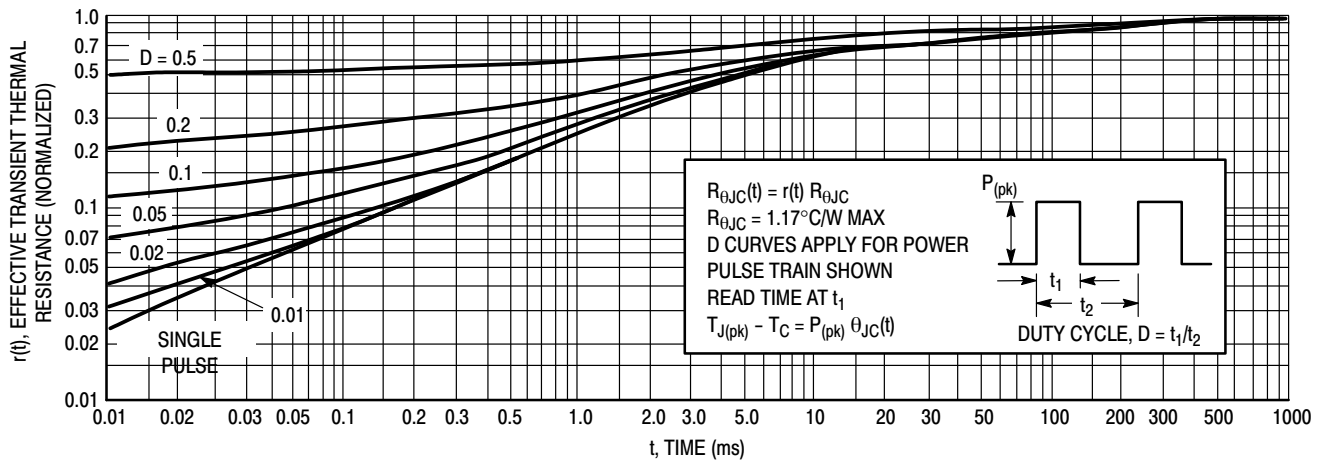


Figure 4. Thermal Response

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, and 6 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^\circ\text{C}$ ;  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

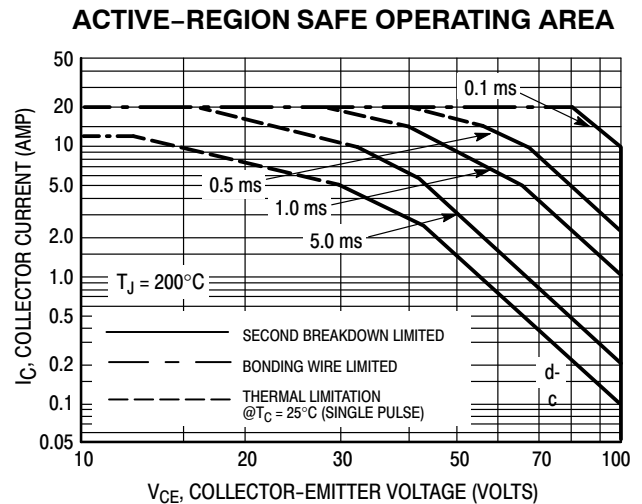


Figure 5.

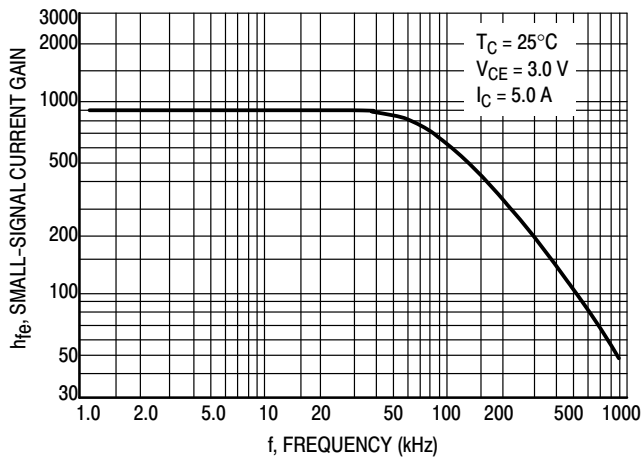


Figure 6. Small-Signal Current Gain

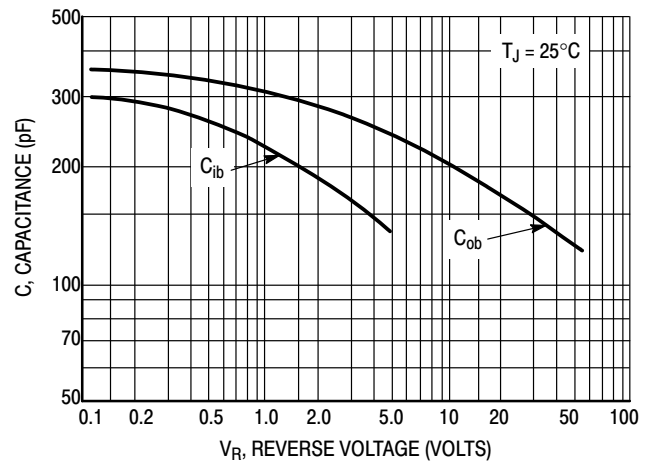


Figure 7. Capacitance

# 2N6052

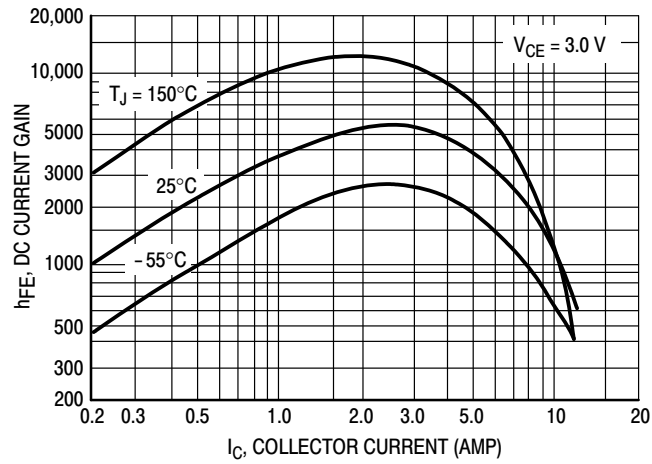


Figure 8. DC Current Gain

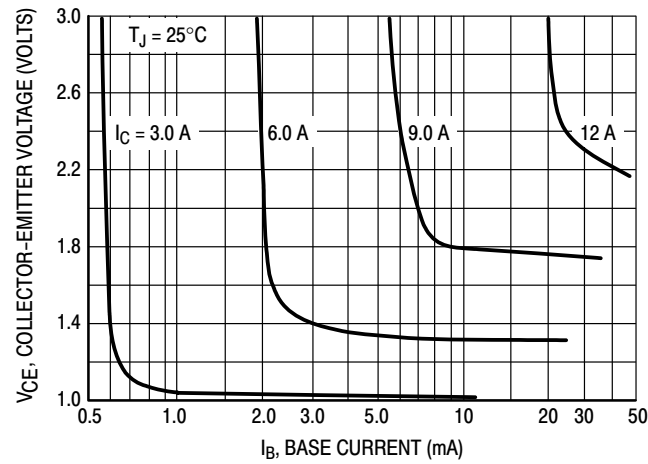


Figure 9. Collector Saturation Region

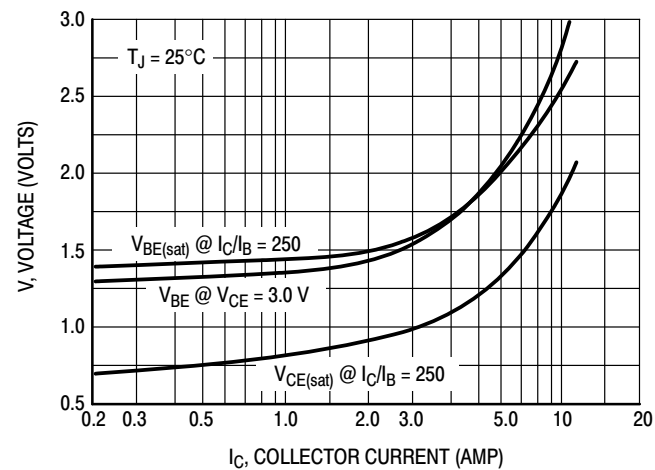
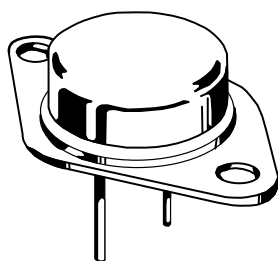


Figure 10. "On" Voltages

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

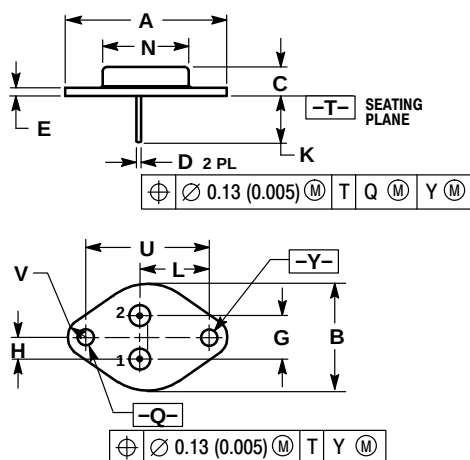
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TO-204 (TO-3)  
CASE 1-07  
ISSUE Z

DATE 05/18/1988

SCALE 1:1



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 1.550 REF |       | 39.37 REF   |       |
| B   | ---       | 1.050 | ---         | 26.67 |
| C   | 0.250     | 0.335 | 6.35        | 8.51  |
| D   | 0.038     | 0.043 | 0.97        | 1.09  |
| E   | 0.055     | 0.070 | 1.40        | 1.77  |
| G   | 0.430 BSC |       | 10.92 BSC   |       |
| H   | 0.215 BSC |       | 5.46 BSC    |       |
| K   | 0.440     | 0.480 | 11.18       | 12.19 |
| L   | 0.665 BSC |       | 16.89 BSC   |       |
| N   | ---       | 0.830 | ---         | 21.08 |
| Q   | 0.151     | 0.165 | 3.84        | 4.19  |
| U   | 1.187 BSC |       | 30.15 BSC   |       |
| V   | 0.131     | 0.188 | 3.33        | 4.77  |

STYLE 1:  
PIN 1. BASE  
2. EMITTER  
CASE: COLLECTOR

STYLE 2:  
PIN 1. BASE  
2. COLLECTOR  
CASE: EMITTER

STYLE 3:  
PIN 1. GATE  
2. SOURCE  
CASE: DRAIN

STYLE 4:  
PIN 1. GROUND  
2. INPUT  
CASE: OUTPUT

STYLE 5:  
PIN 1. CATHODE  
2. EXTERNAL TRIP/DELAY  
CASE: ANODE

STYLE 6:  
PIN 1. GATE  
2. EMITTER  
CASE: COLLECTOR

STYLE 7:  
PIN 1. ANODE  
2. OPEN  
CASE: CATHODE

STYLE 8:  
PIN 1. CATHODE #1  
2. CATHODE #2  
CASE: ANODE

STYLE 9:  
PIN 1. ANODE #1  
2. ANODE #2  
CASE: CATHODE

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