

Industry First Low Capacitance ESD Protection Arrays with Backdrive Protection

Product Description

The CM1223 family of diode arrays has been designed to provide ESD protection for electronic components or subsystems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series, which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N , to absorb positive ESD strikes and provide ESD protection for the V_P rail. An additional diode is integrated to serve as backdrive current protection. The CM1223 protects against ESD pulses up to ± 8 kV per the IEC 61000-4-2 standard. In addition, all pins are protected from contact discharges of greater than ± 15 kV as outlined by the MIL-STD-883D (Method 3015) specification for Human Body Model (HBM) ESD.

These devices are particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (Firewire[®], iLink[™]), serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives, as well as other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

Features

- Two, Four, and Eight Channels of ESD Protection with Integrated Backdrive Protection on all Lines
- Provides ESD Protection to IEC61000-4-2 Level 4: ± 8 kV Contact Discharge, ± 15 kV Air Discharge
- Low Channel Input Capacitance of 1.0 pF (typical)
- Minimal Capacitance Change with Temperature and Voltage
- Channel I/O to GND Capacitance Difference of 0.02 pF Typical is Ideal for Differential Signals
- Mutual Capacitance between Signal Pin and Adjacent Signal Pin at 0.11 pF (typical)
- Zener Diode Protects Supply Rail and Eliminates the Need for External Bypass Capacitors
- Pin Compatible with CM1213-02, -04, and -08
- Each I/O Pin Can Withstand over 1000 ESD Strikes
- Available in SOT, and MSOP Packages
- These Devices are Pb-Free and are RoHS Compliant

Applications

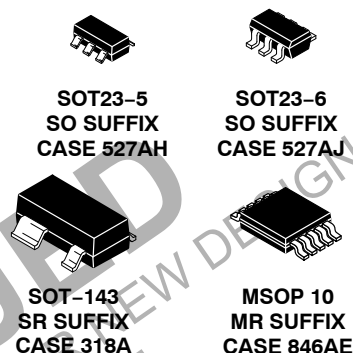
- USB 2.0 Ports at 480 Mbps in Desktop PCs, Notebooks and Peripherals
- IEEE1394 Firewire[®] Ports at 400 Mbps / 800 Mbps
- DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays

- UDI and Display Ports
- Serial ATA Ports in Desktop PCs and Hard Disk Drives
- PCI Express Ports
- General Purpose High-speed Data Line ESD Protection



ON Semiconductor[®]

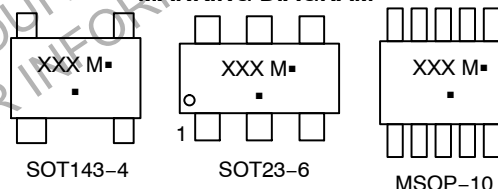
<http://onsemi.com>



BLOCK DIAGRAM

(see page 2)

MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

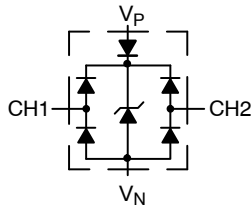
ORDERING INFORMATION

Device	Package	Shipping
CM1223-02SO	SOT23-5 (Pb-Free)	3000/Tape & Reel
CM1223-02SR	SOT143-4 (Pb-Free)	3000/Tape & Reel
CM1223-04SO	SOT23-6 (Pb-Free)	3000/Tape & Reel
CM1223-04MR	MSOP-10 (Pb-Free)	4000/Tape & Reel
CM1223-08MR	MSOP-10 (Pb-Free)	4000/Tape & Reel

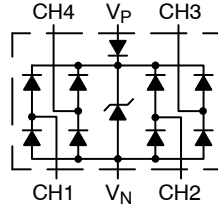
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

CM1223

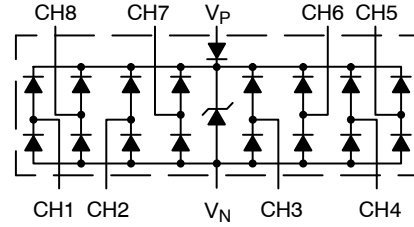
BLOCK DIAGRAM



CM1223-02SO
CM1223-02SR



CM1223-04SO
CM1223-04MR



CM1223-08MR

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

Table 1. PIN DESCRIPTIONS

2-Channel, 5-Lead SOT23-5 Package			
Pin	Name	Type	Description
1	NC		No Connect
2	V _N	GND	Negative voltage supply rail
3	CH1	I/O	ESD Channel
4	CH2	I/O	ESD Channel
5	V _P	PWR	Positive voltage supply rail

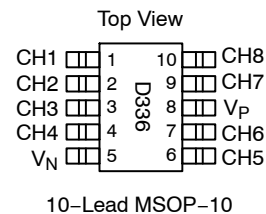
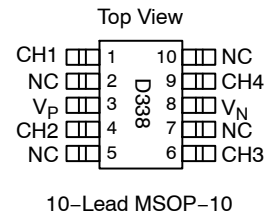
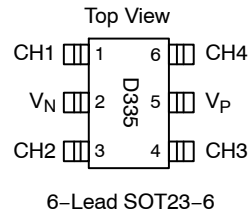
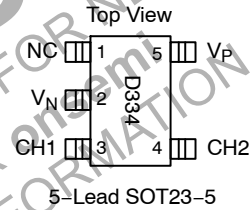
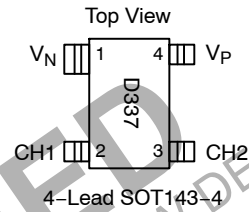
4-Channel, 6-Lead SOT23-6 Package			
Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	V _N	GND	Negative voltage supply rail
3	CH2	I/O	ESD Channel
4	CH3	I/O	ESD Channel
5	V _P	PWR	Positive voltage supply rail
6	CH4	I/O	ESD Channel

4-Channel, 10-Lead MSOP-10 Package			
Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	NC		No Connect
3	V _P	PWR	Positive voltage supply rail
4	CH2	I/O	ESD Channel
5	NC		No Connect
6	CH3	I/O	ESD Channel
7	NC		No Connect
8	V _N	GND	Negative voltage supply rail
9	CH4	I/O	ESD Channel
10	NC		No Connect

8-Channel, 10-Lead MSOP-10 Package			
Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	CH3	I/O	ESD Channel
4	CH4	I/O	ESD Channel
5	V _N	GND	Negative voltage supply rail
6	CH5	I/O	ESD Channel
7	CH6	I/O	ESD Channel
8	V _P	PWR	Positive voltage supply rail
9	CH7	I/O	ESD Channel
10	CH8	I/O	ESD Channel

2-Channel, 4-Lead SOT143-4 Package			
Pin	Name	Type	Description
1	V _N	GND	Negative voltage supply rail
2	CH1	I/O	ESD Channel
3	CH2	I/O	ESD Channel
4	V _P	PWR	Positive voltage supply rail

PACKAGE / PINOUT DIAGRAMS



SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Supply Voltage ($V_P - V_N$)	6.0	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	$(V_N - 0.5)$ to $(V_P + 0.5)$	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	-40 to +85	°C
Package Power Rating SOT143-4 Package (CM1223-02SR) SOT23-5 Package (CM1223-02SO) SOT23-6 Package (CM1223-04SO) MSOP-10 Package (CM1223-04MR) MSOP-10 Package (CM1223-08MR)	225 225 225 400 400	mW

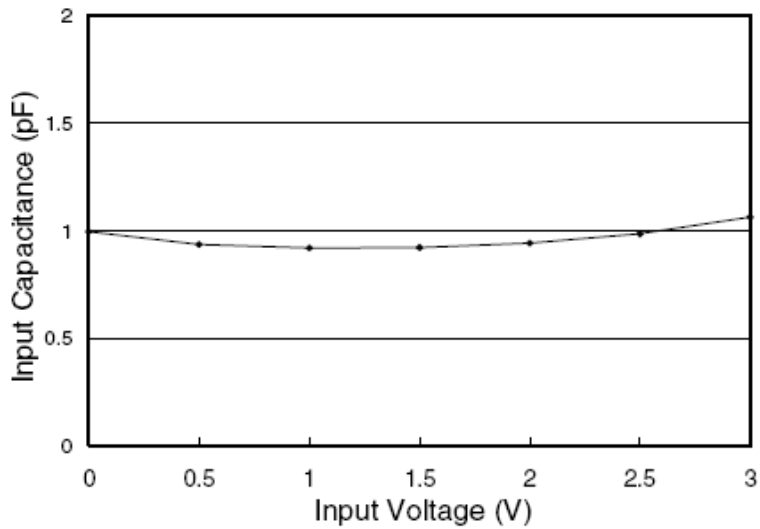
Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_P	Operating Supply Voltage ($V_P - V_N$)			3.3	5.5	V
I_P	Operating Supply Current	$(V_P - V_N) = 3.3$ V			8.0	μA
V_{SCL}	Signal Clamp Voltage Positive Transients Negative Transients	$I_F = 8$ mA; $T_A = 25^\circ\text{C}$	6.7 0.60	8.2 0.80		V
I_{LEAK}	Channel Leakage Current	$T_A = 25^\circ\text{C}$; $V_P = 5$ V, $V_N = 0$ V		±0.1	±1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V		1.0	1.5	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V		0.02		pF
C_{MUTUAL}	Mutual Capacitance between signal pin and adjacent signal pin	At 1 MHz, $V_P = 3.3$ V, $V_N = 0$ V, $V_{IN} = 1.65$ V		0.11		pF
V_{ESD}	ESD Protection – Peak Discharge Voltage at any channel input, in system a) Contact discharge per IEC 61000-4-2 standard b) Human Body Model, MIL-STD-883, Method 3015	$T_A = 25^\circ\text{C}$; (Notes 3 and 4) $T_A = 25^\circ\text{C}$; (Notes 2 and 4)	±8 ±15			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	$T_A = 25^\circ\text{C}$, $I_{PP} = 1$ A, $t_P = 8/20$ μS (Note 4)		+8.8 -1.4		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	$T_A = 25^\circ\text{C}$, $I_{PP} = 1$ A, $t_P = 8/20$ μS Any I/O pin to Ground (Note 4)		0.7 0.4		Ω

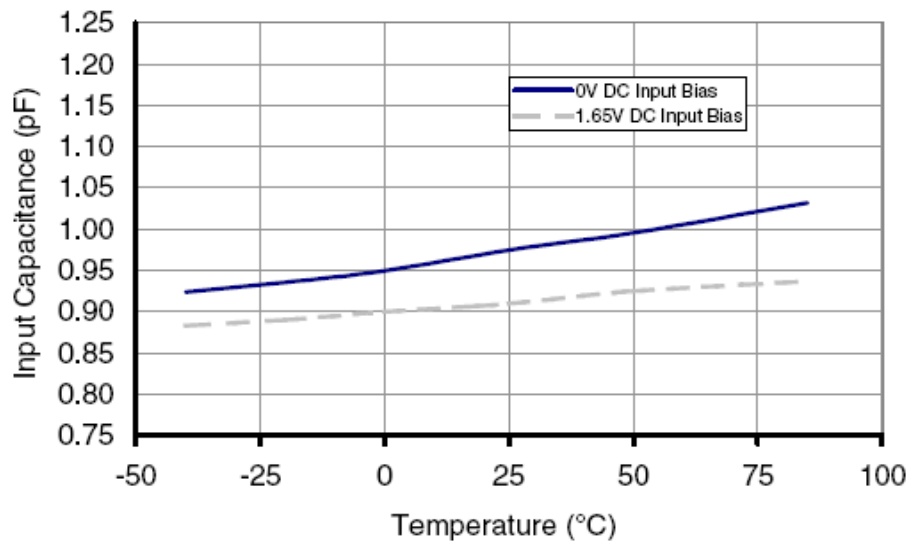
1. All parameters specified at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted.
2. Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge} = 100$ pF, $R_{Discharge} = 1.5$ kΩ, $V_P = 3.3$ V, V_N grounded.
3. Standard IEC 61000-4-2 with $C_{Discharge} = 150$ pF, $R_{Discharge} = 330$ Ω, $V_P = 3.3$ V, V_N grounded.
4. These measurements performed with no external capacitor on V_P (V_P floating).

PERFORMANCE INFORMATION

Input Channel Capacitance Performance Curves

Typical Variation of C_{IN} vs. V_{IN}

($f=1\text{MHz}$, $V_P = 3.3\text{V}$, $V_N = 0\text{V}$, $0.1\text{ }\mu\text{F}$ chip capacitor between V_P and V_N , 25°C)

Typical Variation of C_{IN} vs. Temp

($f=1\text{MHz}$, $V_{IN}=30\text{mV}$, $V_P = 3.3\text{V}$, $V_N = 0\text{V}$, $0.1\text{ }\mu\text{F}$ chip capacitor between V_P and V_N)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

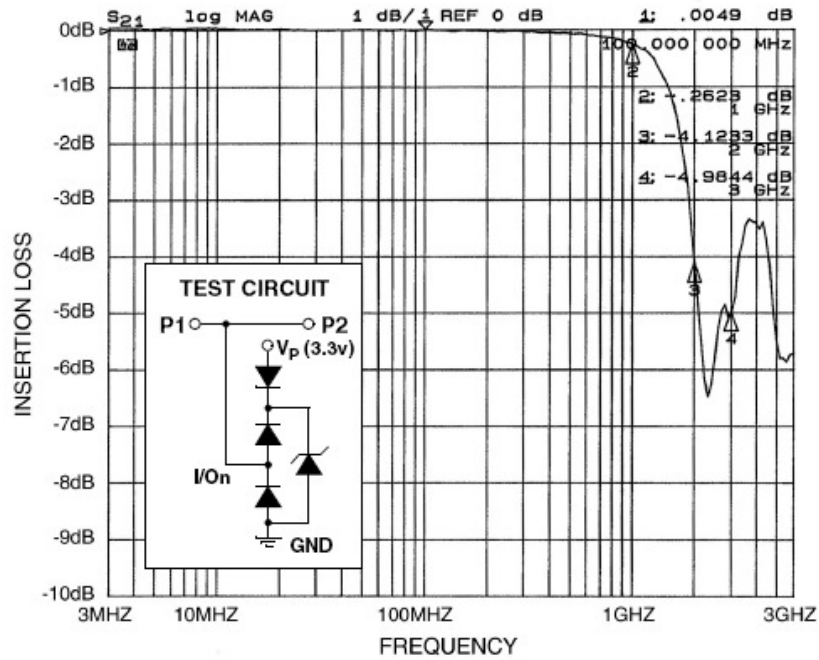


Figure 1. Insertion Loss (S21) vs. Frequency (0 V DC Bias, $V_p = 3.3$ V, MSOP-10 Package)

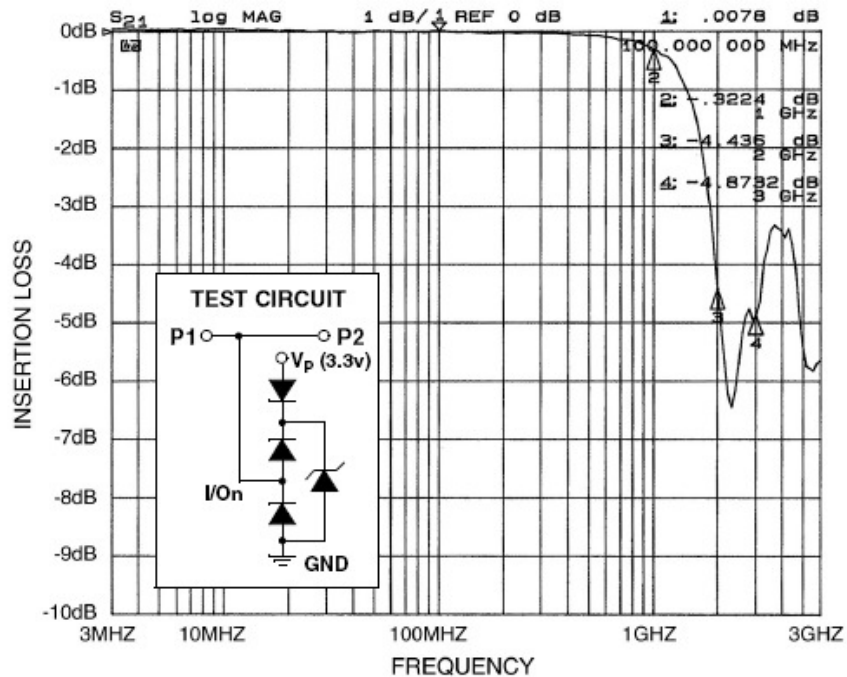


Figure 2. Insertion Loss (S21) vs. Frequency (2.5 V DC Bias, $V_p = 3.3$ V, MSOP-10 Package)

BACKDRIVE PROTECTION

Backdrive protection is needed to block against backdrive current flowing from a high potential voltage node toward a lower potential voltage node through the interface cable.

For example, consider a DVD player connected to a TV via an HDMI interface. If the DVD player is switched off and the TV is left on, there is a possibility of reverse current flow back into the main power supply rail of the DVD player. Typically, the DVD's power supply has some form of associated bulk supply capacitance, and it is possible over time to charge that bulk supply capacitance to some intermediate level.

If that level rises above the power-on-reset (POR) voltage level of some of the integrated circuits, the DVD player may not reset properly when the DVD player is turned back on. This is largely because all CMOS logic exhibits a very high impedance on the power rail node even when "off".

To avoid this situation, the CM1223 with integrated backdrive protection diode was designed to block backdrive current, guaranteeing no more than 5 μ A on any I/O pin when the I/O pin voltage is greater than the CM1223 supply voltage.

APPLICATION INFORMATION

Design Considerations

To realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segments between the signal input (typically a connector) and the ESD protection device. Application of Positive ESD Pulse between Input Channel and Ground illustrates an example of a positive 8 kV ESD pulse striking an input channel. The 8 kV ESD current pulse will divert along the path as indicated in Application of Positive ESD Pulse between Input Channel and Ground, through the D1 diode and the Zener diode back to the ground rail.

An ESD current pulse can rise from zero to its peak value in a very short time. For example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. The CM1223 has a fast response time of less than 1ns and low clamp voltage to handle this pulse scenario.

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1223 also has an integrated backdrive diode between V_P and V_N to prevent backdrive current flow from the powered sources.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges.

ADDITIONAL INFORMATION

See also ON Semiconductor Application Note “Design Considerations for ESD Protection”, in the Applications section.

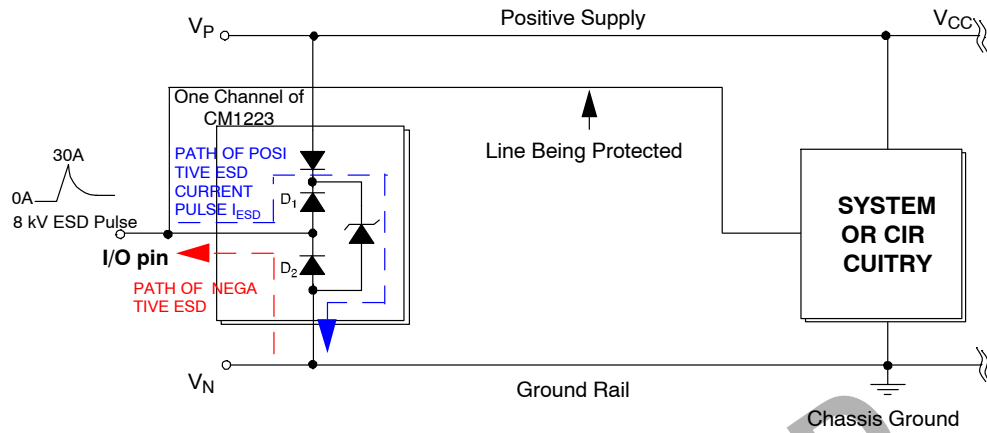


Figure 3. Application of Positive ESD Pulse between Input Channel and Ground

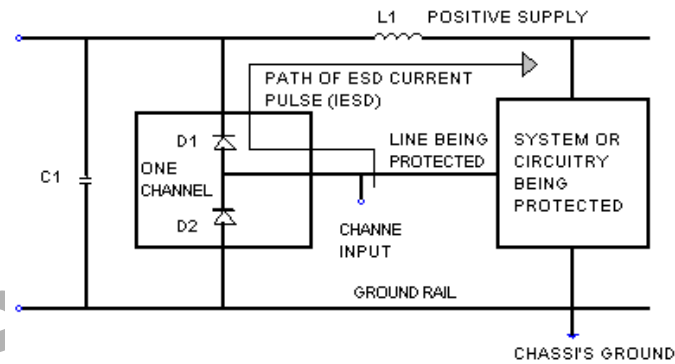


Figure 4. Application of Positive ESD Pulse between Input Channel and Ground

MECHANICAL DETAILS

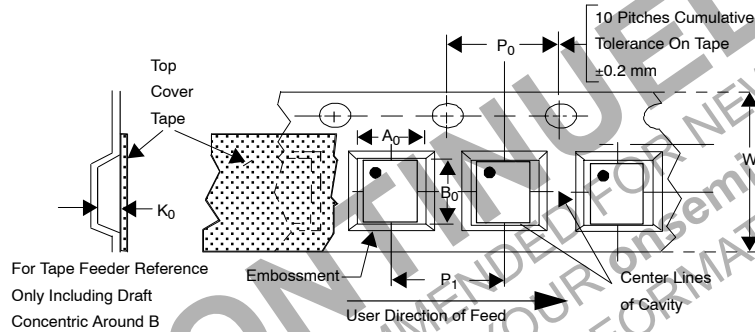
The CM1223 is available in SOT143-4, SOT23-5, SOT23-6, and MSOP-10 packages with a lead-free finishing. The various package drawings are presented below.

SOT143 Mechanical Specifications

The CM1223-02SR is supplied in 4-pin SOT143 package, the CM1223-02SO in a 5-pin SOT23 package, the CM1223-04SO in a 6-pin SOT23 package, and the CM1223-08MR in a 10-lead MSOP package. Dimensions are presented below.

Table 5. TAPE AND REEL SPECIFICATIONS

Part Number	Chip Size (mm)	Pocket Size (mm) $B_0 \times A_0 \times K_0$	Tape Width W	Reel Diameter	Qty per Reel	P_0	P_1
CM1223-02SR	2.92 X 2.37 X 1.01	2.60 X 3.15 X 1.20	8 mm	178 mm (7")	3000	4 mm	4 mm
CM1223-02SO	2.90 X 2.80 X 1.45	3.20 X 3.20 X 1.40	8 mm	178 mm (7")	3000	4 mm	4 mm
CM1223-04SO	2.90 X 2.80 X 1.45	3.20 X 3.20 X 1.40	8 mm	178 mm (7")	3000	4 mm	4 mm
CM1223-08MR	3.00 X 3.00 X 0.85	3.30 X 5.30 X 1.30	12 mm	330 mm (13")	4000	4 mm	8 mm

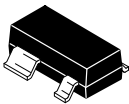


MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

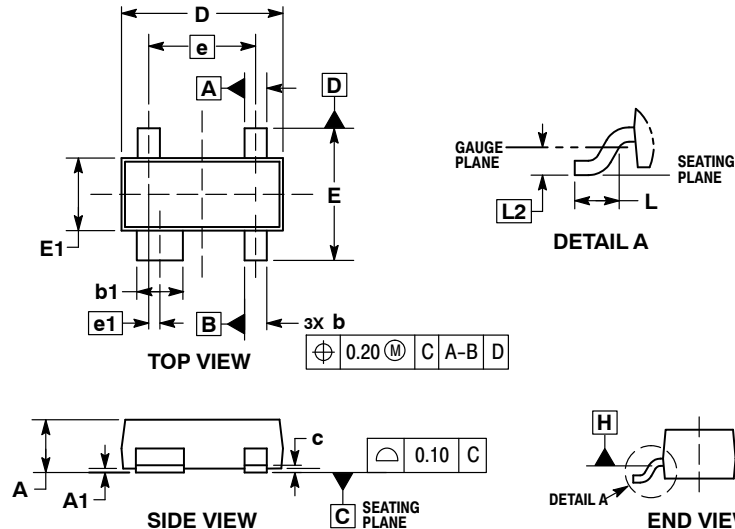
ON



SCALE 4:1

SOT-143
CASE 318A-06
ISSUE U

DATE 07 SEP 2011

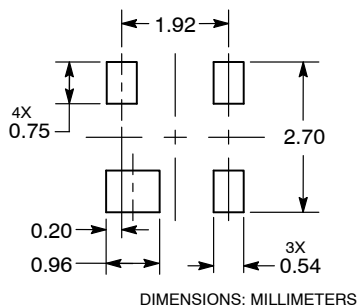


NOTES:

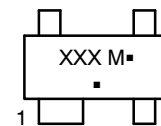
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, AND GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.12
A1	0.01	0.15
b	0.30	0.51
b1	0.76	0.94
c	0.08	0.20
D	2.80	3.05
E	2.10	2.64
E1	1.20	1.40
e	1.92 BSC	
e1	0.20 BSC	
L	0.35	0.70
L2	0.25 BSC	

RECOMMENDED SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. EMITTER
4. BASE

STYLE 2:
PIN 1. SOURCE
2. DRAIN
3. GATE 1
4. GATE 2

STYLE 3:
PIN 1. GROUND
2. SOURCE
3. INPUT
4. OUTPUT

STYLE 4:
PIN 1. OUTPUT
2. GROUND
3. GROUND
4. INPUT

STYLE 5:
PIN 1. SOURCE
2. DRAIN
3. GATE 1
4. SOURCE

STYLE 6:
PIN 1. GND
2. RF IN
3. VREG
4. RF OUT

STYLE 7:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SOURCE

STYLE 8:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. N/C

STYLE 9:
PIN 1. GND
2. IOUT
3. VCC
4. VREF

STYLE 10:
PIN 1. DRAIN
2. N/C
3. SOURCE
4. GATE

STYLE 11:
PIN 1. SOURCE
2. GATE 1
3. GATE 2
4. DRAIN

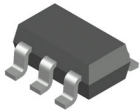
DOCUMENT NUMBER: 98ASB42227B

Electronic versions are uncontrolled except when accessed directly from the Document Repository.
Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

DESCRIPTION: SOT-143

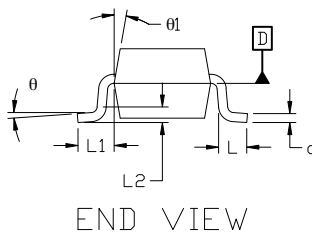
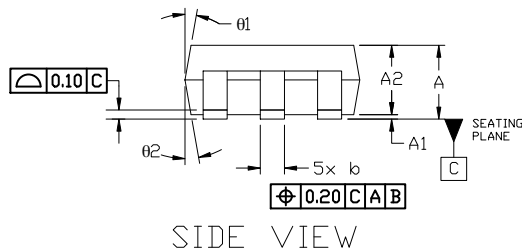
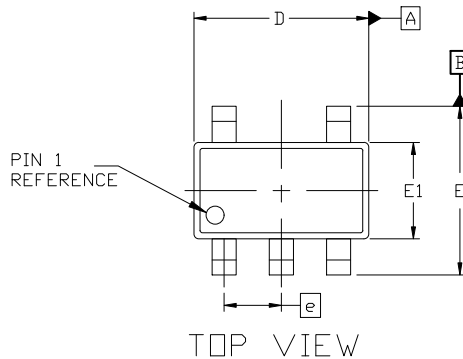
PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

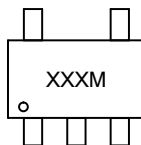


SOT-23, 5 Lead CASE 527AH ISSUE A

DATE 09 JUN 2021



GENERIC MARKING DIAGRAM*



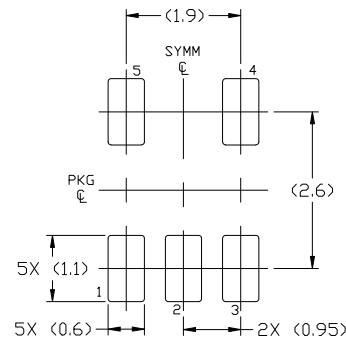
XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1989A
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON34320E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-23, 5 LEAD	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

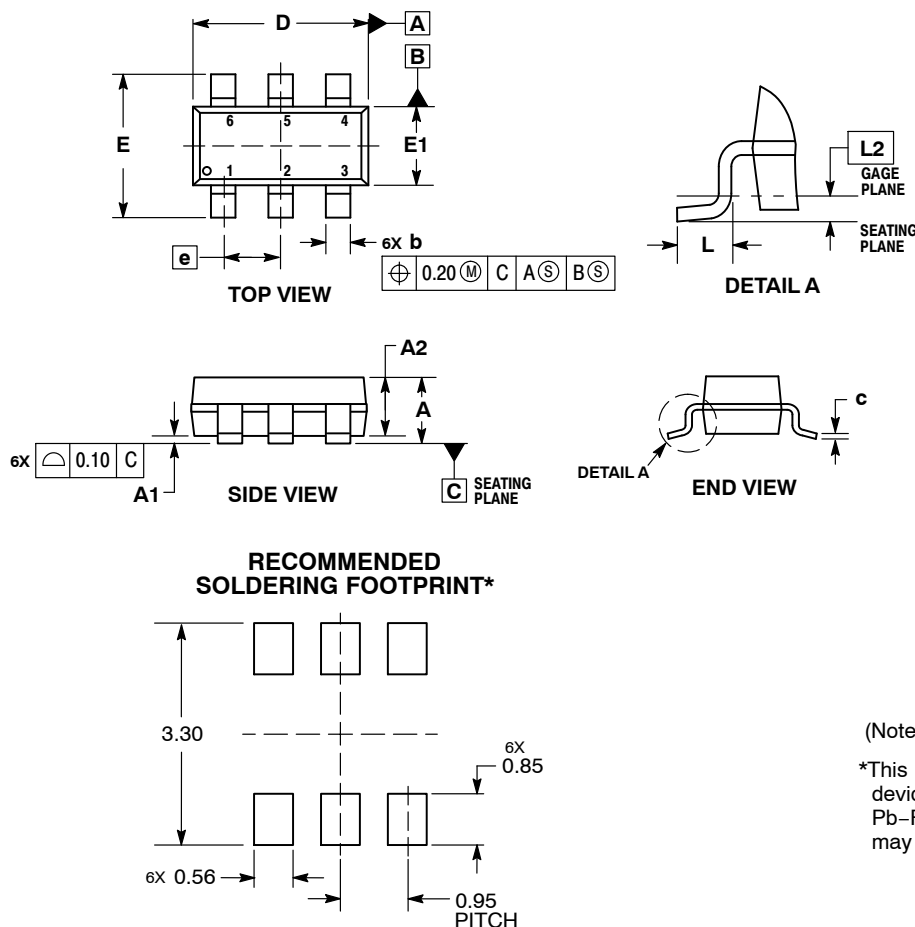
ON Semiconductor®



SCALE 2:1

SOT-23, 6 Lead
CASE 527AJ
ISSUE B

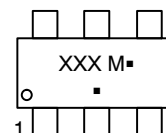
DATE 29 FEB 2012



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DATUM C IS THE SEATING PLANE.

MILLIMETERS		
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.20	0.50
c	0.08	0.26
D	2.70	3.00
E	2.50	3.10
E1	1.30	1.80
e	0.95 BSC	
L	0.20	0.60
L2	0.25 BSC	

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON34321E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-23, 6 LEAD	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

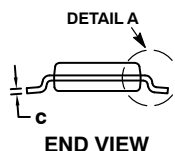
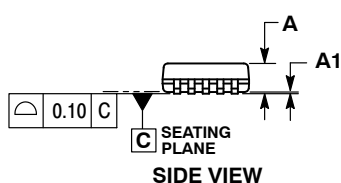
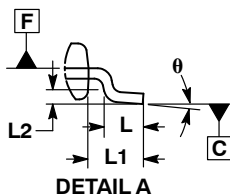
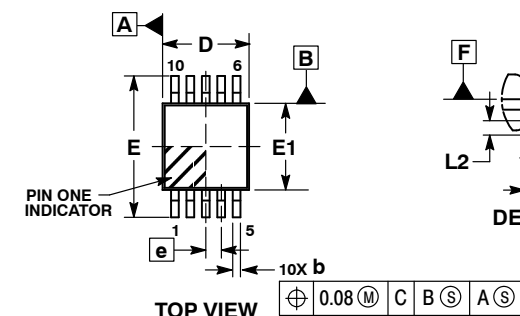
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



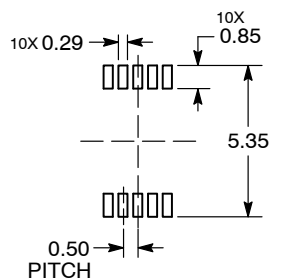
SCALE 1:1

MSOP10, 3x3
CASE 846AE
ISSUE A

DATE 20 JUN 2017



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

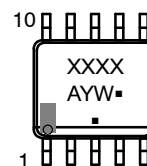
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 MM IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 MM PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	---	---	1.10
A1	0.00	0.05	0.15
A2	0.75	0.85	0.95
b	0.17	---	0.27
c	0.13	---	0.23
D	2.90	3.00	3.10
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
e	0.50 BSC		
L	0.40	0.70	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°	---	8°

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON34098E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	MSOP10, 3X3	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales