

FOD060L, FOD260L

3.3V/5V High Speed-10 MBit/s

Logic Gate Optocouplers

Features

- FOD060L in SO8 and FOD260L in 8-pin DIP
- Very high speed – 10 MBit/s
- Superior CMR — 50 kV/μs at 1,000V peak
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output
- Wired OR-open collector
- Safety and regulatory approvals
 - UL1577
 - DIN EN/IEC 60747-5-2

- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

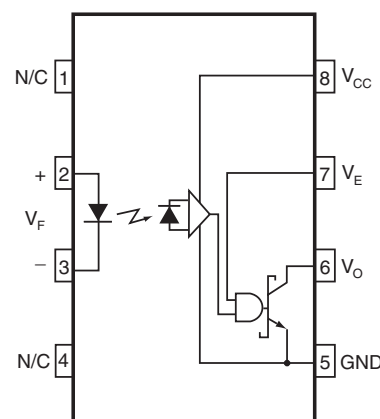
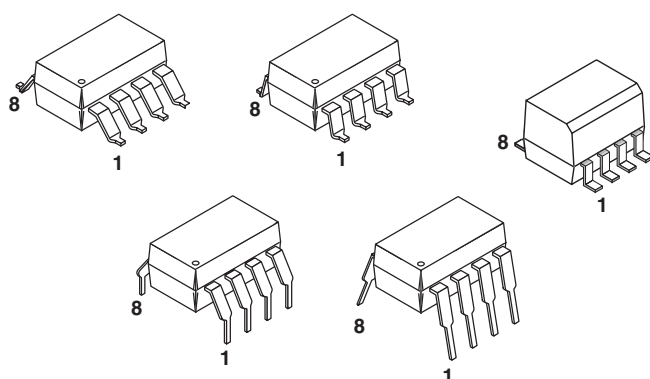
Description

These optocouplers consist of an AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate. Devices include a strobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8). An internal noise shield provides superior common mode rejection of typically 50 kV/μs at 1,000V common mode.

Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS

Package



Truth Table (Positive Logic)

Input	Enable	Output
On	H	L
Off	H	H
On	L	H
Off	L	H
On*	NC*	L*
Off*	NC*	H*

*Devices with pin 7 not connected.

A 0.1 μF bypass capacitor must be connected between pins 5 and 8. (See Note 1)

SAFETY AND INSULATION RATINGS (As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Parameter		Characteristics
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	<150 V _{RMS}	I–IV
	<300 V _{RMS}	I–III
Climatic Classification		55/100/21
Pollution Degree (DIN VDE 0110/1.89)		2
Comparative Tracking Index		175

Symbol	Parameter	Value	Unit
V _{PR}	Input-to-Output Test Voltage, Method A, V _{IORM} × 1.6 = V _{PR} , Type and Sample Test with t _m = 10 s, Partial Discharge < 5 pC	904	V _{peak}
	Input-to-Output Test Voltage, Method B, V _{IORM} × 1.875 = V _{PR} , 100% Production Test with t _m = 1 s, Partial Discharge < 5 pC	1060	V _{peak}
V _{IORM}	Maximum Working Insulation Voltage	565	V _{peak}
V _{IOTM}	Highest Allowable Over-Voltage	4000	V _{peak}
	External Creepage	≥4	mm
	External Clearance	≥4	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥0.4	mm
T _S	Case Temperature (Note 1)	150	°C
I _{S,INPUT}	Input Current (Note 1)	200	mA
P _{S,OUTPUT}	Output Power (Note 1)	300	mW
R _{IO}	Insulation Resistance at T _S , V _{IO} = 500 V (Note 1)	>10 ⁹	Ω

1. Safety limit values – maximum values allowed in the event of a failure.

Absolute Maximum Ratings (No derating required up to 85°C)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-40 to +125	°C
T_{OPR}	Operating Temperature	-40 to +85	°C
EMITTER			
I_F	DC/Average Forward Input Current	50	mA
V_E	Enable Input Voltage, not to exceed V_{CC} by more than 500 mV	$V_{CC} + 0.5V$	V
V_R	Reverse Input Voltage	5.0	V
P_I	Power Dissipation	45	mW
DETECTOR			
V_{CC} (1 minute max)	Supply Voltage	7.0	V
I_O	Output Current	50	mA
V_O	Output Voltage	7.0	V
P_O	Collector Output Power Dissipation	85	mW

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
I_{FL}	Input Current, Low Level	0	250	μA
I_{FH}	Input Current, High Level	*6.3	15	mA
V_{CC}	Supply Voltage, Output	3.0	5.5	V
V_{EL}	Enable Voltage, Low Level	0	0.8	V
V_{EH}	Enable Voltage, High Level	2.0	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C
N	Fan Out (TTL load)		8	
R_L	Output Pull-up Resistor	330	4K	Ω

*6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

Electrical Characteristics ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless otherwise specified. Typical value is measured at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 3.3\text{V}$)

Individual Component Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
EMITTER						
V_F	Input Forward Voltage	$I_F = 10\text{ mA}$ $T_A = 25^{\circ}\text{C}$		1.4	1.8 1.75	V
B_{VR}	Input Reverse Breakdown Voltage	$I_R = 10\text{ }\mu\text{A}$	5.0			V
C_{IN}	Input Capacitance	$V_F = 0$, $f = 1\text{ MHz}$		6.0		pF
$\Delta V_F/\Delta T_A$	Input Diode Temperature Coefficient	$I_F = 10\text{ mA}$		-1.9		mV/ $^{\circ}\text{C}$
DETECTOR						
I_{CCH}	High Level Supply Current	$V_E = 0.5\text{ V}$, $I_F = 0\text{ mA}$, $V_{CC} = 3.3\text{ V}$		3.5	7	mA
I_{CCL}	Low Level Supply Current	$V_E = 0.5\text{ V}$, $I_F = 0\text{ mA}$, $V_{CC} = 3.3\text{ V}$		3.2	10	mA
I_{EL}	Low Level Enable Current	$V_{CC} = 3.3\text{ V}$, $V_E = 0.5\text{ V}$			-1.6	mA
I_{EH}	High Level Enable Current	$V_{CC} = 3.3\text{ V}$, $V_E = 2.0\text{ V}$			-1.6	mA
V_{EH}	High Level Enable Voltage	$V_{CC} = 3.3\text{ V}$, $I_F = 10\text{ mA}$	2.0	1.27		V
V_{EL}	Low Level Enable Voltage	$V_{CC} = 3.3\text{ V}$, $I_F = 10\text{ mA}$ (Note 2)		1.18	0.8	V

Switching Characteristics ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V}$, $I_F = 7.5\text{ mA}$ unless otherwise specified. Typical value is measured at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 3.3\text{V}$)

Symbol	AC Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
T_{PLH}	Propagation Delay Time to Output High Level	$R_L = 350\Omega$, $C_L = 15\text{ pF}$ (Fig. 9) (Note 3)		65	90	ns
T_{PHL}	Propagation Delay Time to Output Low Level	$R_L = 350\Omega$, $C_L = 15\text{ pF}$ (Fig. 9) (Note 4)		43	75	ns
$ T_{PHL} - T_{PLH} $	Pulse Width Distortion	$R_L = 350\Omega$, $C_L = 15\text{ pF}$ (Fig. 9)		23	25	ns
t_{PSK}	Propagation Delay Skew	$R_L = 350\Omega$, $C_L = 15\text{ pF}$ (Note 5)		31	40	ns
t_r	Output Rise Time (10-90%)	$R_L = 350\Omega$, $C_L = 15\text{ pF}$ (Fig. 9)(Note 6)		22		ns
t_f	Output Fall Time (90-10%)	$R_L = 350\Omega$, $C_L = 15\text{ pF}$ (Fig. 12) (Note 7)		3		ns
t_{ELH}	Enable Propagation Delay Time to Output High Level	$V_{EH} = 3\text{ V}$, $R_L = 350\Omega$, $C_L = 15\text{ pF}$ (Fig. 10) (Note 8)		47		ns
t_{EHL}	Enable Propagation Delay Time to Output Low Level	$V_{EH} = 3\text{ V}$, $R_L = 350\Omega$, $C_L = 15\text{ pF}$ (Fig. 10) (Note 9)		27		ns
CM_H	Common Mode Transient Immunity (at Output High Level)	$R_L = 350\Omega$, $T_A = 25^{\circ}\text{C}$, $I_F = 0\text{ mA}$, $V_{OH}(\text{Min.}) = 2.0\text{ V}$, $ V_{CM} = 1,000\text{ V}$ (Fig. 11) (Note 10)	25,000	50,000		V/ μs
CM_L	Common Mode Transient Immunity (at Output Low Level)	$R_L = 350\Omega$, $T_A = 25^{\circ}\text{C}$, $I_F = 7.5\text{ mA}$, $V_{OL}(\text{Max.}) = 0.8\text{ V}$, $ V_{CM} = 1,000\text{ V}$ (Fig. 11) (Note 11)	25,000	50,000		V/ μs

Transfer Characteristics ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ Unless otherwise specified. Typical value is measured at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 3.3\text{V}$)

Symbol	DC Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
I_{OH}	High Level Output Current	$I_F = 250\ \mu\text{A}$, $V_{CC} = 3.3\ \text{V}$, $V_O = 3.3\ \text{V}$, $V_E = 2.0\ \text{V}$ (Note 2)		0.01	50	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = 3.3\ \text{V}$, $I_F = 5\ \text{mA}$, $I_{OL} = 13\ \text{mA}$, $V_E = 2.0\ \text{V}$ (Note 2)		0.3	0.6	V
I_{FT}	Input Threshold Current	$V_{CC} = 3.3\ \text{V}$, $V_O = 0.6\ \text{V}$, $I_{OL} = 13\ \text{mA}$, $V_E = 2.0\ \text{V}$ (Note 2)		1	5	mA

Isolation Characteristics ($T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ Unless otherwise specified. Typical value is measured at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 3.3\text{V}$)

Symbol	Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
I_{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45%, $T_A = 25^{\circ}\text{C}$, $t = 5\ \text{s}$, $V_{I-O} = 3000\ \text{VDC}$ (Note 12)			1.0	μA
V_{ISO}	Withstand Insulation Test Voltage FOD060L FOD260L	$I_{IO} \leq 2\ \mu\text{A}$, $R_H < 50\%$, $T_A = 25^{\circ}\text{C}$, $t = 1\ \text{min.}$ (Note 12)	3750			V_{RMS}
			5000			
R_{I-O}	Resistance (Input to Output)	$V_{I-O} = 500\ \text{V}$ (Note 12)		10^{12}		Ω
C_{I-O}	Capacitance (Input to Output)	$f = 1\ \text{MHz}$ (Note 12)		0.6		pF

Notes

1. The V_{CC} supply to each optoisolator must be bypassed by a $0.1\ \mu\text{F}$ capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. Enable Input – No pull up resistor required as the device has an internal pull up resistor.
3. t_{PLH} – Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
4. t_{PHL} – Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
5. t_{PSK} is the worst case difference between t_{PHL} and t_{PLH} for any devices at the stated test conditions.
6. t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
7. t_f – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
8. t_{ELH} – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
9. t_{EHL} – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
10. CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e., $V_{OUT} > 2.0\ \text{V}$). Measured in volts per microsecond (V/ μs).
11. CM_L – The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., $V_{OUT} < 0.8\ \text{V}$). Measured in volts per microsecond (V/ μs).
12. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Typical Performance Curves

Fig. 1 Input Forward Current vs. Forward Voltage

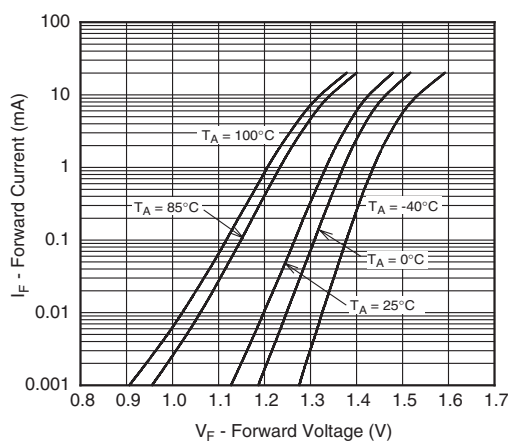


Fig. 2 Input Threshold Current vs. Ambient Temperature

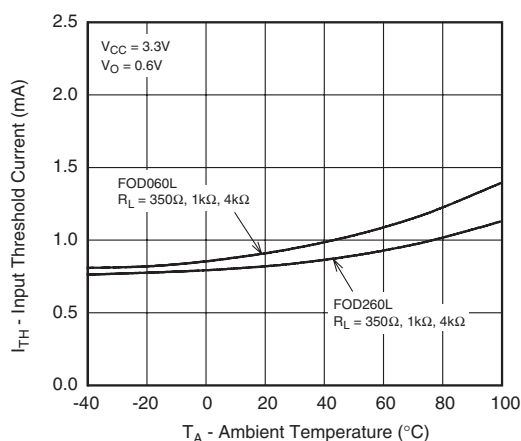


Fig. 3 Low Level Output Voltage vs. Ambient Temperature

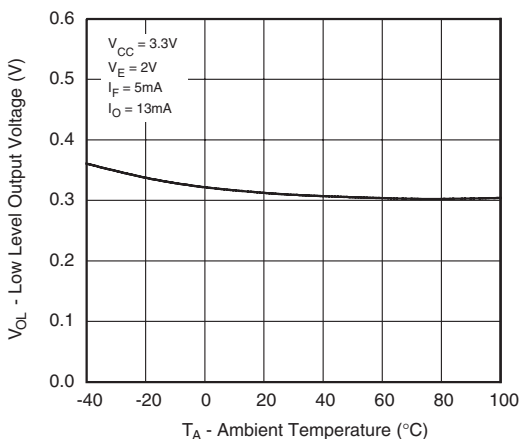


Fig. 4 High Level Output Current vs. Ambient Temperature

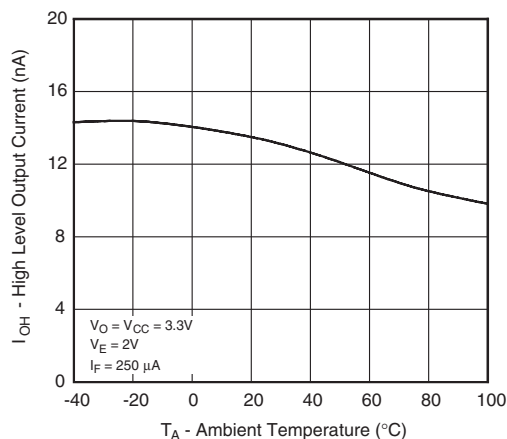


Fig. 5 Low Level Output Current vs. Ambient Temperature

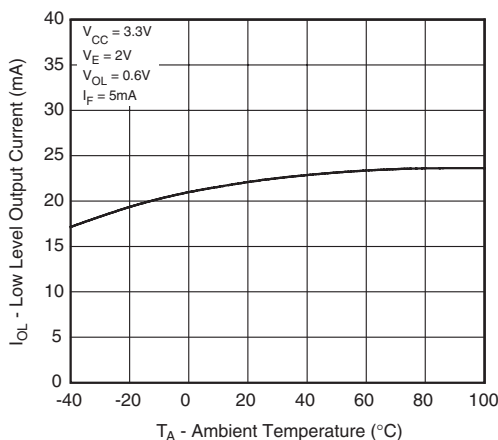
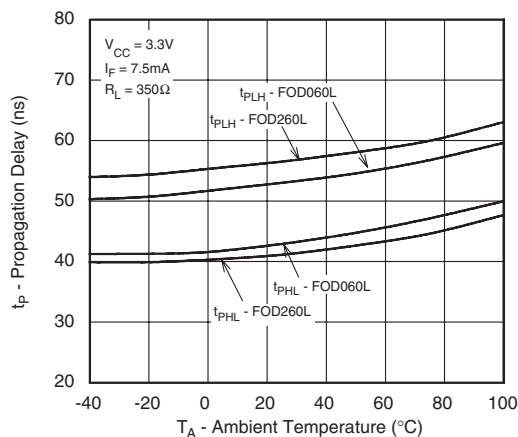


Fig. 6 Propagation Delay vs. Ambient Temperature



Typical Performance Curves

Fig. 7 Rise and Fall Times vs. Ambient Temperature

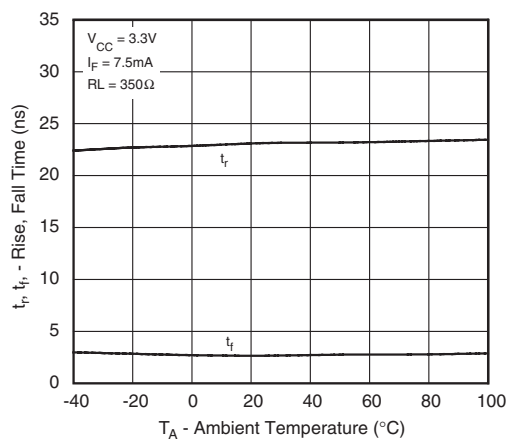
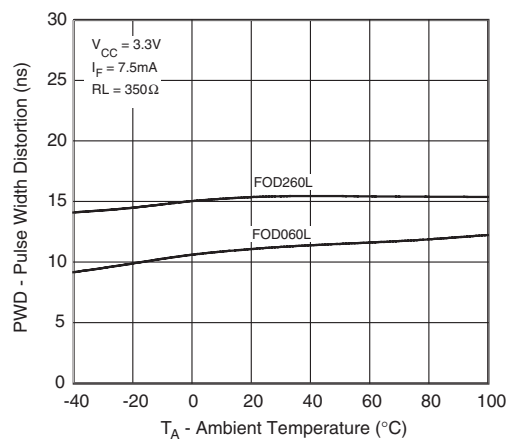


Fig. 8 Pulse Width Distortion vs. Ambient Temperature



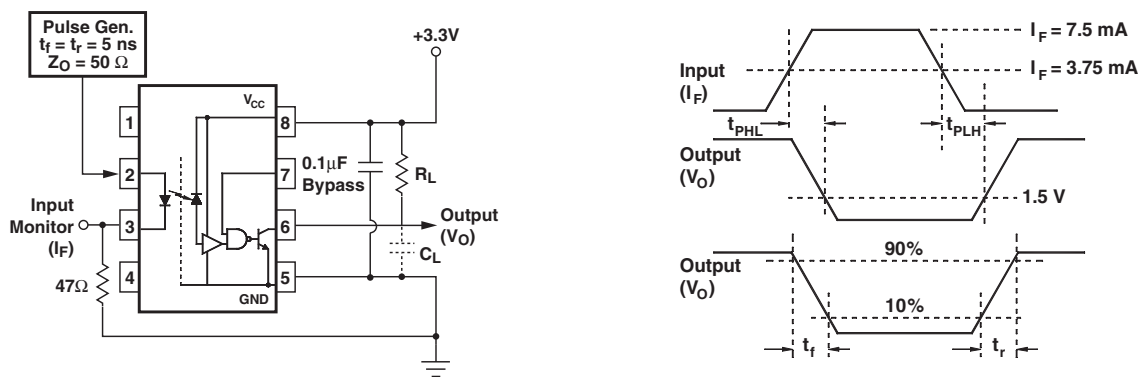


Fig. 9 Test Circuit and Waveforms for t_{PLH} , t_{PHL} , t_r and t_f .

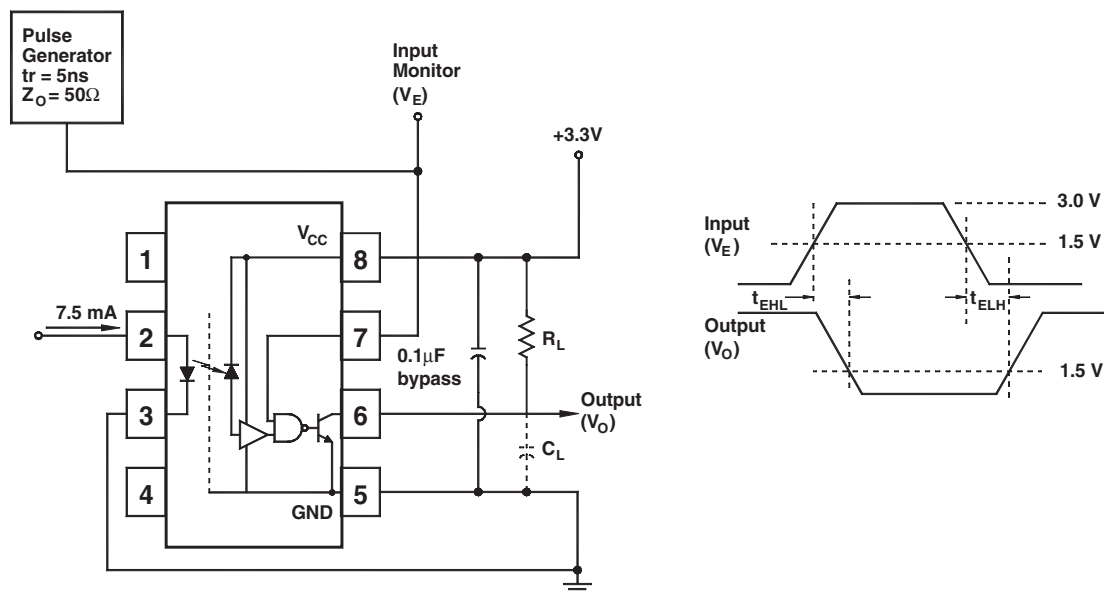


Fig. 10 Test Circuit t_{EHL} and t_{ELH} .

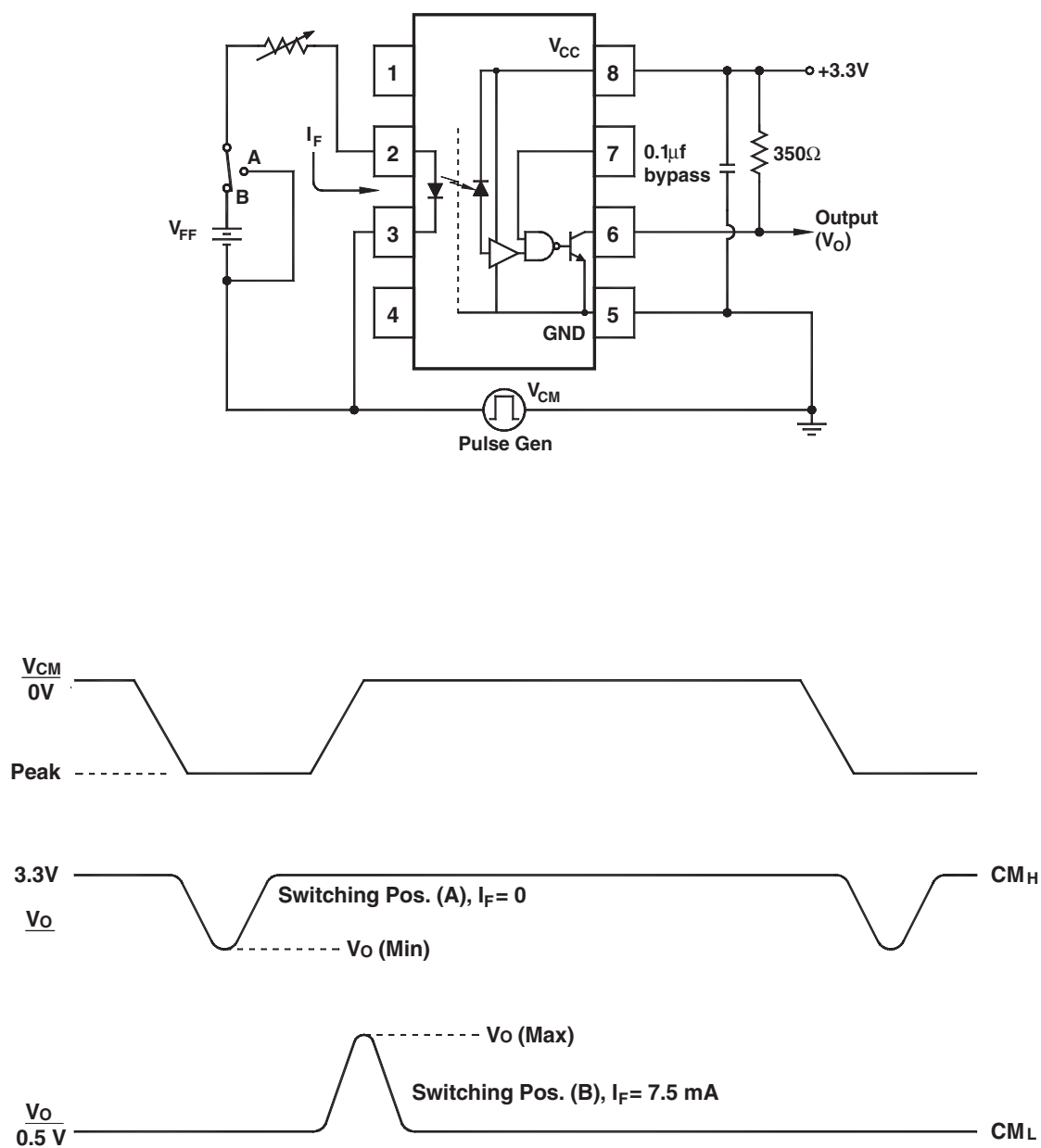


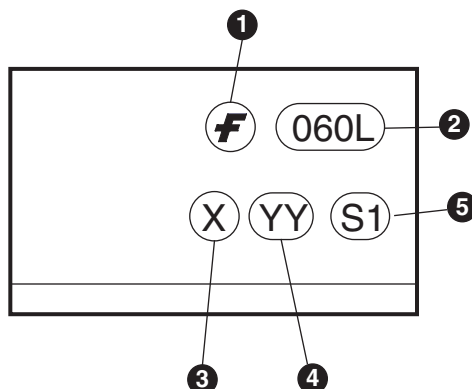
Fig. 11 Test Circuit Common Mode Transient Immunity

Ordering Information

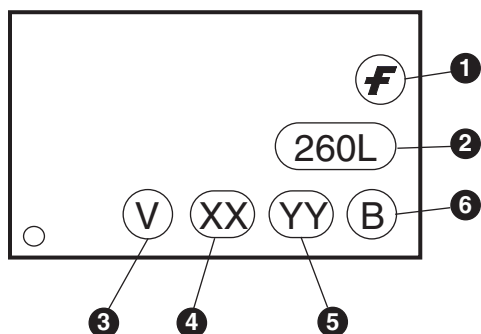
Part Number	Package	Packing Method
FOD060L	Small outline 8-pin	Tube (50 units per tube)
FOD060LR2	Small outline 8-pin	Tape and Reel (2,500 units per reel)
FOD260L	DIP 8-Pin	Tube (50 units per tube)
FOD260LS	SMT 8-Pin (Lead Bend)	Tube (50 units per tube)
FOD260LSD	SMT 8-Pin (Lead Bend)	Tape and Reel (1,000 units per reel)
FOD260LV	DIP 8-Pin, DIN EN/IEC 60747-5-2 option	Tube (50 units per tube)
FOD260LSV	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-2 option	Tube (50 units per tube)
FOD260LSDV	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-2 option	Tape and Reel (1,000 units per reel)
FOD260LTV	DIP 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-2 option	Tube (50 units per tube)
FOD260LTSV	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-2 option	Tube (50 units per tube)
FOD260LTSR2	SMT 8-Pin, 0.4" Lead Spacing	Tape and Reel (700 units per reel)
FOD260LTSR2V	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-2 option	Tape and Reel (700 units per reel)

Marking Information

Small Outline



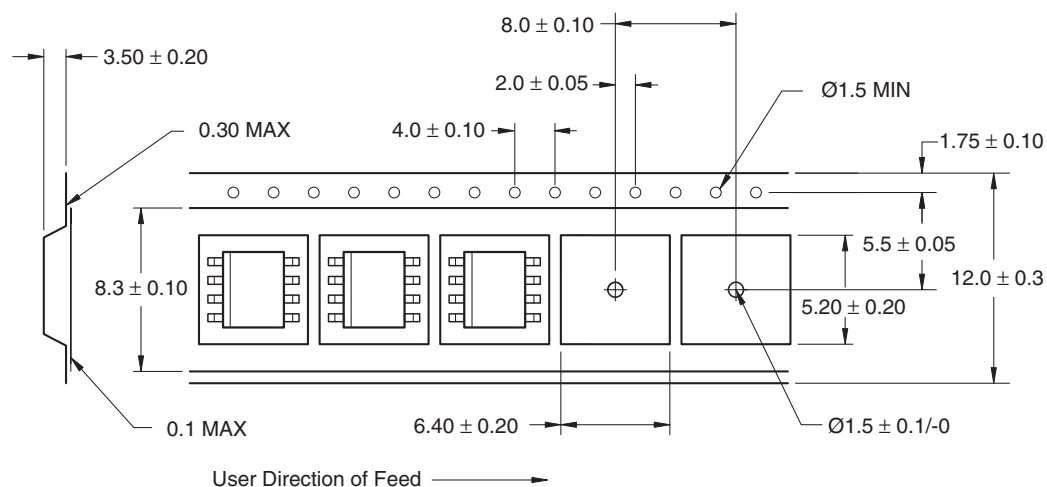
Definitions	
1	onsemi logo
2	Device number
3	One digit year code, e.g., '8'
4	Two digit work week ranging from '01' to '53'
5	Assembly package code

Marking Information (Continued)**DIP and SMT****Definitions**

1	onsemi logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with DIN EN/IEC 60747-5-2 option – See order entry table)
4	Two digit year code, e.g., '11'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

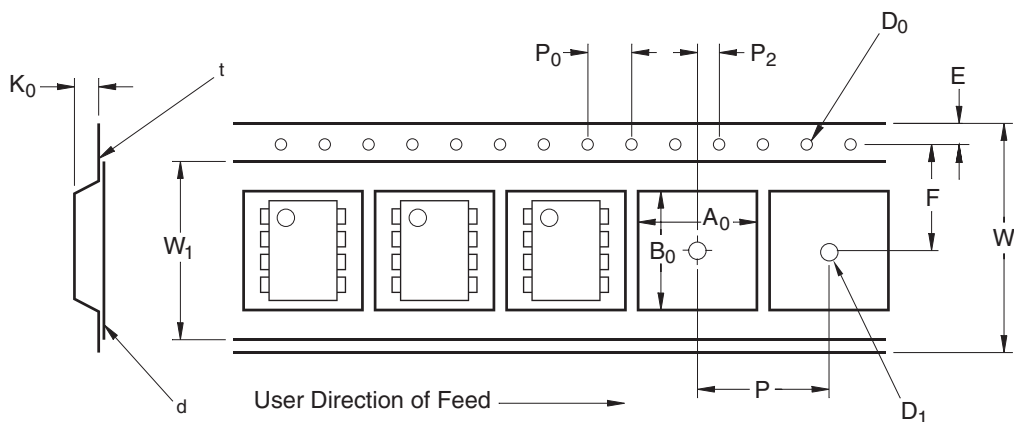
Carrier Tape Specification

Small Outline

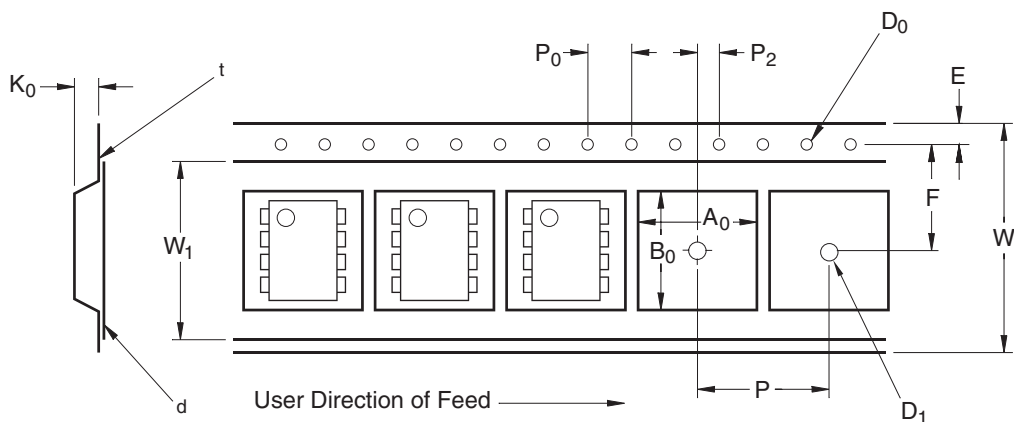


Note:

All dimensions are in millimeters.

Carrier Tape Specification (Continued)**Option S**

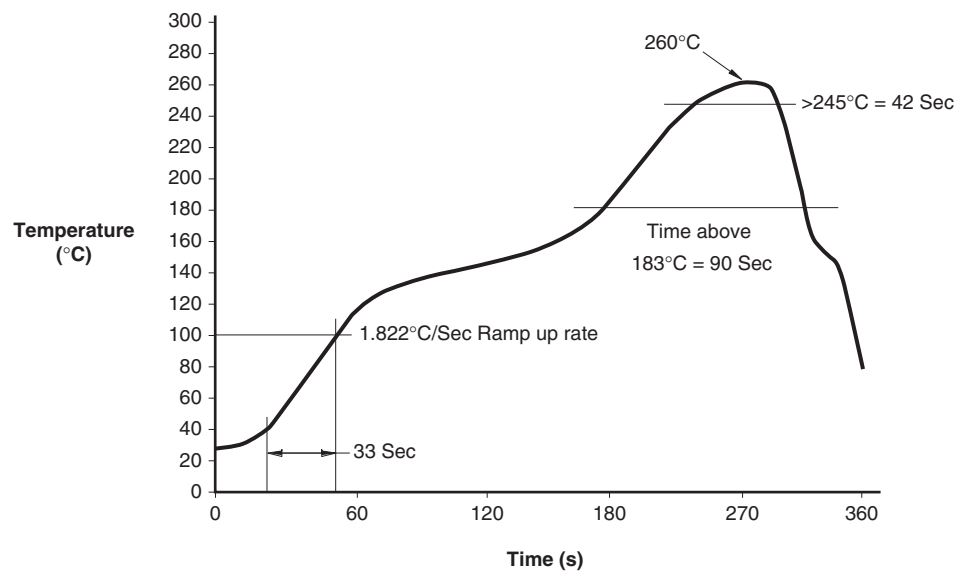
Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A_0	Pocket Dimensions	10.30 ± 0.20
B_0		10.30 ± 0.20
K_0		4.90 ± 0.20
W_1	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

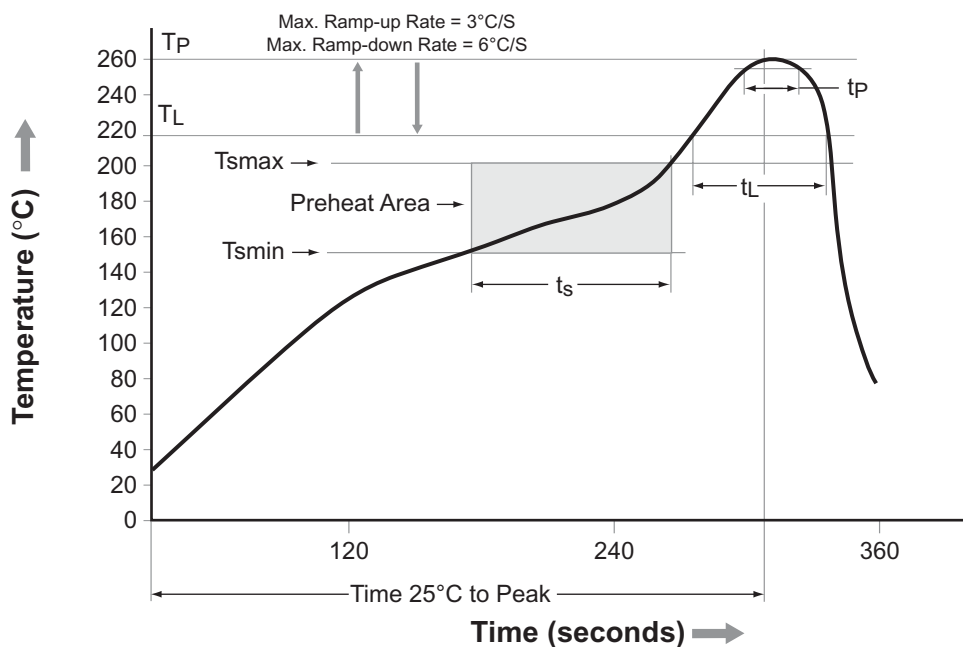
Carrier Tape Specification (Continued)**Option TS**

Symbol	Description	Dimension in mm
W	Tape Width	24.0 ± 0.3
t	Tape Thickness	0.40 ± 0.1
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	11.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	16.0 ± 0.1
A_0	Pocket Dimensions	12.80 ± 0.1
B_0		10.35 ± 0.1
K_0		5.7 ± 0.1
W_1	Cover Tape Width	21.0 ± 0.1
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

Reflow Profile

Small Outline



Reflow Profile (Continued)**DIP and SMT**

Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T _{smin})	150°C
Temperature Max. (T _{smax})	200°C
Time (t _s) from (T _{smin} to T _{smax})	60–120 seconds
Ramp-up Rate (t _L to t _P)	3°C/second max.
Liquidous Temperature (T _L)	217°C
Time (t _L) Maintained Above (T _L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t _P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T _P to T _L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

MECHANICAL CASE OUTLINE

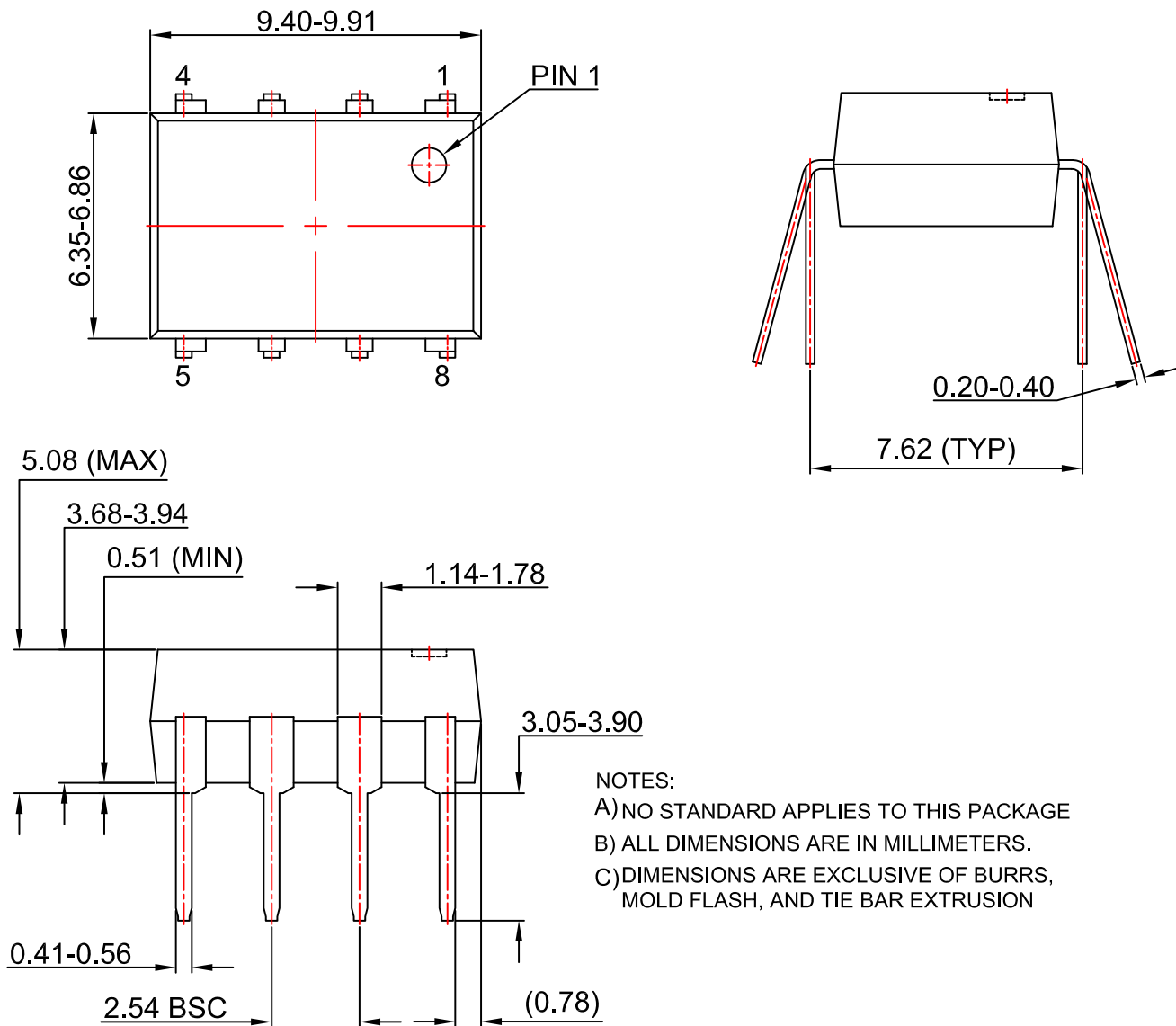
PACKAGE DIMENSIONS

ON Semiconductor®



PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O

DATE 18 SEP 2017

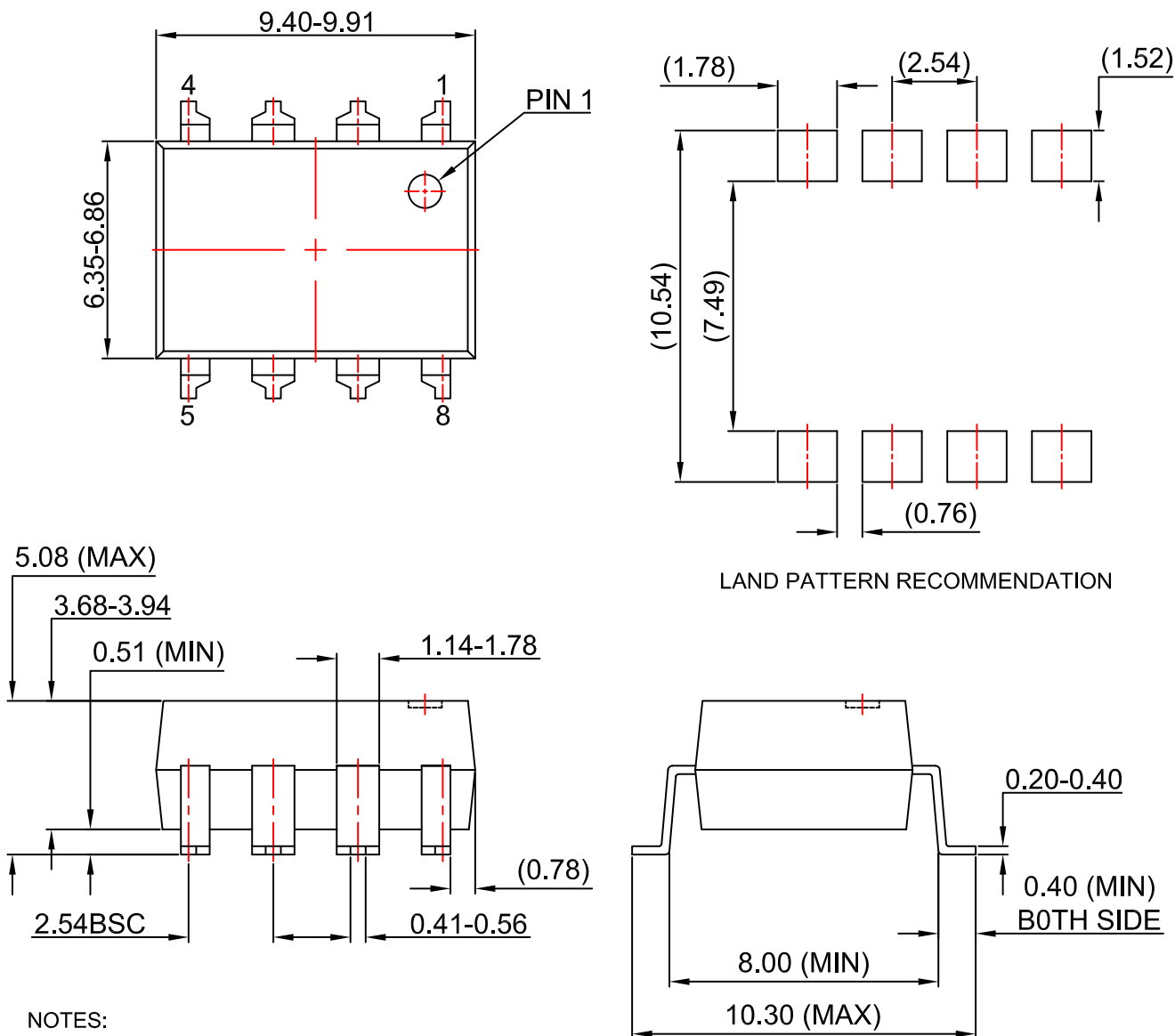


DOCUMENT NUMBER:	98AON13446G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP8 9.655X6.6, 2.54P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

PDIP8 GW
CASE 709AC
ISSUE O

DATE 31 JUL 2016



NOTES:

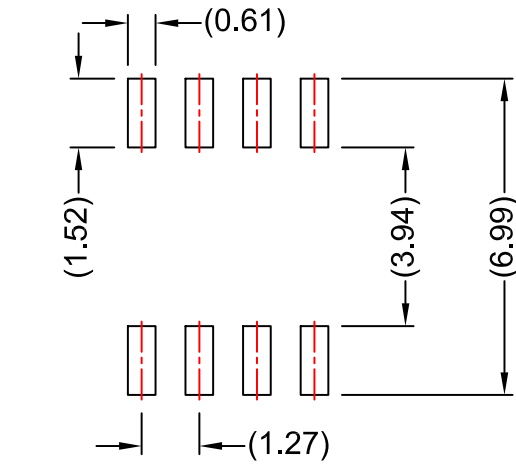
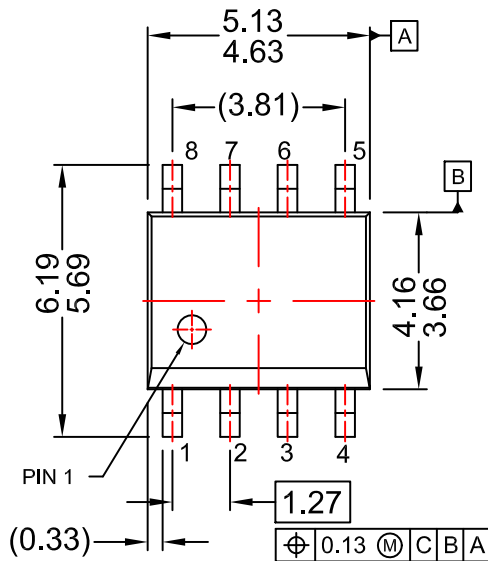
- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	98AON13447G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP8 GW	PAGE 1 OF 1

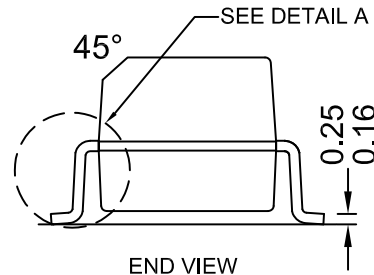
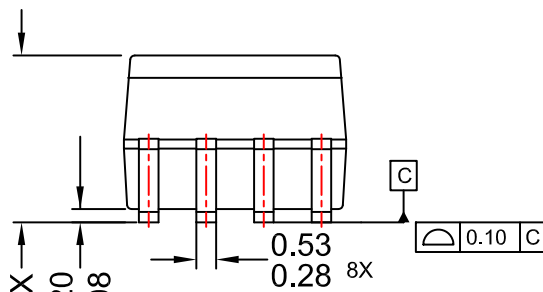
ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

SOIC8
CASE 751DZ
ISSUE O

DATE 30 SEP 2016



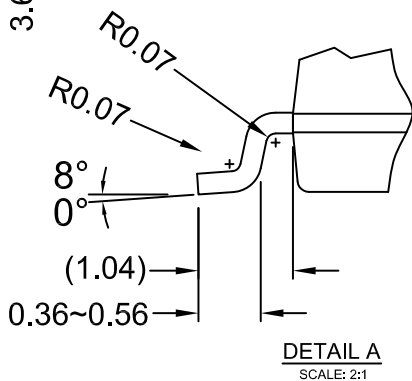
LAND PATTERN RECOMMENDATION



END VIEW

NOTES:

- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M.



DETAIL A
 SCALE: 2:1

DOCUMENT NUMBER:	98AON13733G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC8	PAGE 1 OF 1

ON Semiconductor and **ON** are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales