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Dual 2-to-4 Decoder/Demultiplexer

74VHC139

General Description

The VHC139 is an advanced high speed CMOS Dual 2-to-4 Decoder/Demultiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The active LOW enable input can be used for gating or it can be used as a data input for demultiplexing applications. When the enable input is held HIGH, all four outputs are fixed at a HIGH logic level independent of the other inputs. An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage.

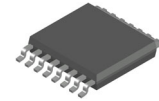
This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

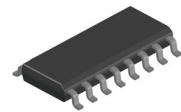
- High Speed: $t_{PD} = 5.0 \text{ ns}$ (typ.) at $T_A = 25^\circ\text{C}$
- Low Power Dissipation: $I_{CC} = 4 \mu\text{A}$ (Max.) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min.)
- Power Down Protection is Provided on All Inputs
- Pin and Function Compatible with 74HC139
- Pb-Free, Halogen Free/BFR Free and RoHS Compliant

TRUTH TABLE

Inputs			Outputs			
$\bar{E}$	A_0	A_1	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

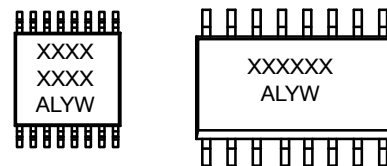


TSSOP-16,
CASE 948AH



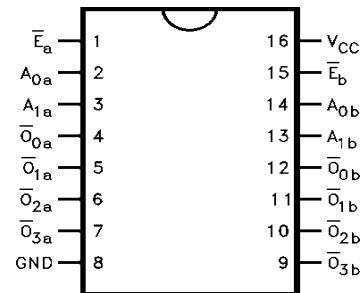
SOIC-16,
CASE 751BG

MARKING DIAGRAM



XXXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW,W = Work Week

CONNECTION DIAGRAM



PIN DESCRIPTION

Pin Names	Description
A_0, A_1	Address Inputs
$\bar{E}$	Enable Inputs
$\bar{O}_0-\bar{O}_3$	Enable Inputs

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Ratings	Unit
V _{CC}	DC Supply Voltage		−0.5 to + 6.5	V
V _I	DC Input Voltage		−0.5 to + 6.5	V
V _{OUT}	DC Output Voltage		−0.5 V to V _{CC} + 0.5	V
I _{IN}	DC Input Current, Per pin		±20	mA
I _{OUT}	DC Output Current, Per pin		±25	mA
I _{CC}	DC Supply Current Current, V _{CC} and GND Per pins		±75	mA
I _{IK}	Input Clamp Current		−20	mA
I _{OK}	Output Clamp Current		±20	°C
T _{STG}	Storage Temperature Range		−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T _J	Junction Temperature Under Bias		+150	°C
θ _{JA}	Thermal Resistance (Note 2)	SOIC−16 QFN16 TSSOP−16	126 118 159	°CW
P _D	Power Dissipation in Still Air at 25°C	SOIC−16 QFN16 TSSOP−16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	–
F _R	Flammability Rating (Note 2)	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.139 in	–
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS (Note 3)

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{IN}	DC Input Voltage (Note 4)	0	5.5	V
V _{OUT}	DC Output Voltage (Note 4)	0	V _{CC}	V
T _A	Operating Temperature	-40	+85	°C
t _r , t _f	Input Rise or Fall Rate	V _{CC} = 3.0 V to 3.6 V V _{CC} = 4.5 V to 5.5 V	0 100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

74VHC139

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C			T _A = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		2.0	1.50	–	–	1.50	–	V
			3.0–5.5	0.7 V _{CC}	–	–	0.7 V _{CC}	–	
V _{IL}	LOW Level Input Voltage		2.0	–	–	0.50	–	0.50	V
			3.0–5.5	–	–	0.3 V _{CC}	–	0.3 V _{CC}	
V _{OH}	HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = –50 µA	2.0	1.9	2.0	–	1.9	V
				3.0	2.9	3.0	–	2.9	
				4.5	4.4	4.5	–	4.4	
			I _{OH} = –4 mA	3.0	2.58	–	–	2.48	
			I _{OH} = –8 mA	4.5	3.94	–	–	3.80	
V _{OL}	LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 µA	2.0	–	0.0	0.1	–	V
				3.0	–	0.0	0.1	–	
				4.5	–	0.0	0.1	–	
			I _{OL} = 4 mA	3.0	–	–	0.36	–	
			I _{OL} = 8 mA	4.5	–	–	0.36	–	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0–5.5	–	–	±0.1	–	±1.0	µA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	–	–	40.0	–	40.0	µA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C			T _A = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	C _L = 15 pF	3.3 ±0.3	–	7.2	11.0	1.0	13.0	ns
		C _L = 50 pF		–	9.7	14.5	1.0	16.5	
t _{PHL}	A _n to $\bar{O}_n$	C _L = 15 pF	5.0 ±0.5	–	5.0	7.2	1.0	8.5	ns
		C _L = 50 pF		–	6.5	9.2	1.0	10.5	
t _{PLH}	Propagation Delay	C _L = 15 pF	3.3 ±0.3	–	6.4	9.2	1.0	11.0	ns
		C _L = 50 pF		–	8.9	12.7	1.0	14.5	
t _{PHL}	$\bar{E}_n$ to $\bar{O}_n$	C _L = 15 pF	5.0 ±0.5	–	4.4	6.3	1.0	7.5	ns
		C _L = 50 pF		–	5.9	8.3	1.0	9.5	
C _{IN}	Input Capacitance	V _{CC} = Open	–	–	4	10	–	10	pF
C _{PD}	Power Dissipation Capacitance	(Note 3)	–	–	26	–	–	–	pF

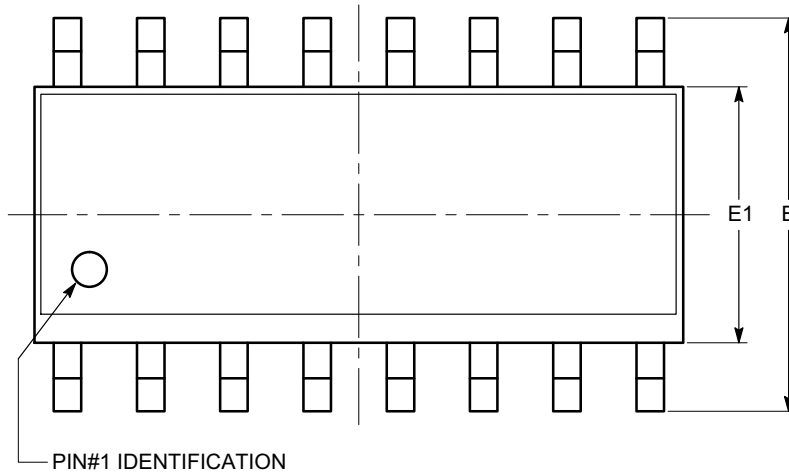
ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
74VHC139MX	VHC139	SOIC–16	2,500 Units / Tape & Reel
74VHC139MTCX	VHC139	TSSOP–16	2,500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

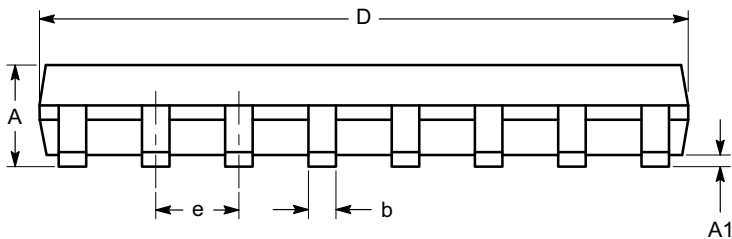
SOIC-16, 150 mils
CASE 751BG-01
ISSUE O

DATE 19 DEC 2008

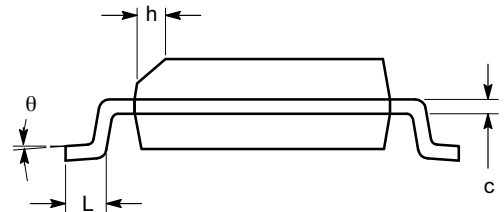


SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

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DESCRIPTION:	SOIC-16, 150 MILS	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE

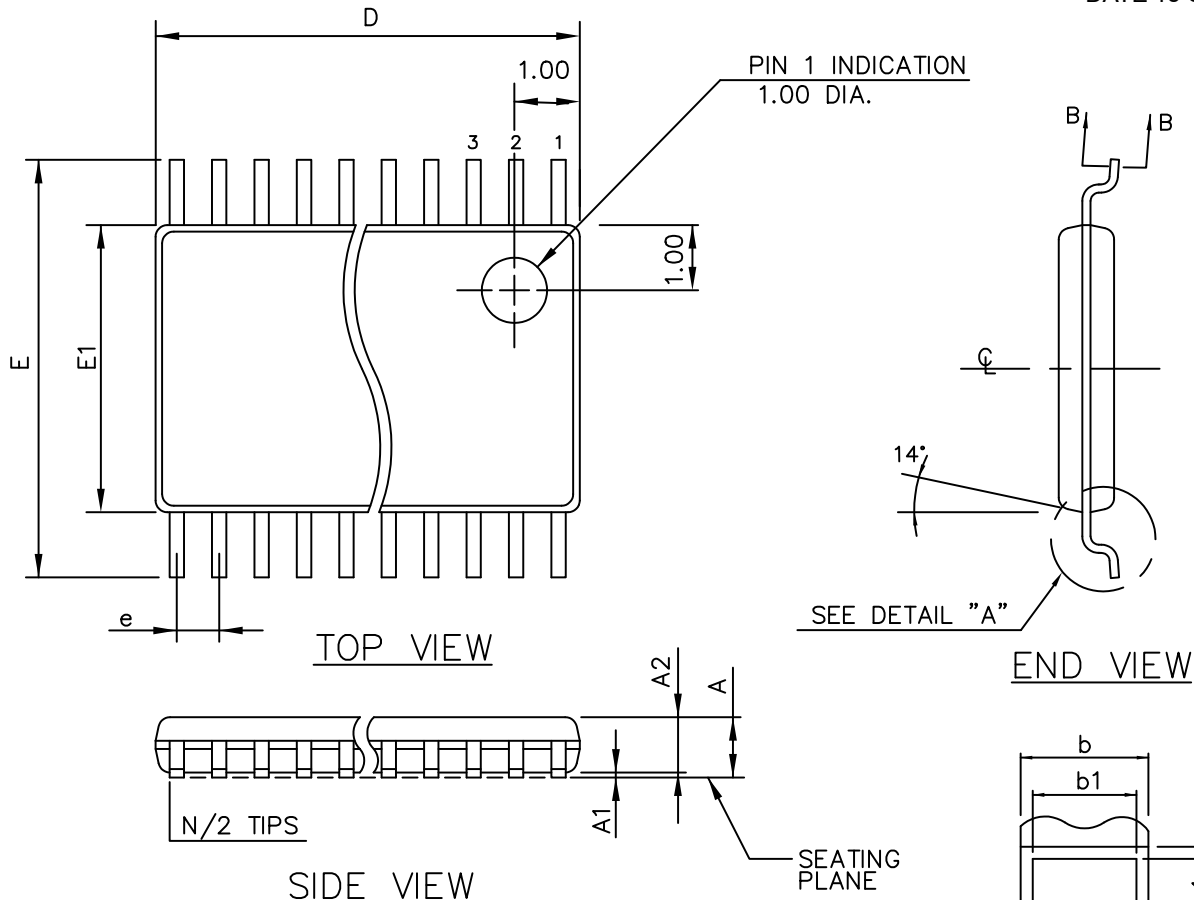
PACKAGE DIMENSIONS

ON Semiconductor®

ON

TSSOP 16
CASE 948AH-01
ISSUE O

DATE 19 SEP 2008

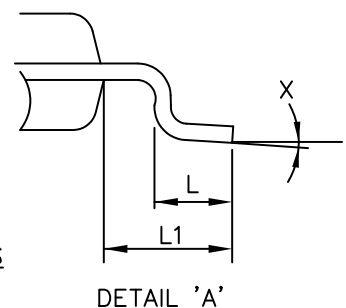


THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	D	N
	MIN.	NOM.	MAX.			
A	—	—	1.10	AA/AAT	3.00 BSC	8
A ₁	0.05	—	0.15	AB-1/ABT	5.00 BSC	14
A ₂	0.85	0.90	0.95	AB/ABT	5.00 BSC	16
b	0.19	—	0.30	AD/ADT	7.80 BSC	24
b ₁	0.19	0.22	0.25			
c	0.09	—	0.20			
c ₁	0.09	0.127	0.16			
D	SEE VARIATIONS					
E ₁	4.30	4.40	4.50			
e	0.65 BSC					
E	6.40 BSC					
L	0.50	0.60	0.70			
L ₁	1.00 REF					
N	SEE VARIATIONS					
X	0°	—	8°			

ALL DIMENSIONS IN MILLIMETERS

SECTION "B-B"



MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

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