

SN74LV125AT 具有三态输出的四路总线缓冲器

1 特性

- 输入兼容 TTL 电压
- 在 4.5V 至 5.5V V_{CC} 下运行
- 电压为 5V 时, t_{pd} 典型值为 3.8ns
- $V_{CC} = 5V$ 、 $T_A = 25^\circ C$ 时, V_{OLP} (输出接地反弹) 典型值小于 0.8V
- $V_{CC} = 5V$ 、 $T_A = 25^\circ C$ 时, V_{OHV} (输出 V_{OH} 下冲) 典型值大于 2.3V
- 所有端口上均支持以混合模式电压运行
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 250mA, 符合 JESD 17 规范

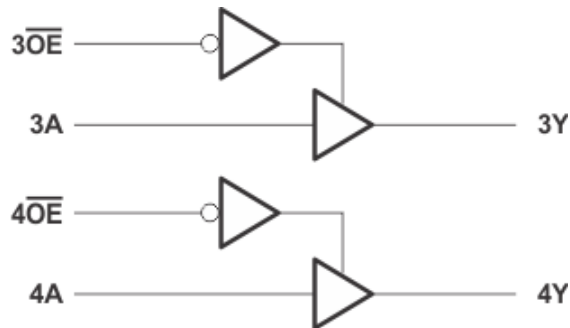
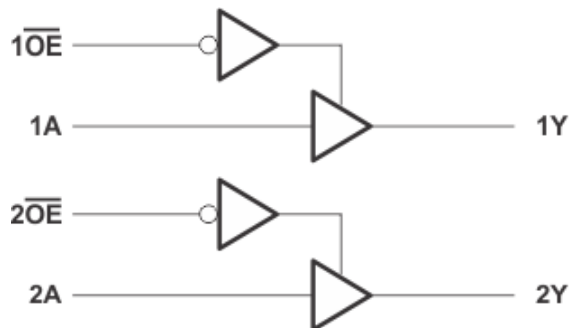
2 说明

SN74LV125AT 器件是一款四路总线缓冲器, 采用具有三态输出的独立线路驱动器。当每个输出的相关输出使能 ($\overline{OE}$) 输入为高电平时, 输出被禁用。

封装信息

器件型号	封装 ¹	封装尺寸 ²
SN74LV125AT	RGY (VQFN , 14)	3.50mm x 3.50mm
	D (SOIC , 14)	8.65mm x 6mm
	NS (SO , 14)	10.20 mm x 7.8 mm
	DB (SSOP , 14)	6.20 mm x 7.8 mm
	PW (TSSOP , 14)	5.00 mm x 6.4 mm

- (1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。
- (2) 封装尺寸 (长 x 宽) 为标称值, 并包括引脚 (如适用)。



简化原理图



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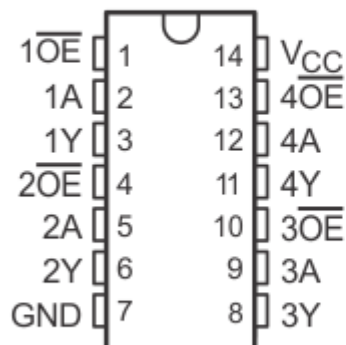
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3 Revision History

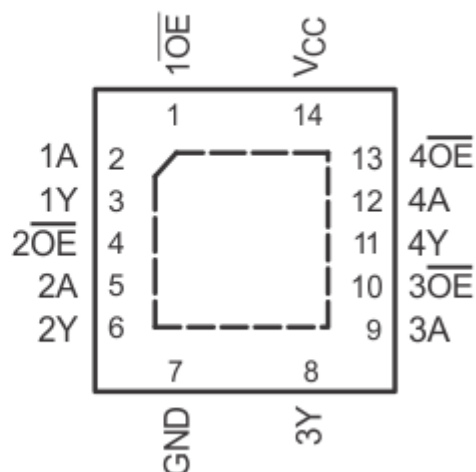
Changes from Revision A (May 2023) to Revision B (July 2023)	Page
• 添加了封装信息表、引脚功能表、ESD 等级表、热信息表、器件功能模式、器件和文档支持部分以及机械、封装和可订购信息部分.....	1

4 Pin Configuration and Functions

SN74LV125A . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV125A . . . RGY PACKAGE
(TOP VIEW)



PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	1OE	I	Output Enable 1, Active Low
2	1A	I	1A Input
3	1Y	O	1Y Output
4	2OE	I	Output Enable 2, Active Low
5	2A	I	2A Input
6	2Y	O	2Y Output
7	GND	—	Ground Pin
8	3Y	O	3Y Output
9	3A	I	3A Input
10	3OE	I	Output Enable 3, Active Low
11	4Y	O	4Y Output
12	4A	I	4A Input
13	4OE	I	Output Enable 4, Active Low
14	VCC	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	- 0.5	7	V
V _I	Input voltage range ⁽²⁾	- 0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	- 0.5	7	V
V _O	Output voltage range ^{(2) (3)}	- 0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		- 20 mA
I _{OK}	Output clamp current	V _O < 0		±50 mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35 mA
	Continuous current through V _{CC} or GND			±70 mA
T _{stg}	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [§ 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

5.2 ESD Ratings

		MAX	UNIT
V _(ESD)	Electrostatic discharge	±2000	V
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN74LV125AT		UNIT
			MIN	MAX	
V _{CC}	Supply voltage		4.5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V		0.8	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 4.5 V to 5.5 V		- 16	mA
I _{OL}	Low-level output current	V _{CC} = 4.5 V to 5.5 V		16	mA
Δt/Δv	Input transition rise or fall rate	V _{CC} = 4.5 V to 5.5 V		20	ns/V
T _A	Operating free-air temperature		- 40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV125AT					UNIT
		D	DB	NS	PW	RGY	
		14 PINS					
R _{θ JA}	Junction-to-ambient thermal resistance	86	96	76	113	47	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			- 40°C to 85°C		- 40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = - 50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = - 16 mA	4.5 V	3.8			3.8		3.8		
V _{OL} Low-level output voltage	I _{OL} = 50 µA	4.5 V		0	0.1		0.1		0.1	V
	I _{OL} = 16 mA	4.5 V			0.55		0.55		0.55	
I _I Input leakage current	V _I = 5.5 V or GND	0 to 5.5 V			±1		±1		±1	µA
I _{OZ} Off-State (High-Impedance State) Output Current	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5	µA
I _{CC} Static supply current	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20		20	µA
ΔI _{CC} ⁽¹⁾ Additional static supply current	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		1.5	
I _{off} Input/Output Power-Off Leakage Current	V _I or V _O = 0 to 5.5 V	0			0.5		5		5	µA
C _i Input capacitance	V _I = V _{CC} or GND				2					pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit And Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			- 40°C to 85°C		- 40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	C _L = 15 pF	1.9	3.8	5.5	1	6.5	1	8.5	ns
t _{en}	OE	Y		2	3.6	5.1	1	6	1	7.5	
t _{dis}	OE	Y		1.5	3.2	6.8	1	8	1	10	
t _{pd}	A	Y	C _L = 50 pF	2.9	5.3	7.5	1	8.5	1	10.5	ns
t _{en}	OE	Y		2.8	5.1	7.1	1	8	1	9.5	
t _{dis}	OE	Y		2.8	6.1	8.8	1	10	1	10	
t _{sk(o)}						1		1		1	

5.7 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER ⁽¹⁾	SN74LV125AT			UNIT
	MIN	TYP	MAX	
V _{OL(P)} Quiet output, maximum dynamic V _{OL}		1.1	1.5	V
V _{OL(V)} Quiet output, minimum dynamic V _{OL}		- 0.3	- 0.8	V
V _{OH(V)} Quiet output, minimum dynamic V _{OH}		3		V
V _{IH(D)} High-level dynamic input voltage	2			V
V _{IL(D)} Low-level dynamic input voltage			0.8	V

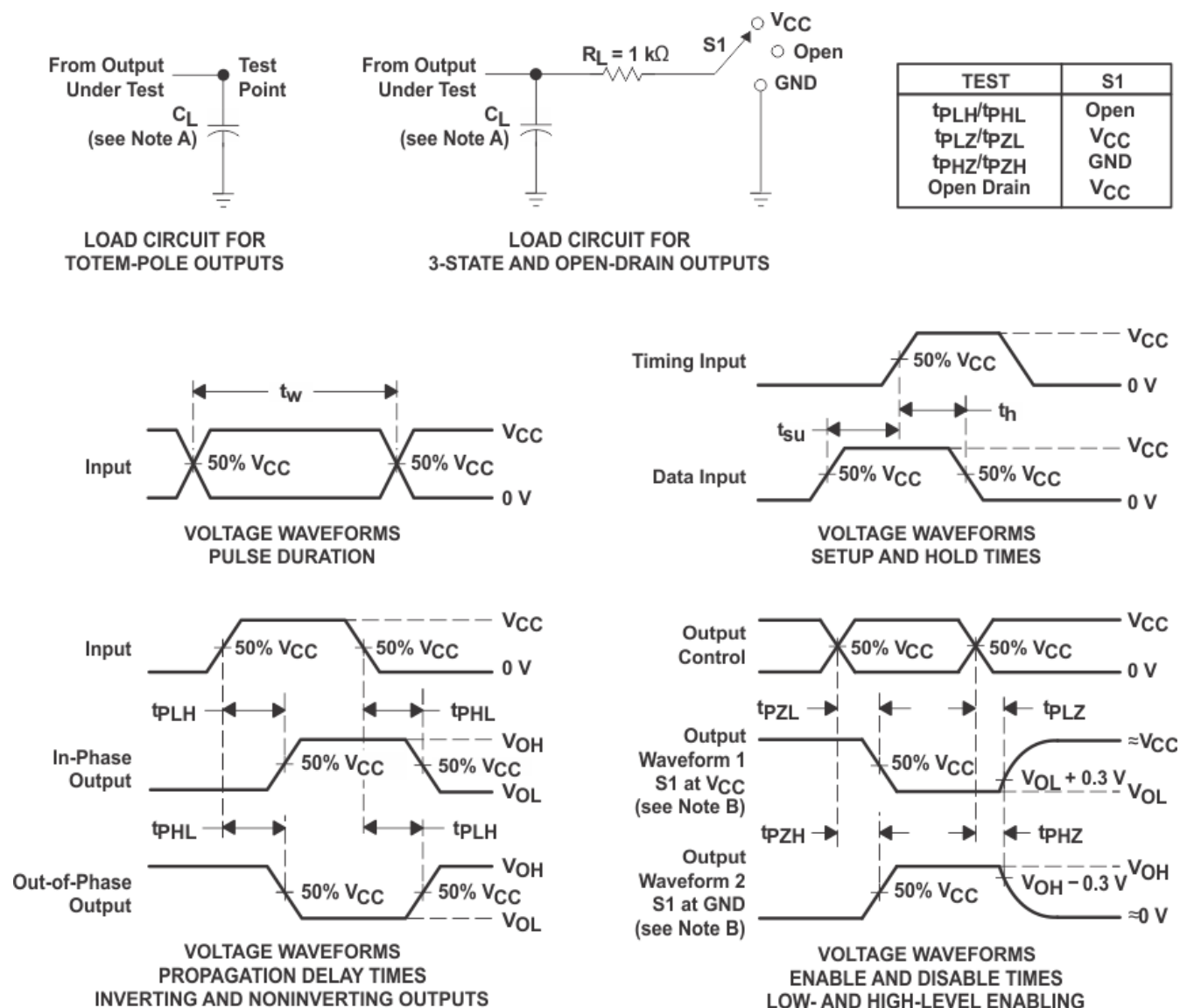
(1) Characteristics are for surface-mount packages only.

5.8 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = -25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	16	pF

6 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit And Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LV125AT is a quadruple bus buffer gate. This device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram

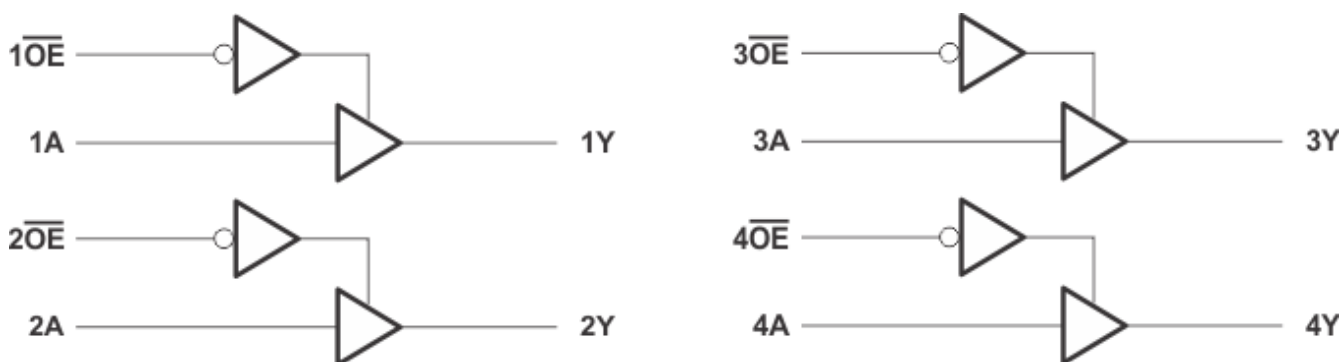


图 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table
(Each Buffer)

INPUTS ⁽¹⁾		OUTPUT ⁽²⁾
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV125AT	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV125ATDBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV125AT	Samples
SN74LV125ATDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LV125AT	Samples
SN74LV125ATNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV125AT	Samples
SN74LV125ATPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV125AT	Samples
SN74LV125ATRGRY	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VV125	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

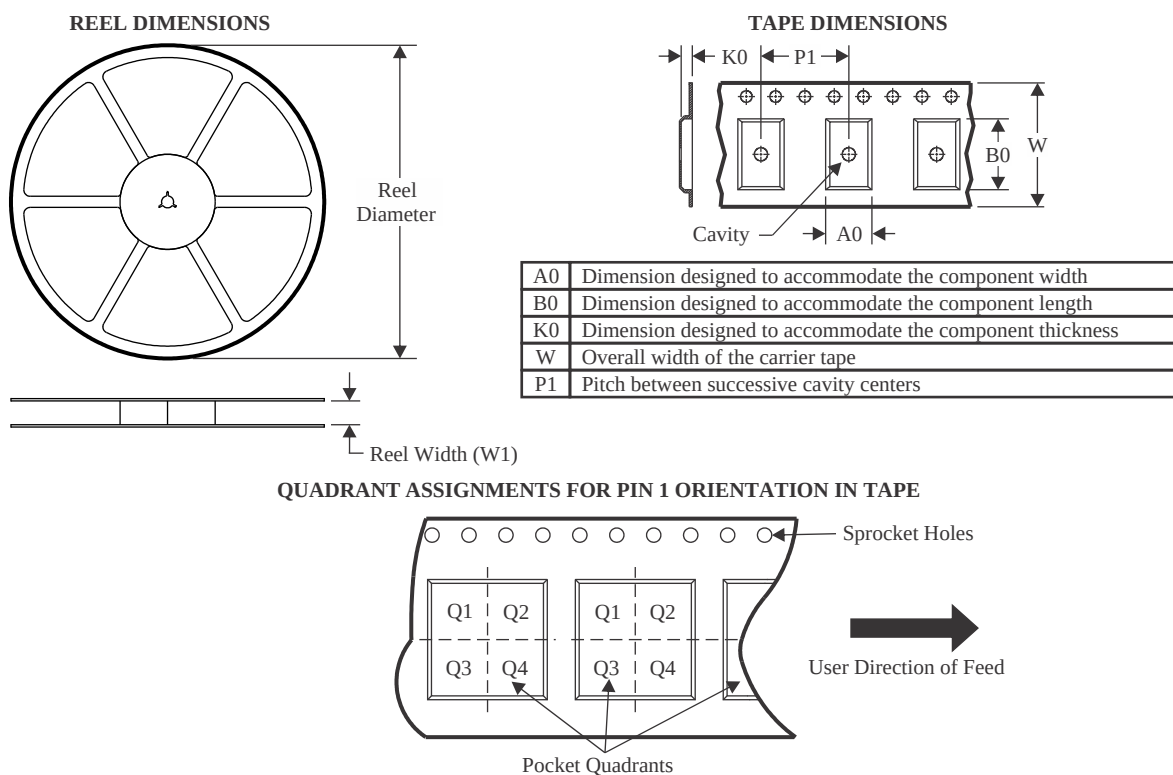
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

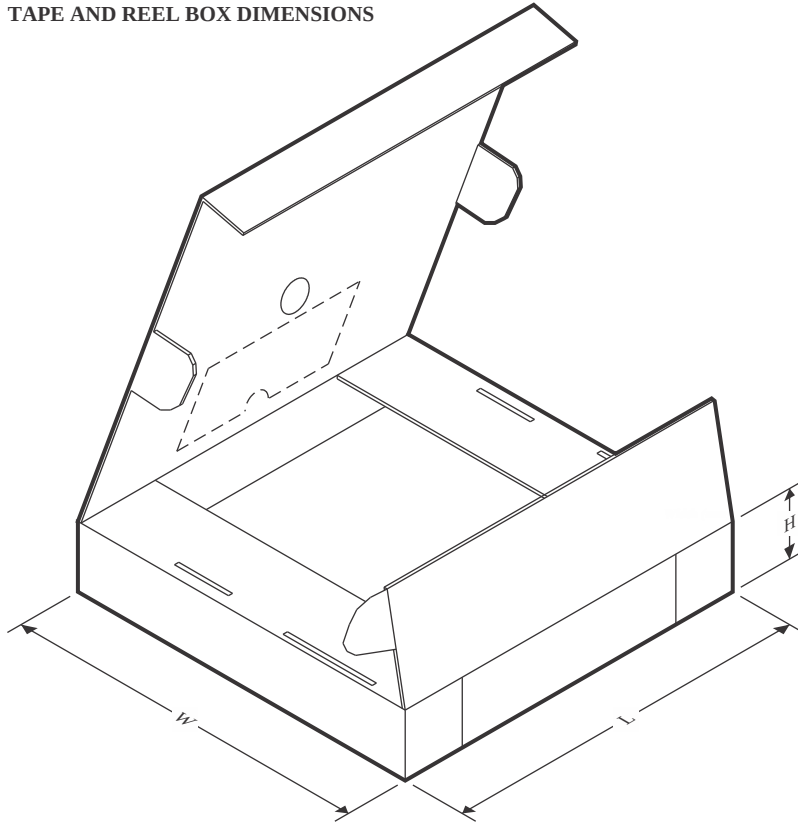
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV125ATDBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV125ATDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV125ATDR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74LV125ATDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV125ATNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV125ATPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV125ATRGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

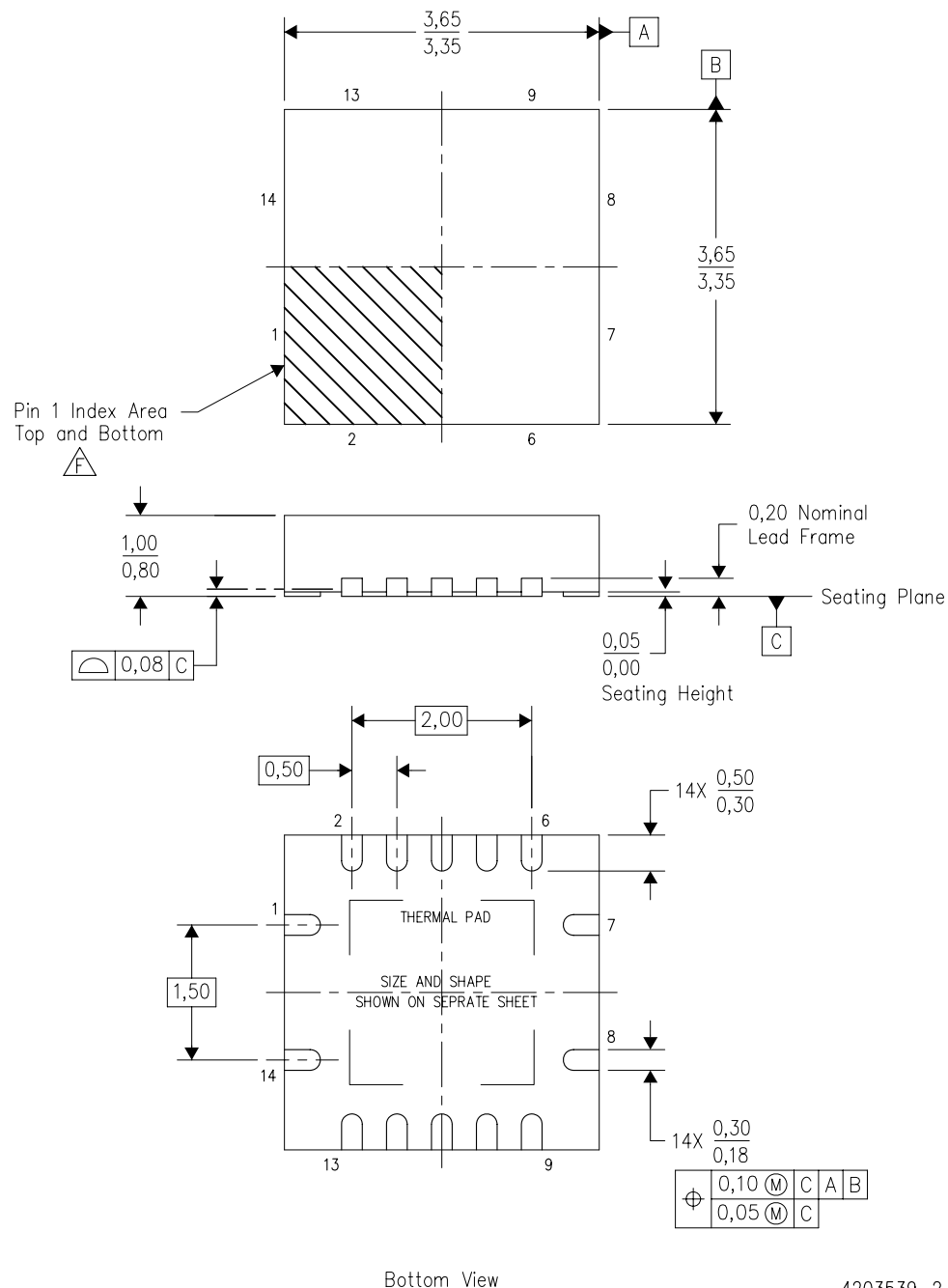


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV125ATDBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV125ATDR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV125ATDR	SOIC	D	14	2500	366.0	364.0	50.0
SN74LV125ATDR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV125ATNSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV125ATPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV125ATRGYR	VQFN	RGY	14	3000	360.0	360.0	36.0

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



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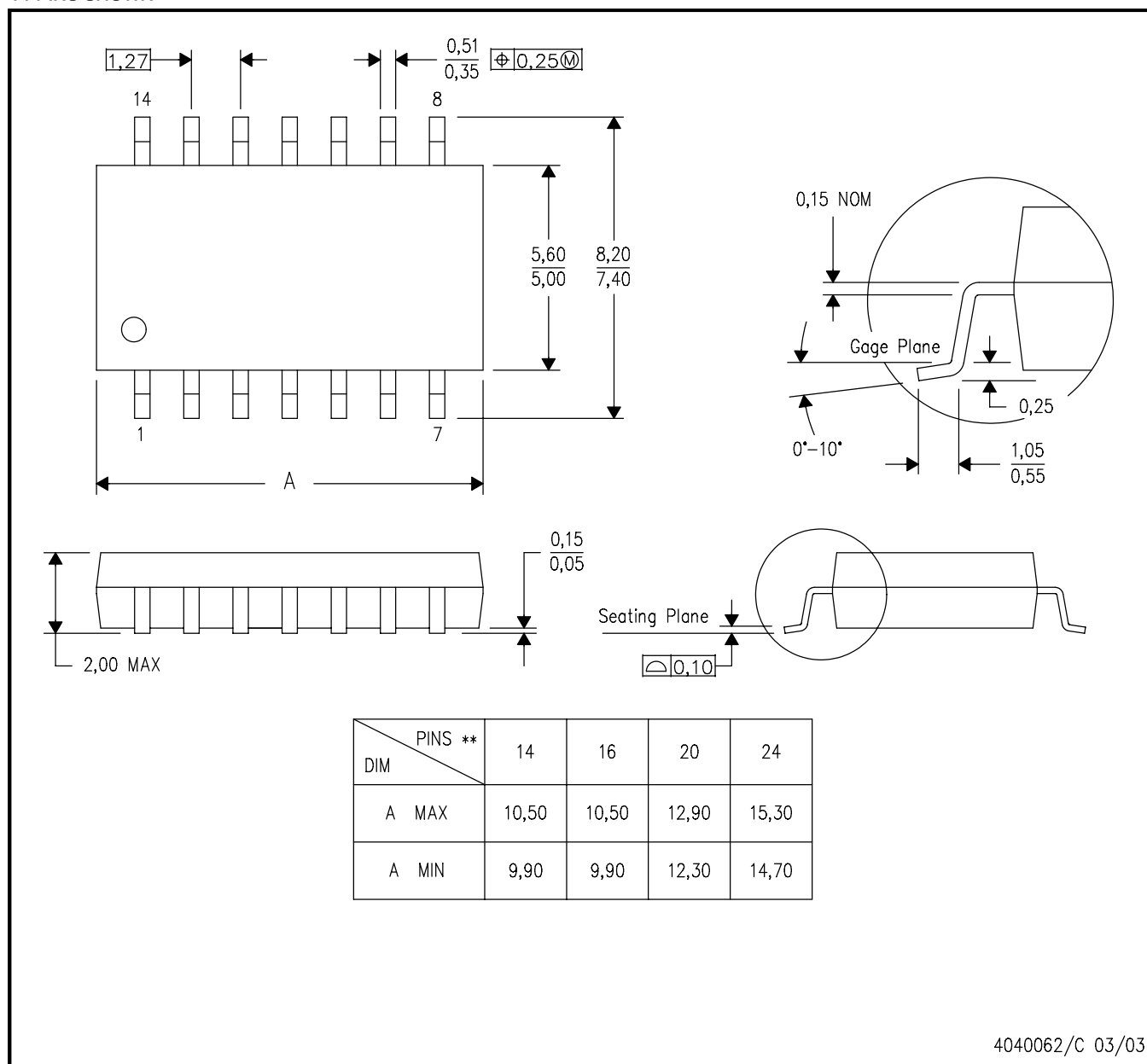
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

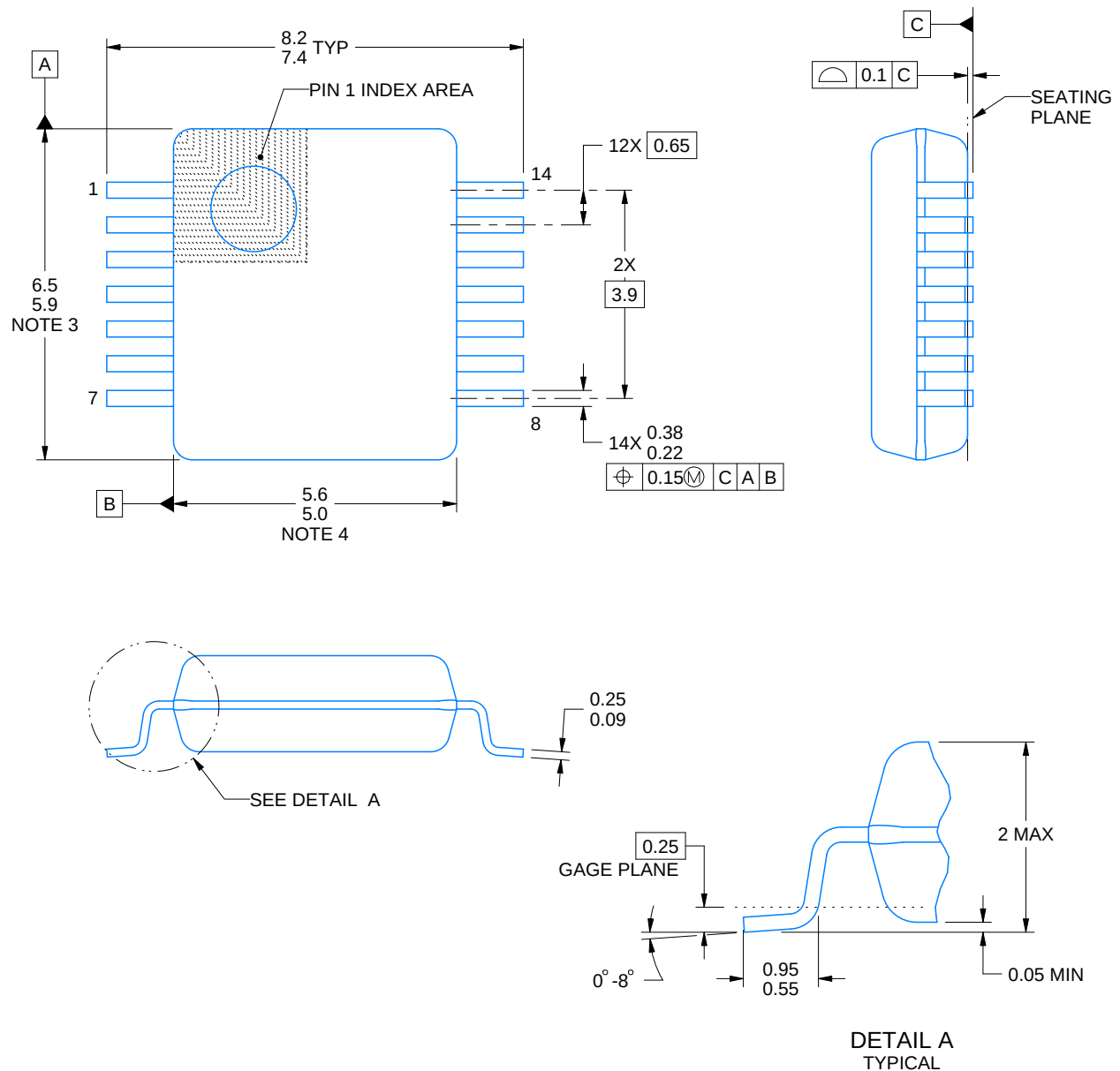
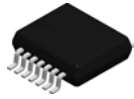
NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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NOTES:

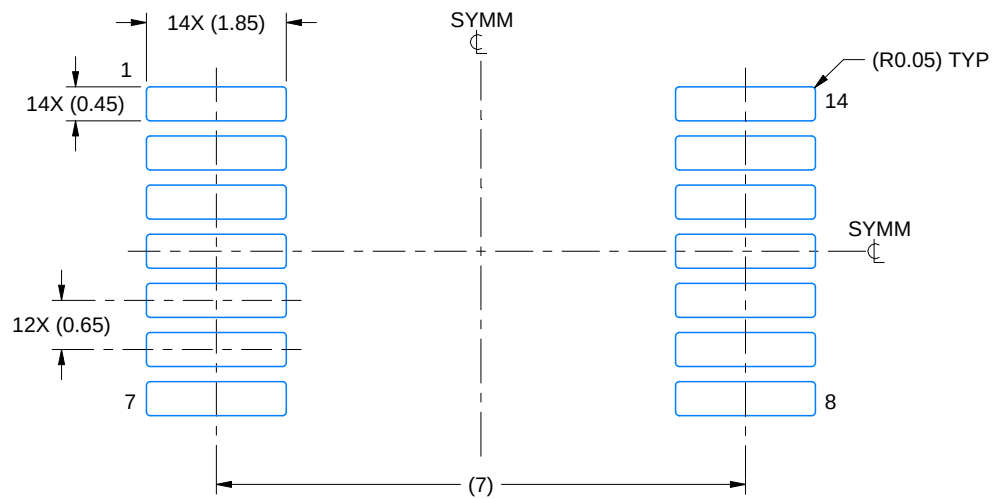
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

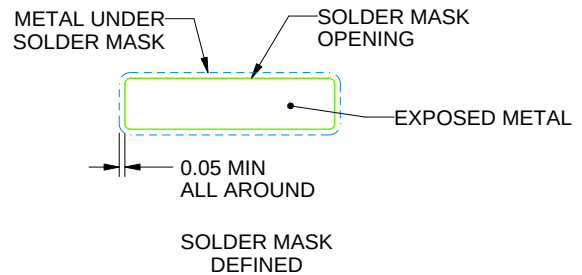
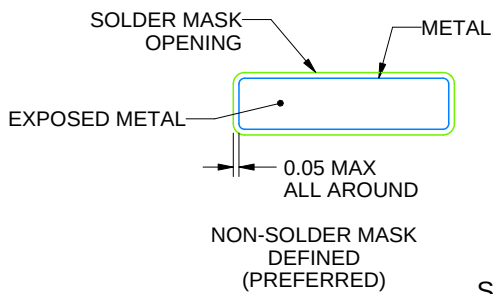
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

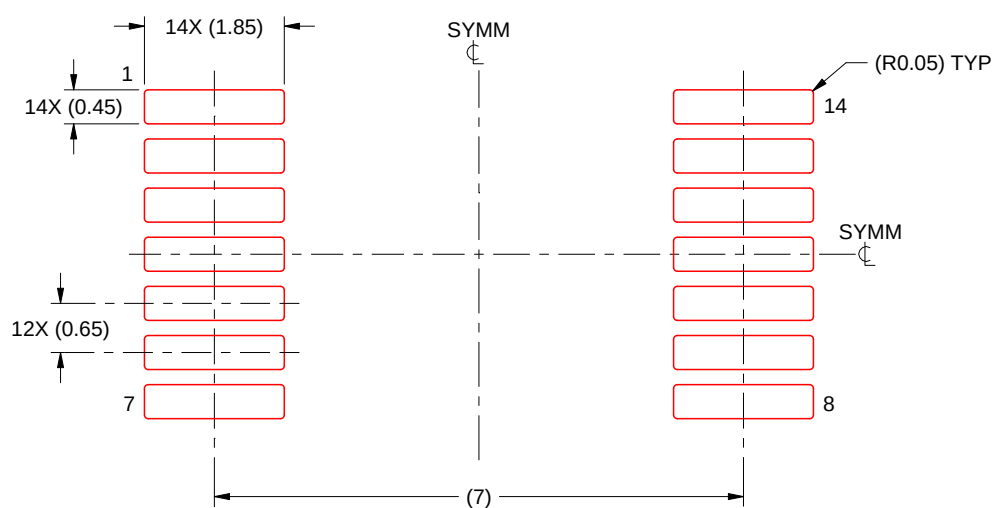
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

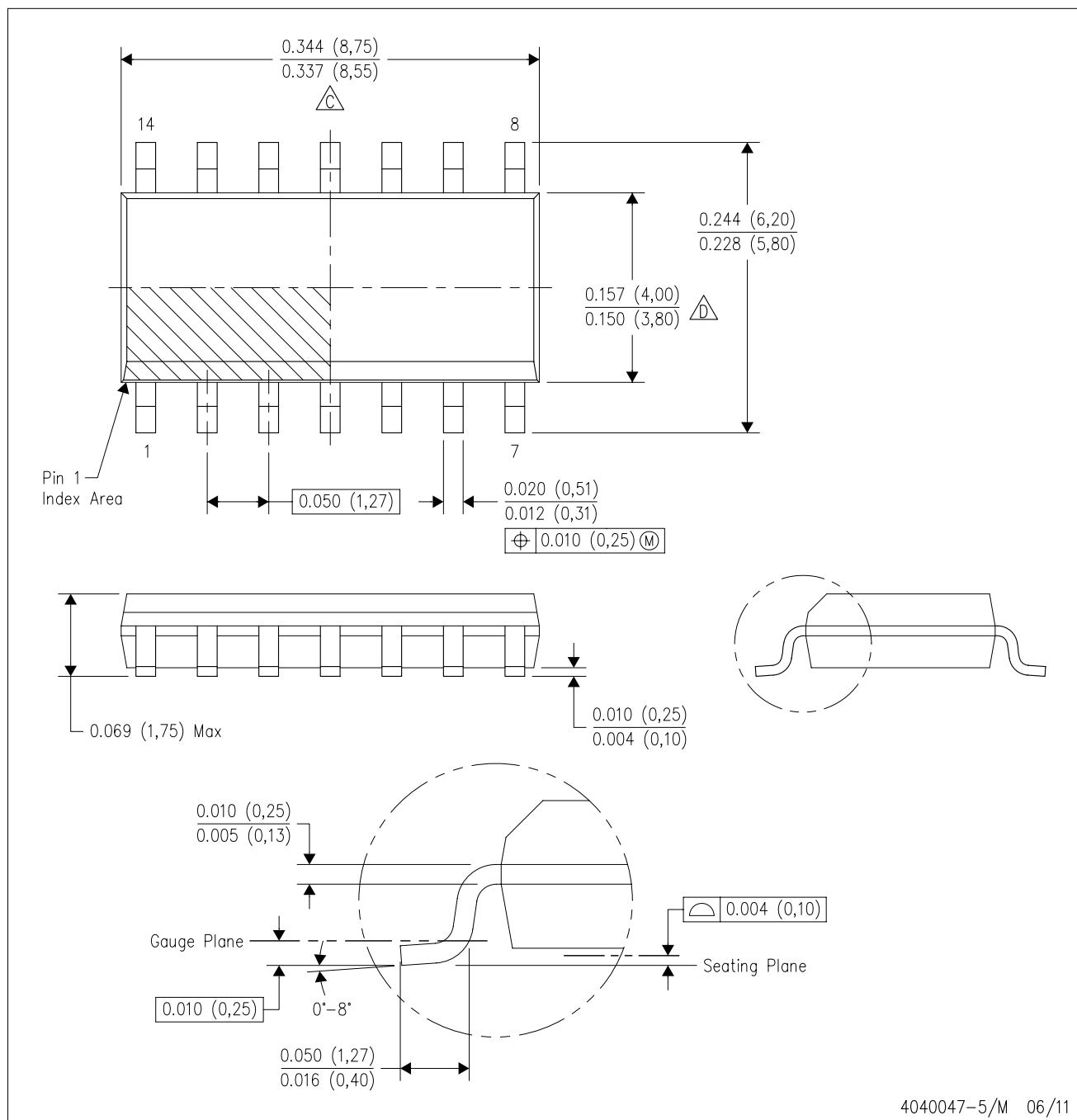
4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

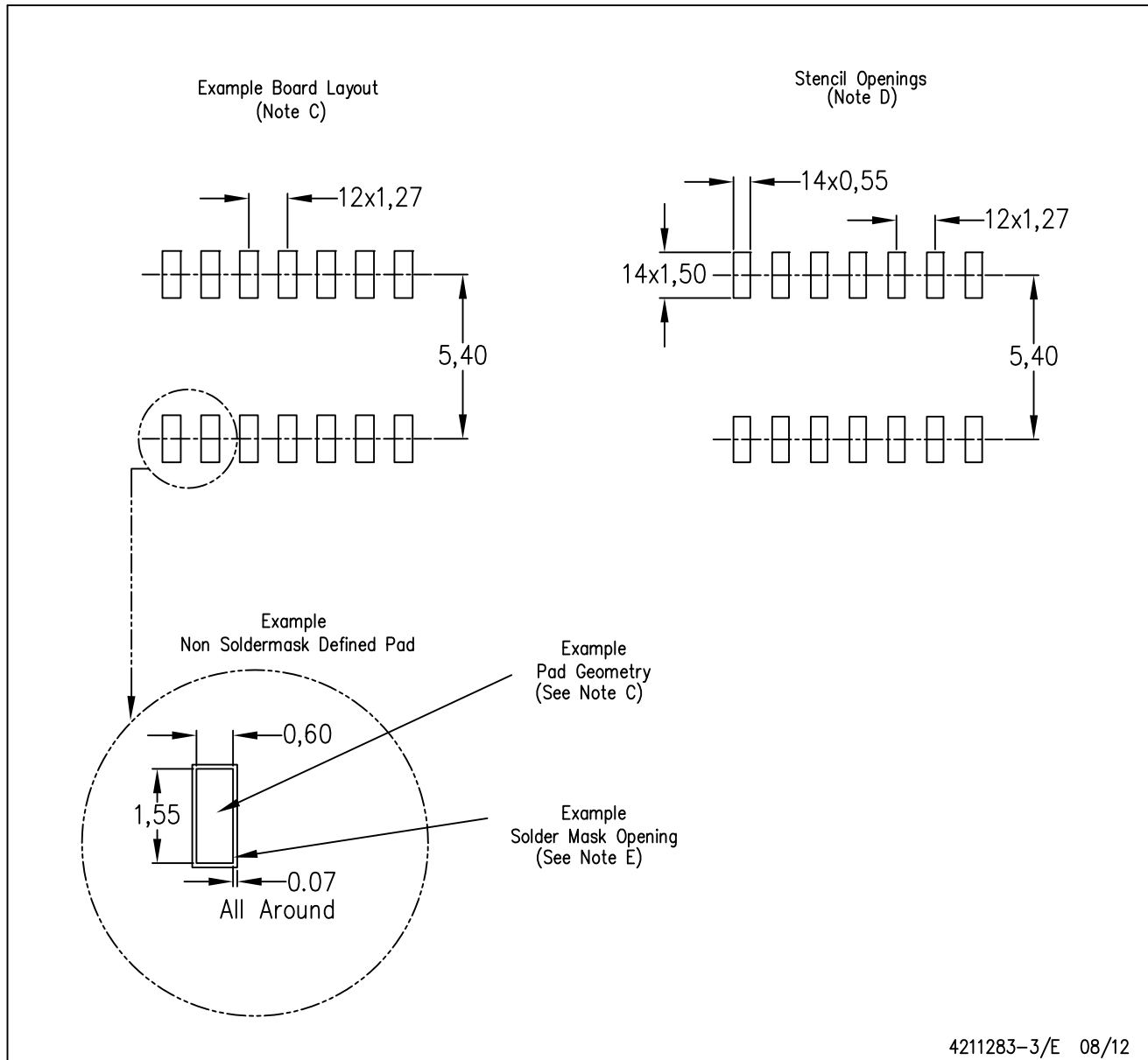


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

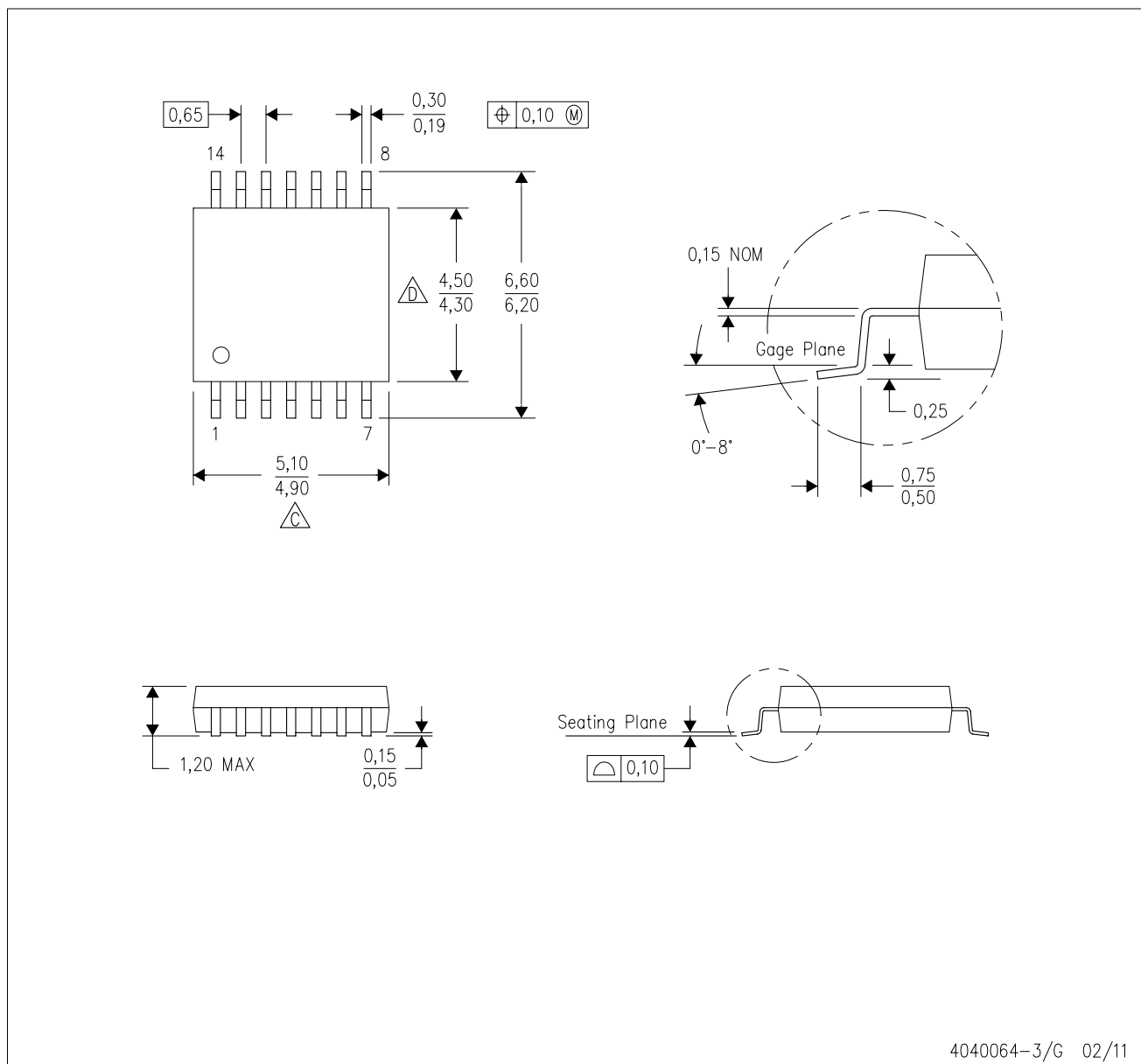
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

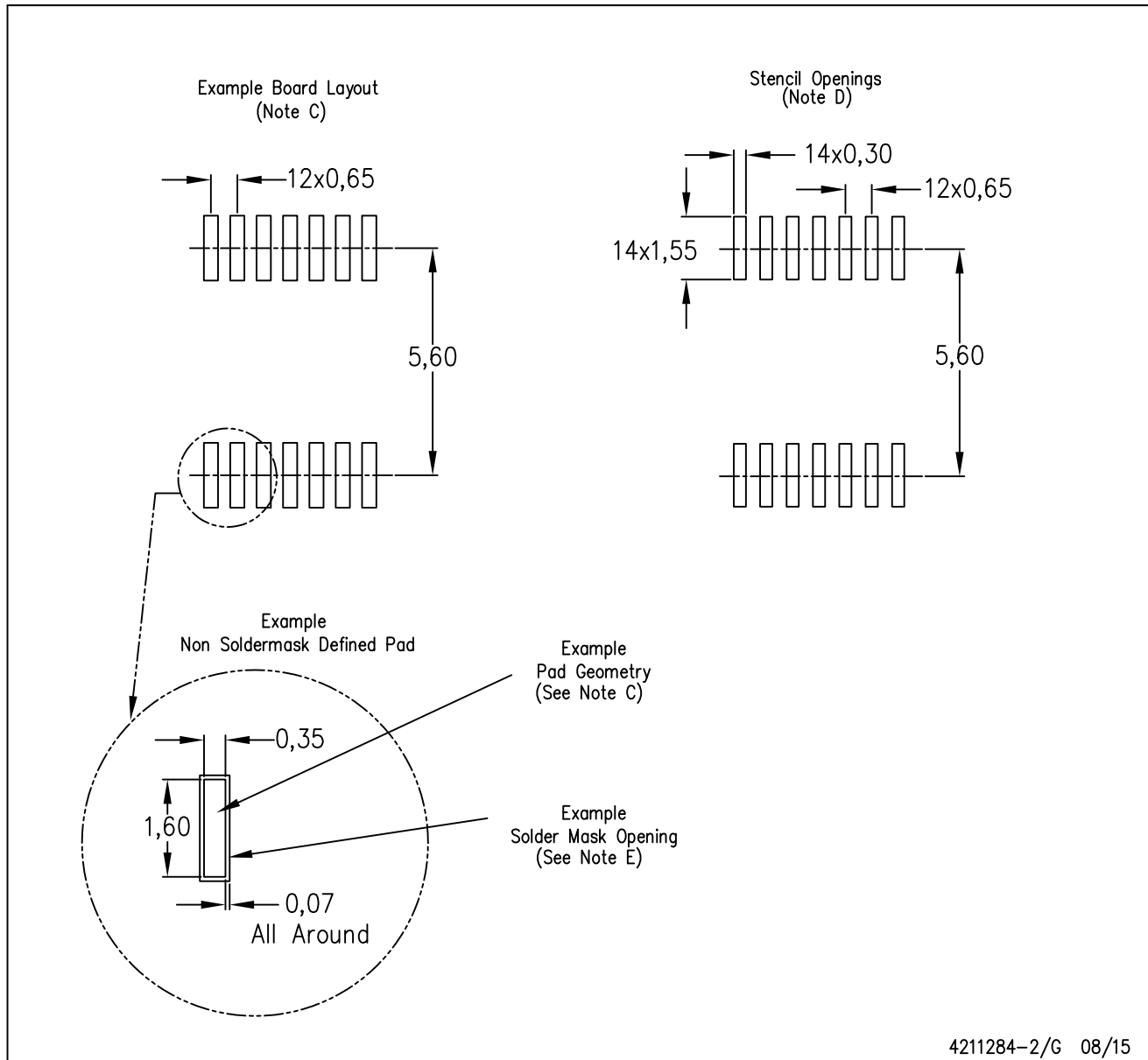
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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