

## SN74AHC244-Q1 具有三态输出的汽车类八路缓冲器/驱动器

### 1 特性

- 符合汽车应用要求
- EPIC™ ( 增强性能植入式 CMOS ) 工艺
- 工作电压范围为 2V 至 5.5V  $V_{CC}$

### 2 说明

SN74AHC244-Q1 包含一个反相器门。该器件执行布尔函数  $Y = \overline{A}$ 。

#### 封装信息

| 器件型号          | 封装 <sup>(1)</sup>    | 封装尺寸 <sup>(2)</sup> |
|---------------|----------------------|---------------------|
| SN74AHC244-Q1 | DBV ( SOT-23 , 5 )   | 2.90 x 1.60mm       |
|               | DCK ( SOT-SC70 , 5 ) | 2.00 x 1.25mm       |

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 ( 长 × 宽 ) 为标称值, 并包括引脚 ( 如适用 )。



简化原理图



## Table of Contents

|                                           |          |                                                                |          |
|-------------------------------------------|----------|----------------------------------------------------------------|----------|
| <b>1 特性</b> .....                         | <b>1</b> | <b>6 Parameter Measurement Information</b> .....               | <b>7</b> |
| <b>2 说明</b> .....                         | <b>1</b> | <b>7 Detailed Description</b> .....                            | <b>8</b> |
| <b>3 Revision History</b> .....           | <b>2</b> | 7.1 Overview.....                                              | 8        |
| <b>4 Function Table</b> .....             | <b>3</b> | 7.2 Functional Block Diagram.....                              | 8        |
| <b>5 Specifications</b> .....             | <b>4</b> | 7.3 Device Functional Modes.....                               | 9        |
| 5.1 Absolute Maximum Ratings.....         | 4        | <b>8 Device and Documentation Support</b> .....                | <b>9</b> |
| 5.2 ESD Ratings.....                      | 4        | 8.1 Documentation Support.....                                 | 9        |
| 5.3 Recommended Operating Conditions..... | 4        | 8.2 接收文档更新通知.....                                              | 9        |
| 5.4 Thermal Information.....              | 5        | 8.3 支持资源.....                                                  | 9        |
| 5.5 Electrical Characteristics.....       | 5        | 8.4 Trademarks.....                                            | 9        |
| 5.6 Switching Characteristics.....        | 5        | 8.5 静电放电警告.....                                                | 9        |
| 5.7 Switching Characteristics.....        | 6        | 8.6 术语表.....                                                   | 9        |
| 5.8 Noise Characteristics.....            | 6        | <b>9 Mechanical, Packaging, and Orderable Information</b> .... | <b>9</b> |
| 5.9 Operating Characteristics.....        | 6        |                                                                |          |

## 3 Revision History

注：以前版本的页码可能与当前版本的页码不同

| <b>Changes from Revision A (April 2008) to Revision B (August 2023)</b> | <b>Page</b> |
|-------------------------------------------------------------------------|-------------|
| • 添加了封装信息表、引脚功能表、ESD 等级表、热信息表、器件功能模式、器件和文档支持部分以及机械、封装和可订购信息部分.....      | <b>1</b>    |

## 4 Function Table

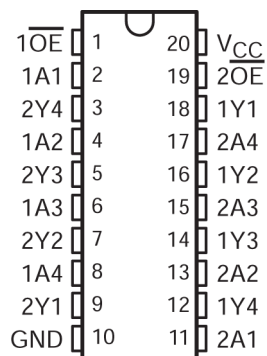


图 4-1. DW or PW Package (Top View)

表 4-1. Pin Functions

| PIN |                   | I/O | DESCRIPTION     |
|-----|-------------------|-----|-----------------|
| NO. | NAME              |     |                 |
| 1   | 1 $\overline{OE}$ | I   | Output Enable 1 |
| 2   | 1A1               | I   | 1A1 Input       |
| 3   | 2Y4               | O   | 2Y4 Output      |
| 4   | 1A2               | I   | 1A2 Input       |
| 5   | 2Y3               | O   | 2Y3 Output      |
| 6   | 1A3               | I   | 1A3 Input       |
| 7   | 2Y2               | O   | 2Y2 Output      |
| 8   | 1A4               | I   | 1A4 Input       |
| 9   | 2Y1               | O   | 2Y1 Output      |
| 10  | GND               | —   | Ground pin      |
| 11  | 2A1               | I   | 2A1 Input       |
| 12  | 1Y4               | O   | 1Y4 Output      |
| 13  | 2A2               | I   | 2A2 Input       |
| 14  | 1Y3               | O   | 1Y3 Output      |
| 15  | 2A3               | I   | 2A3 Input       |
| 16  | 1Y2               | O   | 1Y2 Output      |
| 17  | 2A4               | I   | 2A4 Input       |
| 18  | 1Y1               | O   | 1Y1 Output      |
| 19  | 2 $\overline{OE}$ | I   | Output Enable 2 |
| 20  | VCC               | —   | Power Pin       |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                             |                                                   | MIN                                                       | MAX                   | UNIT |
|-----------------------------|---------------------------------------------------|-----------------------------------------------------------|-----------------------|------|
| V <sub>CC</sub>             | Supply voltage range                              | -0.5                                                      | 7                     | V    |
| V <sub>I</sub> <sup>2</sup> | Input voltage range                               | -0.5                                                      | 7                     | V    |
| V <sub>O</sub> <sup>2</sup> | Output voltage range                              | -0.5                                                      | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>             | Input clamp current                               | (V <sub>I</sub> < 0)                                      | -20                   | mA   |
| I <sub>OK</sub>             | Output clamp current                              | (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> ) | ±20                   | mA   |
| I <sub>O</sub>              | Continuous output current                         | (V <sub>O</sub> = 0 to V <sub>CC</sub> )                  | ±25                   | mA   |
|                             | Continuous current through V <sub>CC</sub> or GND |                                                           | ±50                   | mA   |
| T <sub>stg</sub>            | Storage temperature range                         | -65                                                       | 150                   | °C   |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

|                    |                         |                                                       |          | VALUE | UNIT |
|--------------------|-------------------------|-------------------------------------------------------|----------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>1</sup> | All pins | ±1500 | V    |

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>1</sup>

|                 |                                    | MIN                             | MAX             | UNIT |
|-----------------|------------------------------------|---------------------------------|-----------------|------|
| V <sub>CC</sub> | Supply voltage                     | 2                               | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2 V           | 1.5             | V    |
|                 |                                    | V <sub>CC</sub> = 3 V           | 2.1             |      |
|                 |                                    | V <sub>CC</sub> = 5.5 V         | 3.85            |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2 V           | 0.5             | V    |
|                 |                                    | V <sub>CC</sub> = 3 V           | 0.9             |      |
|                 |                                    | V <sub>CC</sub> = 5.5 V         | 1.65            |      |
| V <sub>I</sub>  | Input voltage                      | 0                               | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     | 0                               | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2 V           | -50             | μA   |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V | -4              | mA   |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   | -8              |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V           | 50              | mA   |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V | 4               | mA   |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   | 8               |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 3.3 V ± 0.3 V | 100             | ns/V |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V   | 20              |      |
| T <sub>A</sub>  | Operating free-air temperature     | -40                             | 125             | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup>                          | SN74AHC244-Q1 |         | UNIT |
|--------------------------------------------------------|---------------|---------|------|
|                                                        | DW            | PW      |      |
|                                                        | 20 PINS       | 20 PINS |      |
| $R_{\theta JA}$ Junction-to-ambient thermal resistance | 58            | 83      | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                                                                 | $V_{CC}$     | $T_A = 25^\circ\text{C}$ |     |            | MIN  | MAX       | UNIT          |
|-----------|---------------------------------------------------------------------------------|--------------|--------------------------|-----|------------|------|-----------|---------------|
|           |                                                                                 |              | MIN                      | TYP | MAX        |      |           |               |
| $V_{OH}$  | $I_{OH} = -50 \mu\text{A}$                                                      | 2 V          | 1.9                      | 2   |            | 1.9  |           | V             |
|           |                                                                                 | 3 V          | 2.9                      | 3   |            | 2.9  |           |               |
|           |                                                                                 | 4.5 V        | 4.4                      | 4.5 |            | 4.4  |           |               |
|           | $I_{OH} = -4 \text{ mA}$                                                        | 3 V          | 2.58                     |     |            | 2.48 |           |               |
|           | $I_{OH} = -8 \text{ mA}$                                                        | 4.5 V        | 3.94                     |     |            | 3.8  |           |               |
| $V_{OL}$  | $I_{OL} = 50 \mu\text{A}$                                                       | 2 V          |                          |     | 0.1        |      | 0.1       | V             |
|           |                                                                                 | 3 V          |                          |     | 0.1        |      | 0.1       |               |
|           |                                                                                 | 4.5 V        |                          |     | 0.1        |      | 0.1       |               |
|           | $I_{OL} = 4 \text{ mA}$                                                         | 3 V          |                          |     | 0.36       |      | 0.5       |               |
|           | $I_{OL} = 8 \text{ mA}$                                                         | 4.5 V        |                          |     | 0.36       |      | 0.5       |               |
| $I_I$     | $V_I = 5.5 \text{ V or GND}$                                                    | 0 V to 5.5 V |                          |     | $\pm 0.1$  |      | $\pm 1$   | $\mu\text{A}$ |
| $I_{OZ}$  | $V_O = V_{CC} \text{ or GND, } V_I (\overline{OE}) = V_{IL} \text{ or } V_{IH}$ | 5.5 V        |                          |     | $\pm 0.25$ |      | $\pm 2.5$ | $\mu\text{A}$ |
| $I_{CC}$  | $V_I = V_{CC} \text{ or GND, } I_O = 0$                                         | 5.5 V        |                          |     | 4          |      | 40        | $\mu\text{A}$ |
| $C_i$     | $V_I = V_{CC} \text{ or GND}$                                                   | 5 V          |                          | 2   | 10         |      |           | pF            |
| $C_o$     | $V_O = V_{CC} \text{ or GND}$                                                   | 5 V          |                          | 3.5 |            |      |           | pF            |

## 5.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | LOAD CAPACITANCE      | $T_A = 25^\circ\text{C}$ |      |     | MIN | MAX  | UNIT |
|-----------|-----------------|-------------|-----------------------|--------------------------|------|-----|-----|------|------|
|           |                 |             |                       | MIN                      | TYP  | MAX |     |      |      |
| $t_{PLH}$ | A               | Y           | $C_L = 15 \text{ pF}$ | 5.8                      | 8.4  |     | 1   | 10   | ns   |
| $t_{PHL}$ |                 |             |                       | 5.8                      | 8.4  |     | 1   | 10   |      |
| $t_{PZH}$ | $\overline{OE}$ | Y           | $C_L = 15 \text{ pF}$ | 6.6                      | 10.6 |     | 1   | 12.5 | ns   |
| $t_{PZL}$ |                 |             |                       | 6.6                      | 10.6 |     | 1   | 12.5 |      |
| $t_{PHZ}$ | $\overline{OE}$ | Y           | $C_L = 15 \text{ pF}$ | 5                        | 9.7  |     | 1   | 11   | ns   |
| $t_{PLZ}$ |                 |             |                       | 5                        | 9.7  |     | 1   | 11   |      |
| $t_{PLH}$ | A               | Y           | $C_L = 50 \text{ pF}$ | 8.3                      | 11.9 |     | 1   | 13.5 | ns   |
| $t_{PHL}$ |                 |             |                       | 8.3                      | 11.9 |     | 1   | 13.5 |      |
| $t_{PZH}$ | $\overline{OE}$ | Y           | $C_L = 50 \text{ pF}$ | 9.1                      | 14.1 |     | 1   | 16   | ns   |
| $t_{PZL}$ |                 |             |                       | 9.1                      | 14.1 |     | 1   | 16   |      |
| $t_{PHZ}$ | $\overline{OE}$ | Y           | $C_L = 50 \text{ pF}$ | 10.3                     | 14   |     | 1   | 16   | ns   |
| $t_{PLZ}$ |                 |             |                       | 10.3                     | 14   |     | 1   | 16   |      |

## 5.7 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT)    | TO (OUTPUT) | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |     |     | MIN | MAX  | UNIT |
|-----------|-----------------|-------------|----------------------|--------------------------|-----|-----|-----|------|------|
|           |                 |             |                      | MIN                      | TYP | MAX |     |      |      |
| $t_{PLH}$ | A               | Y           | $C_L = 15\text{ pF}$ | 3.9                      | 5.5 |     | 1   | 6.5  | ns   |
| $t_{PHL}$ |                 |             |                      | 3.9                      | 5.5 |     | 1   | 6.5  |      |
| $t_{PZH}$ | $\overline{OE}$ | Y           | $C_L = 15\text{ pF}$ | 4.7                      | 7.3 |     | 1   | 8.5  | ns   |
| $t_{PZL}$ |                 |             |                      | 4.7                      | 7.3 |     | 1   | 8.5  |      |
| $t_{PHZ}$ | $\overline{OE}$ | Y           | $C_L = 15\text{ pF}$ | 5                        | 7.2 |     | 1   | 8.5  | ns   |
| $t_{PLZ}$ |                 |             |                      | 5                        | 7.2 |     | 1   | 8.5  |      |
| $t_{PLH}$ | A               | Y           | $C_L = 50\text{ pF}$ | 5.4                      | 7.5 |     | 1   | 8.5  | ns   |
| $t_{PHL}$ |                 |             |                      | 5.4                      | 7.5 |     | 1   | 8.5  |      |
| $t_{PZH}$ | $\overline{OE}$ | Y           | $C_L = 50\text{ pF}$ | 6.2                      | 9.3 |     | 1   | 10.5 | ns   |
| $t_{PZL}$ |                 |             |                      | 6.2                      | 9.3 |     | 1   | 10.5 |      |
| $t_{PHZ}$ | $\overline{OE}$ | Y           | $C_L = 50\text{ pF}$ | 6.7                      | 9.2 |     | 1   | 10.5 | ns   |
| $t_{PLZ}$ |                 |             |                      | 6.7                      | 9.2 |     | 1   | 10.5 |      |

## 5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  <sup>(1)</sup>

| PARAMETER   |                                        | MIN | TYP  | MAX | UNIT |
|-------------|----------------------------------------|-----|------|-----|------|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |     | 0.5  |     | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |     | -0.2 |     | V    |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |     | 4.8  |     | V    |
| $V_{IH(D)}$ | High-level dynamic input voltage       | 3.5 |      |     | V    |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |     |      | 1.5 | V    |

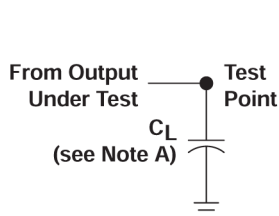
(1) Characteristics are for surface-mount packages only.

## 5.9 Operating Characteristics

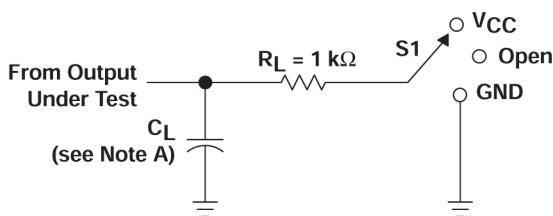
$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS |                    | TYP | UNIT |
|-----------|-------------------------------|-----------------|--------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | No load,        | $f = 1\text{ MHz}$ | 8.6 | pF   |

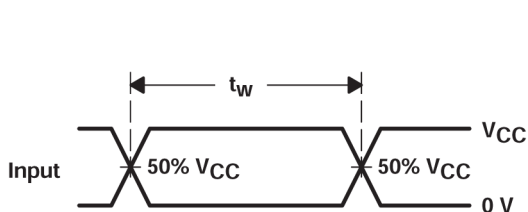
## 6 Parameter Measurement Information



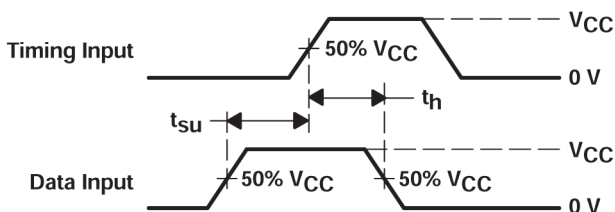
LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS



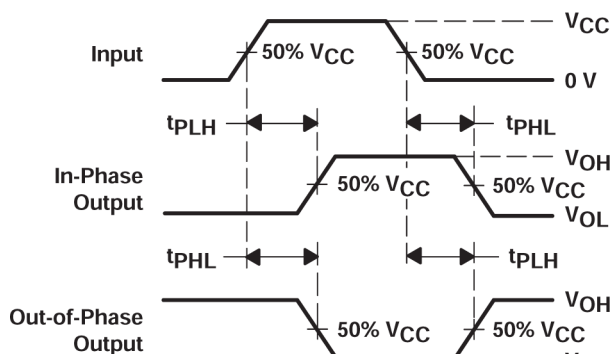
LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS



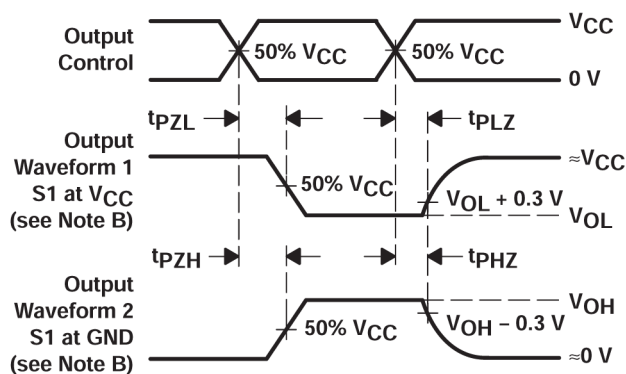
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

图 6-1. Load Circuit and Voltage Waveforms

| TEST              | S1       |
|-------------------|----------|
| $t_{PLH}/t_{PHL}$ | Open     |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND      |
| Open Drain        | $V_{CC}$ |

## 7 Detailed Description

### 7.1 Overview

This octal buffer/driver is designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHC244 is organized as two 4-bit buffers/line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

For the specified high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 7.2 Functional Block Diagram

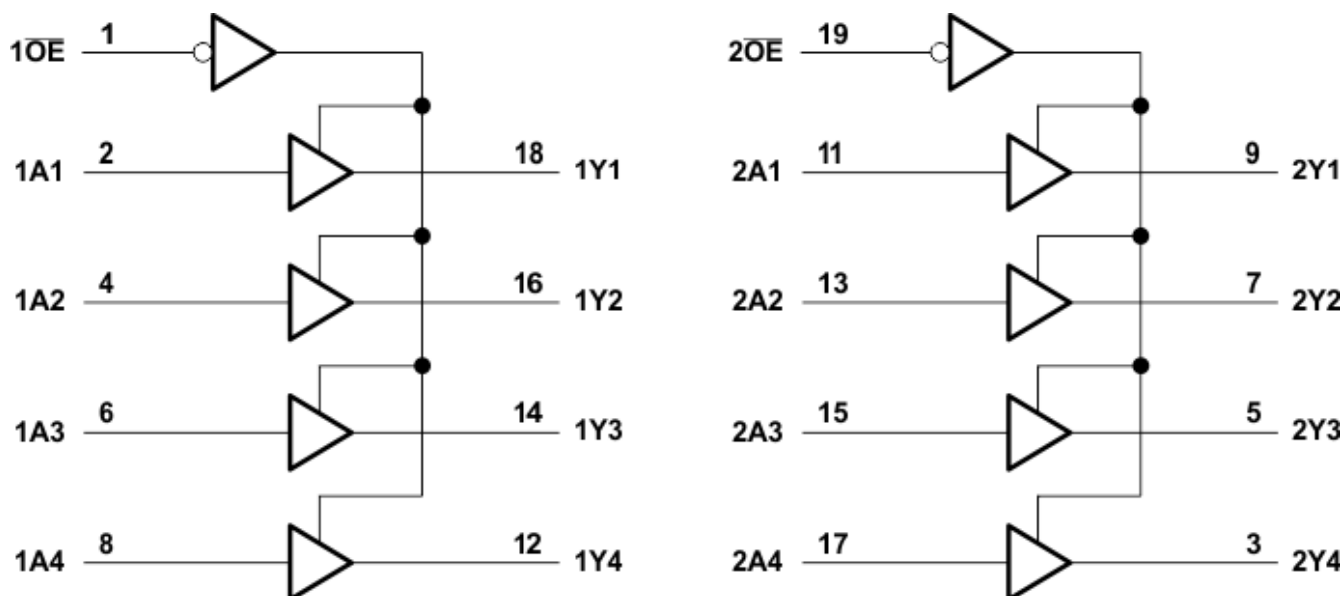
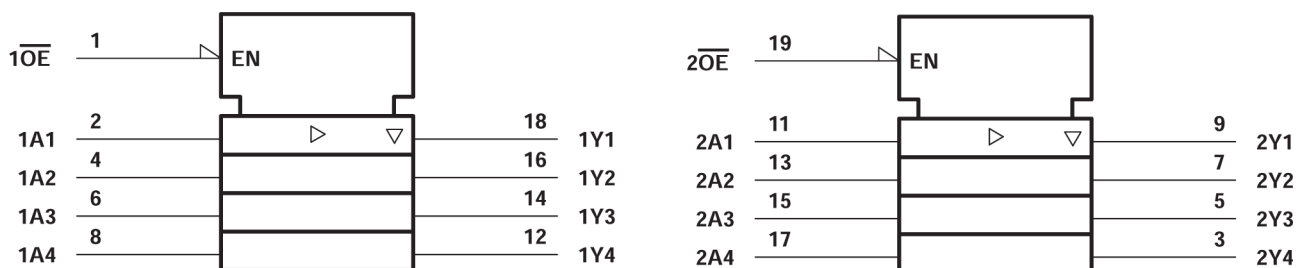


图 7-1. Logic Diagram (Positive Logic)



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

图 7-2. Logic Symbol

## 7.3 Device Functional Modes

表 7-1. (Each 4-Bit Buffer/  
Driver)

| INPUTS |   | OUTPUT Y |
|--------|---|----------|
| OE     | A |          |
| L      | H | H        |
| L      | L | L        |
| H      | X | Z        |

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

| PARTS         | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|---------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN74AHC244-Q1 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

**TI E2E™ 支持论坛** 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 术语表

#### TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device   | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|--------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AHC244QDWRQ1   | ACTIVE        | SOIC         | DW                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | AHC244Q1                | <a href="#">Samples</a> |
| SN74AHC244QPWRG4Q1 | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | AHC244Q1                | <a href="#">Samples</a> |
| SN74AHC244QPWRQ1   | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | AHC244Q1                | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

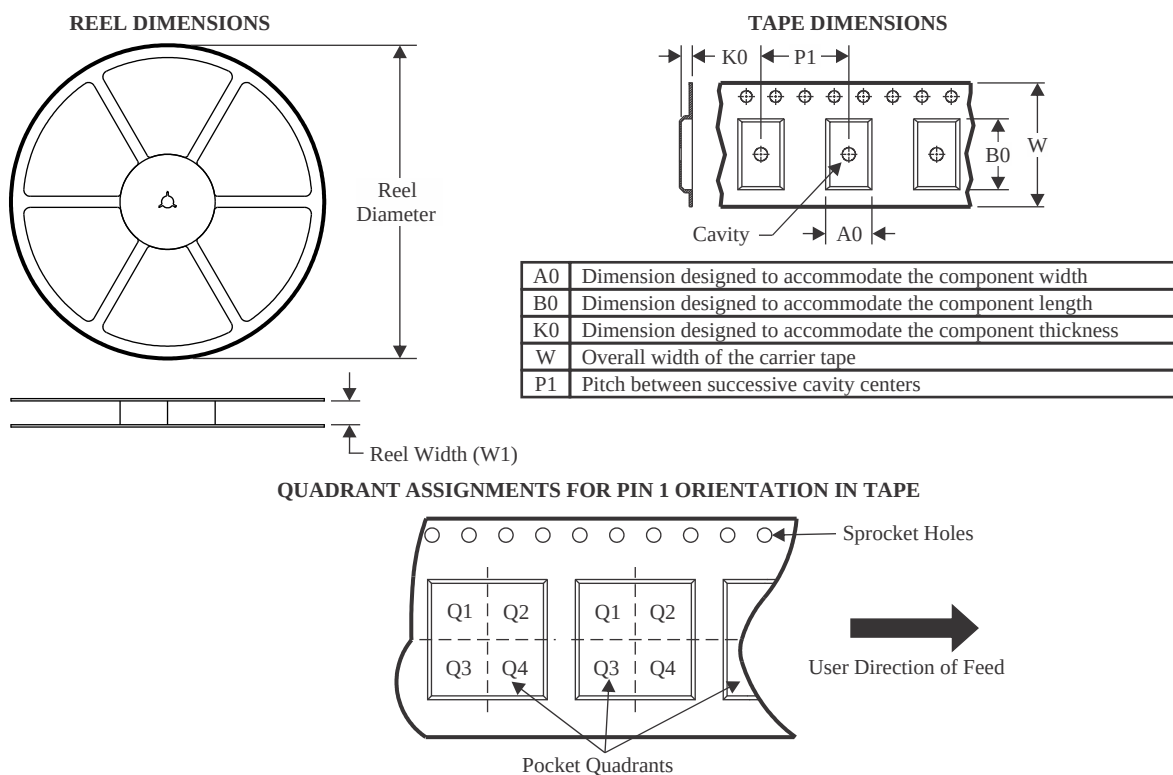
**OTHER QUALIFIED VERSIONS OF SN74AHC244-Q1 :**

- Catalog : [SN74AHC244](#)
- Enhanced Product : [SN74AHC244-EP](#)
- Military : [SN54AHC244](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

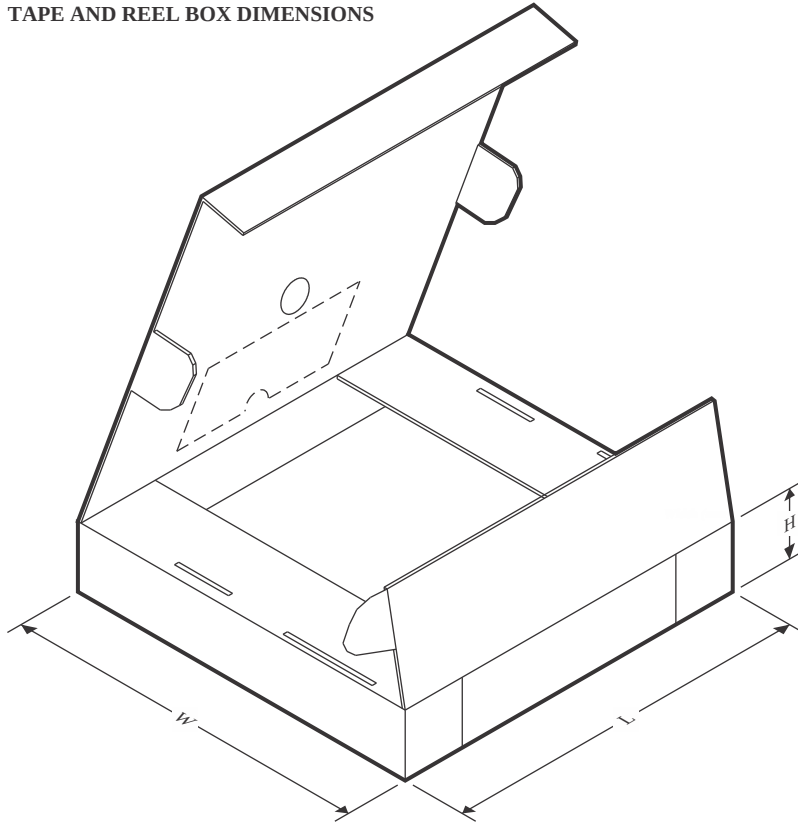
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

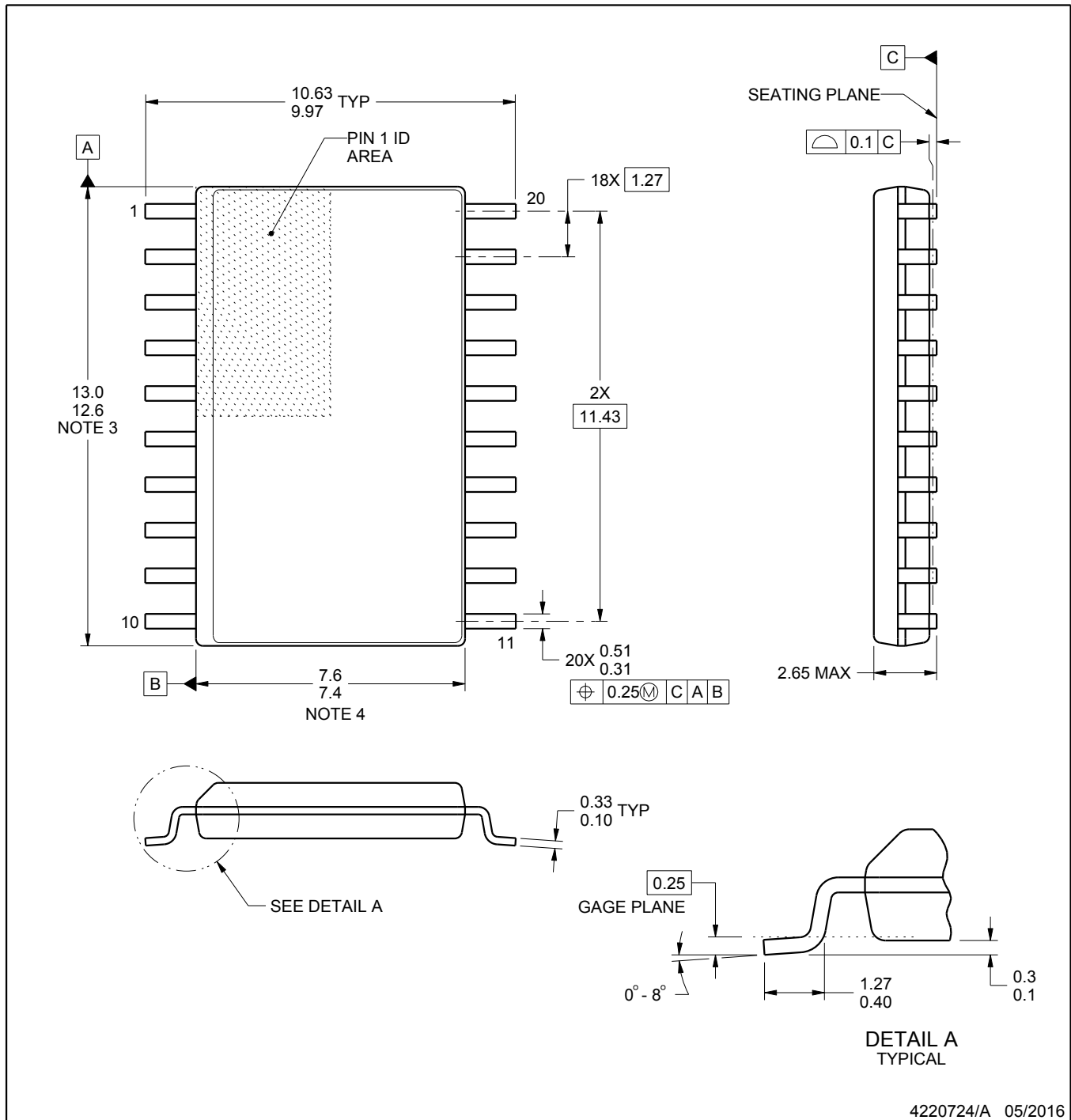
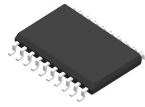
| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC244QDWRQ1   | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74AHC244QPWRG4Q1 | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| SN74AHC244QPWRQ1   | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC244QDWRQ1   | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74AHC244QPWRG4Q1 | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74AHC244QPWRQ1   | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |



4220724/A 05/2016

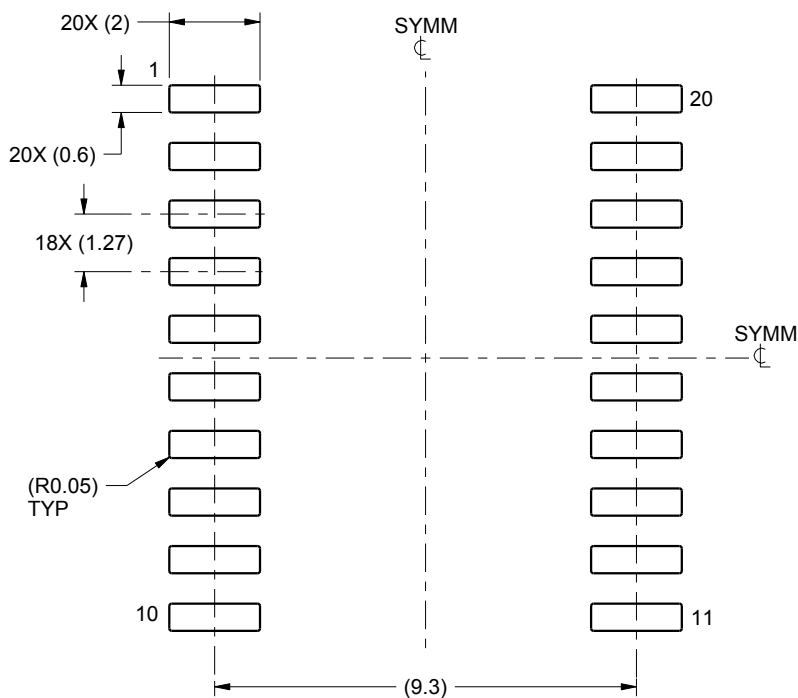
## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

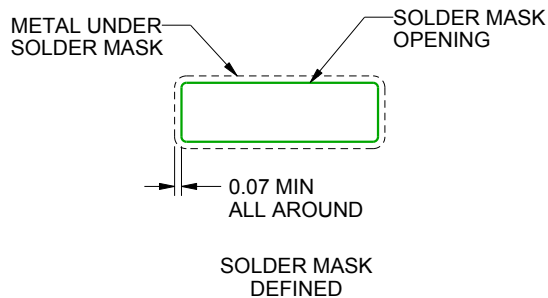
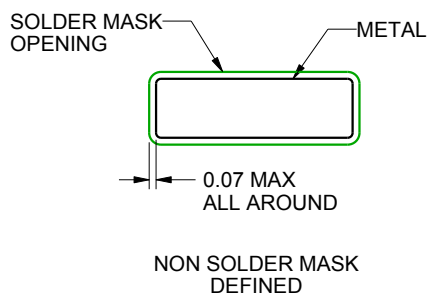
**DW0020A**

### SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

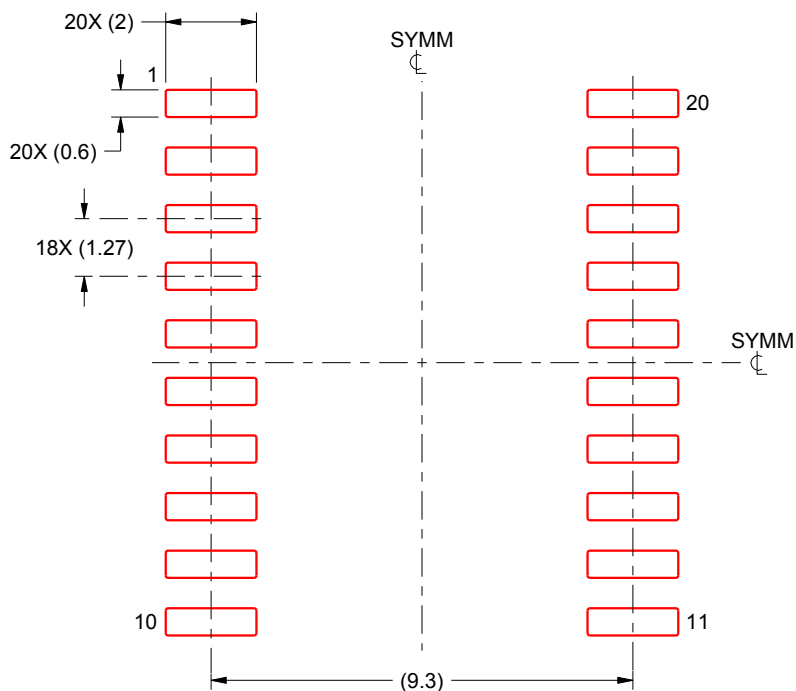
6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

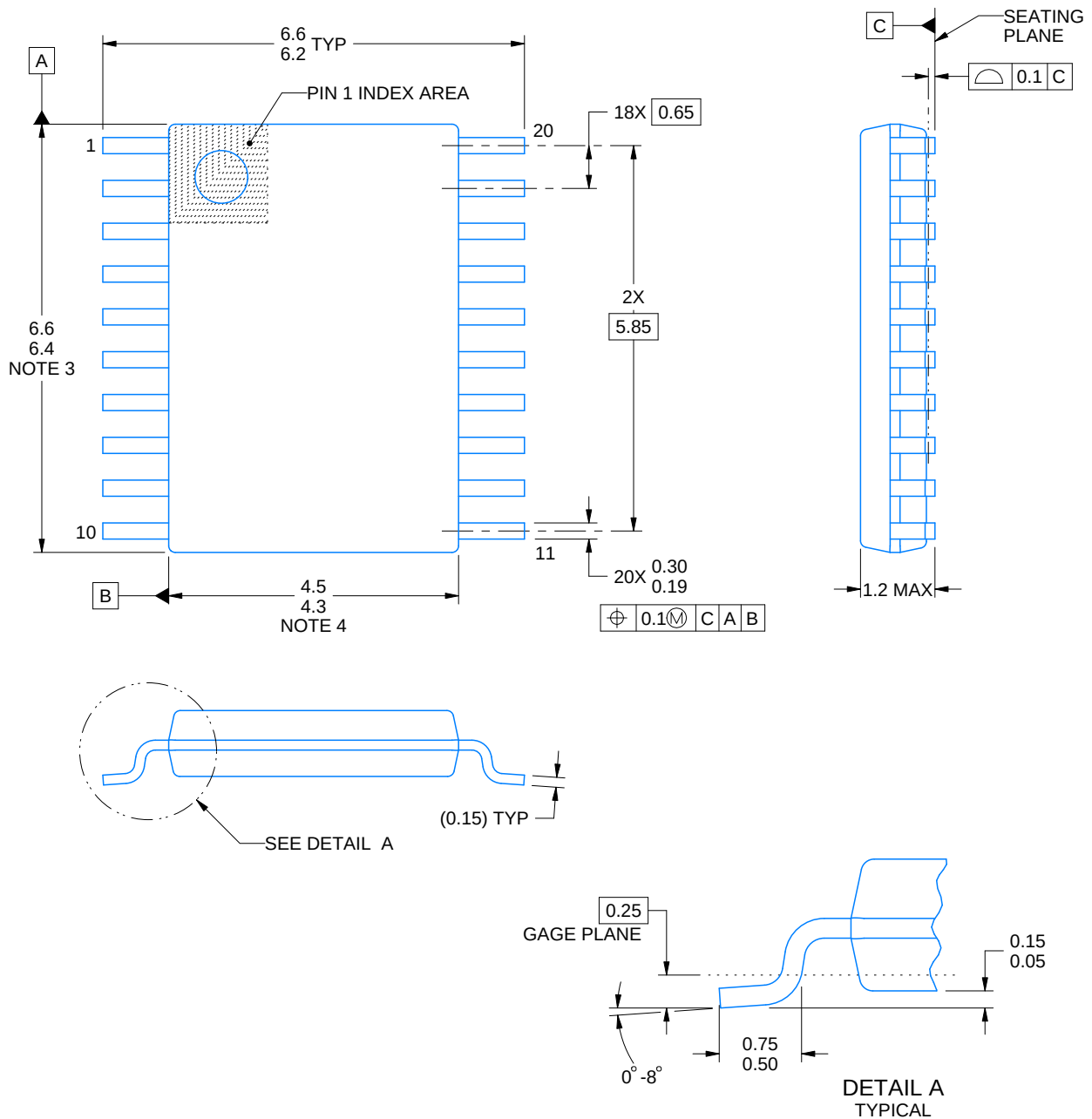
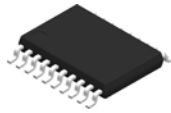


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

## NOTES:

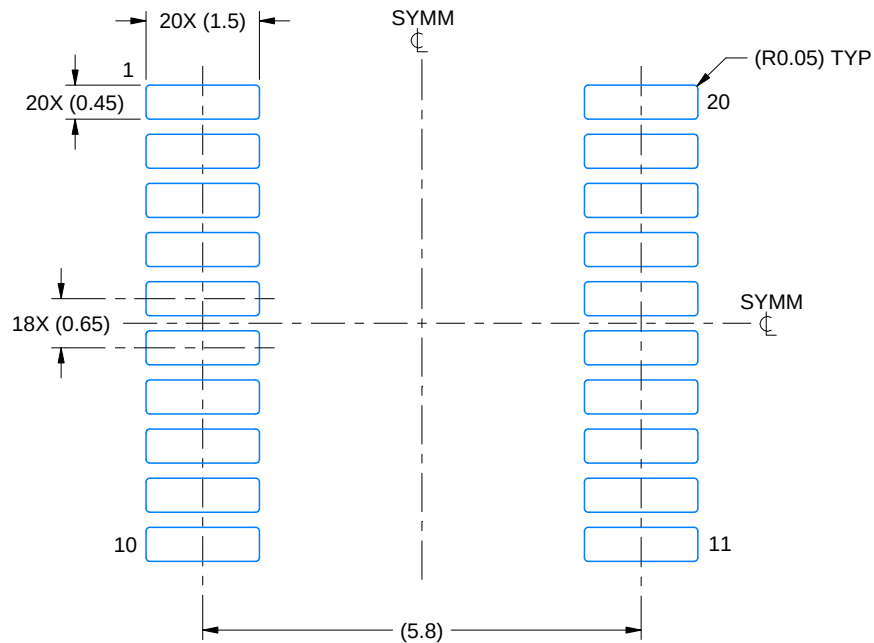
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

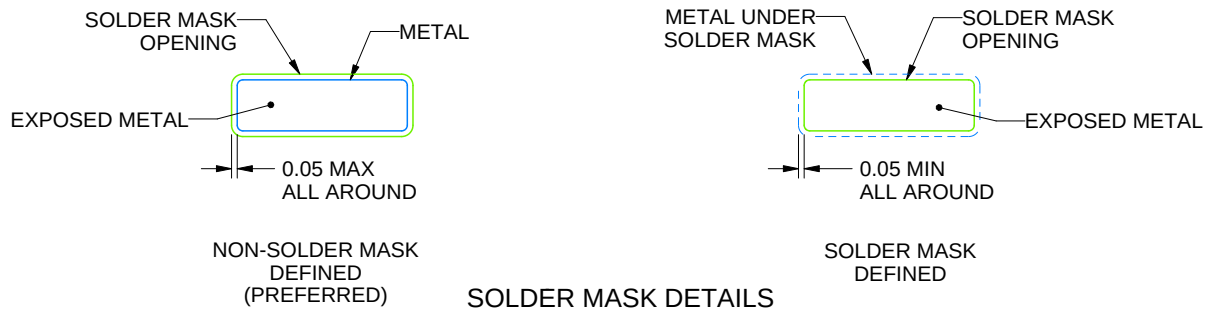
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

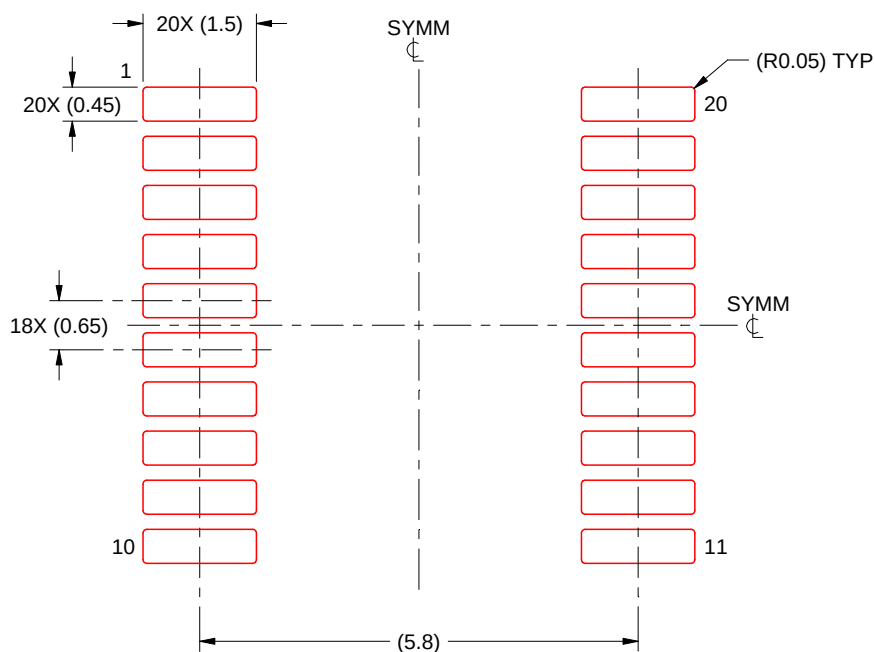
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024，德州仪器 (TI) 公司