

SNx4LVC00A 四路双输入正与非门

1 特性

- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体放电模型
 - 1000V 充电器件模型
- SN74LVC00A 的工作电压范围为 1.65V 至 3.6V
- SN54LVC00A 的工作电压范围为 2V 至 3.6V
- SNx4LVC00A 的额定工作温度范围为 -40°C 至 $+85^{\circ}\text{C}$ 以及 -40°C 至 $+125^{\circ}\text{C}$
- SN54LVC00A 的额定工作温度范围为 -55°C 至 $+125^{\circ}\text{C}$
- 输入电压高达 5.5V
- 电压为 3.3V 时, t_{pd} 最大值为 4.3ns
- V_{OLP} (输出接地反弹) 典型值 $< 0.8\text{V}$ ($V_{\text{CC}} = 3.3\text{V}$ 、 $T_{\text{A}} = 25^{\circ}\text{C}$)
- V_{OHV} (输出 V_{OH} 下冲) 典型值 $> 2\text{V}$ ($V_{\text{CC}} = 3.3\text{V}$ 、 $T_{\text{A}} = 25^{\circ}\text{C}$)
- 闩锁性能超过 250mA, 符合 JESD 17 规范
- 对于符合 MIL-PRF-38535 标准的产品, 所有参数均经过测试, 除非另有说明。对于所有其他产品, 生产流程不一定包含对所有参数的测试。

2 应用

- AV 接收器
- 音频接口盒: 便携
- 蓝光播放器与家庭影院
- MP3 播放器或录像机
- 个人数字助理 (PDA)
- 电源: 电信或服务器交流/直流电源: 单控制器: 模拟和数字
- 固态硬盘 (SSD): 客户端和企业级
- 电视: LCD 电视、数字电视和高清电视 (HDTV)
- 平板电脑: 企业级
- 视频分析: 服务器
- 无线耳机、键盘和鼠标

3 说明

SN54LVC00A 四路双输入正与非门可在 2.7V 至 3.6V V_{CC} 下运行, SN74LVC00A 四路双输入正与非门可在 1.65V 至 3.6V V_{CC} 下运行。

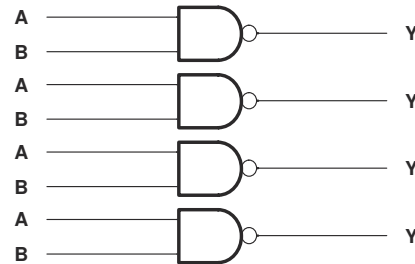
SNx4LVC00A 器件以正逻辑执行布尔函数 $Y = \overline{A \cdot B}$ 或 $Y = \overline{A} + \overline{B}$ 。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V/5V 的混合系统环境中将这些器件用作转换器。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	封装尺寸 ⁽³⁾
SNx4LVC00A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.91mm
	DB (SSOP, 14)	6.2mm × 7.8mm	6.20mm × 5.30mm
	NS (SOP, 14)	10.2mm × 7.8mm	10.30mm × 5.30mm
	PW (TSSOP, 14)	5mm × 4.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.5mm × 3.5mm	3.50mm × 3.50mm
	FK (LCCC, 20)	8.9mm × 8.9mm	8.89mm × 8.89mm
	J (CDIP, 14)	19.55mm × 7.9mm	19.55mm × 6.7mm
	W (CFP, 14)	9.21mm × 9mm	9.21mm × 6.28mm

- 更多信息, 请参阅第 11 节。
- 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。
- 封装尺寸 (长 × 宽) 为标称值, 不包括引脚。



简化原理图



Table of Contents

1 特性	1	7 Detailed Description	9
2 应用	1	7.1 Overview.....	9
3 说明	1	7.2 Functional Block Diagram.....	9
4 Pin Configuration and Functions	3	7.3 Feature Description.....	9
5 Specifications	4	7.4 Device Functional Modes.....	10
5.1 Absolute Maximum Ratings.....	4	8 Application and Implementation	11
5.2 ESD Ratings.....	4	8.1 Application Information.....	11
5.3 Recommended Operating Conditions, SN54LVC00A.....	4	8.2 Typical Application.....	11
5.4 Recommended Operating Conditions, SN74LVC00A.....	5	8.3 Layout.....	12
5.5 Thermal Information.....	5	9 Device and Documentation Support	13
5.6 Electrical Characteristics, SN54LVC00A.....	6	9.1 Related Links.....	13
5.7 Electrical Characteristics, SN74LVC00A.....	6	9.2 Receiving Notification of Documentation Updates....	13
5.8 Switching Characteristics, SN54LVC00A.....	6	9.3 支持资源.....	13
5.9 Switching Characteristics, SN74LVC00A.....	7	9.4 Trademarks.....	13
5.10 Operating Characteristics.....	7	9.5 静电放电警告.....	13
5.11 Typical Characteristics.....	7	9.6 术语表.....	13
6 Parameter Measurement Information	8	11 Mechanical, Packaging, and Orderable Information	14

4 Pin Configuration and Functions

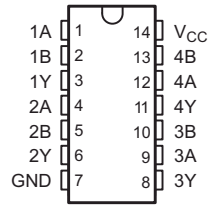
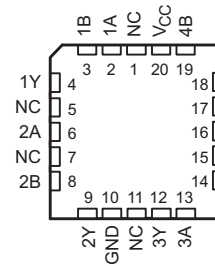


图 4-1. SN54LVC00A J or W Package; SN74LVC00A D, DB, NS, or PW Package 14-Pin CDIP, CFP SOIC, SSOP, SO, or TSSOP (Top View)



NC - No internal connection

图 4-2. SN54LVC00A FK Package 20-Pin LCCC (Top View)

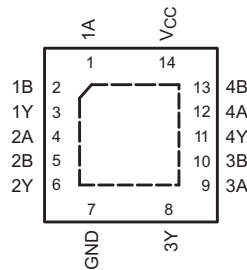


图 4-3. SN74LVC00A BQA or RGY Package 14-Pin WQFN or VQFN (Top View)

表 4-1. Pin Functions

PIN					TYPE	DESCRIPTION
NAME	SN74LVC00A		SN54LVC00A			
	D, DB, NS, PW	BQA, RGY	J, W	FK		
1A	1	1	1	2	I	Gate 1 input
1B	2	2	2	3	I	Gate 1 input
1Y	3	3	3	4	O	Gate 1 output
2A	4	4	4	6	I	Gate 2 input
2B	5	5	5	8	I	Gate 2 input
2Y	6	6	6	9	O	Gate 2 output
GND	7	7	7	10	I	Ground Pin
3Y	8	8	8	12	O	Gate 3 output
3A	9	9	9	13	I	Gate 3 input
3B	10	10	10	14	I	Gate 3 input
4Y	11	11	11	16	O	Gate 4 output
4A	12	12	12	18	I	Gate 4 input
4B	13	13	13	19	I	Gate 4 input
V _{CC}	14	14	14	20	—	Positive supply
NC	—	—	—	1	—	No Connection
				5		
				7		
				11		
				15		
				17		

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	6.5	V
V _I	Input voltage ⁽²⁾		−0.5	6.5	V
V _O	Output voltage ⁽²⁾ ⁽³⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
I _O	Continuous output current		±50		mA
V _{CC}	Continuous current through GND		±100		mA
P _{tot}	Power dissipation ⁽⁴⁾ ⁽⁵⁾	T _A = −40°C to +125°C	500		mW
T _J	Junction temperature		150		°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.
- (4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (5) For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions, SN54LVC00A

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54LVC00A		UNIT
			−55°C to +125°C		
			MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		−12	mA
		V _{CC} = 3 V		−24	
I _{OL}	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.4 Recommended Operating Conditions, SN74LVC00A

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN74LVC00A						UNIT
			T _A = 25°C		–40°C to 85°C		–40°C to 125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		0.7		0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		0.8		
V _I	Input voltage		0	5.5	0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4		–4		–4		mA
		V _{CC} = 2.3 V	–8		–8		–8		
		V _{CC} = 2.7 V	–12		–12		–12		
		V _{CC} = 3 V	–24		–24		–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		4		4		mA
		V _{CC} = 2.3 V	8		8		8		
		V _{CC} = 2.7 V	12		12		12		
		V _{CC} = 3 V	24		24		24		

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC00A						UNIT
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	102.3	127.8	140.4	123.8	150.8	92.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics, SN54LVC00A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC00A		UNIT
			–55°C to +125°C		
			MIN	MAX	
V _{OH}	I _{OH} = –100 μA	2.7 V to 3.6 V	V _{CC} – 0.2		V
	I _{OH} = –12 mA	2.7 V	2.2		
		3 V	2.4		
	I _{OH} = –24 mA	3 V	2.2		
V _{OL}	I _{OL} = 100 μA	2.7 V to 3.6 V	0.2		V
	I _{OL} = 12 mA	2.7 V	0.4		
	I _{OL} = 24 mA	3 V	0.55		
I _I	V _I = 5.5 V or GND	3.6 V	±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500		μA

5.7 Electrical Characteristics, SN74LVC00A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN74LVC00A						UNIT
			$T_A = 25^\circ C$			–40°C to +85°C		–40°C to +125°C	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX
V_{OH}	$I_{OH} = -100\ \mu A$	1.65 V to 3.6 V	$V_{CC} - 0.2$			$V_{CC} - 0.2$		$V_{CC} - 0.3$	
	$I_{OH} = -4\ mA$	1.65 V	1.29			1.2		1.05	
	$I_{OH} = -8\ mA$	2.3 V	1.9			1.7		1.55	
	$I_{OH} = -12\ mA$	2.7 V	2.2			2.2		2.05	
		3 V	2.4			2.4		2.25	
	$I_{OH} = -24\ mA$	3 V	2.3			2.2		2	
V_{OL}	$I_{OL} = 100\ \mu A$	1.65 V to 3.6 V	0.1			0.2		0.3	
	$I_{OL} = 4\ mA$	1.65 V	0.24			0.45		0.6	
	$I_{OL} = 8\ mA$	2.3 V	0.3			0.7		0.85	
	$I_{OL} = 12\ mA$	2.7 V	0.4			0.4		0.6	
	$I_{OL} = 24\ mA$	3 V	0.55			0.55		0.8	
I_I	$V_I = 5.5\ V$ or GND	3.6 V	± 1			± 5		± 20	
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	1			10		40	
ΔI_{CC}	One input at $V_{CC} - 0.6\ V$, Other inputs at V_{CC} or GND	2.7 V to 3.6 V	500			500		5000	
C_i	$V_I = V_{CC}$ or GND	3.3 V	5						

5.8 Switching Characteristics, SN54LVC00A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54LVC00A		UNIT
				–55°C to +125°C		
				MIN	MAX	
t _{pd}	A or B	Y	2.7 V	5.1		ns
			3.3 V ± 0.3 V	1	4.3	

5.9 Switching Characteristics, SN74LVC00A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

over recommended operating free air temperature range (unless otherwise noted) (see Load Check and Voltage Waveforms)												
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74LVC00A								UNIT
				T _A = 25°C			–40°C to +85°C		–40°C to +125°C			
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{pd}	A or B	Y	1.8 V ± 0.15 V	1	6	12	1	12.5	1	14	ns	
			2.5 V ± 0.2 V	1	4.6	5.9	1	6.4	1	7.9		
			2.7 V	1	4.3	4.9	1	5.1	1	6.5		
			3.3 V ± 0.3 V	1	3.5	4.1	1	4.3	1	5.5		
t _{sk(o)}			3.3 V ± 0.3 V					1		1.5	ns	

5.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	18	pF
			2.5 V	18	
			3.3 V	19	

5.11 Typical Characteristics

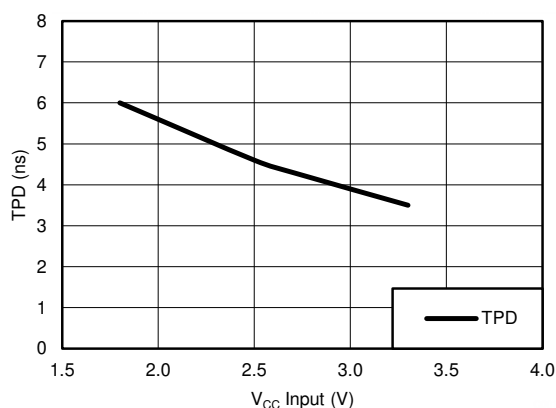
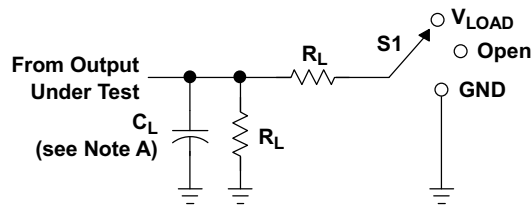


图 5-1. TPD vs V_{CC} (T_A = 25°C)

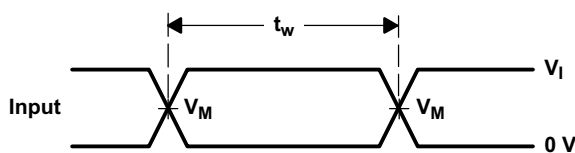
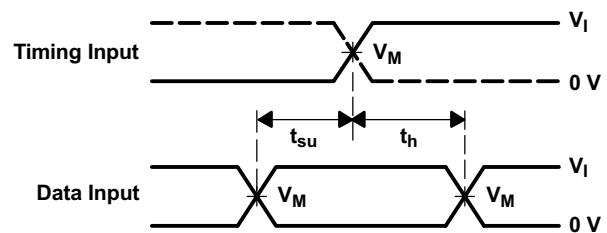
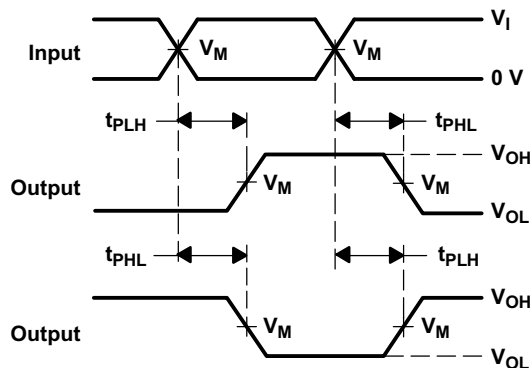
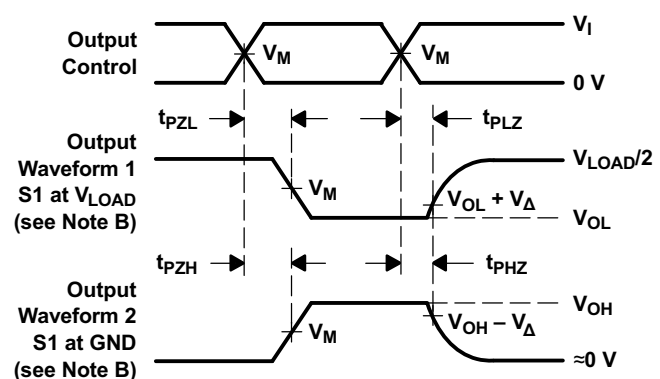
6 Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATIONVOLTAGE WAVEFORMS
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTSVOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The maximum sink and source current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.

7.2 Functional Block Diagram



图 7-1. Logic Diagram, Each Gate (Positive Logic)

7.3 Feature Description

7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [§ 5.1](#) must be followed at all times.

7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the [§ 5.6](#) and [§ 5.7](#). The worst case resistance is calculated with the maximum input voltage, given in the [§ 5.1](#), and the maximum input leakage current, given in the [§ 5.6](#) and [§ 5.7](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in [§ 5.3](#) and [§ 5.4](#) to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

7.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

小心

Voltages beyond the values specified in the [§ 5.1](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

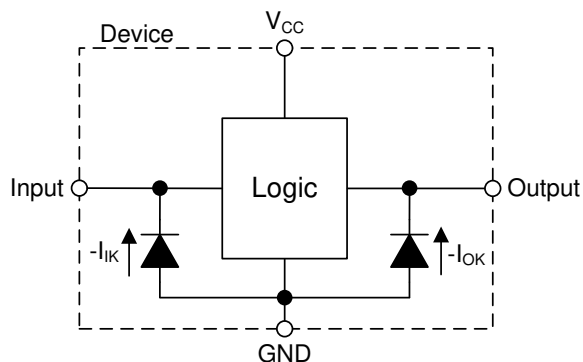


图 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [§ 5.1](#).

7.4 Device Functional Modes

[表 7-1](#) lists the functional modes of SN54LVC00A and SN74LVC00A.

**表 7-1. Function Table
(Each Gate)**

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

SN74LVC00A is a high-drive CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to allowing the device to perform mixed-voltage input down translation. For example the A input can be 3.3 V and the B input can be 5 V, while $V_{CC} = 2.5$ V and the device will operate properly to output a 2.5 V signal.

8.2 Typical Application

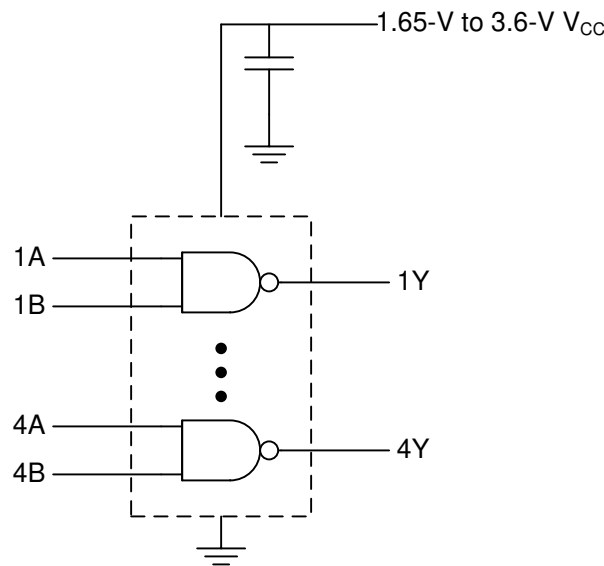


图 8-1. Typical NAND Gate Application and Supply Voltage

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input Conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [§ 5.4](#) table.
 - Specified high and low levels: See $(V_{IH}$ and $V_{IL})$ in the [§ 5.4](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommended Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above 5.5 V.

8.2.3 Application Curve

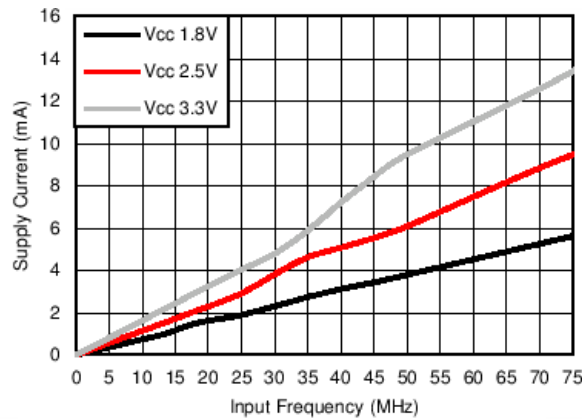


图 8-2. I_{CC} vs Frequency

Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [节 5.4](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.3 Layout

8.3.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [节 8.3.2](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

8.3.2 Layout Example

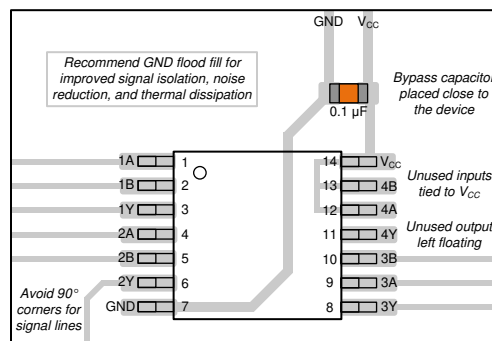


图 8-3. Layout Diagram for the SNx4LVC00A

9 Device and Documentation Support

9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC00A	Click here	Click here	Click here	Click here	Click here
SN74LVC00A	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

9.3.1 Community Resources

9.4 Trademarks

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9.5 静电放电警告



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9.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

10

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision T (May 2024) to Revision U (July 2024)	Page
• Updated RθJA values: D = 86 to 127.8, all values in °C/W.....	5
• Added <i>Typical Characteristics</i>	7

Changes from Revision S (March 2024) to Revision T (May 2024)	Page
• Updated RθJA values: DB = 96 to 140.4, NS = 76 to 123.8, PW = 113 to 150.8, RGY = 47 to 92.1; Updated DB, NS, PW, and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W.....	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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