

SNx4LVC08A 四通道双输入正与门

1 特性

- 门锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体放电模型 (A114-A)
 - 1000V 充电器件模型 (C101)
 - 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数的测试。
- SN74LVC08A 的工作电压范围为 1.65V 至 3.6V
- SN54LVC08A 的工作电压范围为 2.0V 至 3.6V
- SNx4LVC08A 的额定工作温度范围为 -40°C 至 $+85^{\circ}\text{C}$ 和 -40°C 至 $+125^{\circ}\text{C}$
- SN54LVC08A 的额定工作温度范围为 -55°C 至 $+125^{\circ}\text{C}$
- 输入电压高达 5.5V
- 电压为 3.3V 时， t_{pd} 最大值为 4.1ns
- V_{OLP} (输出接地反弹) 典型值 $<0.8\text{V}$ ($V_{\text{CC}} = 3.3\text{V}$ 、 $T_{\text{A}} = 25^{\circ}\text{C}$)
- V_{OHV} (输出 V_{OH} 下冲) 典型值 $>2\text{V}$ ($V_{\text{CC}} = 3.3\text{V}$ 、 $T_{\text{A}} = 25^{\circ}\text{C}$)

2 应用

- 服务器
- LED 显示屏
- 网络交换机
- I/O 扩展器
- 基站处理器板

3 说明

SN54LVC08A 四通道双输入正与门旨在 2.7V 至 3.6V V_{CC} 下运行，SN74LVC08A 四通道双输入正与门旨在 1.65V 至 3.6V V_{CC} 下运行。

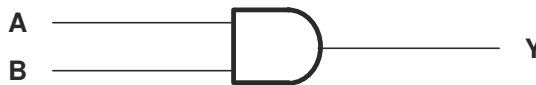
SNx4LVC08A 器件以正逻辑执行布尔函数 $Y = A \cdot B$ or $Y = \overline{A + B}$ 。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V/5V 的混合系统环境中将此类器件用作转换器。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SNx4LVC08A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.91mm
	DB (SSOP, 14)	6.2mm × 7.8mm	6.20mm × 5.30mm
	NS (SOP, 14)	10.2mm × 7.8mm	10.30mm × 5.30mm
	PW (TSSOP, 14)	5mm × 4.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.5mm × 3.5mm	3.50mm × 3.50mm
	FK (LCCC, 20)	8.9mm × 8.9mm	8.89mm × 8.89mm
	J (CDIP, 14)	19.55mm × 7.9mm	19.55mm × 6.7mm
	W (CFP, 14)	9.21mm × 9mm	9.21mm × 6.28mm

- (1) 如需了解更多信息，请参阅第 11 节。
- (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
- (3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



逻辑图，每个逻辑门
(正逻辑)



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表 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC, SSOP, SOP, CDIP, TSSOP, VQFN,WQFN	LCCC		
1A	1	2	I	Channel 1 input A
1B	2	3	I	Channel 1 input B
1Y	3	4	O	Channel 1 output
2A	4	6	I	Channel 2 input A
2B	5	8	I	Channel 2 input B
2Y	6	9	O	Channel 2 output
GND	7	10	Ground	Ground
3Y	8	12	O	Channel 3 output
3A	9	13	I	Channel 3 input A
3B	10	14	I	Channel 3 input B
4Y	11	16	O	Channel 4 output
4A	12	18	I	Channel 4 input A
4B	13	19	I	Channel 4 input B
V _{CC}	14	20	Power	Positive supply
Thermal Information ⁽¹⁾			—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.
NC ⁽²⁾	—	1	—	No connect
		5		
		7		
		11		
		15		
		17		

(1) For BQA package only.

(2) NC – No internal connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	6.5	V
V _I	Input voltage ⁽²⁾		−0.5	6.5	V
V _O	Output voltage ^{(2) (3)}		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		−50	mA
I _{OK}	Output clamp current	V _O < 0		−50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
P _{tot}	Power dissipation ^{(4) (5)}	T _A = −40°C to +125°C		500	mW
T _J	Junction temperature		−65	150	°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.
- (4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (5) For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
		Machine Model (MM) A115-A	200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions, SN54LVC08A

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54LVC08A		UNIT
			−55°C to +125°C		
			MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 2.7V to 3.6V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7V to 3.6V		0.8	V
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7V		−12	mA
		V _{CC} = 3V		−24	
I _{OL}	Low-level output current	V _{CC} = 2.7V		12	mA
		V _{CC} = 3V		24	
Δt/Δv	Input transition rise or fall rate			8	ns/V

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.4 Recommended Operating Conditions, SN74LVC08A

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN74LVC08A						UNIT
			T _A = 25°C		–40°C to +85°C		–40°C to +125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65V to 1.95V	0.65 × V _{CC}		0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3V to 2.7V	1.7		1.7		1.7		
		V _{CC} = 2.7V to 3.6V	2		2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65V to 1.95V	0.35 × V _{CC}		0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3V to 2.7V	0.7		0.7		0.7		
		V _{CC} = 2.7V to 3.6V	0.8		0.8		0.8		
V _I	Input voltage		0	5.5	0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65V	–4		–4		–4		mA
		V _{CC} = 2.3V	–8		–8		–8		
		V _{CC} = 2.7 V	–12		–12		–12		
		V _{CC} = 3V	–24		–24		–24		
I _{OL}	Low-level output current	V _{CC} = 1.65V	4		4		4		mA
		V _{CC} = 2.3V	8		8		8		
		V _{CC} = 2.7V	12		12		12		
		V _{CC} = 3V	24		24		24		
Δt/Δv	Input transition rise or fall rate		8		8		8		ns/V

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC08A						UNIT
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	RGY (LCCC)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	102.3	127.8	140.4	123.8	150.8	92.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	96.8	81.9	65.3	52.7	56.0	56.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	70.9	84.4	60.2	53.9	69.5	27.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	16.6	39.6	25.3	17.9	8.9	4.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	70.9	83.9	59.6	53.6	68.9	27.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	50.1	N/A	N/A	N/A	N/A	19.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics, SN54LVC08A

over recommended operating free-air temperature range (unless otherwise noted)

SN54LVC08A						UNIT
PARAMETER	TEST CONDITIONS	V _{CC}	–55°C to +125°C			
			MIN	TYP ⁽¹⁾	MAX	
V _{OH}	I _{OH} = –100 μA	2.7V to 3.6V	V _{CC} – 0.2			V
	I _{OH} = –12 mA	2.7V	2.2			
		3V	2.4			
		I _{OH} = –24 mA	3V	2.2		
V _{OL}	I _{OL} = 100 μA	2.7V to 3.6V	0.2			V
	I _{OL} = 12 mA	2.7V	0.4			
	I _{OL} = 24 mA	3V	0.55			
I _I	V _I = 5.5 V or GND	3.6V	±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6V	10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7V to 3.6V	500			μA
C _i	V _I = V _{CC} or GND	3.3V	5			pF

(1) T_A = 25°C

5.7 Electrical Characteristics, SN74LVC08A

over recommended operating free-air temperature range (unless otherwise noted)

Not recommended for use at temperature range (unless otherwise noted)										
PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC08A						UNIT	
			T _A = 25°C			–40°C to +85°C		–40°C to +125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V _{OH}	I _{OH} = –100 μA	1.65V to 3.6V	V _{CC} – 0.2			V _{CC} – 0.2		V _{CC} – 0.3		V
	I _{OH} = –4 mA	1.65V	1.29			1.2		1.05		
	I _{OH} = –8 mA	2.3V	1.9			1.7		1.55		
	I _{OH} = –12 mA	2.7V	2.2			2.2		2.05		
		3V	2.4			2.4		2.25		
	I _{OH} = –24 mA	3V	2.3			2.2		2		
V _{OL}	I _{OL} = 100 μA	1.65V to 3.6V	0.1			0.2		0.3		V
	I _{OL} = 4 mA	1.65V	0.24			0.45		0.6		
	I _{OL} = 8 mA	2.3V	0.3			0.7		0.75		
	I _{OL} = 12 mA	2.7V	0.4			0.4		0.6		
	I _{OL} = 24 mA	3V	0.55			0.55		0.8		
I _I	V _I = 5.5 V or GND	3.6V	±1			±5		±20		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6V	1			10		40		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7V to 3.6V	500			500		5000		μA
C _i	V _I = V _{CC} or GND	3.3V	5							pF

5.8 Switching Characteristics, SN54LVC08A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

For recommended operating conditions (unless otherwise noted) (see Logic State and Voltage Definitions)					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54LVC08A	UNIT
				–55°C to +125°C	
				MIN MAX	
t _{pd}	A or B	Y	2.7V	4.8	ns
			3.3V ± 0.3V	1 4.1	

5.9 Switching Characteristics, SN74LVC08A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

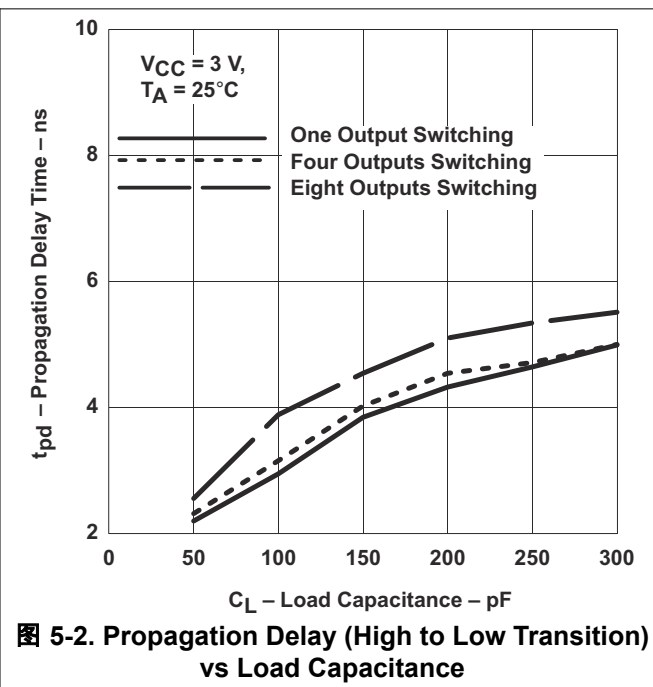
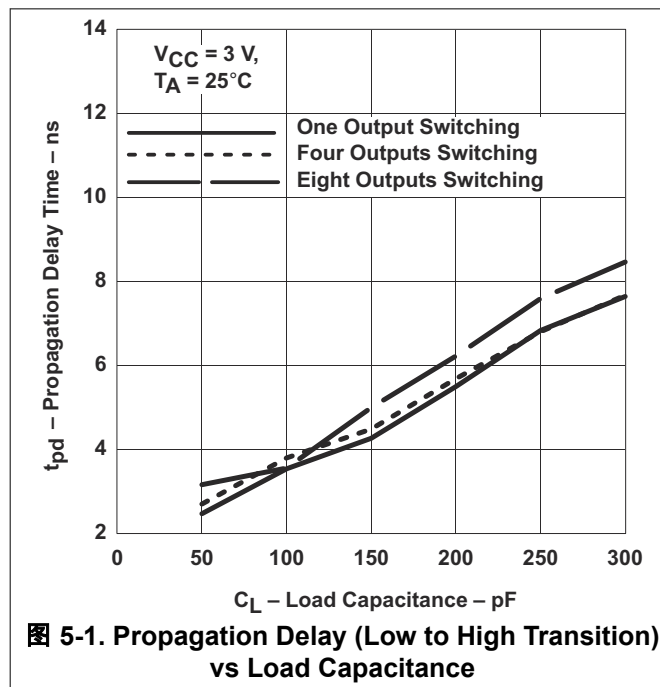
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74LVC08A								UNIT
				T _A = 25°C			–40°C to +85°C		–40°C to +125°C			
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{pd}	A or B	Y	1.8V ± 0.15V	1	5	9.3	1	9.8	1	11.3	ns	
			2.5V ± 0.2V	1	2.9	6.4	1	6.9	1	9		
			2.7V	1	3	4.6	1	4.8	1	6		
			3.3V ± 0.3V	1	2.6	3.9	1	4.1	1	5.5		
t _{sk(o)}			3.3V ± 0.3V				1		1.5	ns		

5.10 Operating Characteristics

T_A = 25°C

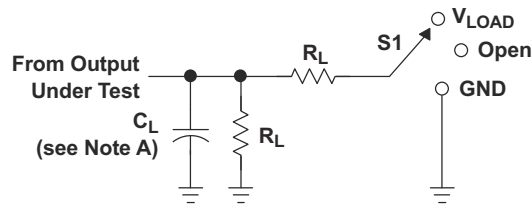
PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	7	pF
			2.5 V	9.8	
			3.3 V	10	

5.11 Typical Characteristics



6 Parameter Measurement Information

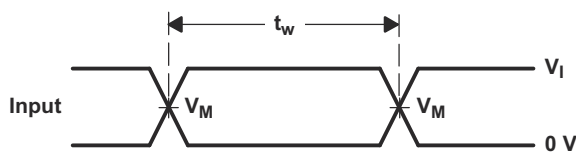
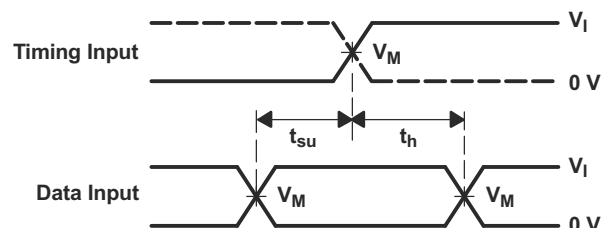
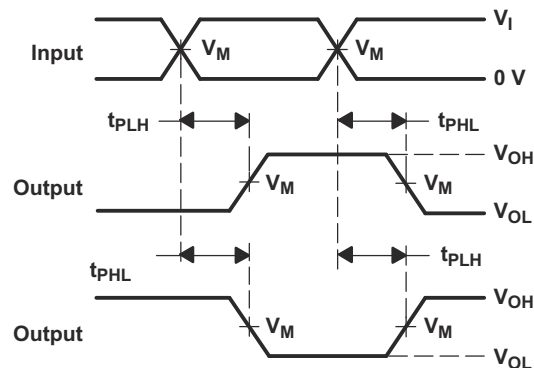
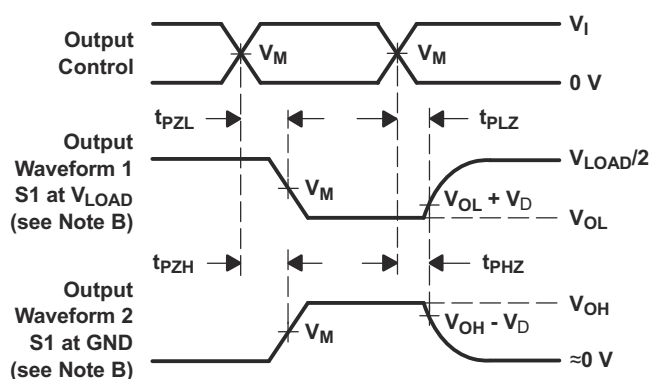
Load Circuit and Voltage Waveforms



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATIONVOLTAGE WAVEFORMS
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTSVOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ W}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

7 Detailed Description

7.1 Overview

The SN74LVC08 device contains four 2-input positive AND gate device and performs the Boolean function $Y = A \times B$. This device is useful when multiple AND function is used in the system.

7.2 Functional Block Diagram

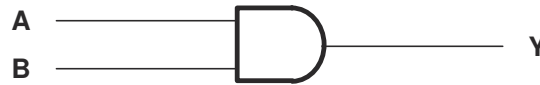


图 7-1. Logic Diagram, Each Gate (Positive Logic)

7.3 Feature Description

7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the 节 5.1 must be followed at all times.

7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the 节 5.6 and 节 5.7. The worst case resistance is calculated with the maximum input voltage, given in the 节 5.1, and the maximum input leakage current, given in the 节 5.6 and 节 5.7, using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in 节 5.3 and 节 5.4 to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

7.3.3 Clamp Diodes

The inputs to this device have negative clamping diodes. The outputs to this device have both positive and negative clamping diodes as shown in 图 7-2.

小心

Voltages beyond the values specified in the 节 5.1 table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

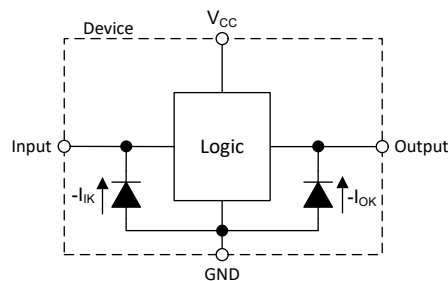


图 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [§ 5.1](#).

7.4 Device Functional Modes

[表 7-1](#) lists the functional modes for the SN54LVC08A and SN74LVC08A devices.

表 7-1. Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN74LVC08A is used to drive CMOS device and used for implementing AND logic. The LVC family can support current drive of about 24 mA at 3-V V_{CC} . The inputs for SN74LVC08A are 5.5-V tolerant allowing it to translate down to V_{CC} .

8.2 Typical Application

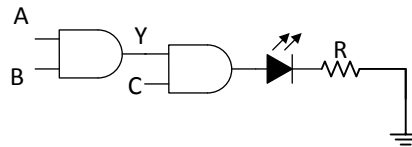


图 8-1. Three Input AND Gate Implementation and Driving LED

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

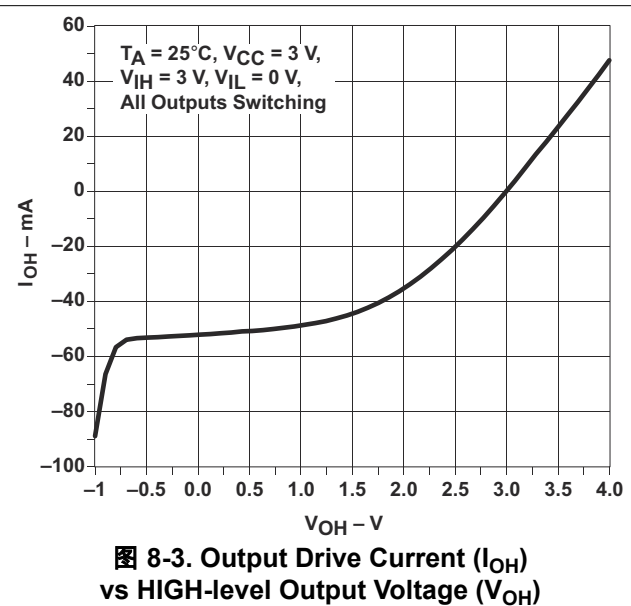
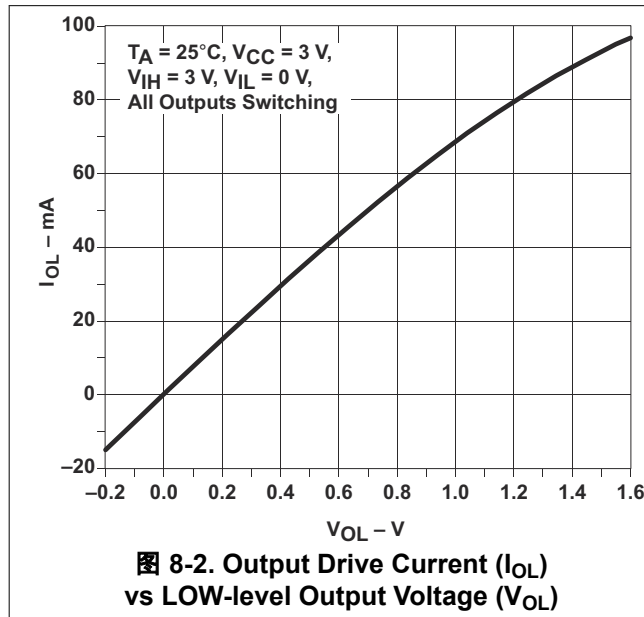
8.2.2 Detailed Design Procedure

SN74LVC08A contains four AND gates in one package which can be used for individual AND function or to implement complex Boolean logic. 图 8-1 shows an example of implementing 3input AND function. AB are inputs for AND gate which are connected to another AND gate. $Z = A \times B \times C$. SN74LVC08A support high drive current of 24 mA which can be used to drive LEDs of even Drive low current signal FETs, an example is shown in 图 8-1 TI recommends to use a series resistance to limit the current. If V_{CC} is 3 V, and LED current should be 10 mA, and the forward-voltage of LED is 2.5 V, then R as shown in 图 8-1 is calculated using 方程式 1:

$$R = (V_{CC} - V_{LED}) / I \quad (1)$$

$$R = (3 - 2.5) / 0.01 = 50 \, \Omega$$

8.2.3 Application Curves



Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

The V_{CC} pin must have a good bypass capacitor to prevent power disturbance. TI recommends to use a 0.1- μ F capacitor. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.3 Layout

8.3.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [图 8-4](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient.

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [图 8-5](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.3.2 Layout Examples

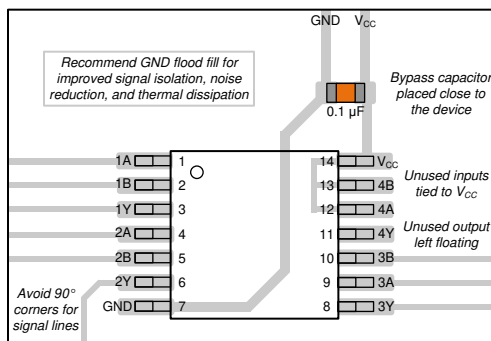


图 8-4. Example Layout

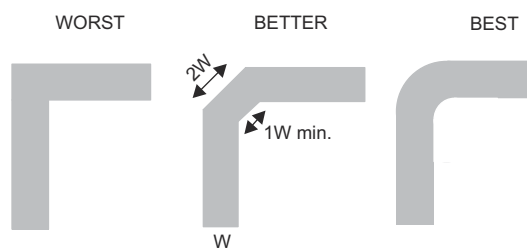


图 8-5. Trace Example

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

9.1.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC08A	Click here	Click here	Click here	Click here	Click here
SN74LVC08A	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 支持资源

TI E2E™ [中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.3.1 Community Resources

9.4 Trademarks

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9.5 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision V (May 2024) to Revision W (July 2024)

Page

- Updated thermal values for D package from RθJA = 98.6 to 127.8, RθJC(top) = 56.0 to 81.9, RθJB = 53.3 to 84.4, ΨJT = 16.4 to 39.6, ΨJB = 53.0 to 83.9, RθJC(bot) = N/A, all values in °C/W 6

Changes from Revision U (March 2024) to Revision V (May 2024)	Page
Updated RθJA values: DB = 112.8 to 140.4, PW = 127.7 to 150.8, RGY = 51.1 to 92.1, NS = 95.1 to 123.8; updated DB, PW, RGY, and NS packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in $^{\circ}$C/W.....	6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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