

SNx4AHC126 具有三态输出的四路总线缓冲门

1 特性

- 工作范围为 2V 至 5.5V V_{CC}
- 低延迟, 3.8ns (5V 电源时的典型值)
- 闩锁性能超过 250mA , 符合 JESD 17 规范

2 应用

- 驱动指示灯 LED
- 使用逻辑电路驱动传输线
- 启用或禁用数字信号

3 说明

SNx4AHC126 器件是四路总线缓冲门, 采用具有三态输出的独立线路驱动器。

要在上电或断电期间处于高阻态, 可以将 OE 通过下拉电阻连接至 GND; 该电阻的最小值取决于驱动器的拉电流能力。

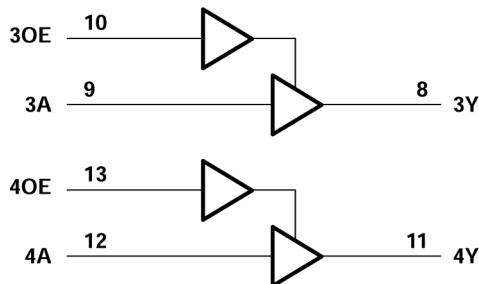
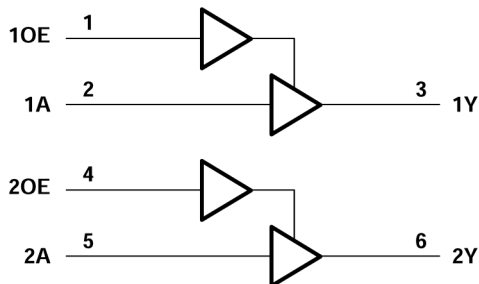
封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	封装尺寸 ⁽³⁾
SNx4AHC126	BQA (WQFN , 14)	3mm × 2.5mm	3mm × 2.5mm
	PW (TSSOP , 14)	5mm × 6.4mm	5mm × 4.4mm

(1) 更多相关信息, 请参阅第 10 节。

(2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。

(3) 封装尺寸 (长 × 宽) 为标称值, 不包括引脚。



逻辑图 (正逻辑)



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4 引脚配置和功能

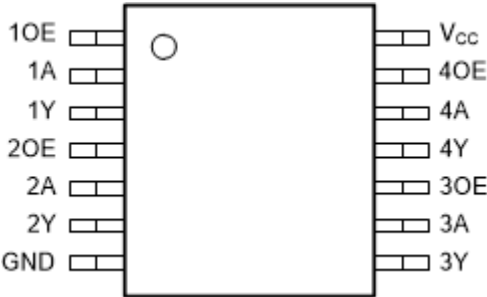


图 4-1. PW 封装，14 引脚（顶视图）

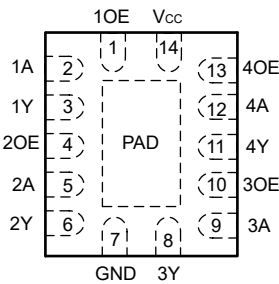


图 4-2. BQA 封装，WQFN 14 引脚（透明顶视图）

表 4-1. 引脚功能

引脚		类型 ⁽¹⁾	说明
名称	编号		
10E	1	I	通道 1，输出使能
1A	2	I	通道 1，A 输入
1Y	3	O	通道 1，Y 输出
2OE	4	I	通道 2，输出使能
2A	5	I	通道 2，A 输入
2Y	6	O	通道 2，Y 输出
GND	7	G	地
3Y	8	O	通道 3，Y 输出
3A	9	I	通道 3，A 输入
3OE	10	I	通道 3，OE 输入
4Y	11	O	通道 4，Y 输出
4A	12	I	通道 4，A 输入
4OE	13	I	通道 4，OE 输入
V _{CC}	14	P	正电源
散热焊盘 ⁽²⁾		—	散热焊盘；连接至 GND 或保持悬空

(1) I = 输入，O = 输出，P = 电源，G = 接地

(2) 仅限 BQA 封装

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得 (除非另有说明) ⁽¹⁾

		最小值	最大值	单位
V_{CC}	电源电压范围	-0.5	7	V
V_I ⁽²⁾	输入电压范围	-0.5	7	V
V_O ⁽²⁾	输出电压范围	-0.5	$V_{CC}+0.5$	V
I_{IK}	输入钳位电流	$(V_I < 0)$		-20 mA
I_{OK}	输出钳位电流	$(V_O < 0 \text{ 或 } V_O > V_{CC})$		± 20 mA
I_O	持续输出电流	$(V_O = 0 \text{ 至 } V_{CC})$		± 25 mA
	通过 V_{CC} 或 GND 的持续电流		± 50	mA
T_{stg}	贮存温度范围	-65	150	°C

- (1) 超出绝对最大额定值运行可能会对器件造成损坏。绝对最大额定值并不表示器件在这些条件下或在建议运行条件以外的任何其他条件下能够正常运行。如果在建议运行条件之外但又在绝对最大额定值范围内使用，器件可能不会完全正常运行，这可能会影响器件的可靠性、功能性和性能，并缩短器件的寿命。
- (2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM), 符合 ANSI/ESDA/JEDEC JS-001 标准 ⁽¹⁾	± 2000	V
		充电器件模型 (CDM), 符合 ANSI/ESDA/JEDEC JS-002 标准 ⁽²⁾	± 1000	

- (1) JEDEC 文档 JEP155 指出：500V HBM 可实现在标准 ESD 控制流程下安全生产。
- (2) JEDEC 文件 JEP157 指出：250V CDM 可实现在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

			最小值	最大值	单位
V_{CC}	电源电压		2	5.5	V
V_{IH}	高电平输入电压	$V_{CC} = 2V$	1.5		V
		$V_{CC} = 3V$	2.1		
		$V_{CC} = 5.5V$	3.85		
V_{IL}	低电平输入电压	$V_{CC} = 2V$		0.5	V
		$V_{CC} = 3V$		0.9	
		$V_{CC} = 5.5V$		1.65	
$V_I^{(1)}$	输入电压		0	5.5	V
V_O	输出电压		0	V_{CC}	V
$I_{OH}^{(2)}$	高电平输出电流	$V_{CC} = 2V$		-50	μA
		$V_{CC}=3.3V\pm0.3V$		-4	mA
		$V_{CC}=5V\pm0.5V$		-8	
$I_{OL}^{(2)}$	低电平输出电流	$V_{CC} = 2V$		50	μA
		$V_{CC}=3.3V\pm0.3V$		4	mA
		$V_{CC}=5V\pm0.5V$		8	
$\Delta t/\Delta v$	输入转换上升或下降速率	$V_{CC}=3.3V\pm0.3V$		100	ns/V
		$V_{CC}=5V\pm0.5V$		20	
T_A	自然通风条件下的工作温度范围	SN74AHC126	-40	85	$^{\circ}C$
		SN54AHC126	-55	125	$^{\circ}C$

- (1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 **CMOS 输入缓慢变化或悬空的影响**，文献编号 SCBA004。
- (2) 提供的建议电流值用于根据相关输出电压规格 (V_{OL} 对应 I_{OL} ， V_{OH} 对应 I_{OH}) 保持适当的输出状态。有关详细信息，请参阅 **电气特性表**。

5.4 热性能信息

热指标 ⁽¹⁾		SN74AHC126						单位
		D	DB	DGV	N	NS	PW	
		14 引脚						
R _{θJA}	结至环境热阻	124.6					147.7	°C/W
R _{θJC(top)}	结至外壳（顶部）热阻	79.7					77.4	
R _{θJB}	结至电路板热阻	81.2					90.9	
ψ _{JT}	结至顶部特征参数	39.3					27.2	
ψ _{JB}	结至电路板特征参数	80.8					90.2	
R _{θJC(bot)}	结至外壳（底部）热阻	不适用	不适用	不适用	不适用	不适用	不适用	

- (1) 有关新旧热指标的更多信息，请参阅 **IC 封装热指标** 应用报告 **SPRA953**。

5.5 电气特性

在推荐的自然通风条件下的工作温度范围内测得 (除非另外注明)

参数	测试条件	V _{CC}	T _A =25°C			-40°C 至 +85°C		-55 至 125° C		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V _{OH}	I _{OH} =-50 μA	2V	1.9	2		1.9		1.9		V
		3V	2.9	3		2.9		2.9		
		4.5V	4.4	4.5		4.4		4.4		
	I _{OH} =-4mA	3V	2.58			2.48		2.48		
	I _{OH} = -8mA	4.5V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2V			0.1		0.1		0.1	V
		3V			0.1		0.1		0.1	
		4.5V			0.1		0.1		0.1	
	I _{OL} =4mA	3V			0.36		0.44		0.5	
	I _{OL} = 8mA	4.5V			0.36		0.44		0.5	
I _I	V _I =5.5V 或 GND	0V 至 5.5V			±0.1		±1		±1 ⁽¹⁾	μA
I _{OZ}	V _I =V _{CC} 或 GND	5.5V			±0.25				±2.5	μA
I _{CC}	V _I = V _{CC} 或 GND , I _O = 0	5.5V			4				40	μA
C _i	V _I =V _{CC} 或 GND	5V		4	10		10			pF

(1) 对于符合 MIL-PRF-38535 标准的产品, 此参数未经量产测试 (在 V_{CC} = 0V 时)。

5.6 开关特性, V_{CC} = 3.3V ± 0.3V

在推荐的自然通风条件下的工作温度范围内测得, V_{CC} = 3.3V ± 0.3V (除非另外注明) (请参阅节 6)

参数	从 (输入)	至 (输出)	负载电容	T _A = 25°C			-40°C 至 +85°C		-55 至 125° C		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t _{PLH}	A	Y	C _L = 15pF	5.6 ⁽¹⁾		8 ⁽¹⁾	1	9.5	1 ⁽¹⁾	9.5 ⁽¹⁾	ns
t _{PHL}				5.6 ⁽¹⁾		8 ⁽¹⁾	1	9.5	1 ⁽¹⁾	9.5 ⁽¹⁾	
t _{PZH}	OE	Y	C _L = 15pF	5.4 ⁽¹⁾		8 ⁽¹⁾	1	9.5	1 ⁽¹⁾	9.5 ⁽¹⁾	ns
t _{PZL}				5.4 ⁽¹⁾		8 ⁽¹⁾	1	9.5	1 ⁽¹⁾	9.5 ⁽¹⁾	
t _{PHZ}	OE	Y	C _L = 15pF	7 ⁽¹⁾		9.7 ⁽¹⁾	1	11.5	1 ⁽¹⁾	11.5 ⁽¹⁾	ns
t _{PLZ}				7 ⁽¹⁾		9.7 ⁽¹⁾	1	11.5	1 ⁽¹⁾	11.5 ⁽¹⁾	
t _{PLH}	A	Y	C _L = 50pF	8.1		11.5	1	13	1	13	ns
t _{PHL}				8.1		11.5	1	13	1	13	
t _{PZH}	OE	Y	C _L = 50pF	7.9		11.5	1	13	1	13	ns
t _{PZL}				7.9		11.5	1	13	1	13	
t _{PHZ}	OE	Y	C _L = 50pF	9.5		13.2	1	15	1	15	ns
t _{PLZ}				9.5		13.2	1	15	1	15	
t _{sk(o)}			C _L = 50pF			1.5 ⁽²⁾		1.5			ns

(1) (2)

5.7 开关特性, $V_{CC} = 5V \pm 0.5V$

在推荐的自然通风条件下的工作温度范围内测得, $V_{CC} = 5V \pm 0.5V$ (除非另外注明) (请参阅节 6)

参数	从 (输入)	至 (输出)	负载电容	$T_A = 25^\circ C$			$-40^\circ C$ 至 $+85^\circ C$		-55 至 $125^\circ C$		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	A	Y	$C_L = 15pF$	3.8 ⁽¹⁾	5.5 ⁽¹⁾		1	6.5	1 ⁽¹⁾	6.5 ⁽¹⁾	ns
t_{PHL}				3.8 ⁽¹⁾	5.5 ⁽¹⁾		1	6.5	1 ⁽¹⁾	6.5 ⁽¹⁾	
t_{PZH}	OE	Y	$C_L = 15pF$	3.6 ⁽¹⁾	5.1 ⁽¹⁾		1	6	1 ⁽¹⁾	6 ⁽¹⁾	ns
t_{PZL}				3.6 ⁽¹⁾	5.1 ⁽¹⁾		1	6	1 ⁽¹⁾	6 ⁽¹⁾	
t_{PHZ}	OE	Y	$C_L = 15pF$	4.6 ⁽¹⁾	6.8 ⁽¹⁾		1	8	1 ⁽¹⁾	8 ⁽¹⁾	ns
t_{PLZ}				4.6 ⁽¹⁾	6.8 ⁽¹⁾		1	8	1 ⁽¹⁾	8 ⁽¹⁾	
t_{PLH}	A	Y	$C_L = 50pF$	5.3	7.5		1	8.5	1	8.5	ns
t_{PHL}				5.3	7.5		1	8.5	1	8.5	
t_{PZH}	OE	Y	$C_L = 50pF$	5.1	7.1		1	8	1	8	ns
t_{PZL}				5.1	7.1		1	8	1	8	
t_{PHZ}	OE	Y	$C_L = 50pF$	6.1	8.8		1	10	1	10	ns
t_{PLZ}				6.1	8.8		1	10	1	10	
$t_{sk(o)}$			$C_L = 50pF$		1 ⁽²⁾			1			ns

(1) 对于符合 MIL-PRF-38535 标准的产品, 此参数未经量产测试。

(2) 对于符合 MIL-PRF-38535 标准的产品, 此参数不适用。

5.8 噪声特性

$V_{CC} = 5V$, $C_L = 50pF$, $T_A = 25^\circ C$ ⁽¹⁾

参数	最小值	典型值	最大值	单位
$V_{OL(P)}$ 安静输出, 最大动态 V_{OL}		0.2	0.8	V
$V_{OL(V)}$ 安静输出, 最小动态 V_{OL}	-0.9	-0.2		V
$V_{OH(V)}$ 安静输出, 最小动态 V_{OH}	4.4	4.7		V
$V_{IH(D)}$ 高电平动态输入电压	3.5			V
$V_{IL(D)}$ 低电平动态输入电压			1.5	V

(1) 特性仅适用于表面贴装封装。

5.9 工作特性

$V_{CC} = 5V$, $T_A = 25^\circ C$

参数	测试条件	典型值	单位
C_{pd} 功率耗散电容	无负载, $f = 1MHz$	14	pF

5.10 典型特性

$T_A = 25^\circ\text{C}$ (除非另有说明)

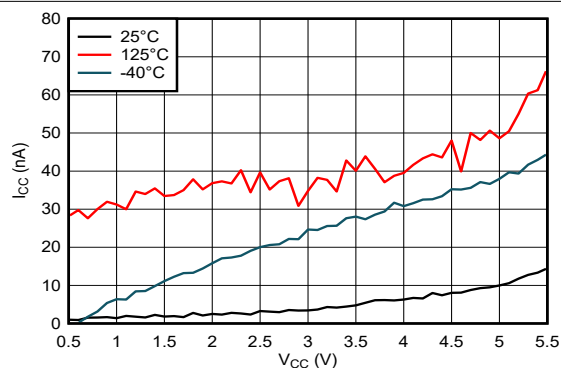


图 5-1. 电源电压两端的电源电流

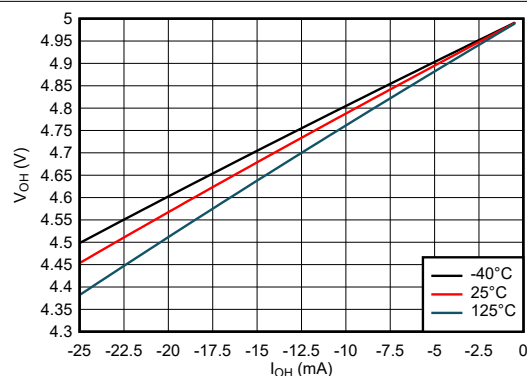


图 5-2. 高电平状态下输出电压与电流间的关系 (5V 电源)

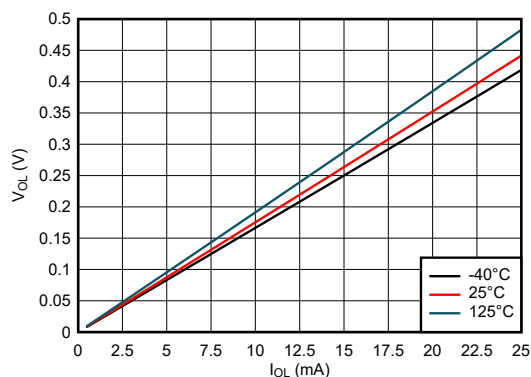


图 5-3. 低电平状态下输出电压与电流间的关系；5V 电源

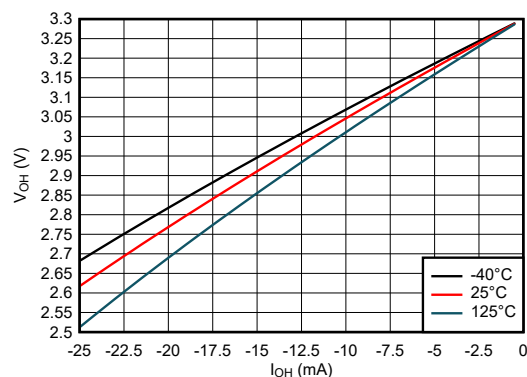


图 5-4. 高电平状态下输出电压与电流间的关系；3.3V 电源

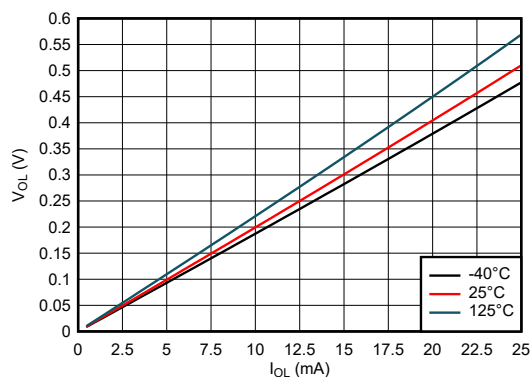


图 5-5. 低电平状态下输出电压与电流间的关系；3.3V 电源

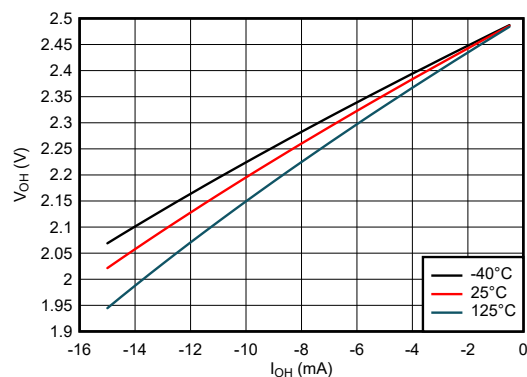


图 5-6. 高电平状态下输出电压与电流间的关系；2.5V 电源

5.10 典型特性 (续)

$T_A = 25^\circ\text{C}$ (除非另有说明)

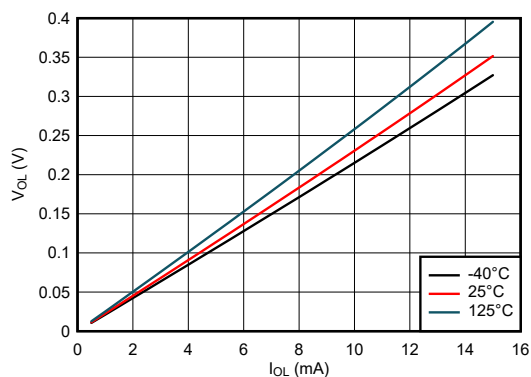


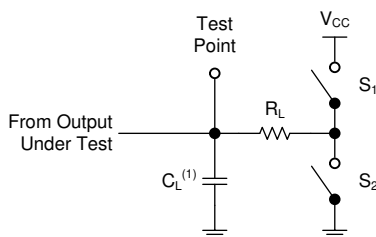
图 5-7. 低电平状态下输出电压与电流间的关系；2.5V 电源

6 参数测量信息

对于下表中列出的示例，波形之间的相位关系是任意选择的。所有输入脉冲均由具有以下特性的发生器提供：
 $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_f < 2.5\text{ns}$ 。

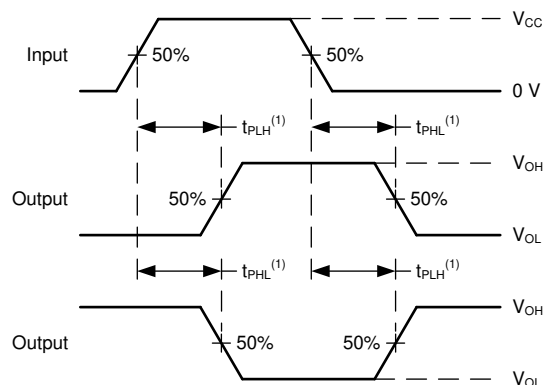
输出单独测量，每次测量一个输入转换。

测试	S1	S2	R_L	C_L	ΔV	V_{CC}
t_{PLH} , t_{PHL}	断开	断开	—	15pF、50pF	—	全部
t_{PLZ} , t_{PZL}	闭合	断开	1k Ω	15pF、50pF	0.15V	$\leq 2.5\text{V}$
t_{PHZ} , t_{PZH}	断开	闭合	1k Ω	15pF、50pF	0.15V	$\leq 2.5\text{V}$
t_{PLZ} , t_{PZL}	闭合	断开	1k Ω	15pF、50pF	0.3V	$> 2.5\text{V}$
t_{PHZ} , t_{PZH}	断开	闭合	1k Ω	15pF、50pF	0.3V	$> 2.5\text{V}$



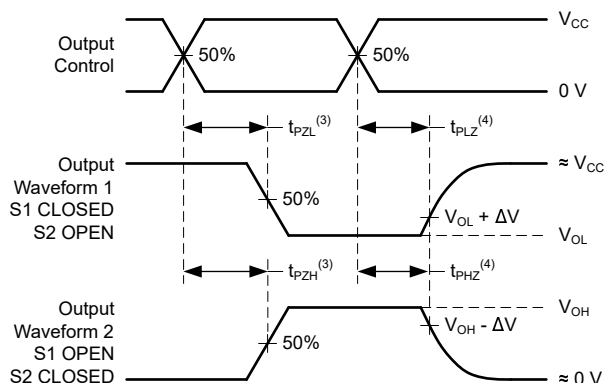
(1) C_L 包括探头和测试夹具电容。

图 6-1. 三态输出的负载电路



(1) t_{PLH} 和 t_{PHL} 之间的较大者与 t_{pd} 相同。

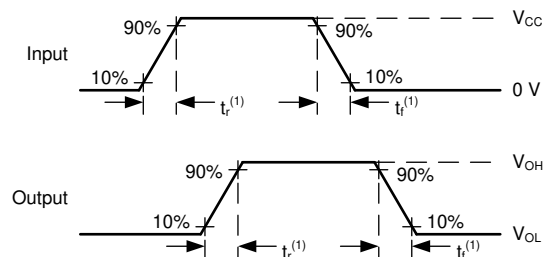
图 6-2. 电压波形传播延迟



(3) t_{PZL} 和 t_{PZH} 之间的较大者与 t_{en} 相同。

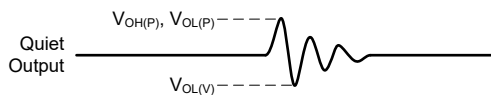
(4) t_{PLZ} 和 t_{PHZ} 之间的较大者与 t_{dis} 相同。

图 6-3. 电压波形传播延迟



(1) t_r 和 t_f 之间的较大值与 t_t 相同。

图 6-4. 电压波形，输入和输出转换时间



在所有其他输出同时切换时测得的噪声值。

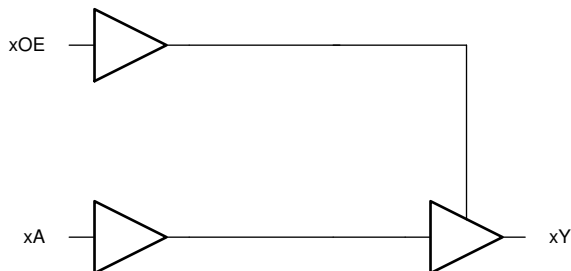
图 6-5. 电压波形和噪声

7 详细说明

7.1 概述

该器件包含四个具有三态输出的独立缓冲器。每个逻辑门以正逻辑执行布尔函数 $Y = A$ 。

7.2 功能方框图



四个通道之一

7.3 特性说明

7.3.1 平衡 CMOS 三态输出

此器件包含平衡 CMOS 三态输出。这些输出可以处于三种状态：高驱动、低驱动和高阻抗。术语 *平衡* 表示器件可以灌入和拉出相似的电流。此器件的驱动能力可能在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。此外，该器件的输出能够驱动的电流比此器件能够承受、不会损坏的电流更大。务必限制器件的输出功率，以避免因过电流而损坏器件。必须始终遵守 *绝对最大额定值* 中规定的电气和热限值。

当置于高阻态时，输出既不会拉出电流，也不会灌入电流，但 *电气特性* 表中定义的小漏电流除外。在高阻抗状态下，输出电压不受器件控制，而取决于外部因素。如果没有其他驱动器连接到该节点，则这称为悬空节点且电压未知。上拉或下拉电阻可以连接到输出端，以便当输出端处于高阻抗状态时在输出端提供已知电压。电阻值将取决于多种因素，包括寄生电容和功耗限制。通常，可以使用 10k Ω 电阻器来满足这些要求。

未使用的三态 CMOS 输出应保持断开状态。

7.3.2 标准 CMOS 输入

此器件包括标准 CMOS 输入。标准 CMOS 输入为高阻抗，通常建模为与输入电容并联的电阻器，如 *电气特性* 中所示。最坏情况下的电阻是根据 *绝对最大额定值* 中给出的最大输入电压和 *电气特性* 中给出的最大输入漏电流，使用欧姆定律 ($R = V \div I$) 计算得出的。

标准 CMOS 输入要求输入信号在有效逻辑状态之间快速转换，如 *建议运行条件* 表中的输入转换时间或速率所定义。不符合此规范将导致功耗过大并可能导致振荡。更多详细信息，请参阅 [CMOS 输入缓慢或悬空的影响](#)。

在运行期间，任何时候都不要让标准 CMOS 输入悬空。未使用的输入必须在 V_{CC} 或 GND 端接。如果系统不会一直主动驱动输入，则可以添加上拉或下拉电阻器，以在这些时间段提供有效的输入电压。电阻值将取决于多种因素；但建议使用 10k Ω 电阻器，这通常可以满足所有要求。

7.3.3 钳位二极管结构

该器件的输出同时具有正负钳位二极管，而该器件的输入只有负钳位二极管，如图 7-1 所示。

小心

电压超出 *绝对最大额定值* 表中规定的值可能会损坏器件。如果遵守输入和输出钳制电流额定值，输入和输出电压可超过额定值。

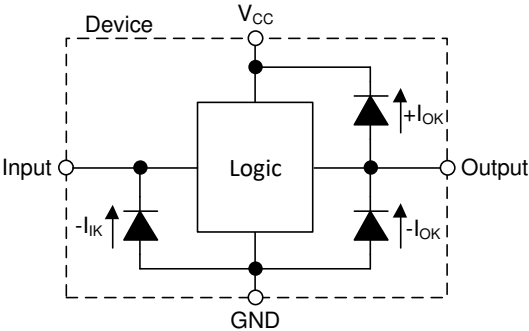


图 7-1. 每个输入和输出的钳位二极管的电气布置

7.4 器件功能模式

表 7-1. 功能表

输入		输出
OE	A	Y
L	X	Z
H	L	L
H	H	H

8 器件和文档支持

8.1 文档支持

8.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，[慢速或浮点 CMOS 输入的影响](#)

8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

8.4 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (August 2023) to Revision N (February 2024)	Page
---	------

- | | |
|---|---|
| • 添加了 D 封装的热性能值：R _{θJA} = 124.6，R _{θJC(top)} = 79.7，R _{θJB} = 81.2，Ψ _{JT} = 39.3，Ψ _{JB} = 80.8，R _{θJC(bot)} = N/A，所有值均以 °C/W 为单位..... | 5 |
|---|---|

Changes from Revision L (July 2003) to Revision M (August 2023)	Page
---	------

- | | |
|---|---|
| • 更改了整个文档中的表格、图和交叉参考的编号格式..... | 1 |
| • 向数据表添加了 <i>BQA</i> 封装..... | 1 |
| • 从数据表中删除了 <i>J</i> 、 <i>W</i> 、 <i>D</i> 、 <i>DB</i> 、 <i>DGV</i> 、 <i>N</i> 、 <i>NS</i> 和 <i>FK</i> 封装..... | 1 |

10 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686201Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9686201Q2A SNJ54AHC 126FK	Samples
5962-9686201QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201QD A SNJ54AHC126W	Samples
SN74AHC126BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC126	Samples
SN74AHC126DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC126	Samples
SN74AHC126N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC126N	Samples
SN74AHC126NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC126	Samples
SN74AHC126PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SNJ54AHC126FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9686201Q2A SNJ54AHC 126FK	Samples
SNJ54AHC126W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201QD A SNJ54AHC126W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC126, SN74AHC126 :

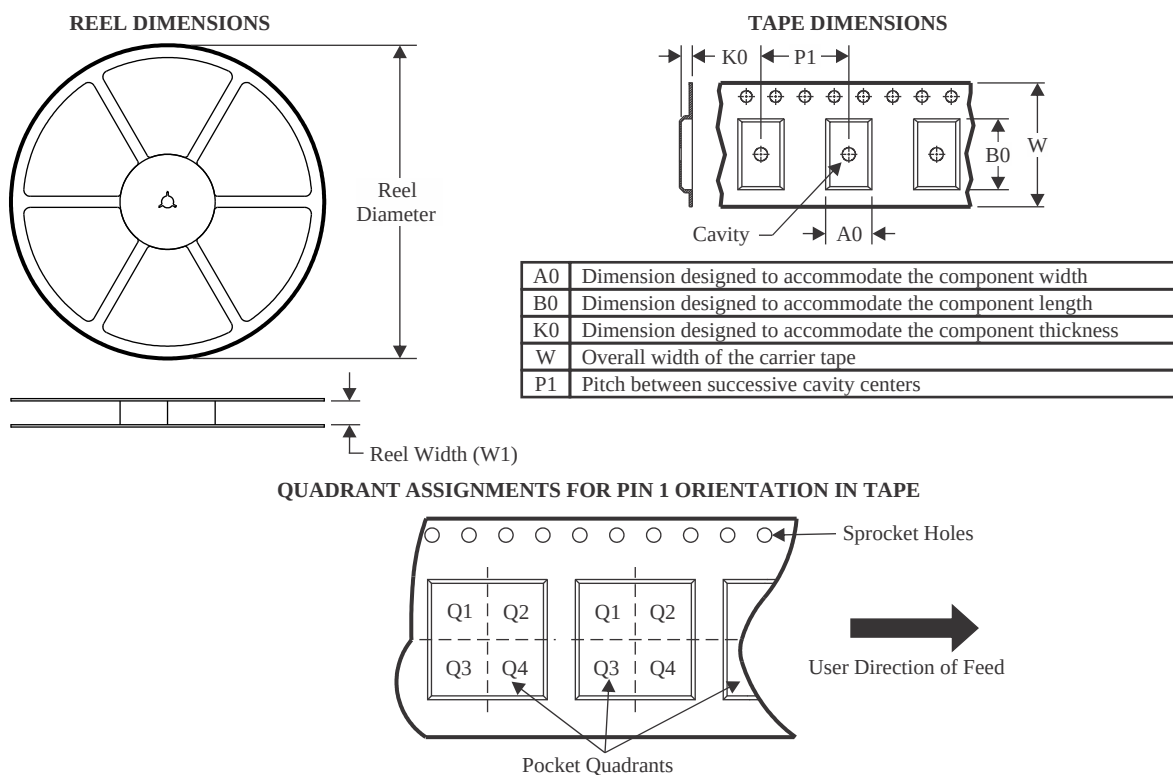
- Catalog : [SN74AHC126](#)
- Automotive : [SN74AHC126-Q1](#), [SN74AHC126-Q1](#)
- Military : [SN54AHC126](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

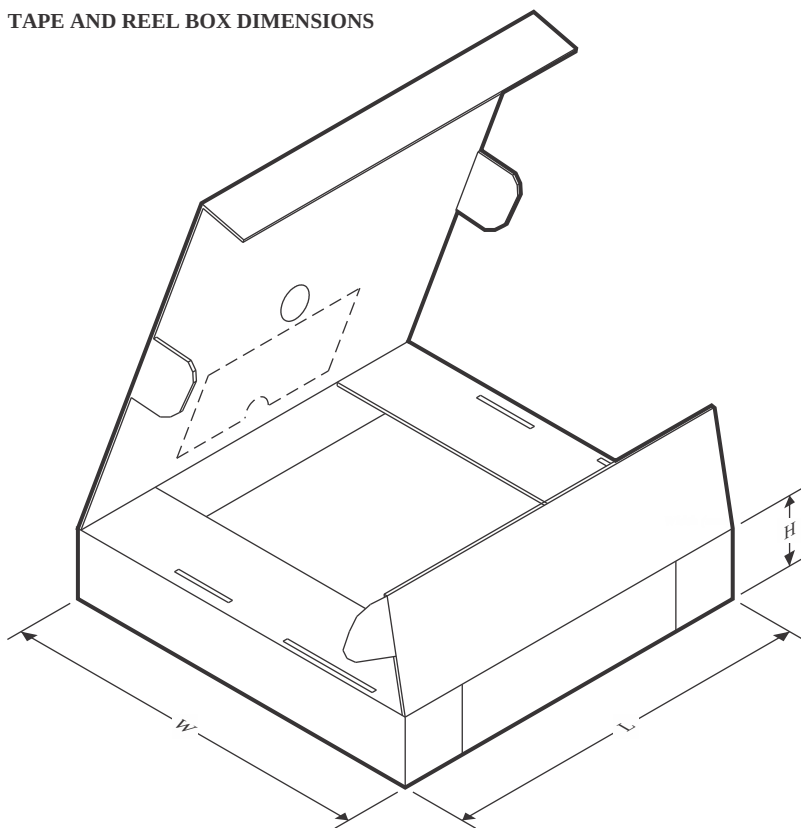
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC126BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC126DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC126DGV	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC126NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC126PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74AHC126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

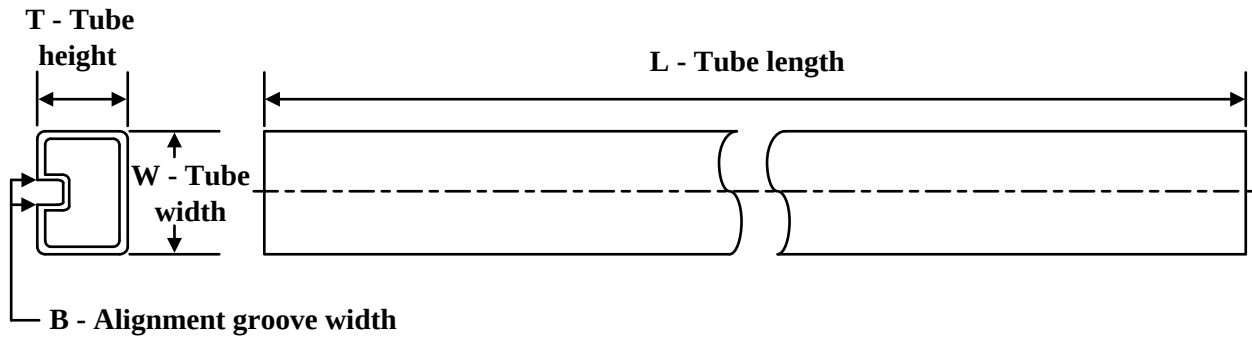
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC126BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC126DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC126DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC126DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHC126DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC126NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHC126PWR	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74AHC126PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC126PWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9686201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9686201QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHC126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC126N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC126FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC126W	W	CFP	14	25	506.98	26.16	6220	NA

GENERIC PACKAGE VIEW

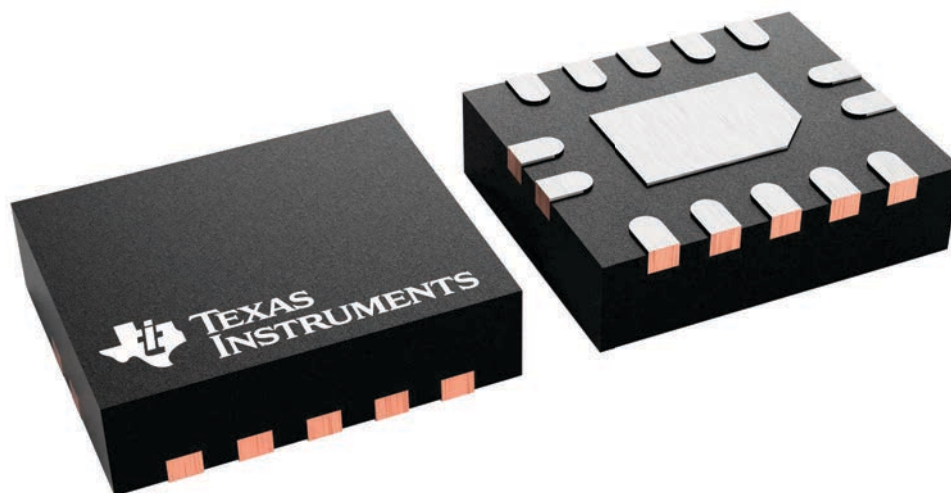
BQA 14

WQFN - 0.8 mm max height

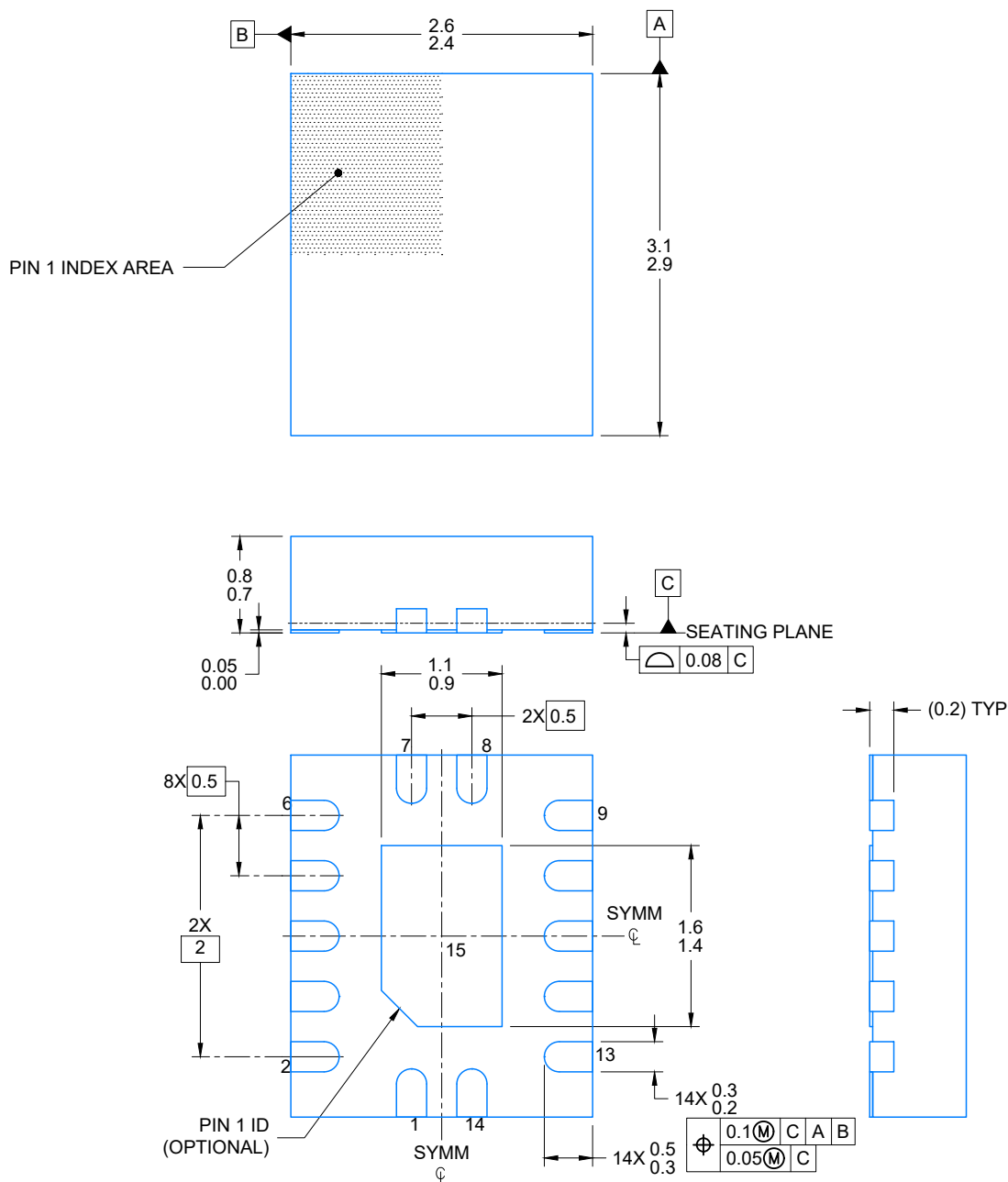
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



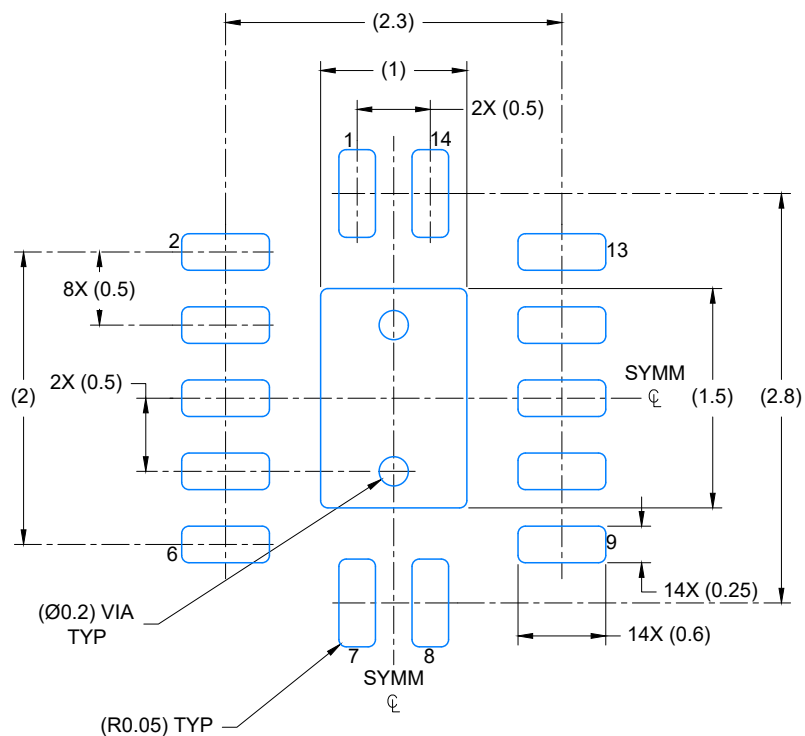
4227145/A



4224636/A 11/2018

NOTES:

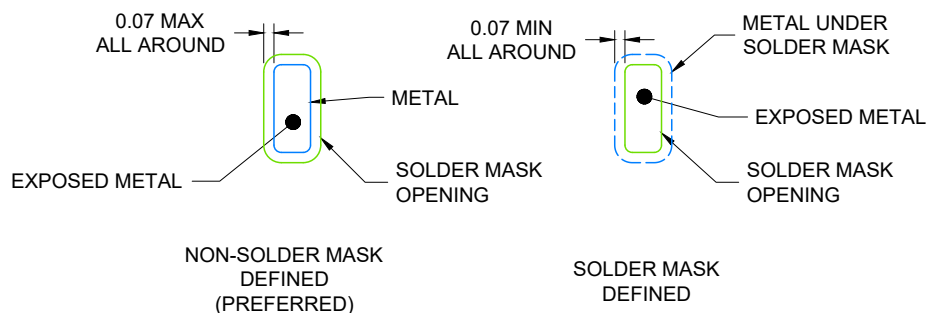
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

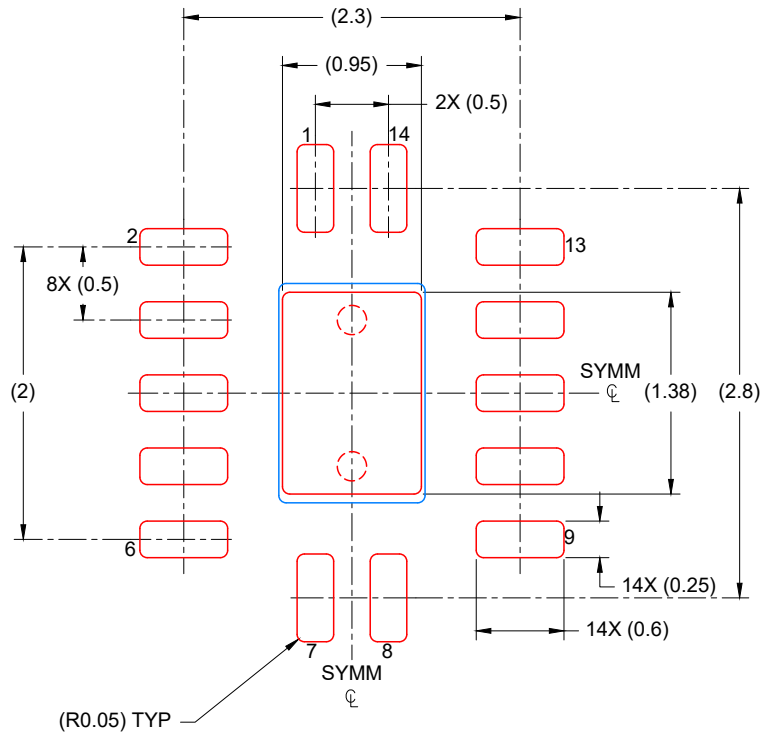
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

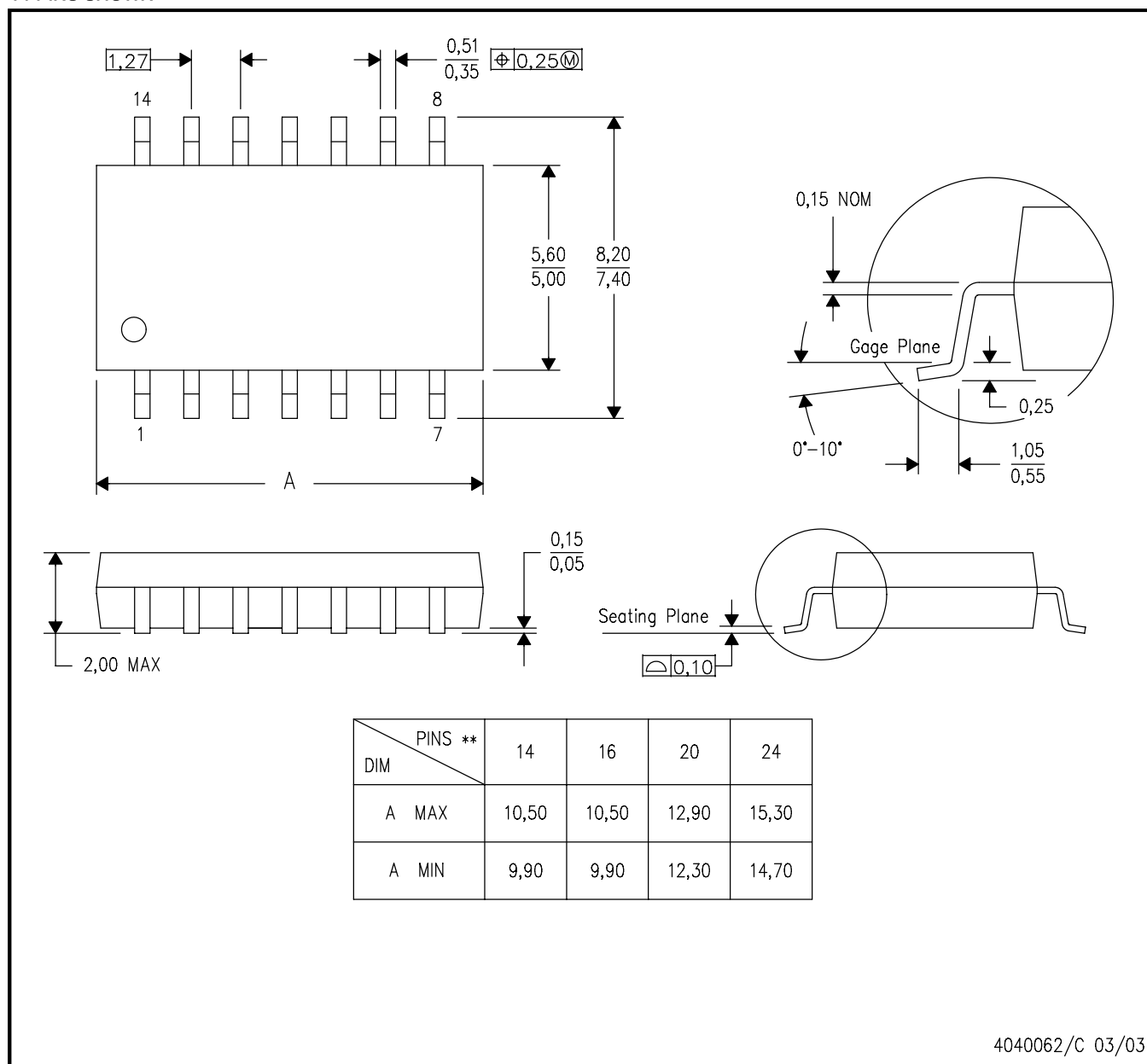
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

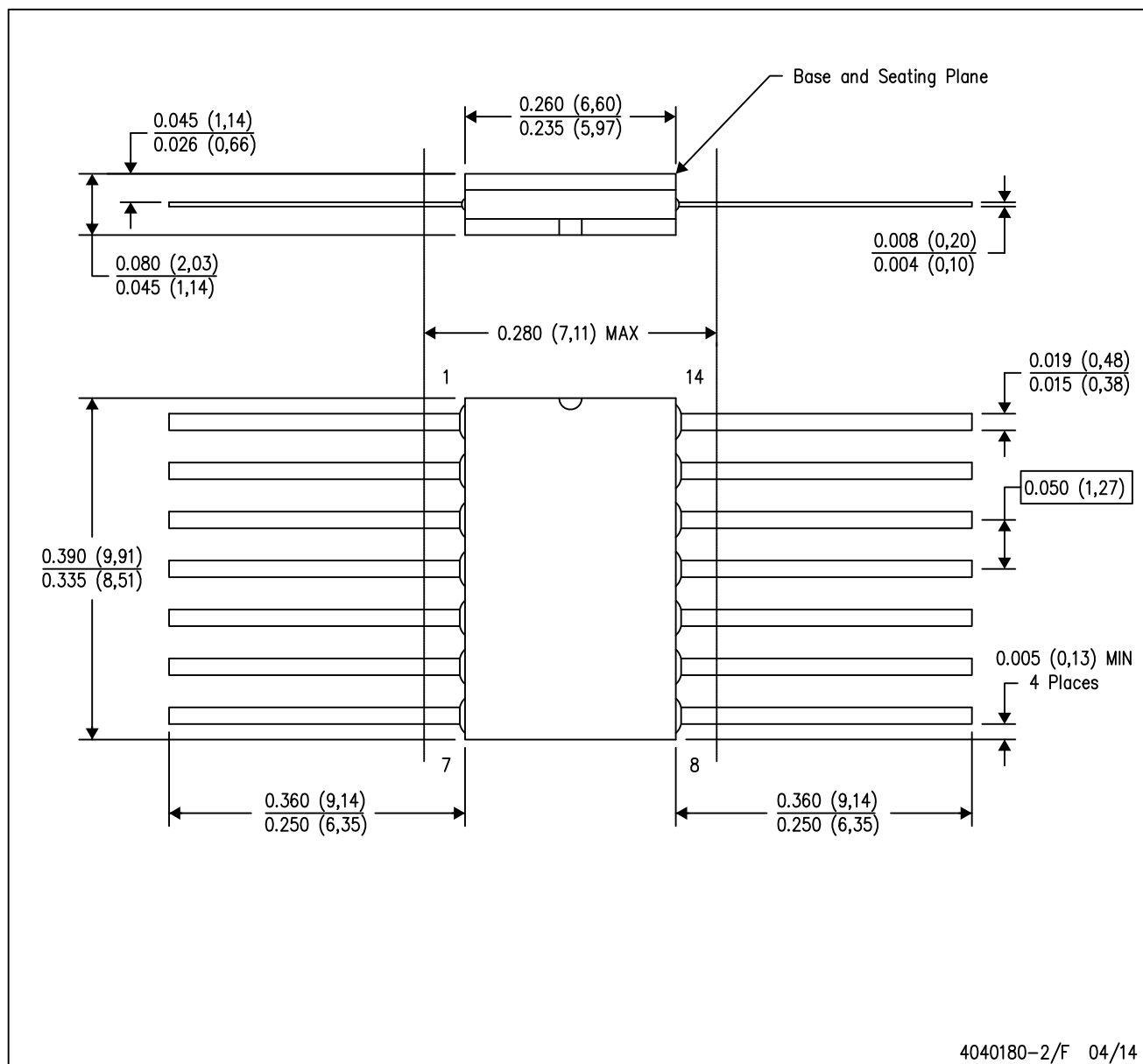
14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



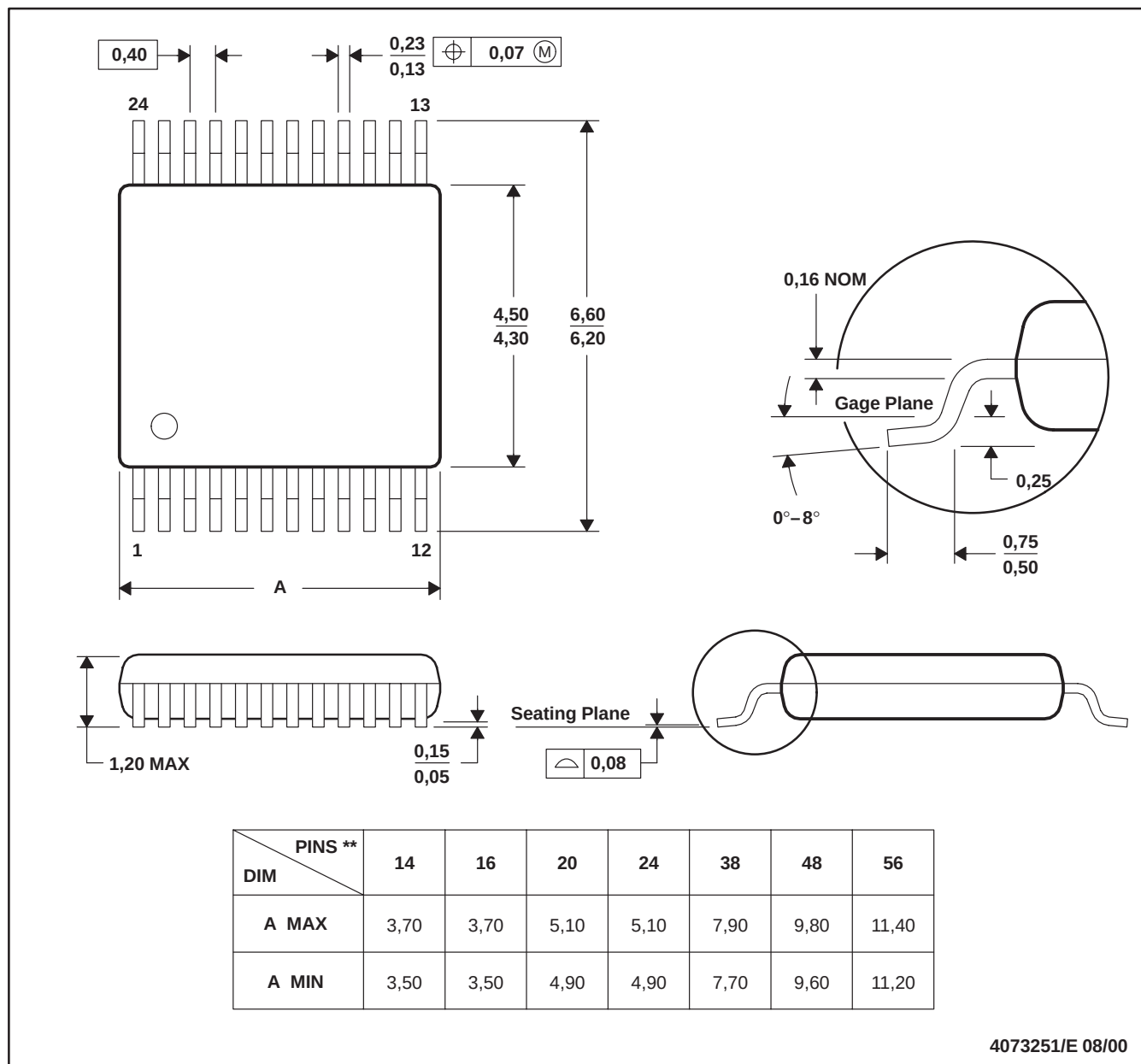
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL STD 1835 GDFP1-F14

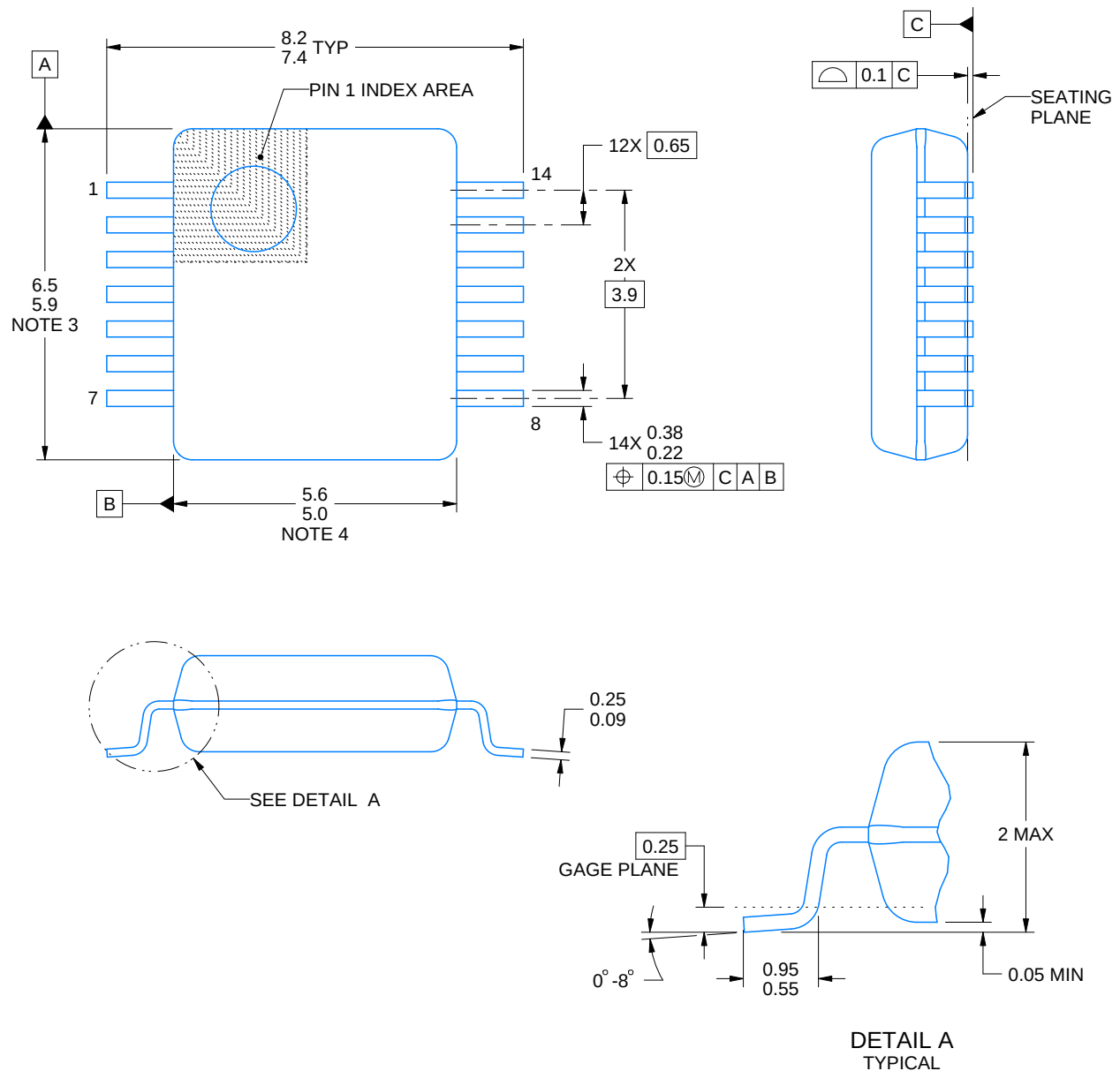
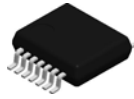
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4220762/A 05/2024

NOTES:

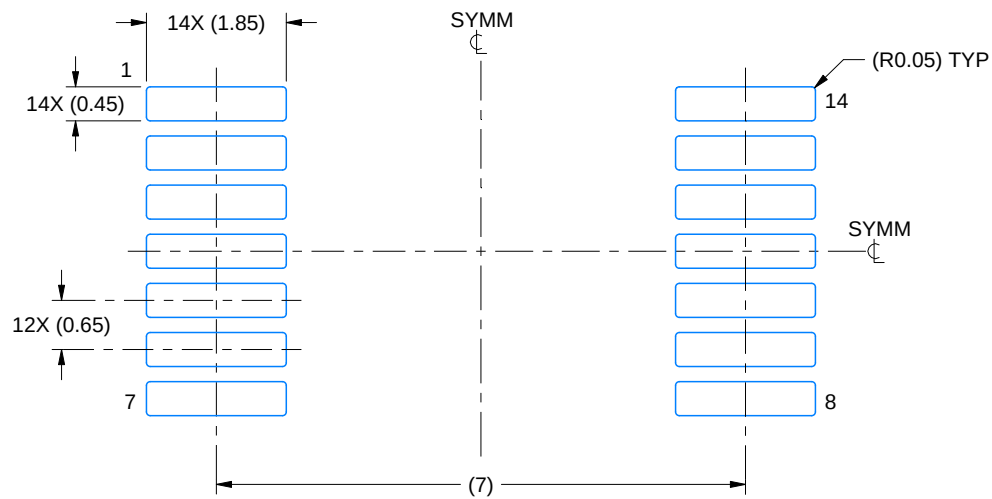
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

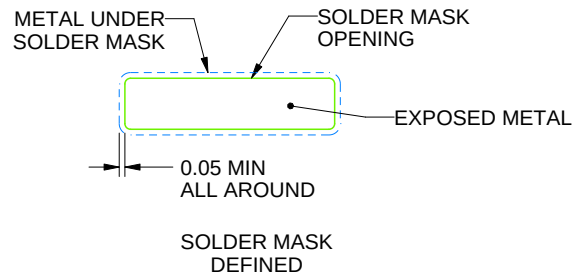
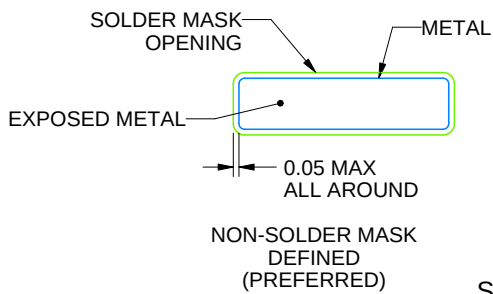
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

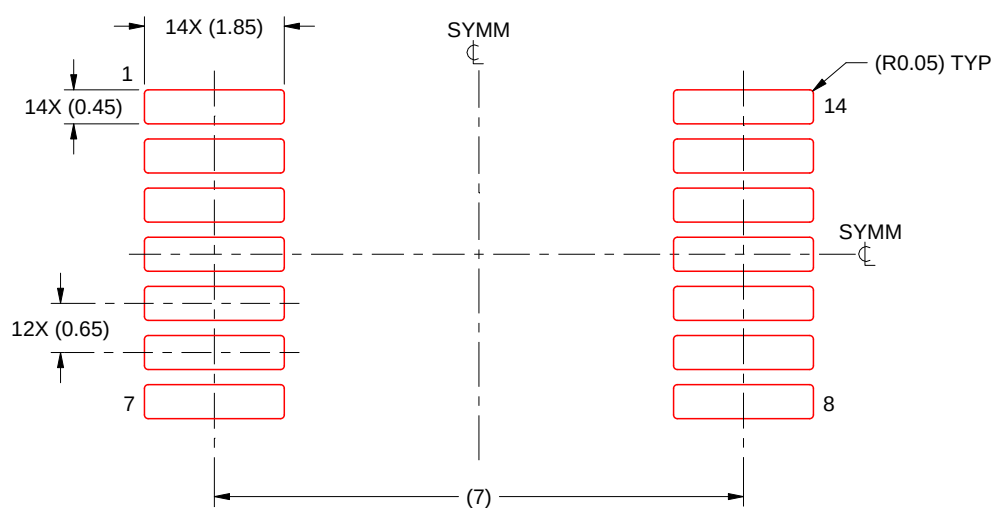
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

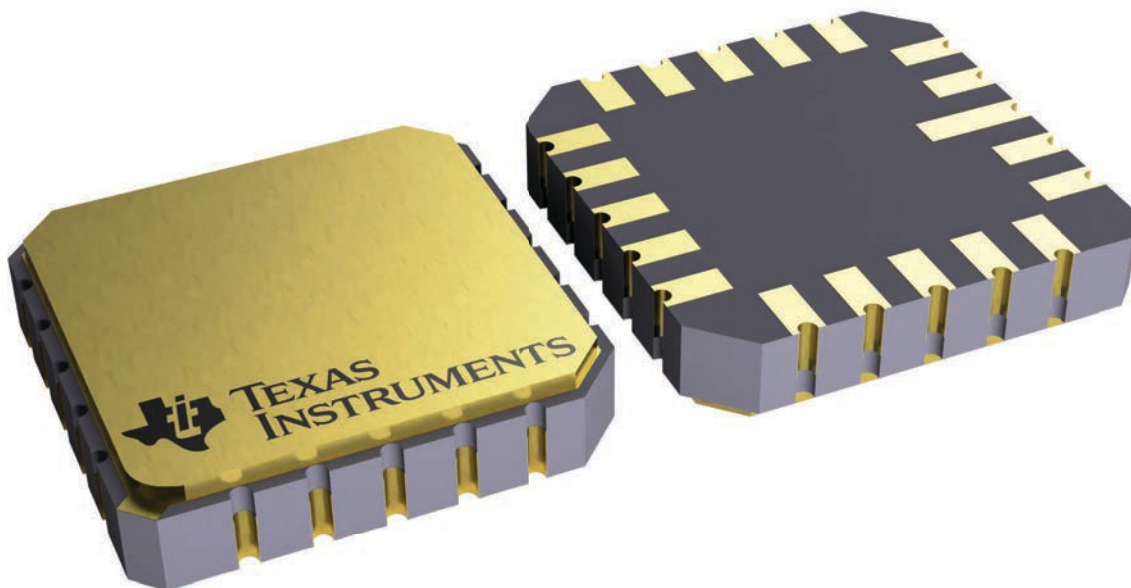
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

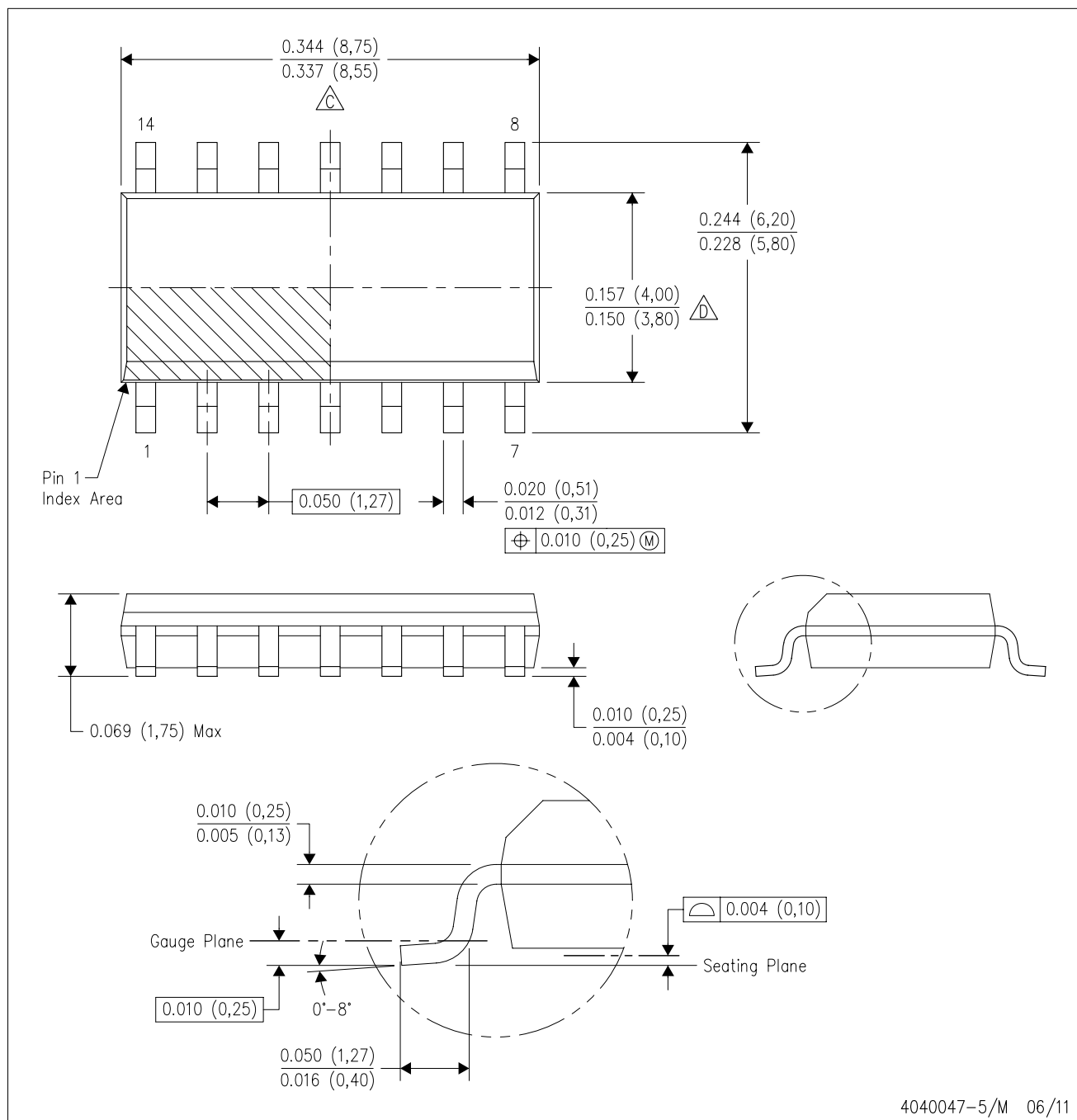
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

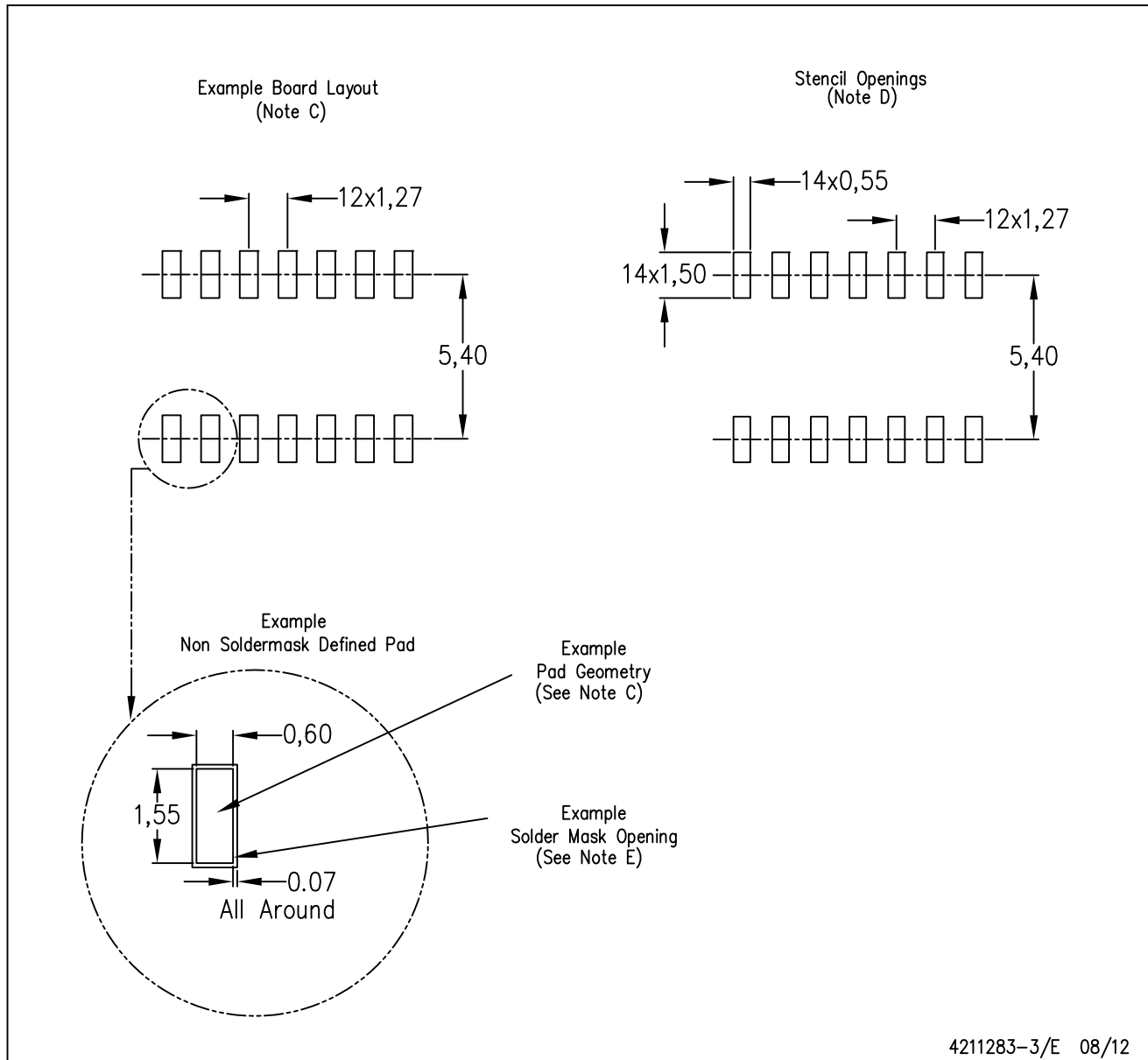


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

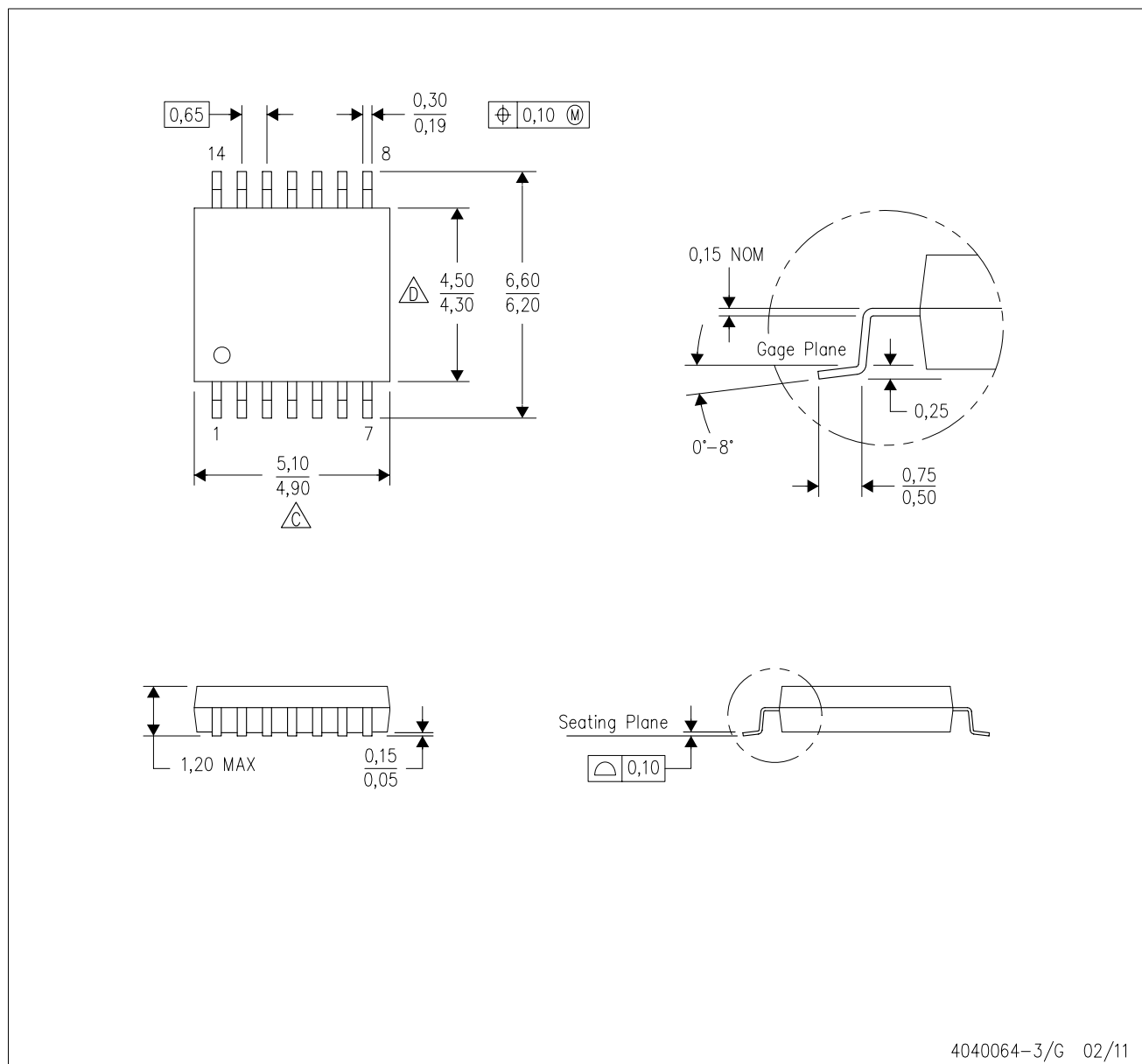
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

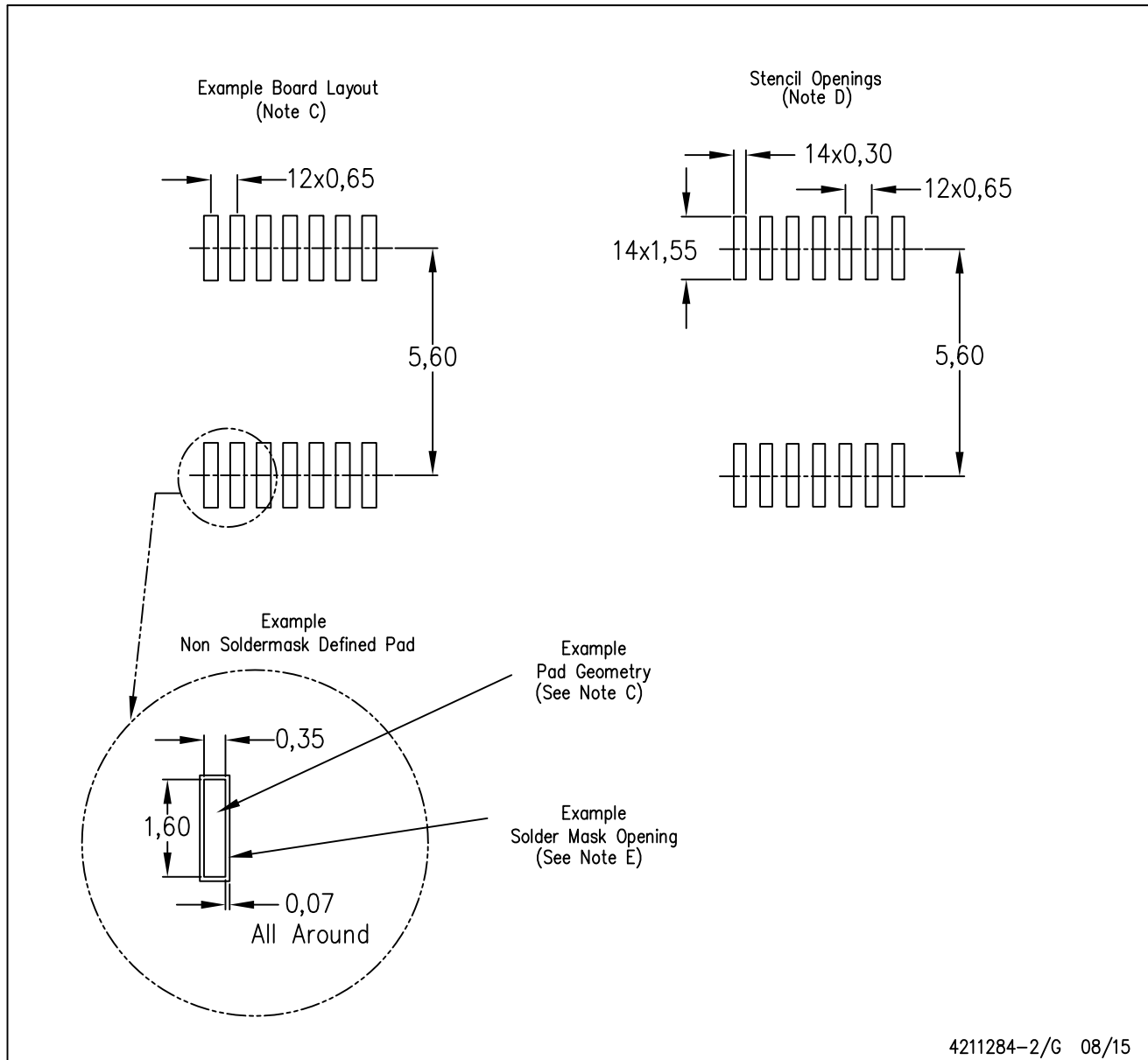
PLASTIC SMALL OUTLINE



4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

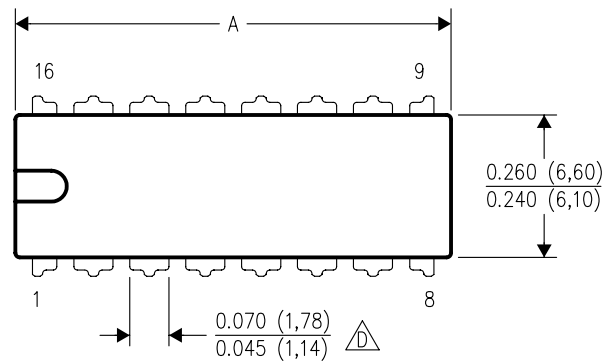


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

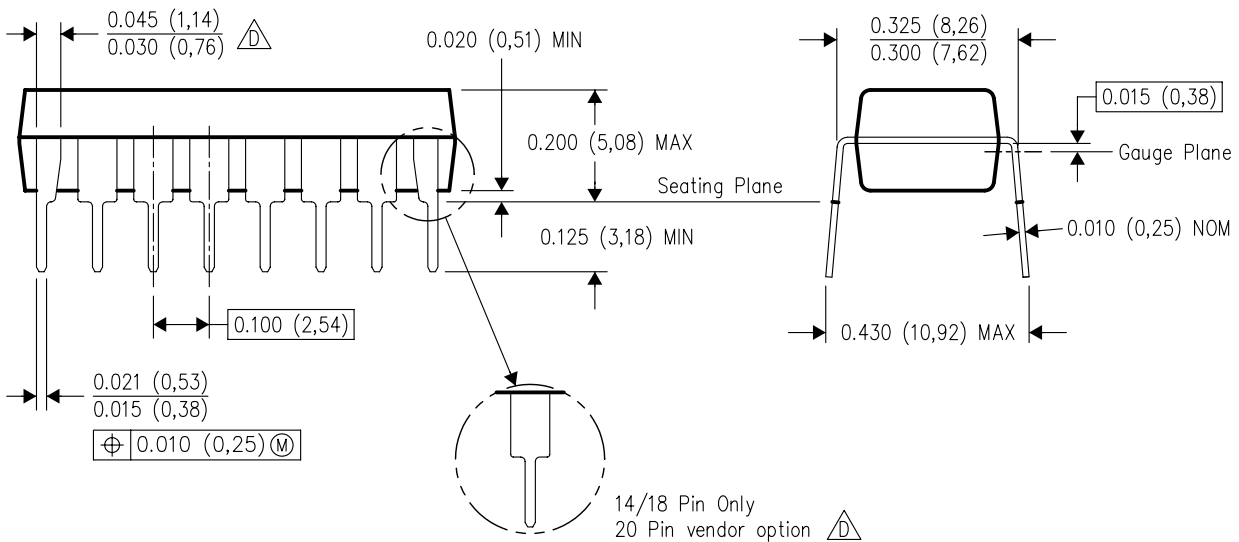
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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