



SN74LV32A Quadruple 2-Input Positive-Or Gates

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
> 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 200-V Machine Model
 - 1000-V Charged-Device Model

2 Applications

- Printers
- E-Meters
- Motor Controls: Permanent Magnets
- Servers and High Performance Computing
- Automotive Infotainment

3 Description

This quadruple 2-input positive-OR gates is designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV32A device performs the Boolean function $Y = A + B$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV32A	TVSOP (14)	3.60 mm x 4.40 mm
	SOIC (14)	8.65 mm x 3.91 mm
	VQFN (14)	3.50 mm x 3.50 mm
	SSOP (14)	6.20 mm x 5.30 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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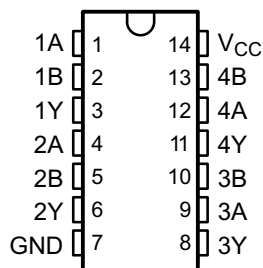
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5 Revision History

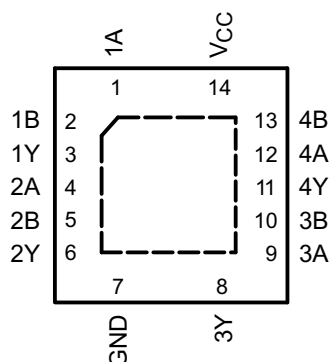
Changes from Revision J (April 2005) to Revision K	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.	1
• Deleted <i>Ordering Information</i> table.	1
• Changed MAX operating temperature to 125°C in <i>Recommended Operating Conditions</i> table.	5

6 Pin Configuration and Functions

**SN74LV32A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)**



**SN74LV32A . . . RGY PACKAGE
(TOP VIEW)**



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SN74LV32A			
	D, DB, DGV, NS, PW	RGY		
1A	1	1	I	1A Input
1B	2	2	I	1B Input
1Y	3	3	O	1Y Output
2A	4	4	I	2A Input
2B	5	5	I	2B Input
2Y	6	6	O	2Y Output
3Y	8	8	O	3Y Output
3A	9	9	I	3A Input
3B	10	10	I	3B Input
4Y	11	11	O	4Y Output
4A	12	12	I	4A Input
4B	13	13	I	4B Input
GND	7	7	—	Ground Pin
V _{CC}	14	14	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range ⁽²⁾		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		–0.5	7	V
V_O	Output voltage range ⁽²⁾⁽³⁾		–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		–50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous channel current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed. 2. This value is limited to 5.5 V maximum.
- (3) This value is limited to 5.5-V maximum.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 2.3 to 2.7 V	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 2.3 to 2.7 V		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		–50	μA
		V _{CC} = 2.3 to 2.7 V		–2	
		V _{CC} = 3 V to 3.6 V		–6	
		V _{CC} = 4.5 V to 5.5 V		–12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	μA
		V _{CC} = 2.3 to 2.7 V		2	
		V _{CC} = 3 V to 3.6 V		6	
		V _{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 to 2.7 V		200	ns/V
		V _{CC} = 3 V to 3.6 V		100	
		V _{CC} = 4.5 V to 5.5 V		20	
T _A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV32A						UNIT
		D	DBV	DVG	NS	PW	RGY	
		14 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	90.6	107.1	129.0	90.7	122.6	57.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	50.9	59.6	52.1	48.3	51.4	70.8	
R _{θJB}	Junction-to-board thermal resistance	44.8	54.4	62.0	49.4	64.4	33.6	
Ψ _{JT}	Junction-to-top characterization parameter	14.7	20.5	6.5	14.6	6.7	3.4	
Ψ _{JB}	Junction-to-board characterization parameter	44.5	53.8	61.3	49.1	63.8	33.7	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	13.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1		V _{CC} – 0.1		V
	I _{OH} = –2 mA	2.3 V	2			2		2		
	I _{OH} = –6 mA	3 V	2.48			2.48		2.48		
	I _{OH} = –12 mA	4.5 V	3.8			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1		0.1		V
	I _{OL} = 2 mA	2.3 V	0.4			0.4		0.4		
	I _{OL} = 6 mA	3 V	0.44			0.44		0.44		
	I _{OL} = 12 mA	4.5 V	0.55			0.55		0.55		
I _I	V _I = 5.5 V or GND	0 to 5.5 V	±1			±1		±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20		20		μA
I _{off}	V _I or V _O = 0 to 5.5 V	0	5			5		5		μA
C _i	V _I = V _{CC} or GND	3.3 V	3.3							pF
		5 V	3.3							

7.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	C _L = 15 pF	7.1 ⁽¹⁾	12.8 ⁽¹⁾		1 ⁽¹⁾	15 ⁽¹⁾	1	16	ns
			C _L = 50 pF	9.6	16.2		1	19	1	20	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	C _L = 15 pF	5 ⁽¹⁾	7.9 ⁽¹⁾		1 ⁽¹⁾	9.5 ⁽¹⁾	1	10.5	ns
			C _L = 50 pF	6.9	11.4		1	13	1	14	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	C _L = 15 pF	3.6 ⁽¹⁾	5.5 ⁽¹⁾		1 ⁽¹⁾	6.5 ⁽¹⁾	1	7.5	ns
			C _L = 50 pF	4.9	7.5		1	8.5	1	9.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.9 Noise Characteristics⁽¹⁾

 $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		SN74LV32A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.1	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.0		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

7.10 Operating Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$		3.3 V	9.5	pF
				5 V	11.5	

7.11 Typical Characteristics

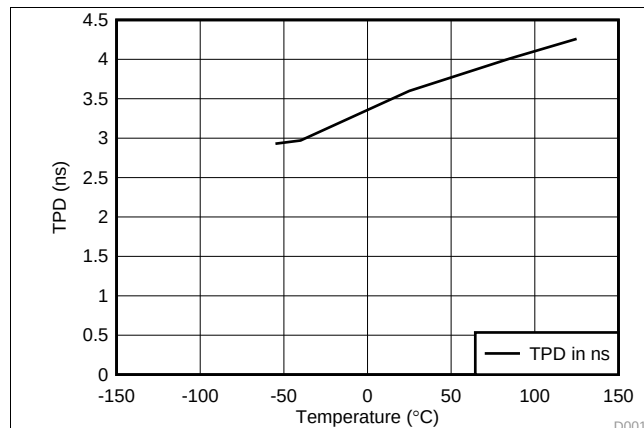


Figure 1. TPD vs Temperature at 5V

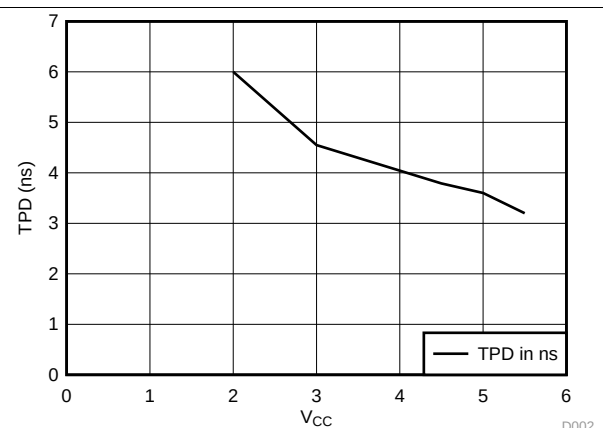
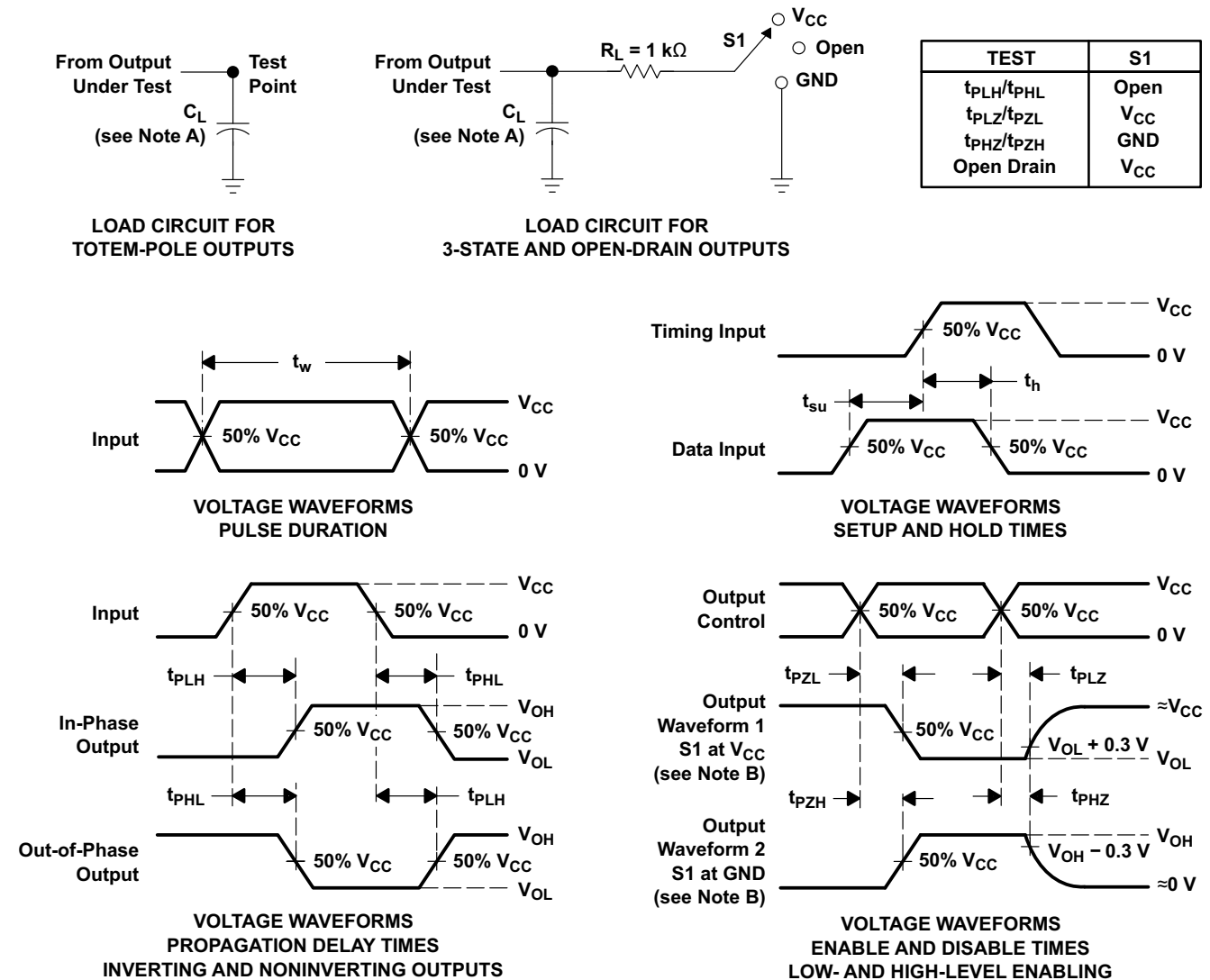


Figure 2. TPD vs V_{CC} at 25°C

8 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit And Voltage Waveforms

9 Detailed Description

9.1 Overview

This quadruple 2-input positive-OR gate is designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV32A device performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

This part has low drive which produces slower rise and fall times that will reduce ringing on the output signal. The inputs and outputs are of high impedance when $V_{CC} = 0$ V.

9.2 Functional Block Diagram



Figure 4. Logic Diagram, Each Gate (Positive Logic)

9.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down-voltage translation
 - Inputs accept voltages to 5.5 V
- I_{off} feature
 - Supports Live Insertion, Partial Power DownMode, and Back Drive Protection

9.4 Device Functional Modes

**Table 1. Function Table
(Each Gate)**

INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

SN74LV04A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it Ideal for down translation.

10.2 Typical Application

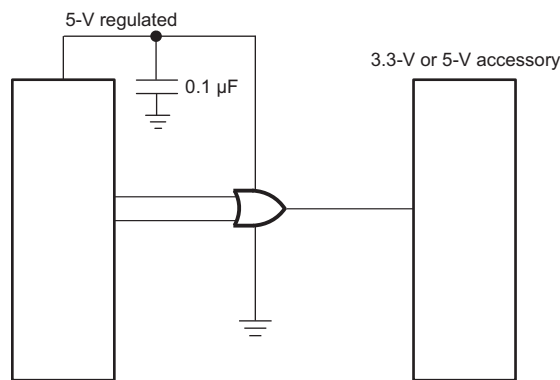


Figure 5. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Recommended Operating Conditions](#) table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves

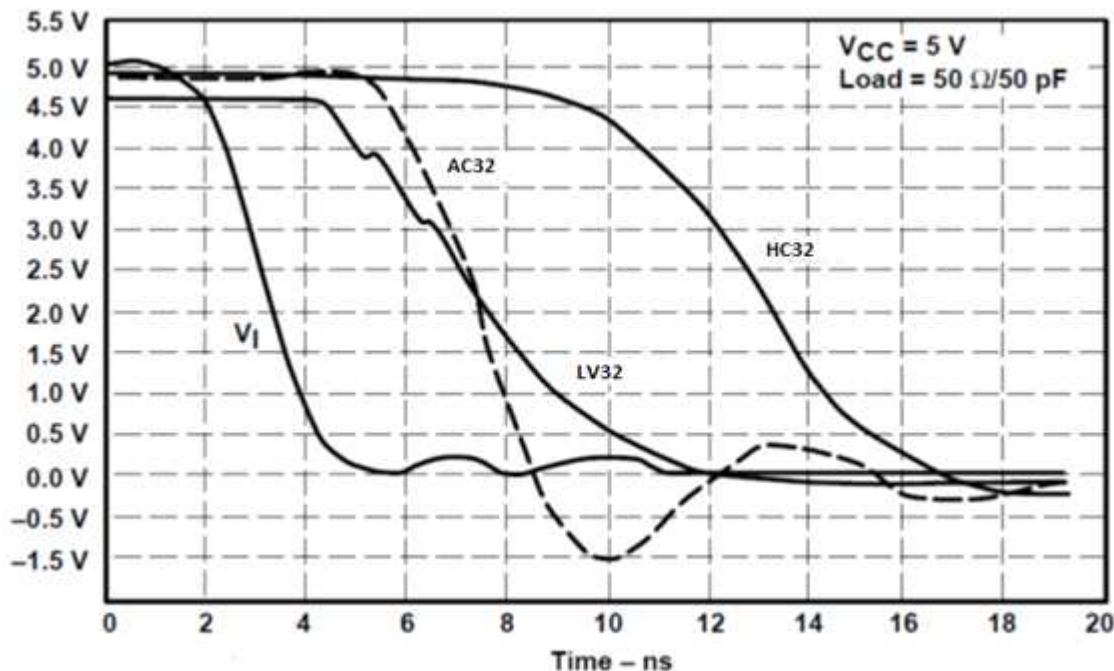


Figure 6. Typical Application Curve

11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 7](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

12.2 Layout Example

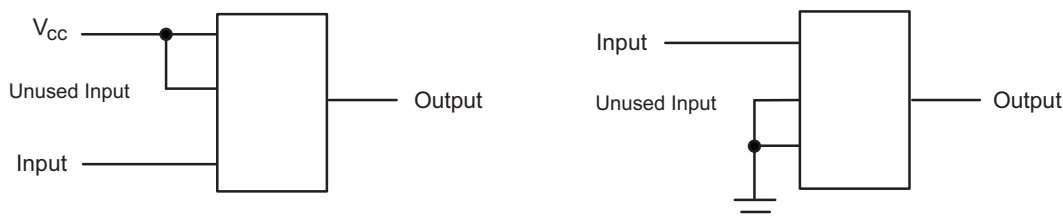


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV32A	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV32AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	LV32A	
SN74LV32ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV32A	Samples
SN74LV32ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV32A	Samples
SN74LV32ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV32A	Samples
SN74LV32ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV32A	Samples
SN74LV32APW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	LV32A	
SN74LV32APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV32A	Samples
SN74LV32APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV32A	Samples
SN74LV32APWT	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	LV32A	
SN74LV32ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV32A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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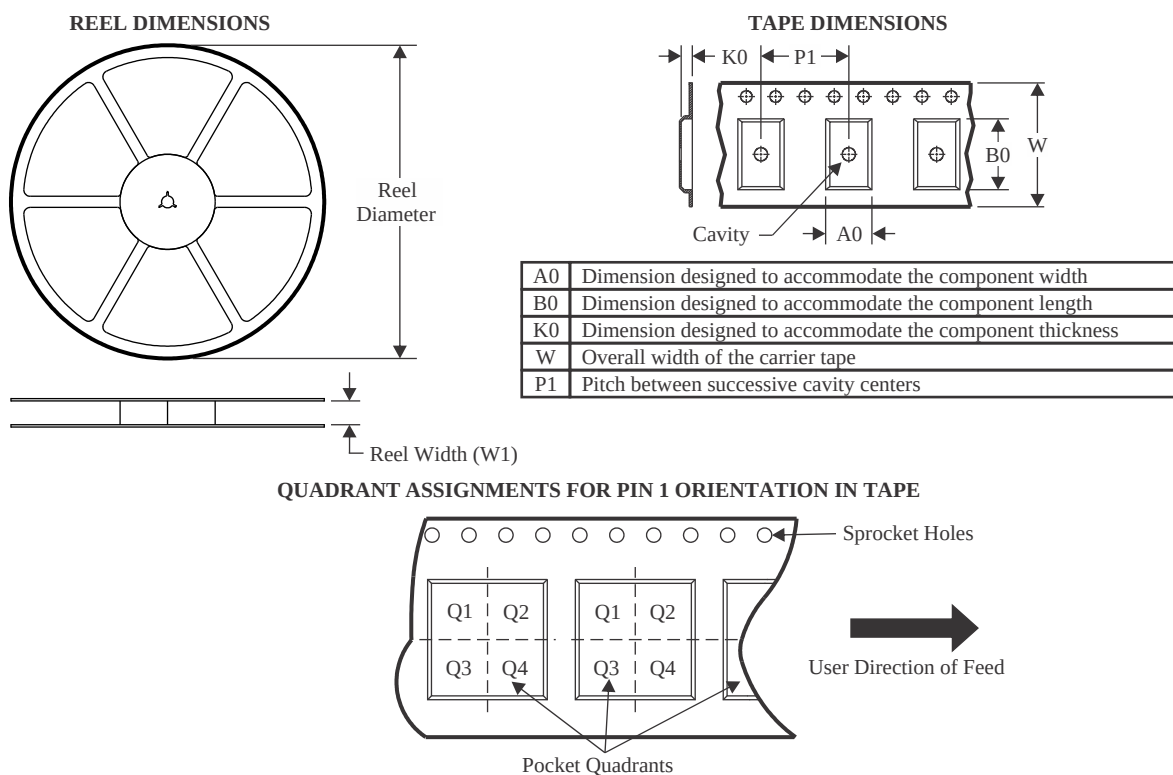
OTHER QUALIFIED VERSIONS OF SN74LV32A :

- Automotive : [SN74LV32A-Q1](#)
- Enhanced Product : [SN74LV32A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

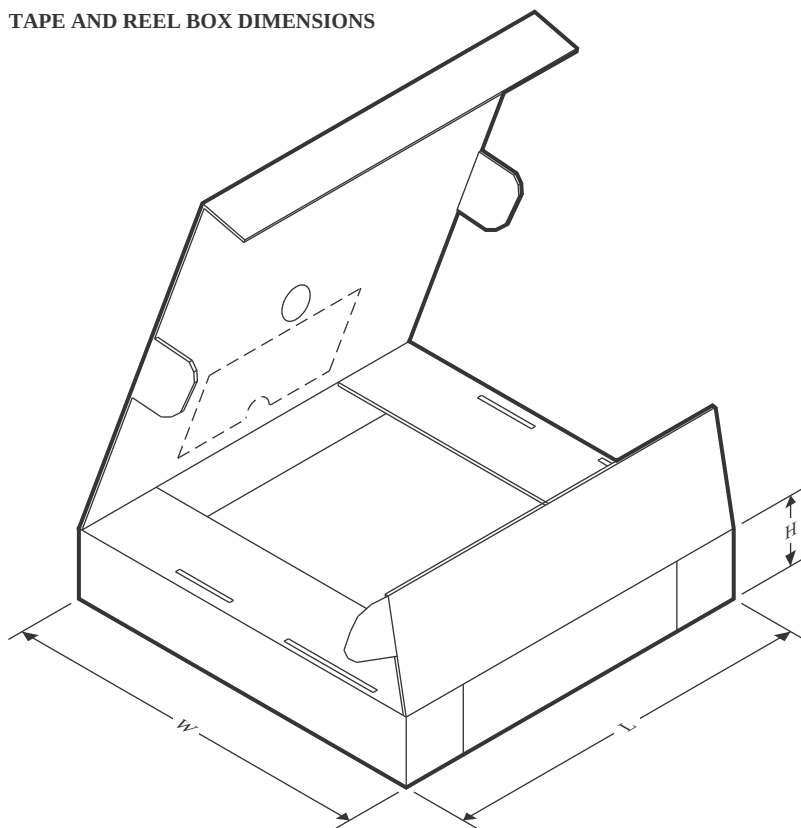
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV32ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV32ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV32ADR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74LV32ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV32ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV32ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV32APWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74LV32APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV32APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV32APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV32APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV32ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

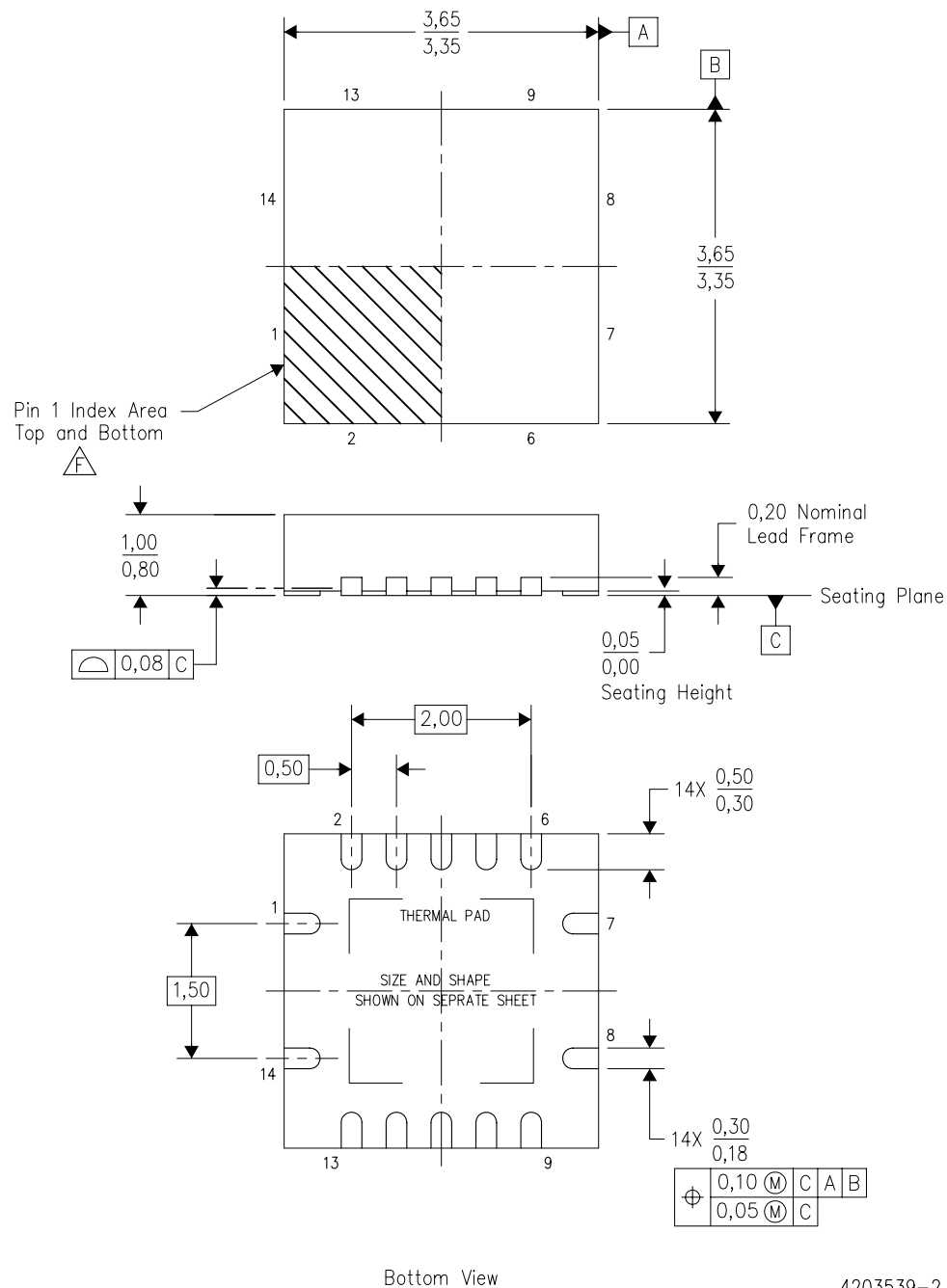


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV32ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV32ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV32ADR	SOIC	D	14	2500	366.0	364.0	50.0
SN74LV32ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV32ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV32ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV32APWR	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74LV32APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV32APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV32APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV32APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV32ARGYR	VQFN	RGY	14	3000	360.0	360.0	36.0

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/I 06/2011

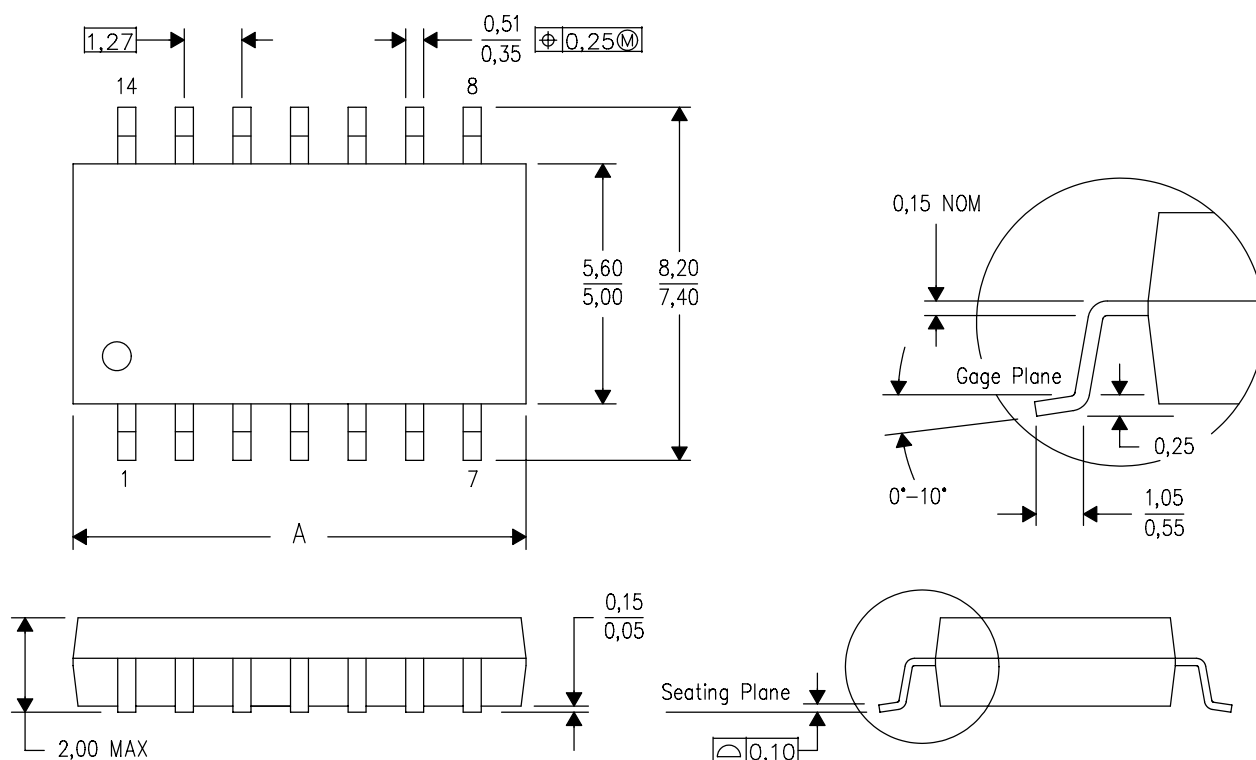
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

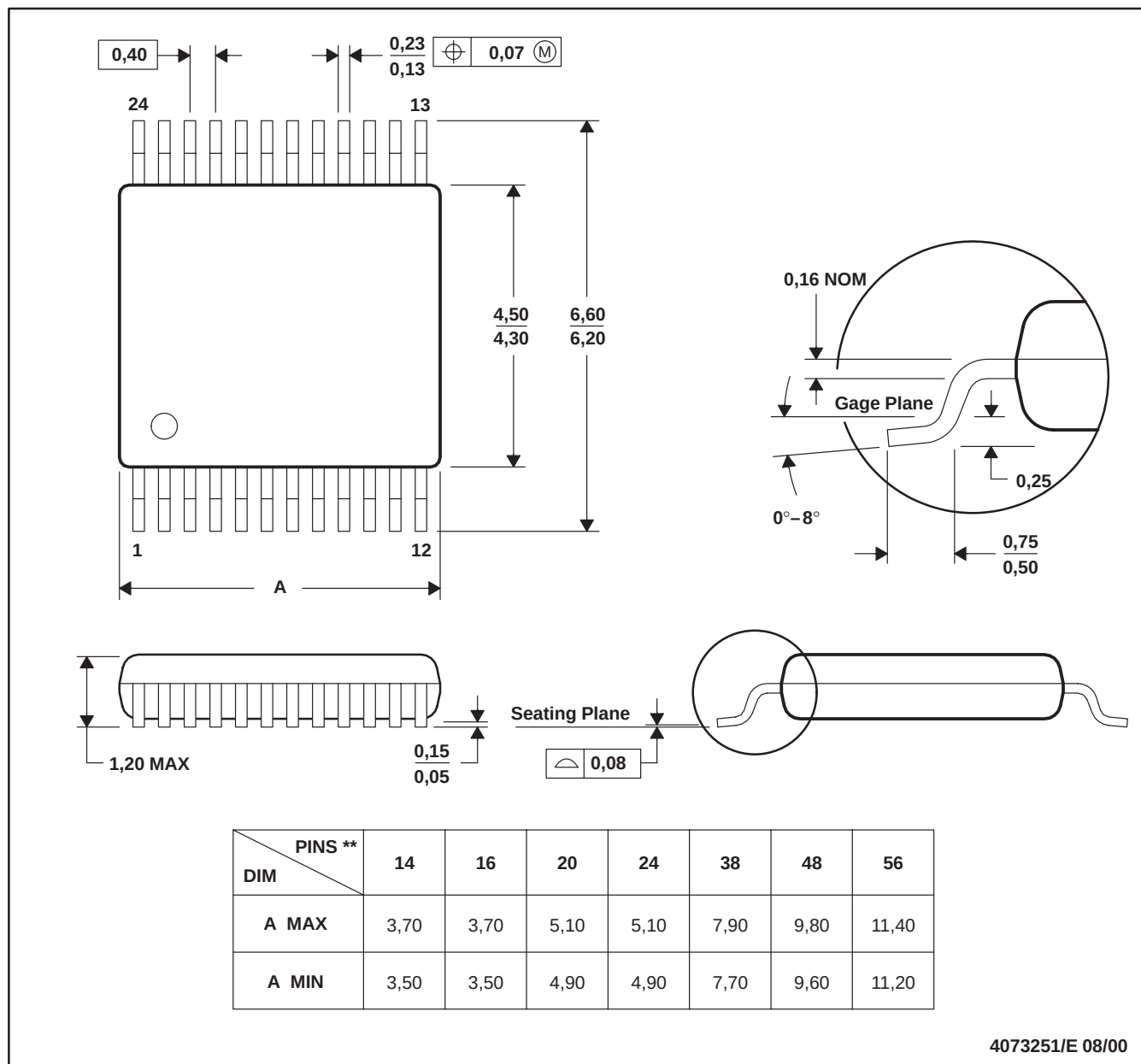
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

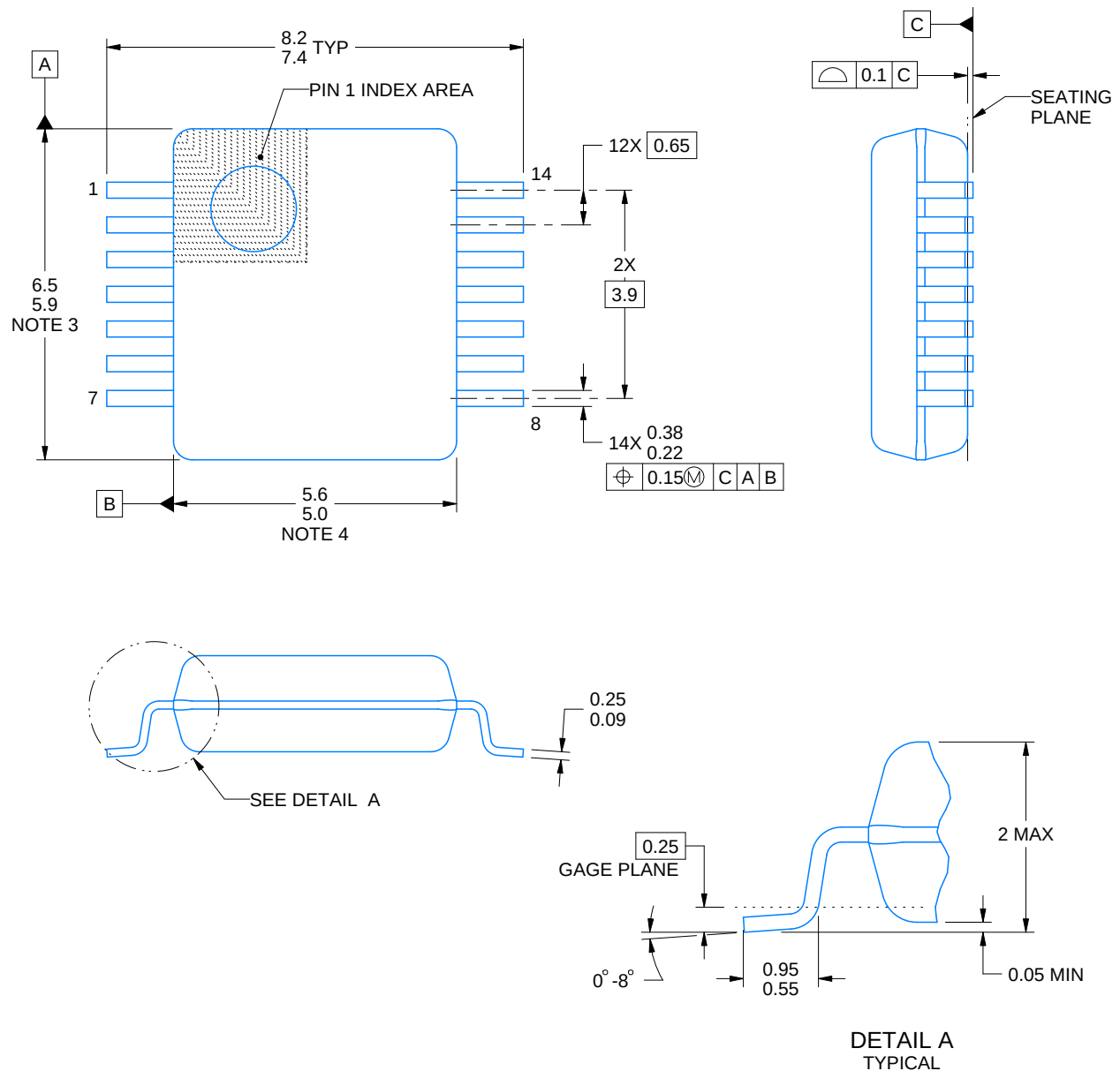
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4220762/A 05/2024

NOTES:

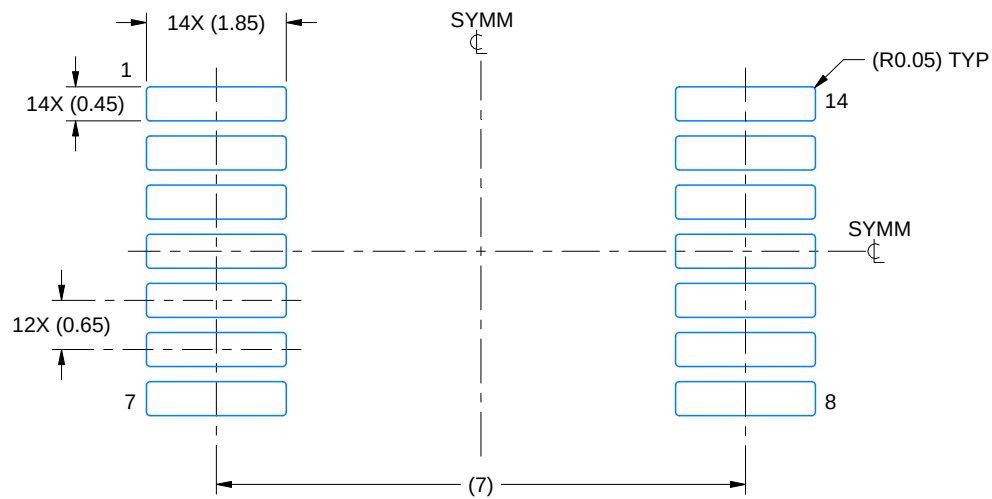
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

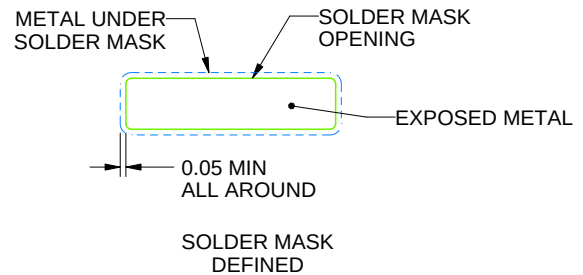
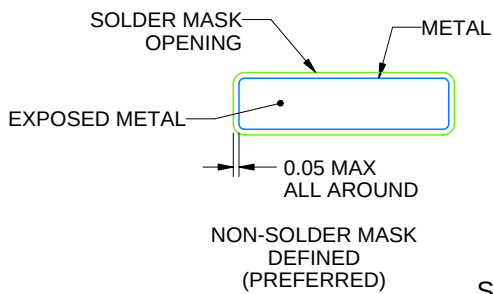
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

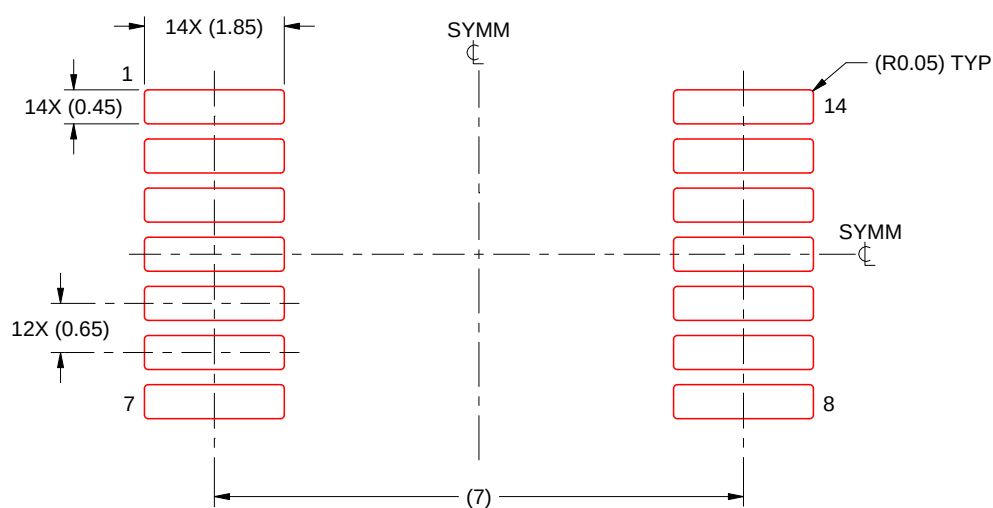
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

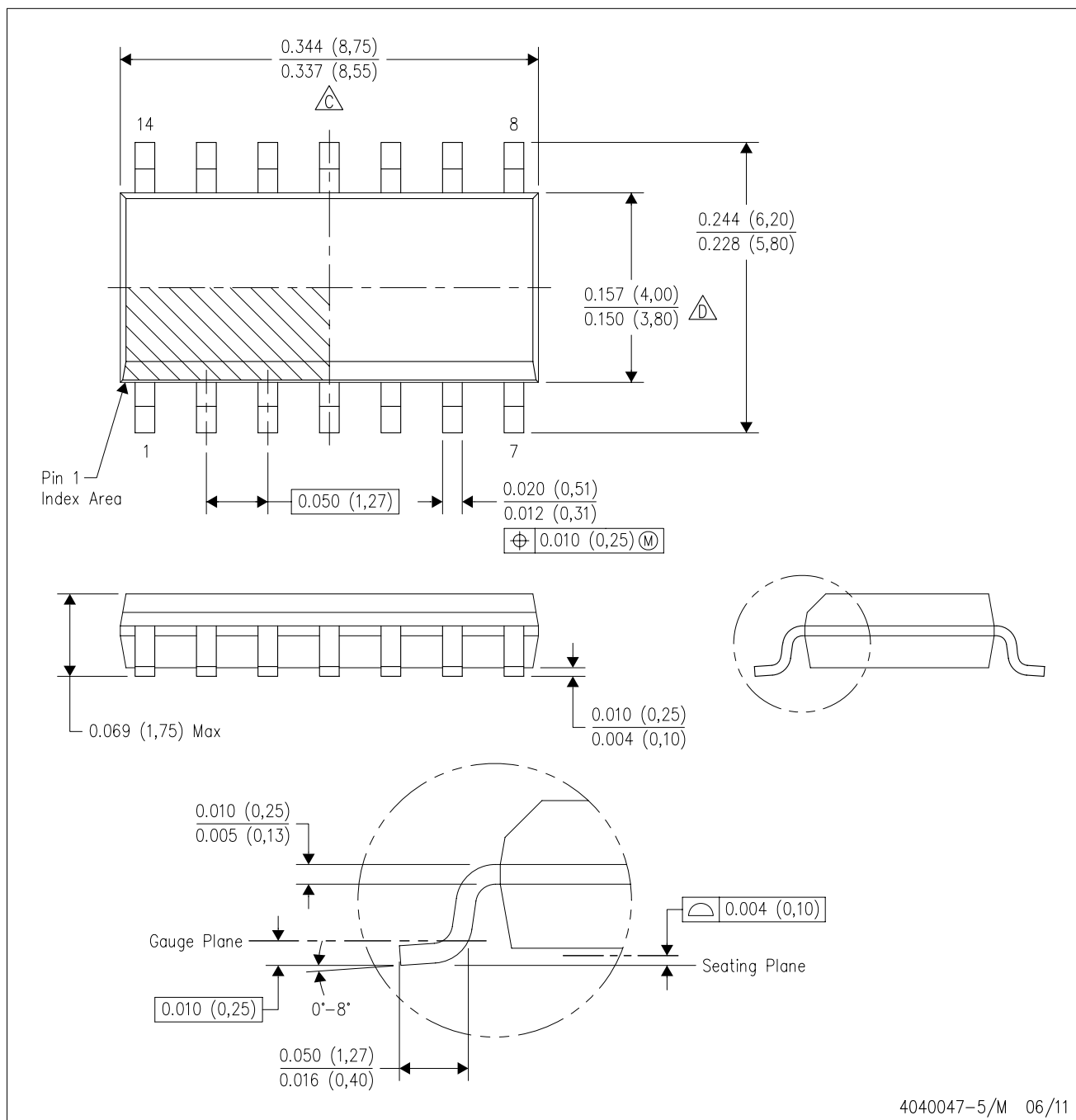
4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



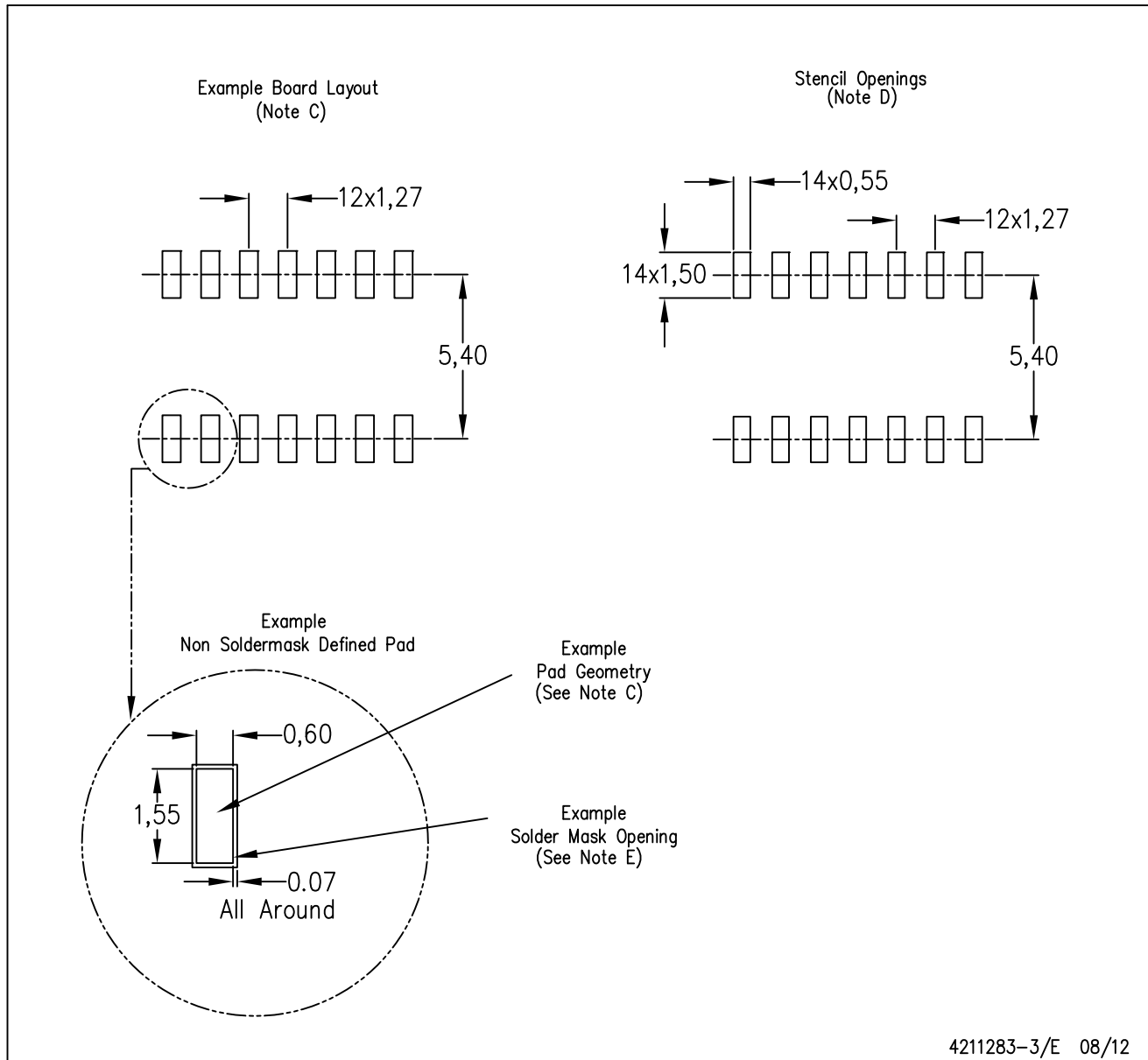
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

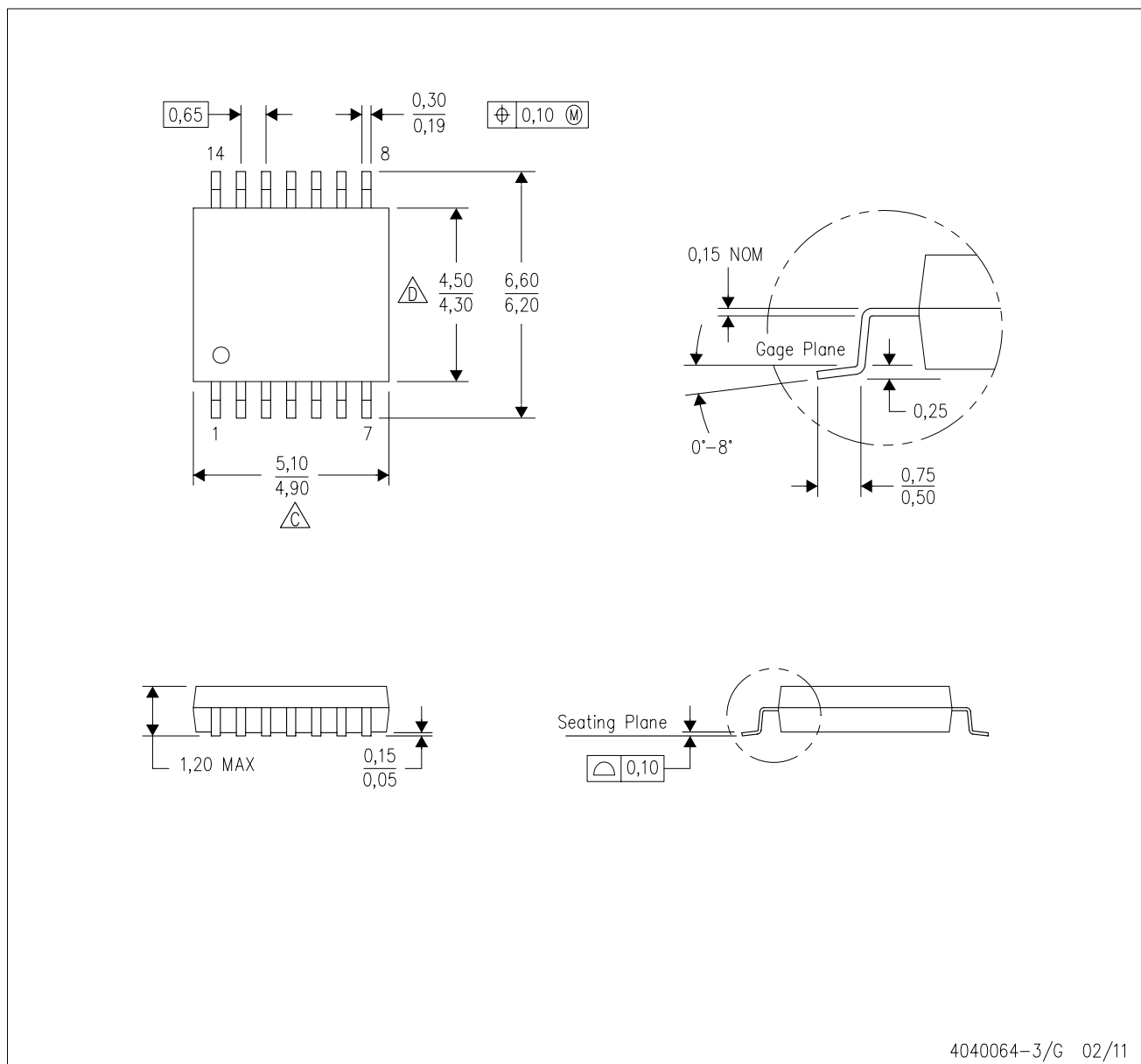
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

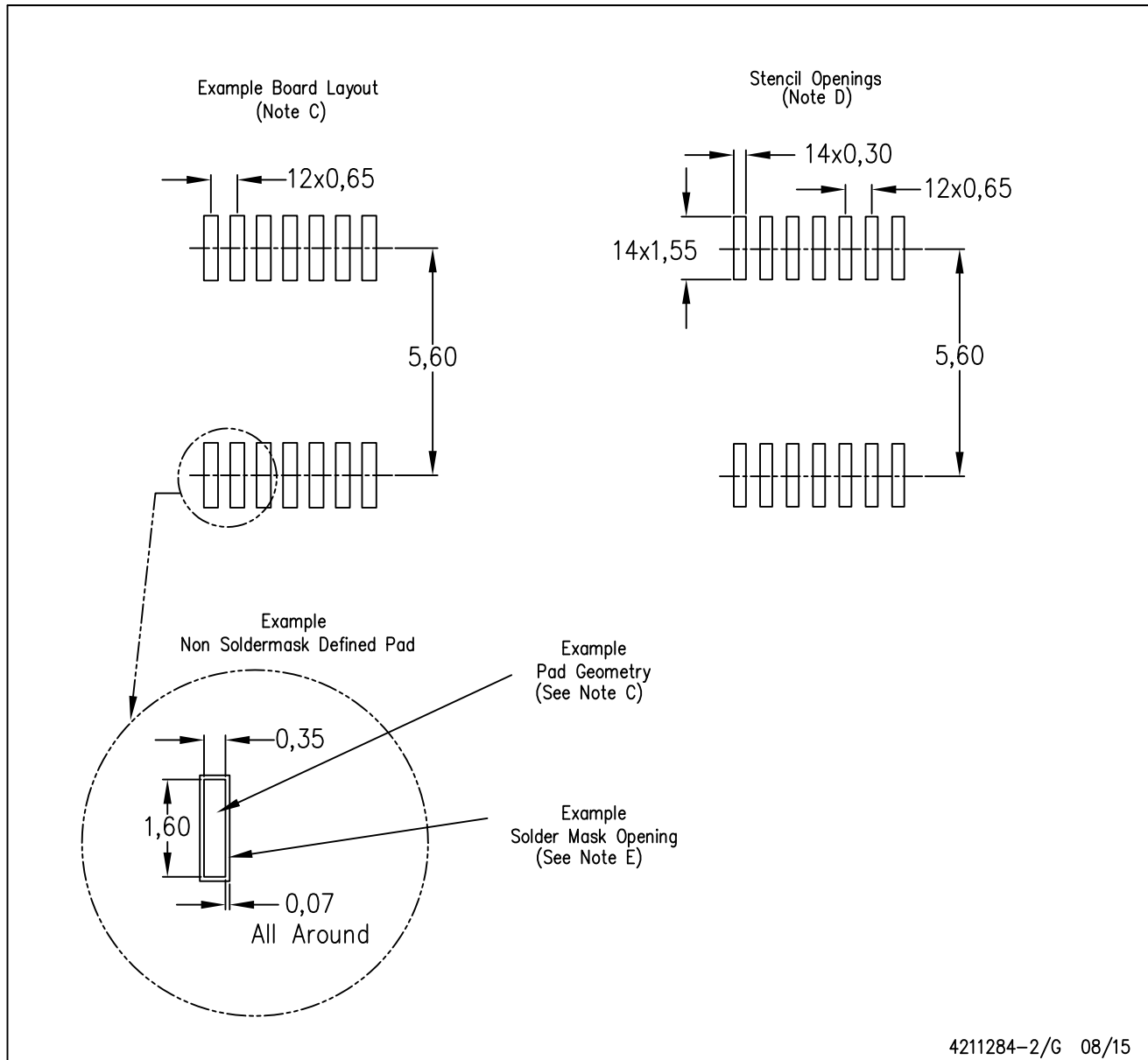
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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