

## SN74LV175A 具有清零功能的四路 D 型触发器

### 1 特性

- $V_{CC}$  工作电压范围为 2V 至 5.5V
- 5V 时  $t_{pd}$  最大值为 7.5 ns
- $V_{OLP}$  (输出接地反弹)  
典型值小于 0.8V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ )
- $V_{OHV}$  (输出  $V_{OH}$  下冲) 典型值  
大于 2.3V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ )
- $I_{off}$  支持局部断电模式运行
- 所有端口上均支持以混合模式电压运行
- 包含四个具有双轨输出的触发器

### 2 应用

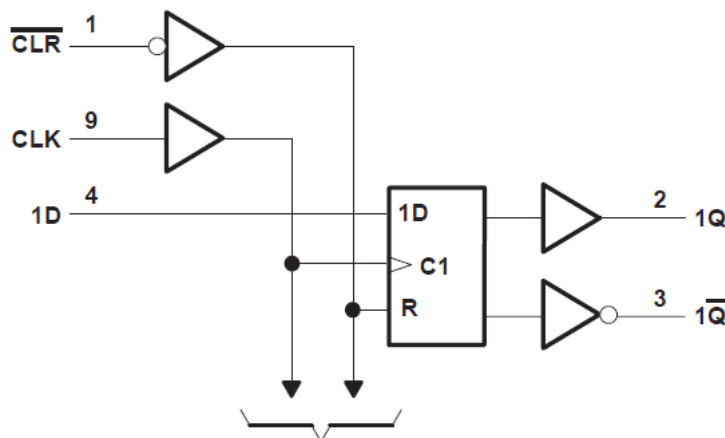
- 缓冲或存储寄存器
- 移位寄存器
- 图形发生器

### 3 说明

SN74LV175A 器件是一款四路 D 型触发器，可在 2V 至 5.5  $V_{CC}$  下运行。这些器件具有直接清零 ( $\overline{CLR}$ ) 输入，并具有来自每个触发器的互补输出。

#### 封装信息

| 器件型号       | 封装         | 封装尺寸 (标称值)      |
|------------|------------|-----------------|
| SN74LV175A | SOIC (16)  | 9.9mm × 3.9mm   |
|            | SOP (16)   | 10.3mm × 1.95mm |
|            | TSSOP (16) | 5mm × 4.4mm     |
|            | TVSOP (16) | 3.6mm × 4.4mm   |



逻辑图 (正逻辑)



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision I (January 2023) to Revision J (March 2023)                         | Page |
|-------------------------------------------------------------------------------------------|------|
| • Updated thermal values for PW package from R0JA = 108 to 138.7, all values in °C/W..... | 5    |
| Changes from Revision H (December 2022) to Revision I (January 2023)                      | Page |
| • 添加了典型应用部分、布局示例、引脚功能表和引脚配置图像.....                                                        | 1    |
| Changes from Revision G (April 2005) to Revision H (December 2022)                        | Page |
| • 通篇更新了表格、图和交叉参考的格式.....                                                                  | 1    |

## 5 Pin Configurations and Functions

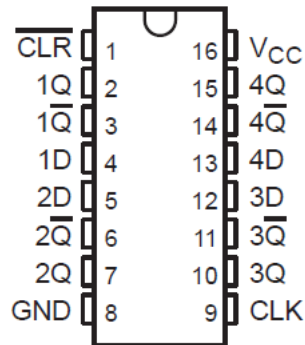


图 5-1. D, DGV, NS, or PW Package (Top View)

表 5-1. Pin Functions

| PIN |                 | TYPE | DESCRIPTION |
|-----|-----------------|------|-------------|
| NO. | NAME            |      |             |
| 1   | CLR             | I    | Clear Pin   |
| 2   | 1Q              | O    | 1Q Output   |
| 3   | 1Q̄             | O    | 1Q̄ Output  |
| 4   | 1D              | I    | 1D Input    |
| 5   | 2D              | I    | 2D Input    |
| 6   | 2Q̄             | O    | 2Q̄ Output  |
| 7   | 2Q              | O    | 2Q Output   |
| 8   | GND             | —    | Ground Pin  |
| 9   | CLK             | I    | Clock Input |
| 10  | 3Q              | O    | 3Q Output   |
| 11  | 3Q̄             | O    | 3Q̄ Output  |
| 12  | 3D              | I    | 3D Input    |
| 13  | 4D              | I    | 4D Input    |
| 14  | 4Q̄             | O    | 4Q̄ Output  |
| 15  | 4Q              | O    | 4Q Output   |
| 16  | V <sub>CC</sub> | —    | Power Pin   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

|           |                                                                              |                       | MIN  | MAX            | UNIT |
|-----------|------------------------------------------------------------------------------|-----------------------|------|----------------|------|
| $V_{CC}$  | Supply voltage range                                                         |                       | –0.5 | 7              | V    |
| $V_I$     | Input voltage range                                                          |                       | –0.5 | 7              | V    |
| $V_O$     | Voltage range applied to any output in the high-impedance or power-off state |                       | –0.5 | 7              | V    |
| $V_O$     | Output voltage range                                                         |                       | –0.5 | $V_{CC} + 0.5$ | V    |
| $I_{IK}$  | Input clamp current                                                          | $V_I < 0$             |      | –20            | mA   |
| $I_{OK}$  | Output clamp current                                                         | $V_O < 0$             |      | –50            | mA   |
| $I_O$     | Continuous output current                                                    | $V_O = 0$ to $V_{CC}$ |      | ±25            | mA   |
|           | Continuous current through $V_{CC}$ or GND                                   |                       |      | ±50            | mA   |
| $T_{stg}$ | Storage temperature range                                                    |                       | –65  | 150            | °C   |

### 6.2 ESD Ratings

|             |                         |                             | VALUE | UNIT |
|-------------|-------------------------|-----------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-Body Model (A114-A)   | ±2000 | V    |
|             |                         | Machine Model (A115-A)      | ±200  |      |
|             |                         | Charged-Device Model (C101) | ±1000 |      |

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                 |                                    |                                  | MIN                   | MAX                   | UNIT |
|-----------------|------------------------------------|----------------------------------|-----------------------|-----------------------|------|
| V <sub>CC</sub> | Supply voltage                     |                                  | 2                     | 5.5                   | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 2 V            | 1.5                   |                       | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V | V <sub>CC</sub> × 0.7 |                       |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   | V <sub>CC</sub> × 0.7 |                       |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V | V <sub>CC</sub> × 0.7 |                       |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 2 V            |                       | 0.5                   | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | V <sub>CC</sub> × 0.3 |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | V <sub>CC</sub> × 0.3 |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | V <sub>CC</sub> × 0.3 |      |
| V <sub>I</sub>  | Input voltage                      |                                  | 0                     | 5.5                   | V    |
| V <sub>O</sub>  | Output voltage                     |                                  | 0                     | V <sub>CC</sub>       | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 2 V            |                       | –50                   | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | –2                    | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | –6                    |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | –12                   |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 2 V            |                       | 50                    | μA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | 2                     | mA   |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | 6                     |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | 12                    |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 2.3 V to 2.7 V |                       | 200                   | ns/V |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V   |                       | 100                   |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V |                       | 20                    |      |
| T <sub>A</sub>  | Operating free-air temperature     |                                  | –40                   | 85                    | °C   |

## 6.4 Thermal Information

| THERMAL METRIC   |                                        | D       | DB | DGV | NS | PW    | UNIT |
|------------------|----------------------------------------|---------|----|-----|----|-------|------|
|                  |                                        | 16 PINS |    |     |    |       |      |
| R <sub>θJA</sub> | Junction-to-ambient thermal resistance | 73      | 82 | 20  | 64 | 138.7 | °C/W |

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS               | V <sub>CC</sub> | MIN                   | TYP | MAX  | UNIT |
|-----------------|-------------------------------|-----------------|-----------------------|-----|------|------|
| V <sub>OH</sub> | I <sub>OH</sub> = –50 μA      | 2 V to 5.5 V    | V <sub>CC</sub> – 0.1 |     |      | V    |
|                 | I <sub>OH</sub> = –2 mA       | 2.3 V           | 2                     |     |      |      |
|                 | I <sub>OH</sub> = –6 mA       | 3 V             | 2.48                  |     |      |      |
|                 | I <sub>OH</sub> = –12 mA      | 4.5 V           | 3.8                   |     |      |      |
| V <sub>OL</sub> | I <sub>OL</sub> = 50 μA       | 2 V to 5.5 V    |                       |     | 0.1  | V    |
|                 | I <sub>OL</sub> = 2 mA        | 2.3 V           |                       |     | 0.4  |      |
|                 | I <sub>OL</sub> = 6 mA        | 3 V             |                       |     | 0.44 |      |
|                 | I <sub>OL</sub> = 12 mA       | 4.5 V           |                       |     | 0.55 |      |
| I <sub>I</sub>  | V <sub>I</sub> = 5.5 V or GND | 0 to 5.5 V      |                       |     | ±1   | μA   |

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                  | $V_{CC}$ | MIN | TYP | MAX | UNIT    |
|-----------|----------------------------------|----------|-----|-----|-----|---------|
| $I_{CC}$  | $V_I = V_{CC}$ or GND, $I_O = 0$ | 5.5 V    |     |     | 20  | $\mu A$ |
| $I_{off}$ | $V_I$ or $V_O = 0$ to 5.5 V      | 0 V      |     |     | 5   | $\mu A$ |
| $C_i$     | $V_I = V_{CC}$ or GND            | 3.3 V    |     | 1.4 |     | pF      |

## 6.6 Timing Requirements, $V_{CC} = 2.5 V \pm 0.2 V$

over recommended operating free-air temperature range (unless otherwise noted)

|          |                                      |                           | $T_A = 25^\circ C$ |     | SN74LV175A |     | UNIT |
|----------|--------------------------------------|---------------------------|--------------------|-----|------------|-----|------|
|          |                                      |                           | MIN                | MAX | MIN        | MAX |      |
| $t_w$    | Pulse duration                       | $\overline{CLR}$ low      | 6                  |     | 6          |     | ns   |
|          |                                      | CLK high or low           | 6.5                |     | 7          |     |      |
| $t_{su}$ | Setup time before CLK $\uparrow$     | Data                      | 7                  |     | 7.5        |     | ns   |
|          |                                      | $\overline{CLR}$ inactive | 7                  |     | 7.5        |     |      |
| $t_h$    | Hold time, data after CLK $\uparrow$ |                           | 0.5                |     | 1          |     | ns   |

## 6.7 Timing Requirements, $V_{CC} = 3.3 V \pm 0.3 V$

over recommended operating free-air temperature range (unless otherwise noted)

|          |                                      |                           | $T_A = 25^\circ C$ |     | SN74LV175A |     | UNIT |
|----------|--------------------------------------|---------------------------|--------------------|-----|------------|-----|------|
|          |                                      |                           | MIN                | MAX | MIN        | MAX |      |
| $t_w$    | Pulse duration                       | $\overline{CLR}$ low      | 5                  |     | 5          |     | ns   |
|          |                                      | CLK high or low           | 5                  |     | 5          |     |      |
| $t_{su}$ | Setup time before CLK $\uparrow$     | Data                      | 5                  |     | 5          |     | ns   |
|          |                                      | $\overline{CLR}$ inactive | 5                  |     | 5          |     |      |
| $t_h$    | Hold time, data after CLK $\uparrow$ |                           | 1                  |     | 1          |     | ns   |

## 6.8 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

|          |                                      |                 | $T_A = 25^\circ\text{C}$ |     | SN74LV175A |     | UNIT |
|----------|--------------------------------------|-----------------|--------------------------|-----|------------|-----|------|
|          |                                      |                 | MIN                      | MAX | MIN        | MAX |      |
| $t_w$    | Pulse duration                       | CLR low         | 5                        |     | 5          |     | ns   |
|          |                                      | CLK high or low | 5                        |     | 5          |     |      |
| $t_{su}$ | Setup time before CLK $\uparrow$     | Data            | 4                        |     | 4          |     | ns   |
|          |                                      | CLR inactive    | 5                        |     | 5          |     |      |
| $t_h$    | Hold time, data after CLK $\uparrow$ |                 | 1                        |     | 1          |     | ns   |

## 6.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |      |     | SN74LV175A |      | UNIT |
|-------------|-----------------|----------------|----------------------|--------------------------|------|-----|------------|------|------|
|             |                 |                |                      | MIN                      | TYP  | MAX | MIN        | MAX  |      |
| $f_{max}$   |                 |                | $C_L = 15\text{ pF}$ | 50                       | 105  |     | 45         |      | MHz  |
|             |                 |                | $C_L = 50\text{ pF}$ | 40                       | 80   |     | 35         |      |      |
| $t_{pd}$    | CLR             | Any            | $C_L = 15\text{ pF}$ | 7.9                      | 16.6 |     | 1          | 20   | ns   |
| $t_{pd}$    | CLK             | Any            |                      | 9.3                      | 18.8 |     | 1          | 22   | ns   |
| $t_{sk(o)}$ | CLR             | Any            | $C_L = 50\text{ pF}$ | 10.4                     | 21.6 |     | 1          | 25.5 | ns   |
| $t_{PHL}$   | CLK             | Any            |                      | 12                       | 23.3 |     | 1          | 27   | ns   |
| $t_{sk(o)}$ |                 |                |                      |                          |      | 2   |            | 2    | ns   |

over operating free-air temperature range (unless otherwise noted)

## 6.10 Switching Characteristics, $V_{CC} = 3.5\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |      |     | SN74LV175A |      | UNIT |
|-------------|-----------------|----------------|----------------------|--------------------------|------|-----|------------|------|------|
|             |                 |                |                      | MIN                      | TYP  | MAX | MIN        | MAX  |      |
| $f_{max}$   |                 |                | $C_L = 15\text{ pF}$ | 90                       | 155  |     | 75         |      | MHz  |
|             |                 |                | $C_L = 50\text{ pF}$ | 50                       | 120  |     | 45         |      |      |
| $t_{pd}$    | CLR             | Any            | $C_L = 15\text{ pF}$ | 5.5                      | 10.1 |     | 1          | 12   | ns   |
|             | CLK             |                |                      | 6.5                      | 11.5 |     | 1          | 13.5 |      |
|             | CLR             | Any            | $C_L = 50\text{ pF}$ | 7.4                      | 13.6 |     | 1          | 15.5 | ns   |
|             | CLK             |                |                      | 8.4                      | 15   |     | 1          | 17   |      |
| $t_{sk(o)}$ |                 |                | $C_L = 50\text{ pF}$ |                          |      | 1.5 |            | 1.5  | ns   |

## 6.11 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER   | FROM<br>(INPUT) | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |     |     | SN74LV175A |      | UNIT |
|-------------|-----------------|----------------|----------------------|--------------------------|-----|-----|------------|------|------|
|             |                 |                |                      | MIN                      | TYP | MAX | MIN        | MAX  |      |
| $f_{\max}$  |                 |                | $C_L = 15\text{ pF}$ | 150                      | 215 |     | 125        |      | MHz  |
|             |                 |                | $C_L = 50\text{ pF}$ | 85                       | 165 |     | 75         |      |      |
| $t_{pd}$    | CLR             | Any            | $C_L = 15\text{ pF}$ |                          | 3.7 | 6.4 | 1          | 7.5  | ns   |
|             | CLK             |                |                      |                          | 4.6 | 7.3 | 1          | 8.5  |      |
|             | CLR             | Any            | $C_L = 50\text{ pF}$ |                          | 5.3 | 8.4 | 1          | 9.5  | ns   |
|             | CLK             |                |                      |                          | 6   | 9.3 | 1          | 10.5 |      |
| $t_{sk(o)}$ |                 |                | $C_L = 50\text{ pF}$ |                          |     | 1   |            | 1    | ns   |

## 6.12 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

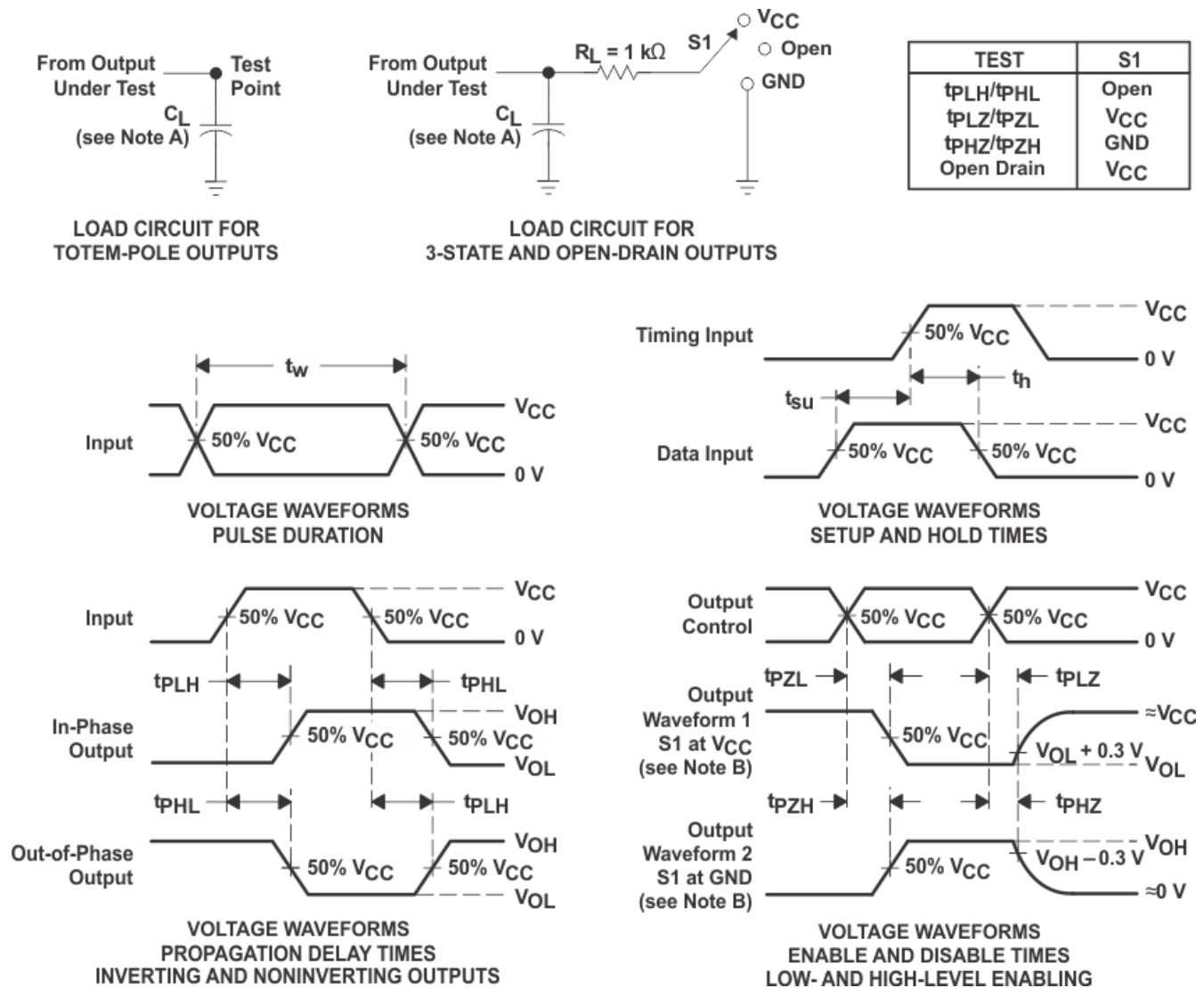
| PARAMETER   |                                        | MIN  | TYP  | MAX  | UNIT |
|-------------|----------------------------------------|------|------|------|------|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ |      | 0.3  | 0.8  | V    |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ |      | −0.3 | −0.8 | V    |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ |      | 3    |      | V    |
| $V_{IH(D)}$ | High-level dynamic input voltage       | 2.31 |      |      | V    |
| $V_{IL(D)}$ | Low-level dynamic input voltage        |      |      | 0.99 | V    |

## 6.13 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS      |                     | $V_{CC}$ | TYP  | UNIT |
|-----------|-------------------------------|----------------------|---------------------|----------|------|------|
| $C_{pd}$  | Power dissipation capacitance | $C_L = 50\text{ pF}$ | $f = 10\text{ MHz}$ | 3.3 V    | 13.6 | pF   |
|           |                               |                      |                     | 5 V      | 14.5 |      |

## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**图 7-1. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SN74LV175A device is an octal D-type flip-flop designed for 2 V to 5.5 V  $V_{CC}$  operation.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

This device is a positive-edge-triggered flip-flop with direct clear ( $\overline{CLR}$ ) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV175A device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### 8.2 Functional Block Diagram

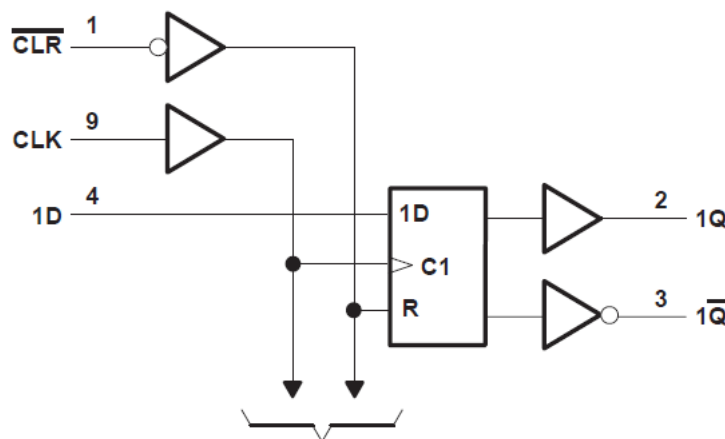


图 8-1. Logic Diagram (Positive Logic)

## 8.3 Feature Description

## 8.4 Device Functional Modes

表 8-1. Function Table

| INPUTS |     |   | OUTPUTS        |   |
|--------|-----|---|----------------|---|
| CLR    | CLK | D | Q <sub>0</sub> | Q |
| L      | X   | X | L              | H |
| H      | ↑   | H | H              | L |
| H      | ↑   | L | L              | H |
| H      | L   | X | Q <sub>0</sub> | Q |

## 9 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

The SN74LV175A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid  $V_{CC}$ . This feature makes it ideal for translating down to the  $V_{CC}$  level. Figure 9-2 shows the reduction in ringing compared to higher drive parts such as the AC or LVC families of logic parts.

### 9.2 Typical Application

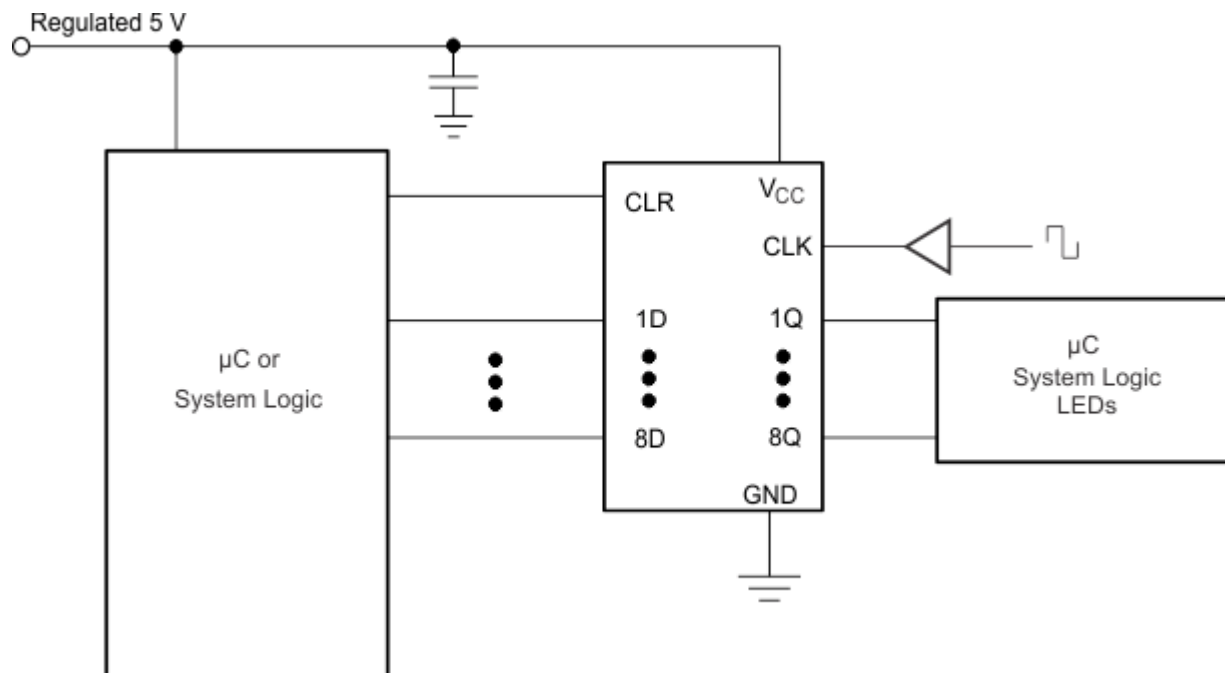


图 9-1. Typical Application Schematic

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV175A to one or more of the receiving devices.

3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Recommended Operating Conditions table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1  $\mu F$  capacitor is recommended. If there are multiple  $V_{CC}$  terminals then 0.01  $\mu F$  or 0.022  $\mu F$  capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1  $\mu F$  and 1.0  $\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

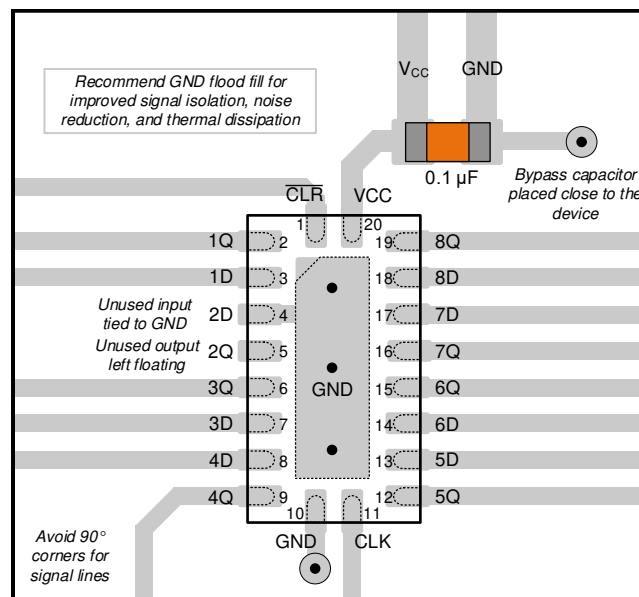
### 9.4 Layout

#### 9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in the Layout Example for SN74LV175A are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver.

##### 9.4.1.1 Layout Example



**图 9-2. Layout Example for SN74LV175A**

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application report](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application report](#)

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.4 Trademarks

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### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV175ADGVR   | ACTIVE        | TVSOP        | DGV                | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LV175A                  | <a href="#">Samples</a> |
| SN74LV175ADR     | ACTIVE        | SOIC         | D                  | 16   | 2500           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | LV175A                  | <a href="#">Samples</a> |
| SN74LV175ANSR    | ACTIVE        | SO           | NS                 | 16   | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | 74LV175A                | <a href="#">Samples</a> |
| SN74LV175APWR    | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 85    | LV175A                  | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

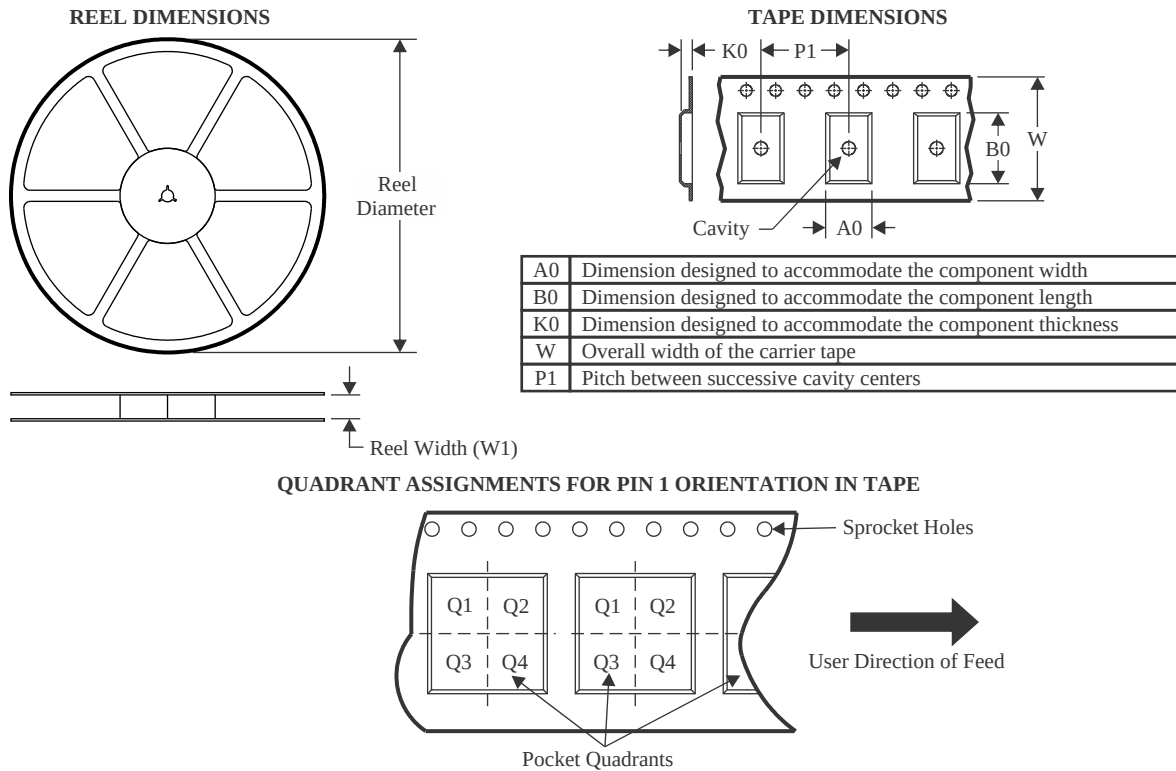
<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

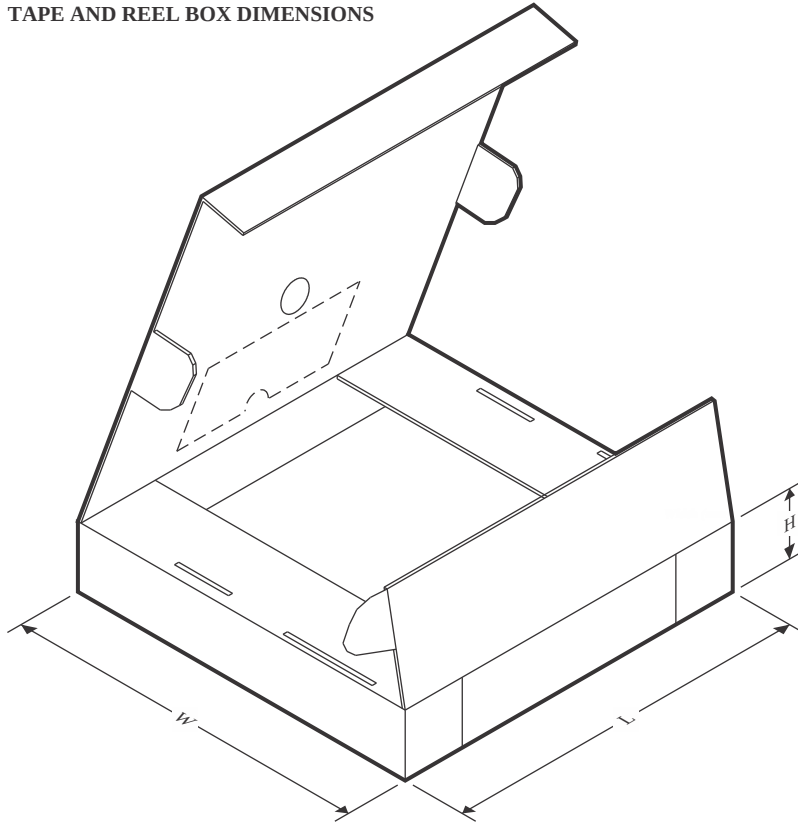
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

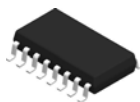
| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV175ADGVR | TVSOP        | DGV             | 16   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV175ADR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LV175ANSR  | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV175APWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV175APWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.85    | 5.45    | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV175APWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV175ADGVR | TVSOP        | DGV             | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV175ADR   | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| SN74LV175ANSR  | SO           | NS              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV175APWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LV175APWR  | TSSOP        | PW              | 16   | 2000 | 366.0       | 364.0      | 50.0        |
| SN74LV175APWR  | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |

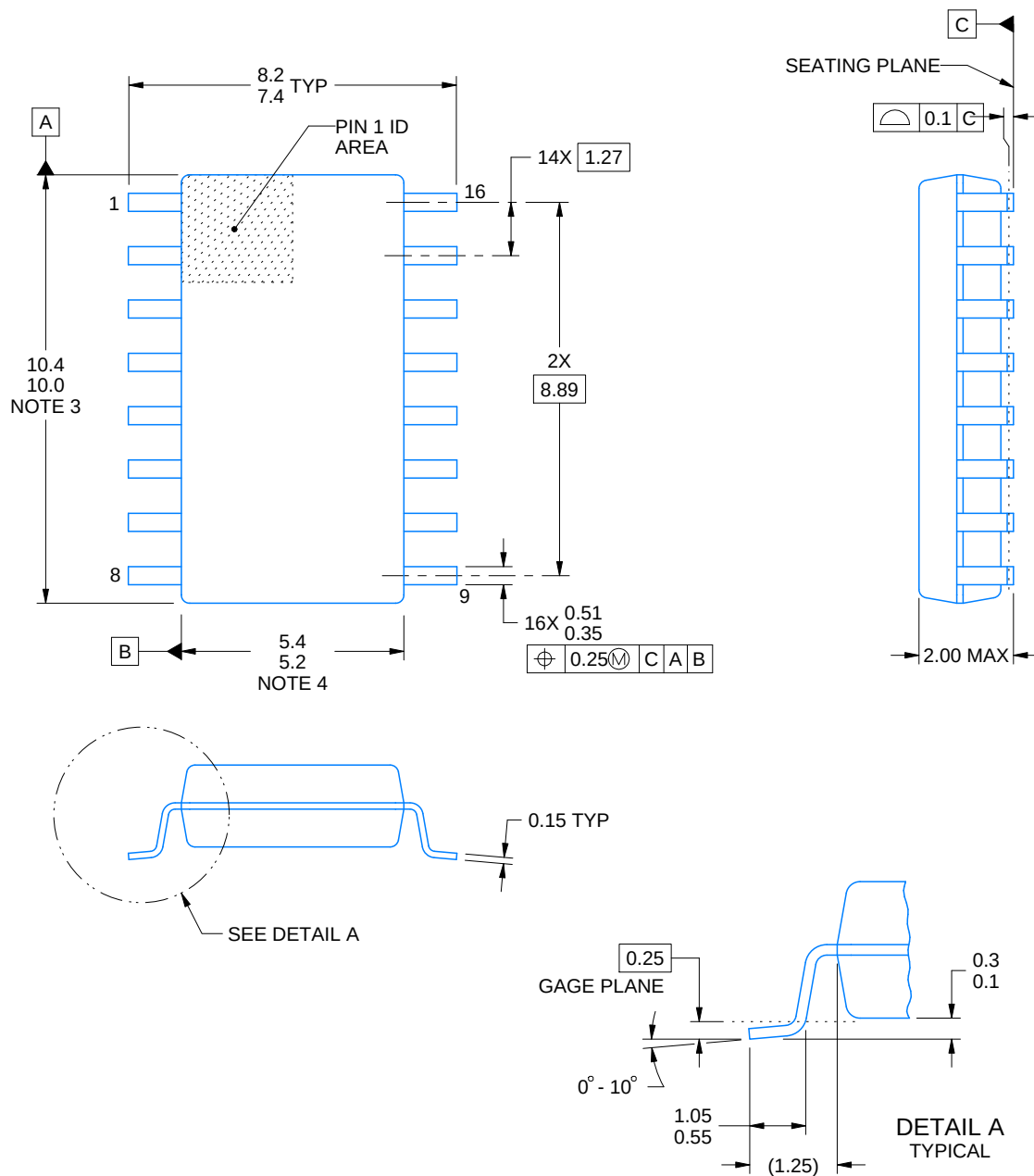


# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

## NOTES:

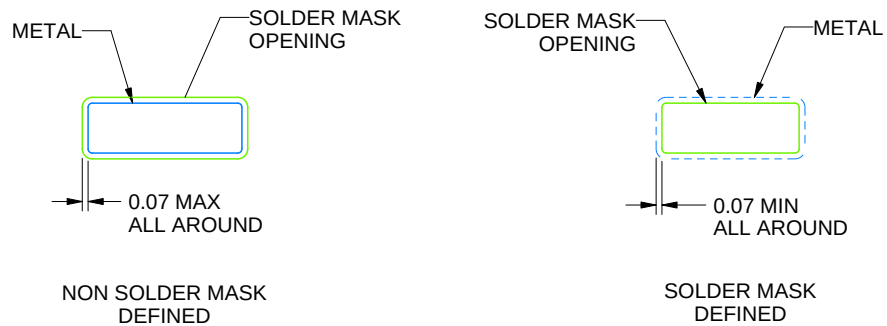
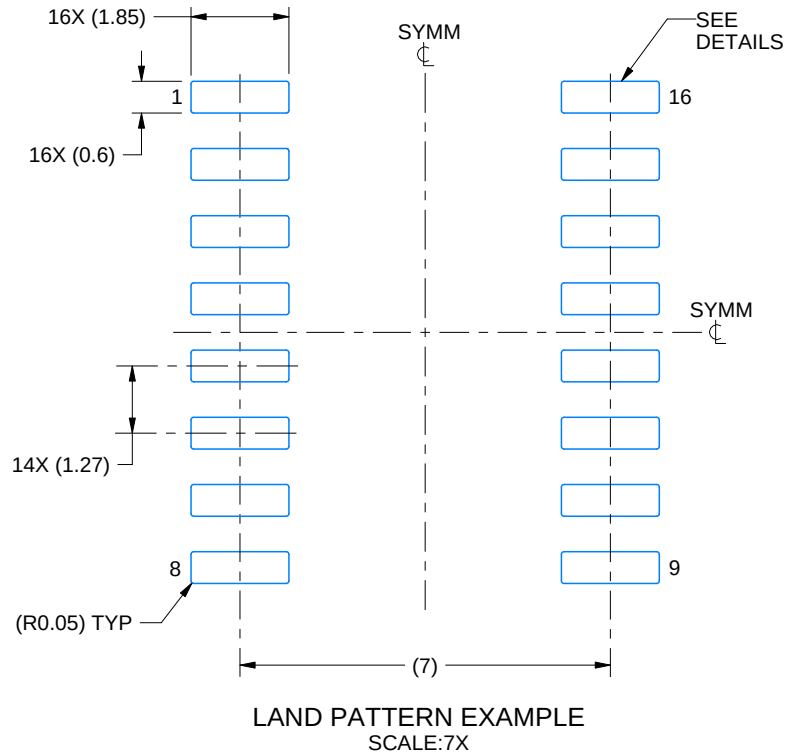
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP

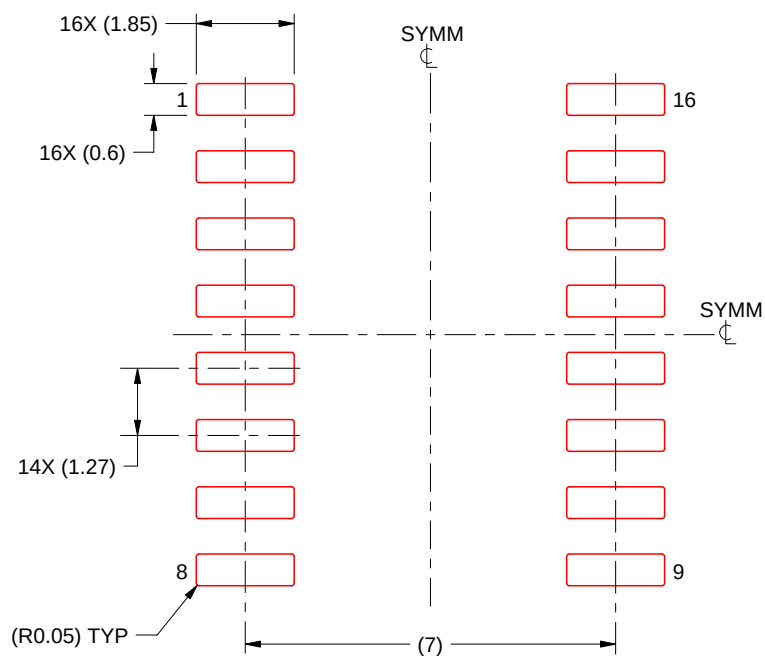


4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:7X

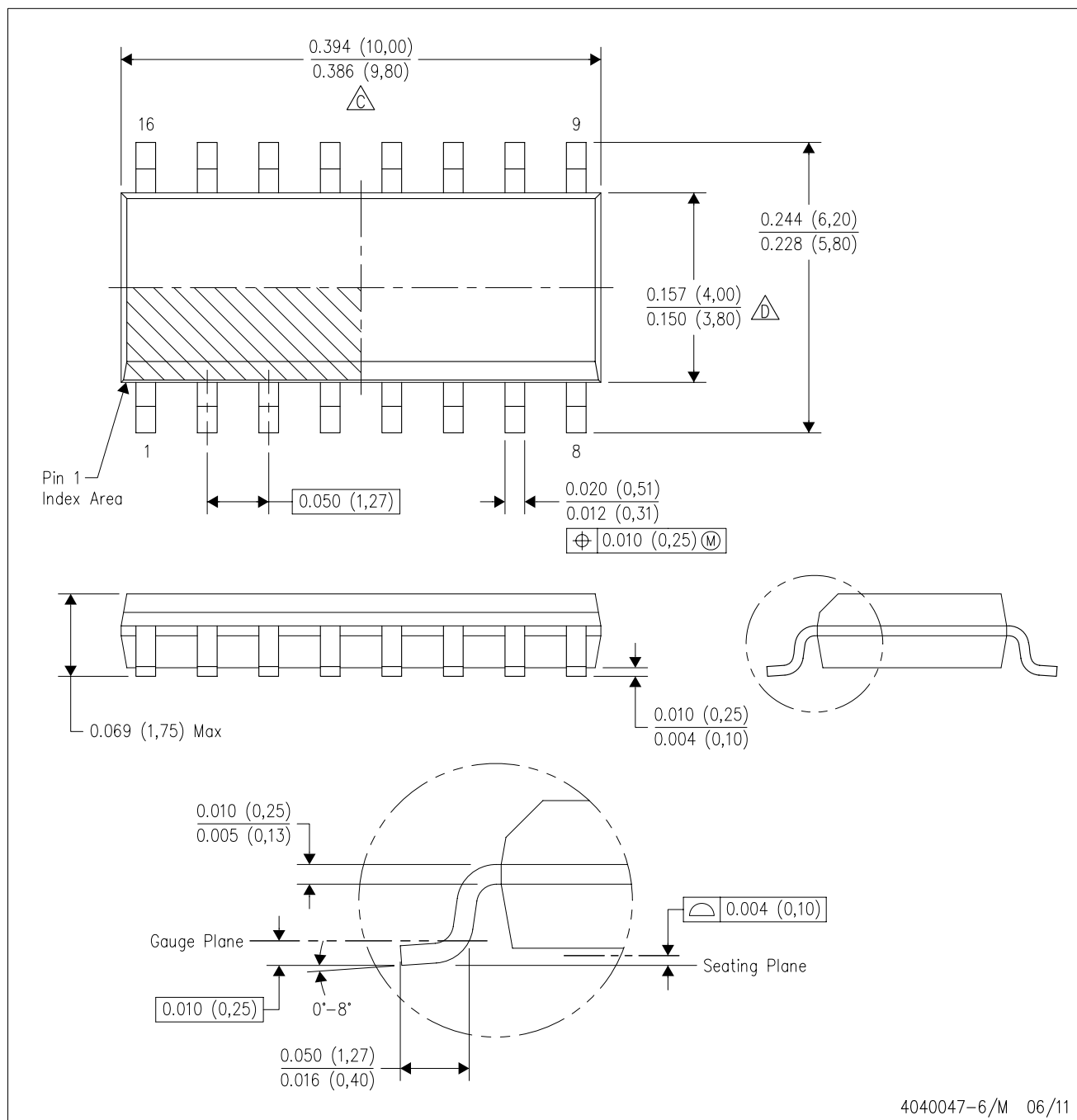
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

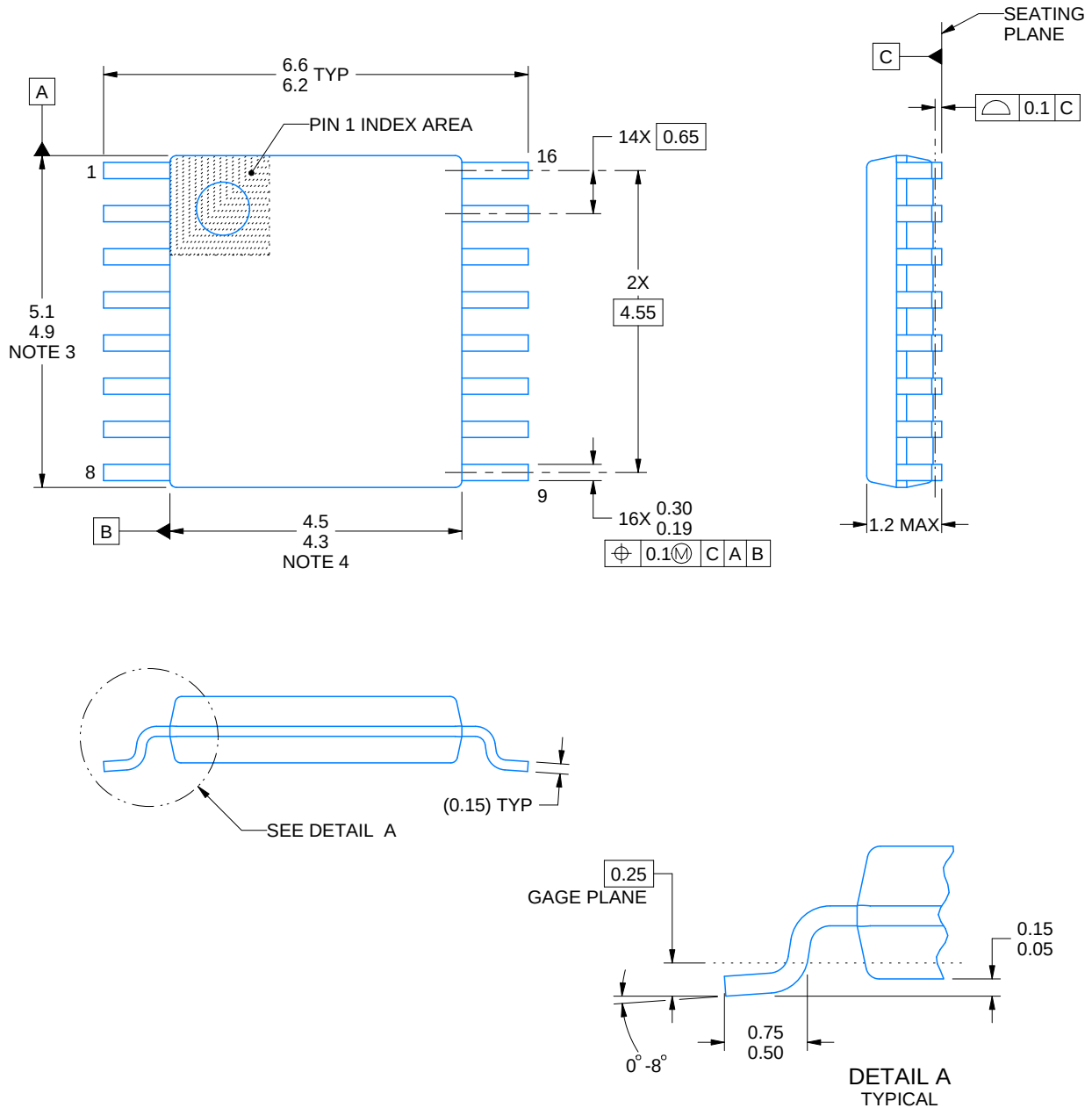
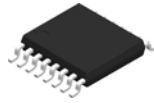
PLASTIC SMALL OUTLINE



4040047-6/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

## NOTES:

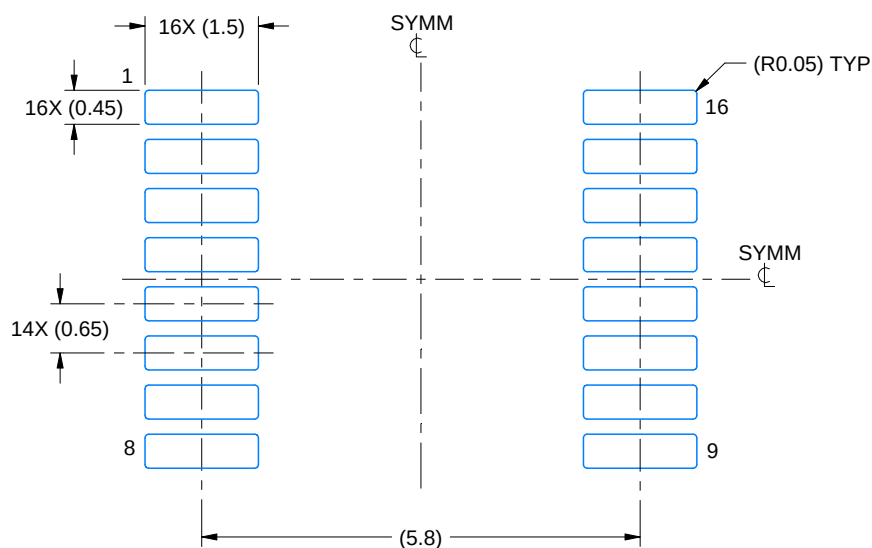
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

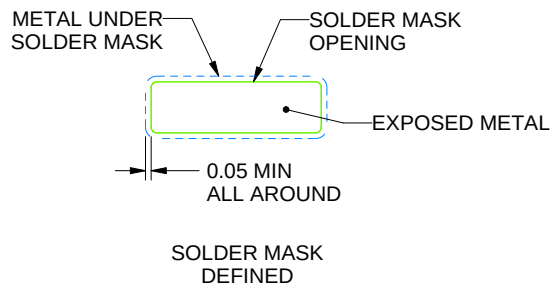
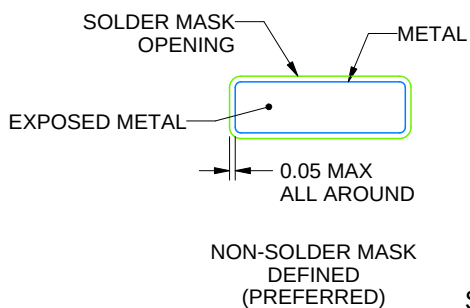
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

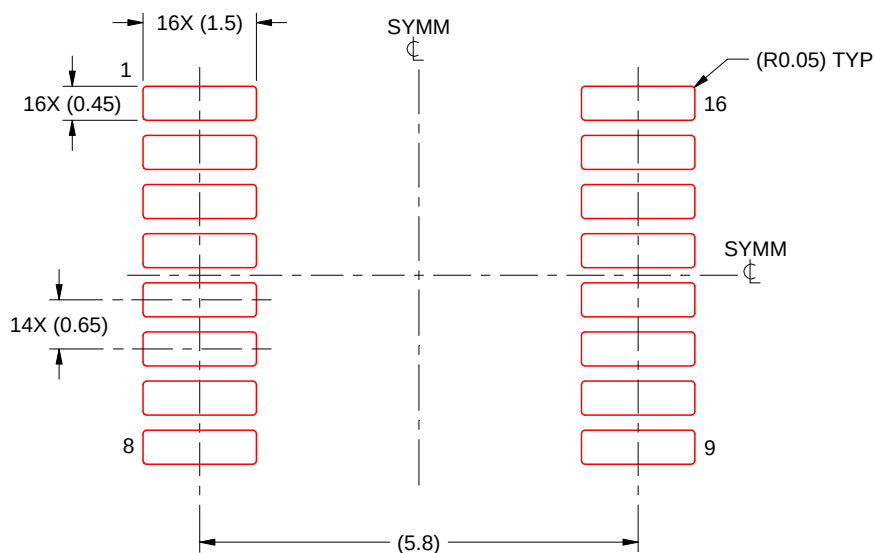
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

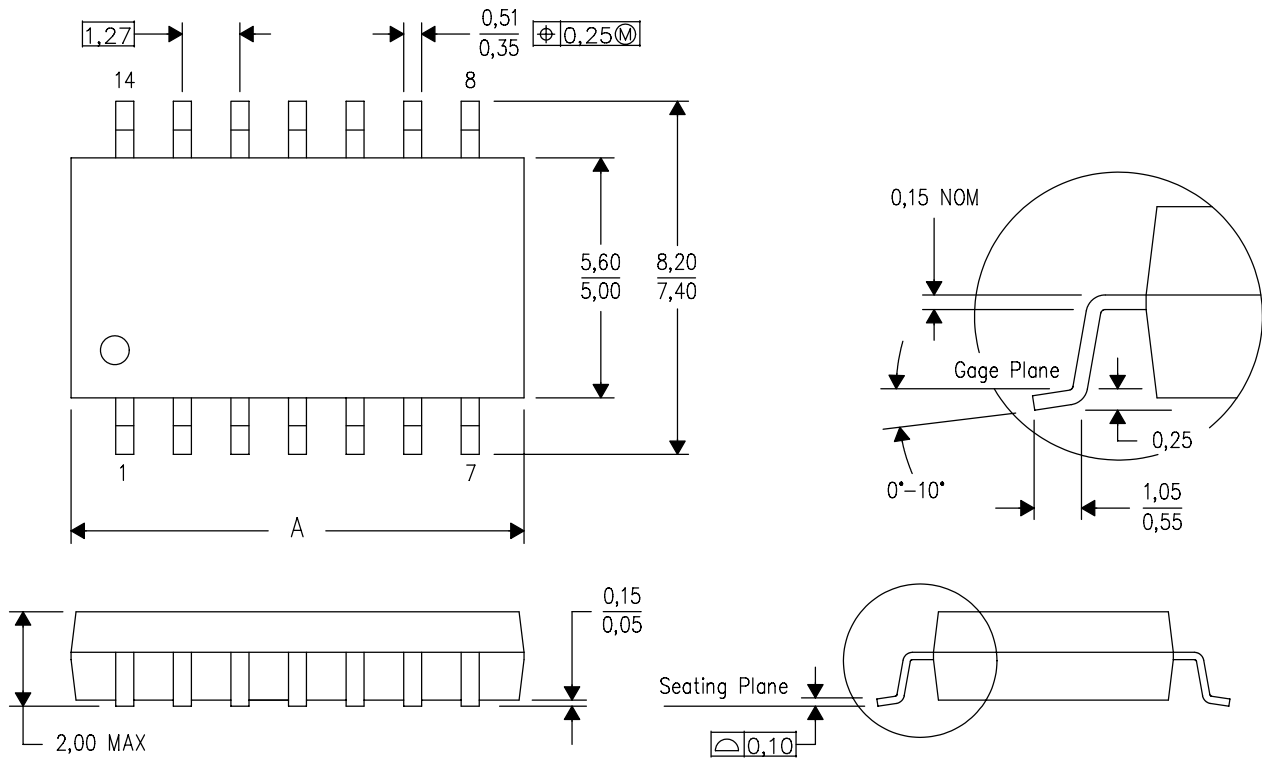
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

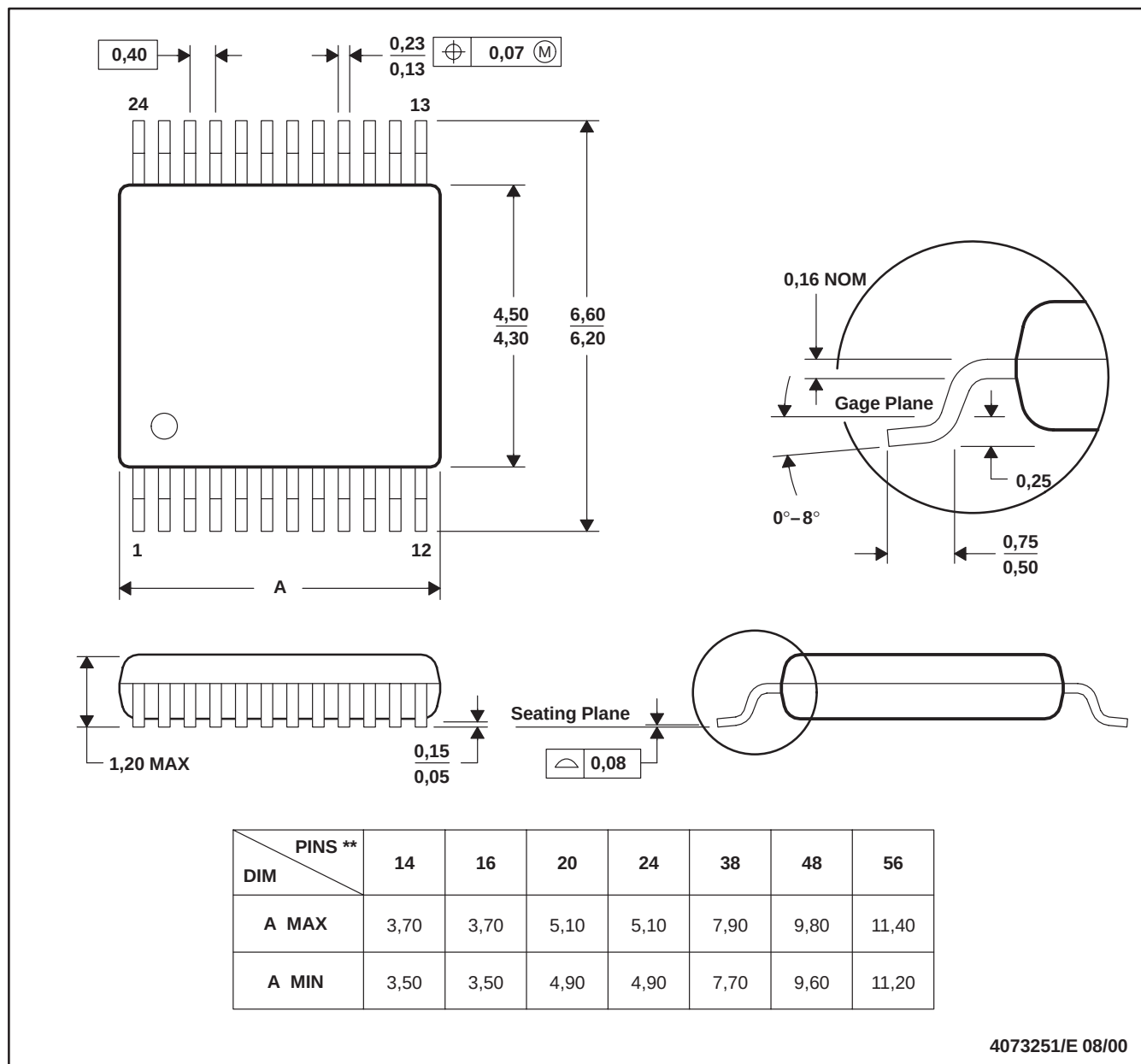
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

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