

CD74AC14 六路施密特触发反相器

1 特性

- 工作电压为 1.5V 至 5.5V，并在电源电压的 30% 时具有平衡的噪声抗扰度
- 双极 F、AS 和 S 的速度，同时功耗显著降低
- 比标准反相器具有更高的噪声抗扰度
- 工作时的压摆率比标准输入上升和下降压摆率慢得多
- 平衡传播延迟
- $\pm 24\text{mA}$ 输出驱动电流 - 扇出至 15 个 F 器件
- 防 SCR 门锁 CMOS 工艺和电路设计

2 说明

CD74AC14 包含六个独立的反相器。

封装信息

器件型号	封装 1	封装尺寸 (标称值)
CD74AC14	D (SOIC, 14)	9.9mm x 3.9mm
	N (PDIP, 14)	20.32 mm x 12.7 mm

- 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图



Table of Contents

1 特性	1	5.4 Electrical Characteristics.....	5
2 说明	1	5.5 Switching Characteristics.....	5
3 Revision History	2	5.6 Operating Characteristics.....	5
4 Pin Configuration and Functions	3	6 Parameter Measurement Information	6
5 Specifications	4	7 Detailed Description	7
5.1 Absolute Maximum Ratings.....	4	7.1 Overview.....	7
5.2 Recommended Operating Conditions.....	4	7.2 Functional Block Diagram.....	7
5.3 Thermal Information.....	4	7.3 Device Functional Modes.....	7

3 Revision History

Changes from Revision B (March 2004) to Revision C (May 2023)	Page
• 添加了封装信息表、引脚功能表和热性能信息表.....	1

4 Pin Configuration and Functions

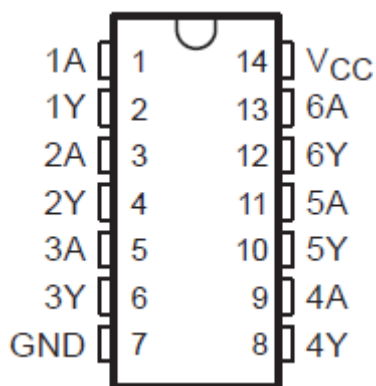


图 4-1. E or M Package Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1Y	2	Output	Channel 1, Output Y
2A	3	Input	Channel 2, Input A
2Y	4	Output	Channel 2, Output Y
3A	5	Input	Channel 3, Input A
3Y	6	Output	Channel 3, Output Y
GND	7	—	Ground
4Y	8	Output	Channel 4, Output Y
4A	9	Input	Channel 4, Input A
5Y	10	Output	Channel 5, Output Y
5A	11	Input	Channel 5, Input A
6Y	12	Output	Channel 6, Output Y
6A	13	Input	Channel 6, Input A
V _{CC}	14	—	Positive Supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6	V
I _{IK}	Input clamp current	(V _I < 0 or V _I > V _{CC}) ¹		±20 mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC}) ¹		±50 mA
	Continuous output current	(V _O = 0 to V _{CC})		±50 mA
	Continuous current through V _{CC} or GND			±100 mA
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		T _A = 25°C		– 55°C to 125°C		– 40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 4.5 V to 5.5 V		– 24		– 24		mA
I _{OL}	Low-level output current	V _{CC} = 4.5 V to 5.5 V		24		24		mA

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		CD74AC14		UNIT
		E	M	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	80	86	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	TA = 25°C		– 55°C to 125°C		– 40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{T+} Positive-going threshold		5 V	2.6	3.4	2.6	3.4	2.6	3.4	V
V _{T–} Negative-going threshold		5 V	1.6	2.4	1.6	2.4	1.6	2.4	V
ΔVT Hysteresis (V _{T+} – V _{T–})		5 V	0.5		0.5		0.5		V
V _{OH}	V _I = V _{T+}	I _{OH} = –50 μA	1.5 V	1.4	1.4		1.4		V
			3 V	2.9	2.9		2.9		
			4.5 V	4.4	4.4		4.4		
		I _{OH} = –4 mA	3 V	2.58	2.4		2.48		
		I _{OH} = –24 mA	4.5 V	3.94	3.7		3.8		
		I _{OH} = –50 mA ¹	5.5 V		3.85				
		I _{OH} = –75 mA ¹	5.5 V				3.85		
V _{OL}	V _I = V _{T–}	I _{OL} = 50 μA	1.5 V	0.1	0.1		0.1		V
			3 V	0.1	0.1		0.1		
			4.5 V	0.1	0.1		0.1		
		I _{OL} = 12 mA	3 V	0.36	0.5		0.44		
		I _{OL} = 24 mA	4.5 V	0.36	0.5		0.44		
		I _{OL} = 50 mA ¹	5.5 V		1.65				
		I _{OL} = 75 mA ¹	5.5 V						
I _I	V _I = V _{CC} or GND	5.5 V	± 0.1		± 0.1		± 0.1		μA
I _{CC}	V _I = V _{CC} or GND I _O = 0	5.5 V	4		80		40		μA
C _i			10		10		10		pF

- Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

5.5 Switching Characteristics

over operating free-air temperature range V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted)

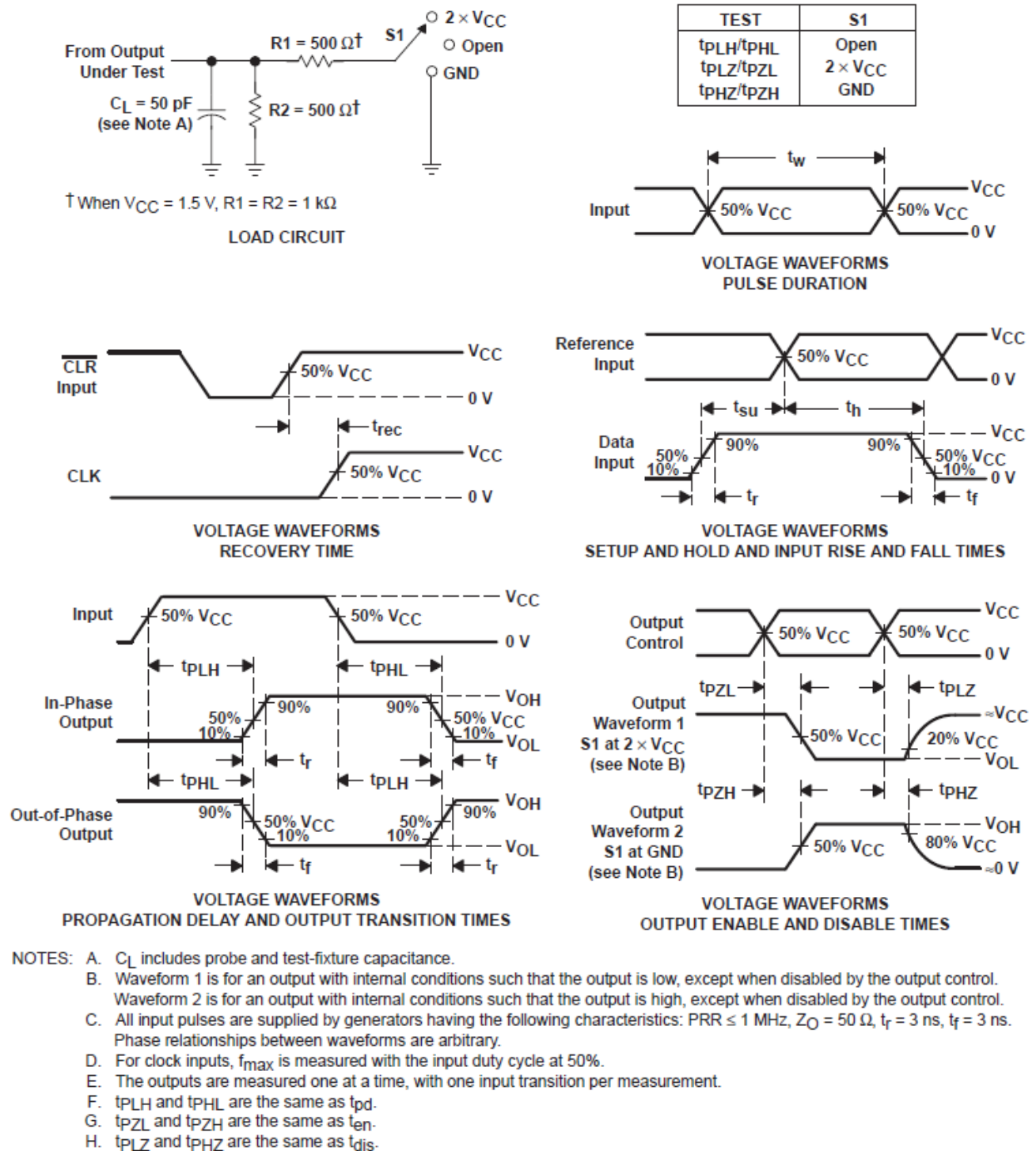
PARAMETER	FROM (INPUT)	TO (OUTPUT)	– 55°C TO 125°C		– 40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	2.6	10.5	2.7	9.5	ns
t _{PHL}			2.6	10.5	2.7	9.5	

5.6 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TYP	UNIT
C _{pd}	Power dissipation capacitance	45	pF

6 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time, with one input transition per measurement.
 - F. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

图 6-1.

7 Detailed Description

7.1 Overview

The CD74AC14 device performs the Boolean function $Y = \bar{A}$. Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

7.2 Functional Block Diagram



图 7-1. Logic Diagram, Each Inverter (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table (Each Inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74AC14E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC14E	Samples
CD74AC14EE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC14E	Samples
CD74AC14M	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	AC14M	
CD74AC14M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC14M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

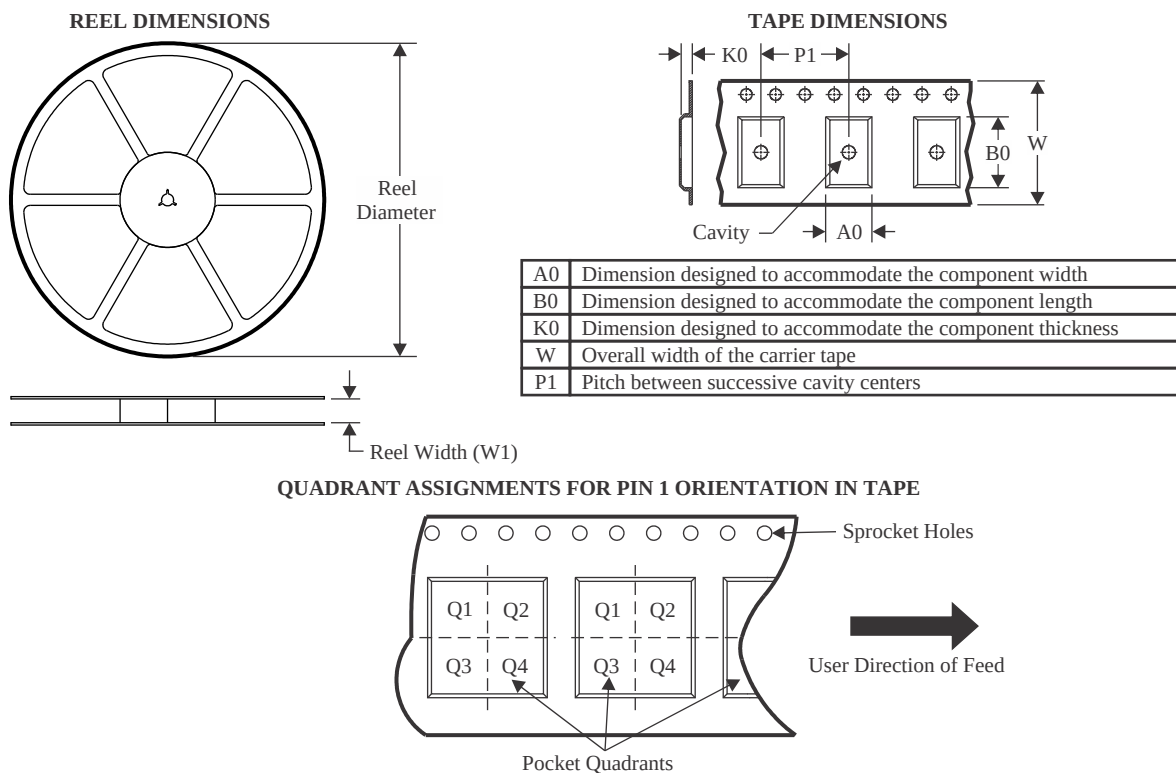
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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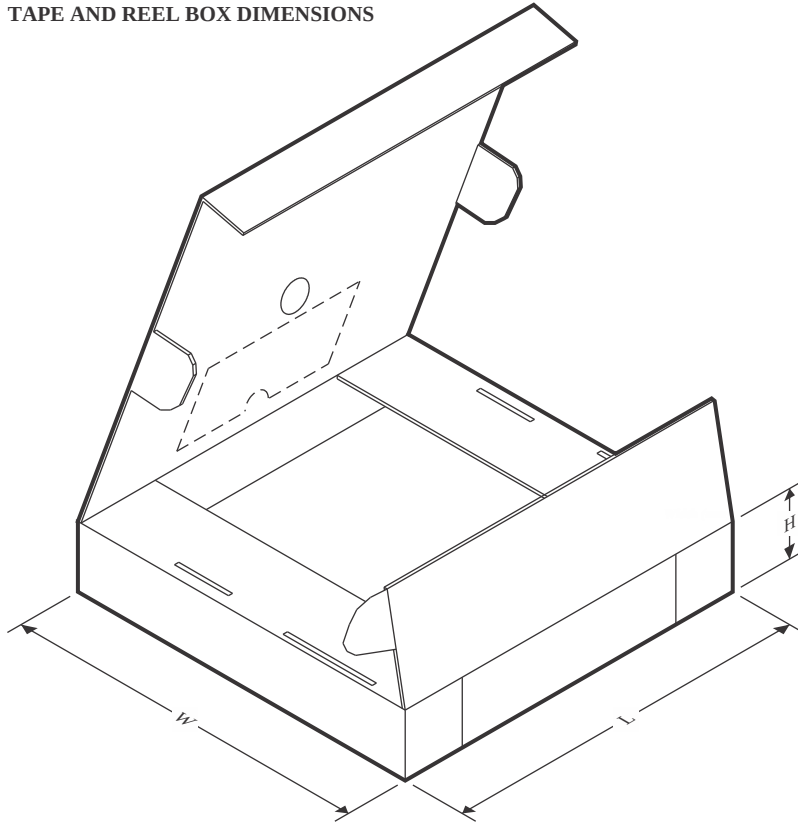
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC14M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

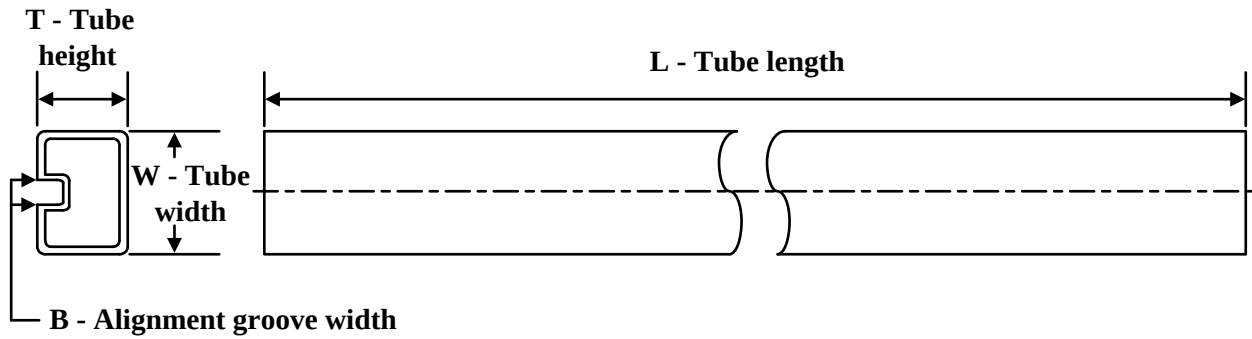
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC14M96	SOIC	D	14	2500	356.0	356.0	35.0

TUBE

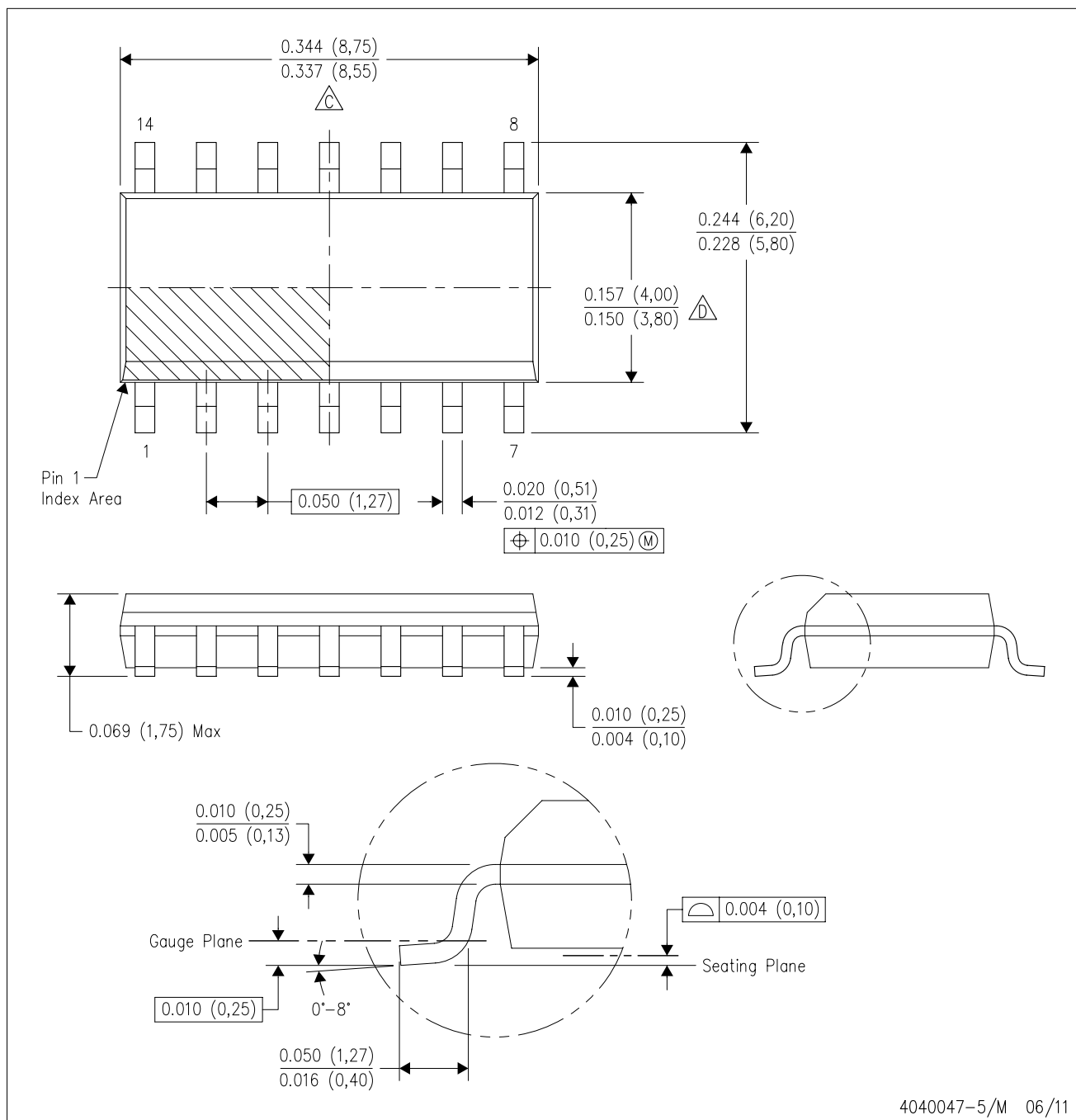


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74AC14E	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC14E	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC14EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC14EE4	N	PDIP	14	25	506	13.97	11230	4.32

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



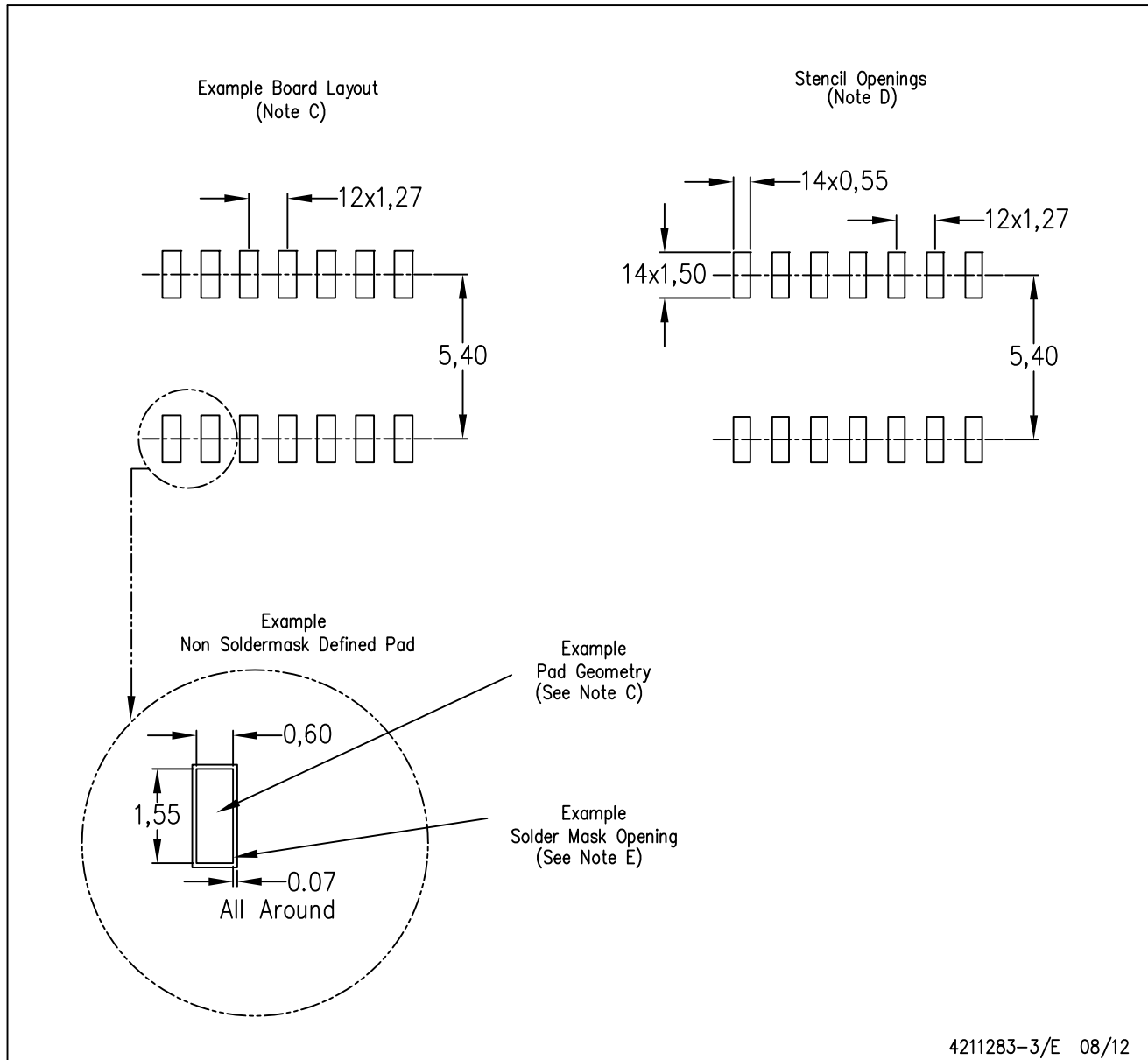
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

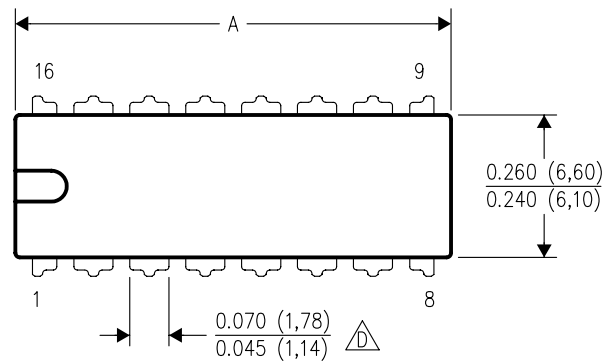


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

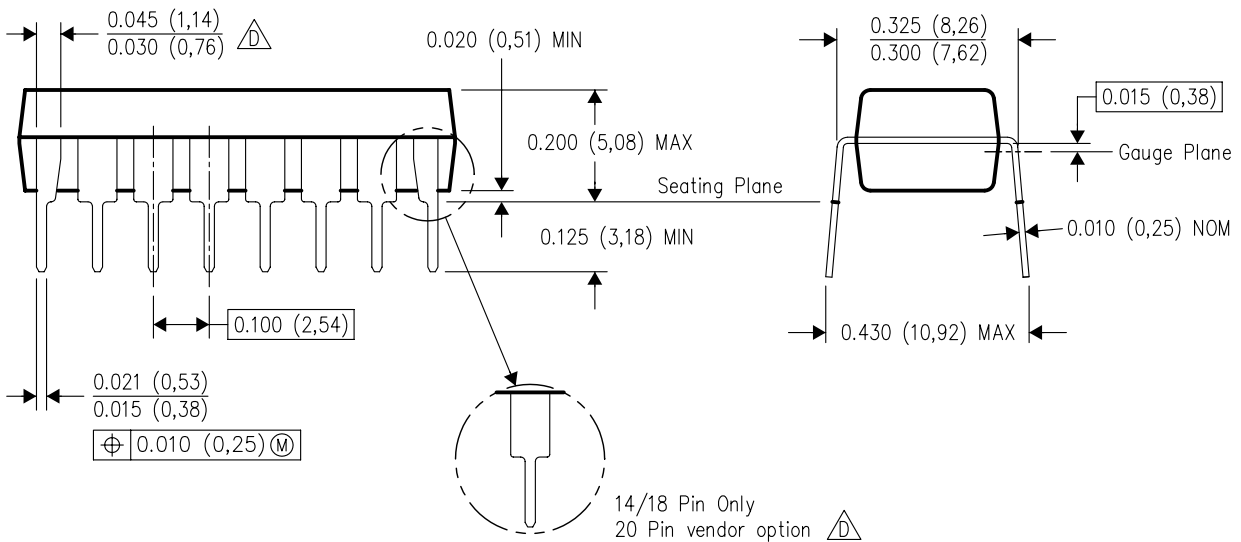
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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