

CDx4ACT04 六路反相器

1 特性

- 输入兼容 TTL 电压
- 双极 F、AS 和 S 的速度，同时功耗显著降低
- 平衡传播延迟
- $\pm 24\text{mA}$ 输出驱动电流
 - 扇出至 15 个 F 器件
- 防 SCR 闩锁 CMOS 工艺和电路设计
- ESD 保护超过 2kV (根据 MIL-STD-883 方法 3015)

2 说明

'ACT04 器件包含六个独立的反相器。这些器件执行布尔函数 $Y = \overline{A}$ 。

封装信息

器件型号	封装 ¹	封装尺寸 (标称值)
CD54ACT04	J (CDIP , 14)	19.56 mm x 6.67 mm
CDx4ACT04	D (SOIC , 14)	9.9mm x 3.9mm
	N (PDIP , 14)	20.32 mm x 12.7 mm

1. 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图，每个反相器 (正逻辑)

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3 Revision History

Changes from Revision B (June 2002) to Revision C (May 2023)	Page
• 添加了封装信息表、引脚功能表和热性能信息表.....	1

4 Pin Configuration and Functions

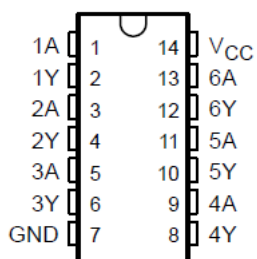


图 4-1. CD54ACT04 F Package, CD74ACT04 E or M Package (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1Y	2	Output	Channel 1, Output Y
2A	3	Input	Channel 2, Input A
2Y	4	Output	Channel 2, Output Y
3A	5	Input	Channel 3, Input A
3Y	6	Output	Channel 3, Output Y
GND	7	—	Ground
4Y	8	Output	Channel 4, Output Y
4A	9	Input	Channel 4, Input A
5Y	10	Output	Channel 5, Output Y
5A	11	Input	Channel 5, Input A
6Y	12	Output	Channel 6, Output Y
6A	13	Input	Channel 6, Input A
V _{CC}	14	—	Positive Supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ¹

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	6	V
I _{IK}	Input clamp current (V _I < 0 or V _I > V _{CC}) ¹		±20	mA
I _{OK}	Output clamp current (V _O < 0 or V _O > V _{CC}) ¹		±50	mA
I _O	Continuous output current (V _O = 0 to V _{CC})		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _{stg}	Storage temperature	-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) ¹

		T _A = 25°C		- 40°C to 85°C		- 55°C to 125°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		2		V
V _{IL}	Low-level input voltage		0.8		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		- 24		- 24		- 24	mA
I _{OL}	Low-level output current		24		24		24	mA
Δt/Δv	Inputut transition rise or fall rate		10		10		10	ns/V

- All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾	CDx4ACT04		UNIT
	E	M	
	14 PINS	14 PINS	
R _{θJA} Junction-to-ambient thermal resistance	80	86	°C/W

- For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	TA = 25°C		– 40°C to 85°C		– 55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –50 µA	4.5 V	4.4	4.4		4.4		V
		I _{OH} = –24 mA	4.5 V	3.94	3.8		3.7		
		I _{OH} = –50 mA ¹	5.5 V				3.85		
		I _{OH} = –75 mA ¹	5.5 V		3.85				
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 µA	4.5 V	0.1	0.1		0.1		V
		I _{OL} = 24 mA	4.5 V	0.36	0.44		0.5		
		I _{OL} = 50 mA ¹	5.5 V				1.65		
		I _{OL} = 75 mA ¹	5.5 V		1.65				
I _I	V _I = V _{CC} or GND	5.5 V		± 0.1	± 0.1		± 0.1		µA
I _{CC}	V _I = V _{CC} or GND I _O = 0	5.5 V		4	40		80		µA
ΔI _{CC}	V _I = V _{CC} – 2.1 V	4.5 V to 5.5 V		2.4	2.8		3		mA
C _i				10	10		10		pF

- Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

表 5-1. Act Input Load Table

INPUT	UNIT LOAD
A	0.18

- Unit load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

5.5 Switching Characteristics

over operating free-air temperature range V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see [load circuit and voltage wave forms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	– 40°C TO 85°C		– 55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	2.4	8.5	2.3	9.3	ns
t _{PHL}			2.4	8.5	2.3	9.3	

5.6 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TYP	UNIT
C _{pd} Power dissipation capacitance	105	pF

6 Parameter Measurement Information

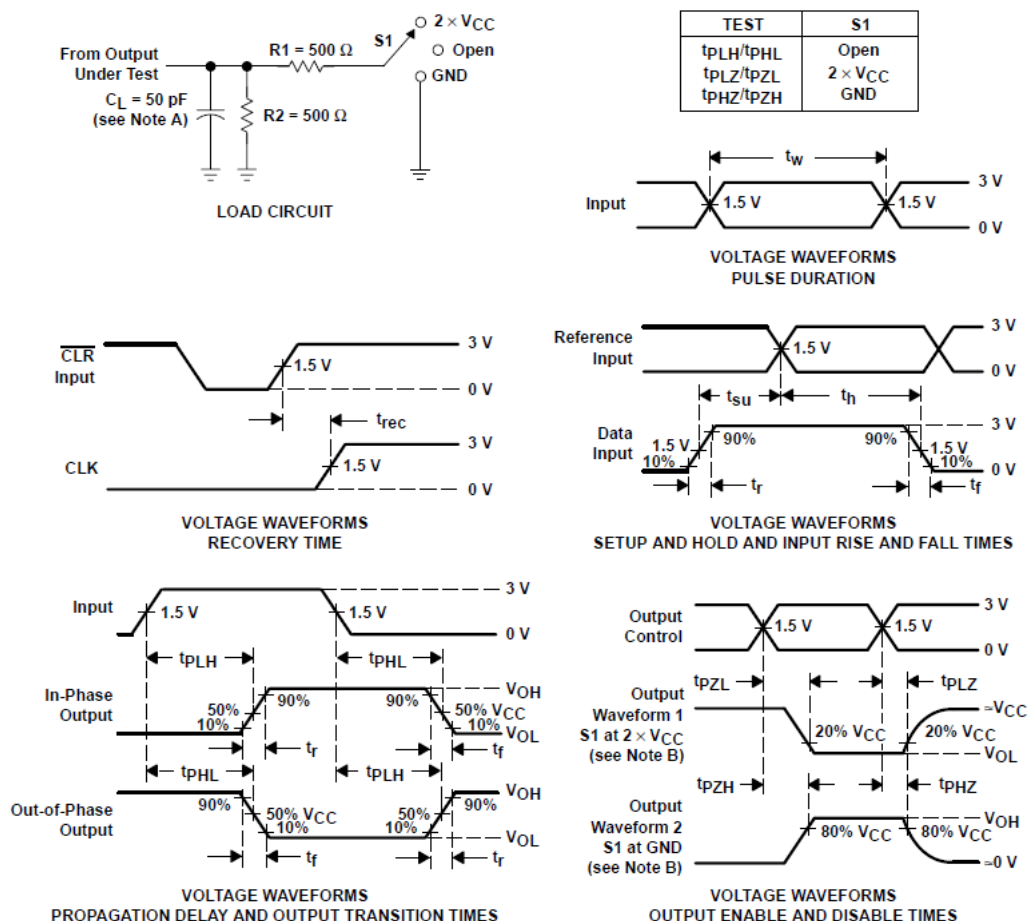


图 6-1.

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- The outputs are measured one at a time, with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PHL} and t_{PLH} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

7 Detailed Description

7.1 Functional Block Diagram

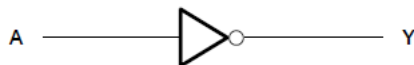


图 7-1. Logic Diagram, Each Inverter (Positive Logic)

7.2 Device Functional Modes

表 7-1. Function Table (Each Inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54ACT04	Click here	Click here	Click here	Click here	Click here
CD74ACT04	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.4 Trademarks

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8.5 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54ACT04F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54ACT04F3A	Samples
CD74ACT04E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT04E	Samples
CD74ACT04M	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	ACT04M	
CD74ACT04M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT04M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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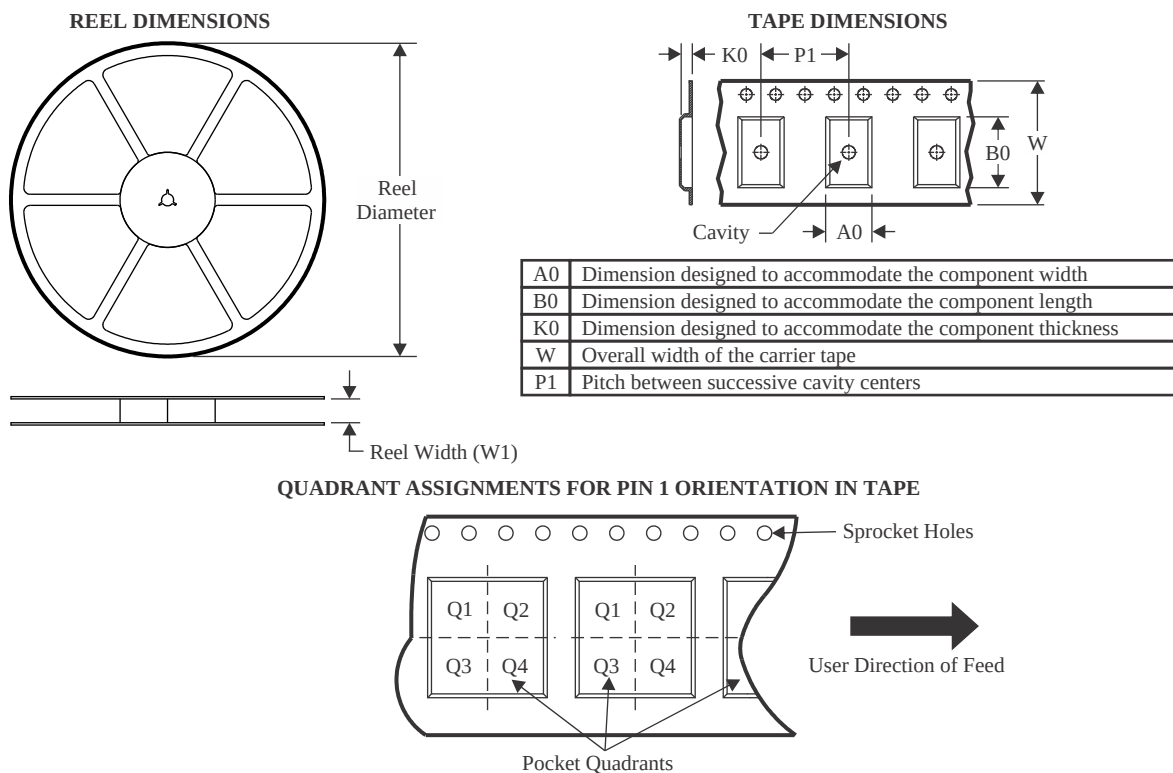
OTHER QUALIFIED VERSIONS OF CD54ACT04, CD74ACT04 :

- Catalog : [CD74ACT04](#)
- Military : [CD54ACT04](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

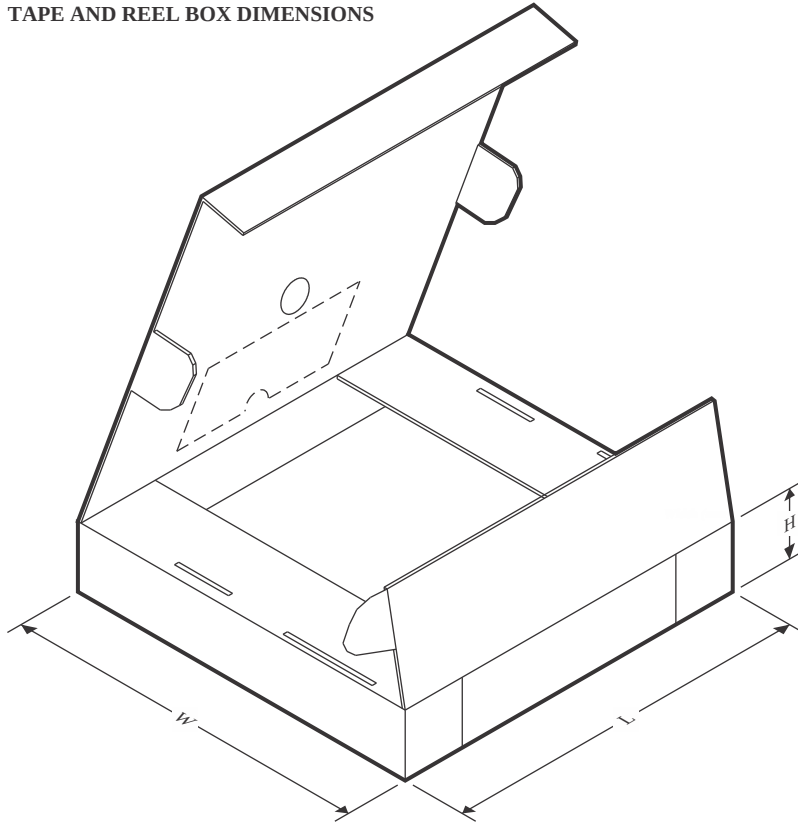
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT04M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

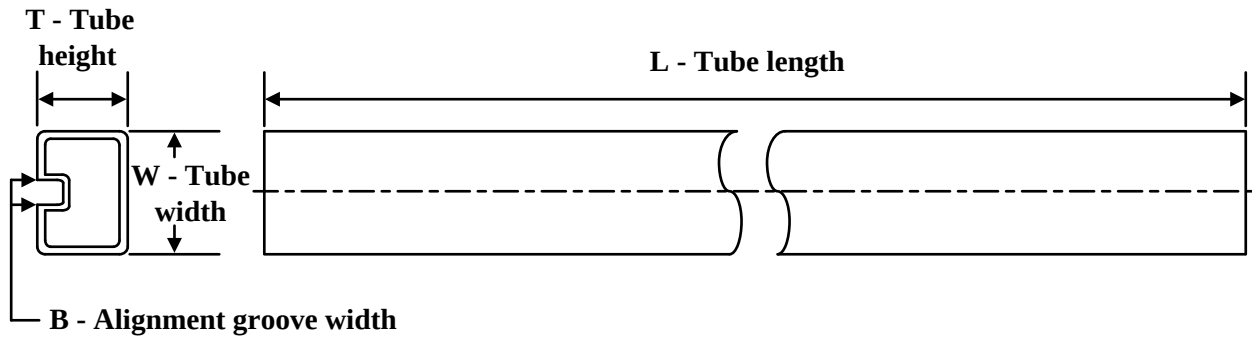
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT04M96	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

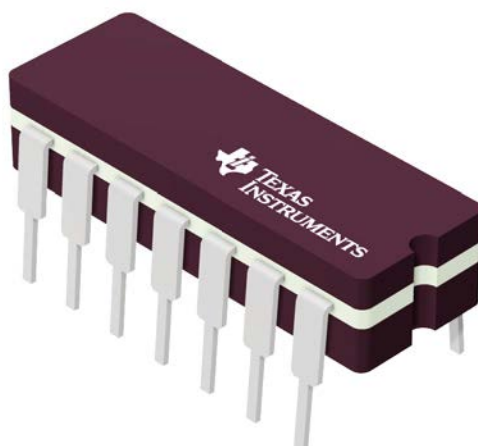
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74ACT04E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT04E	N	PDIP	14	25	506	13.97	11230	4.32

J 14

GENERIC PACKAGE VIEW

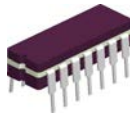
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

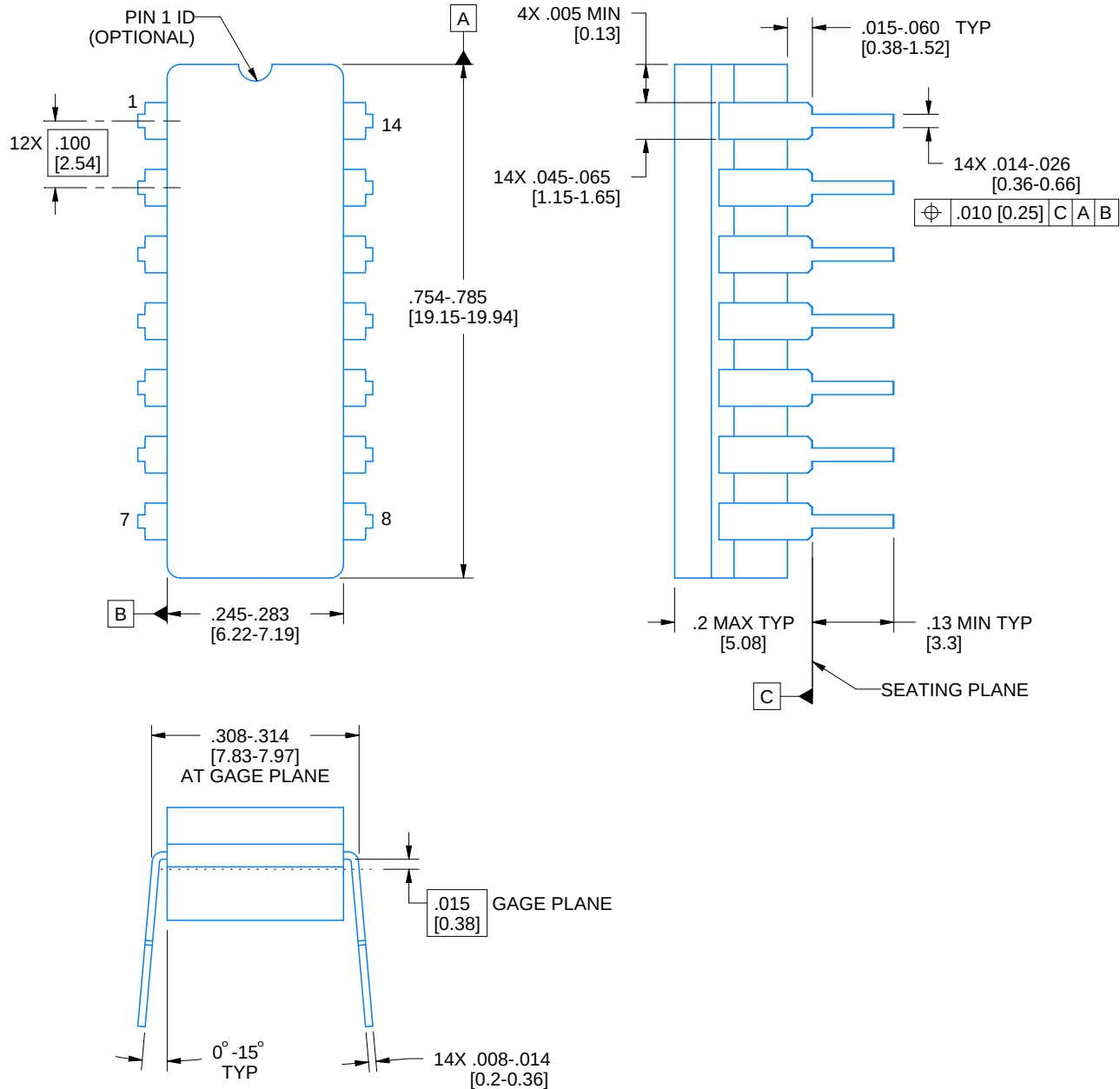


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

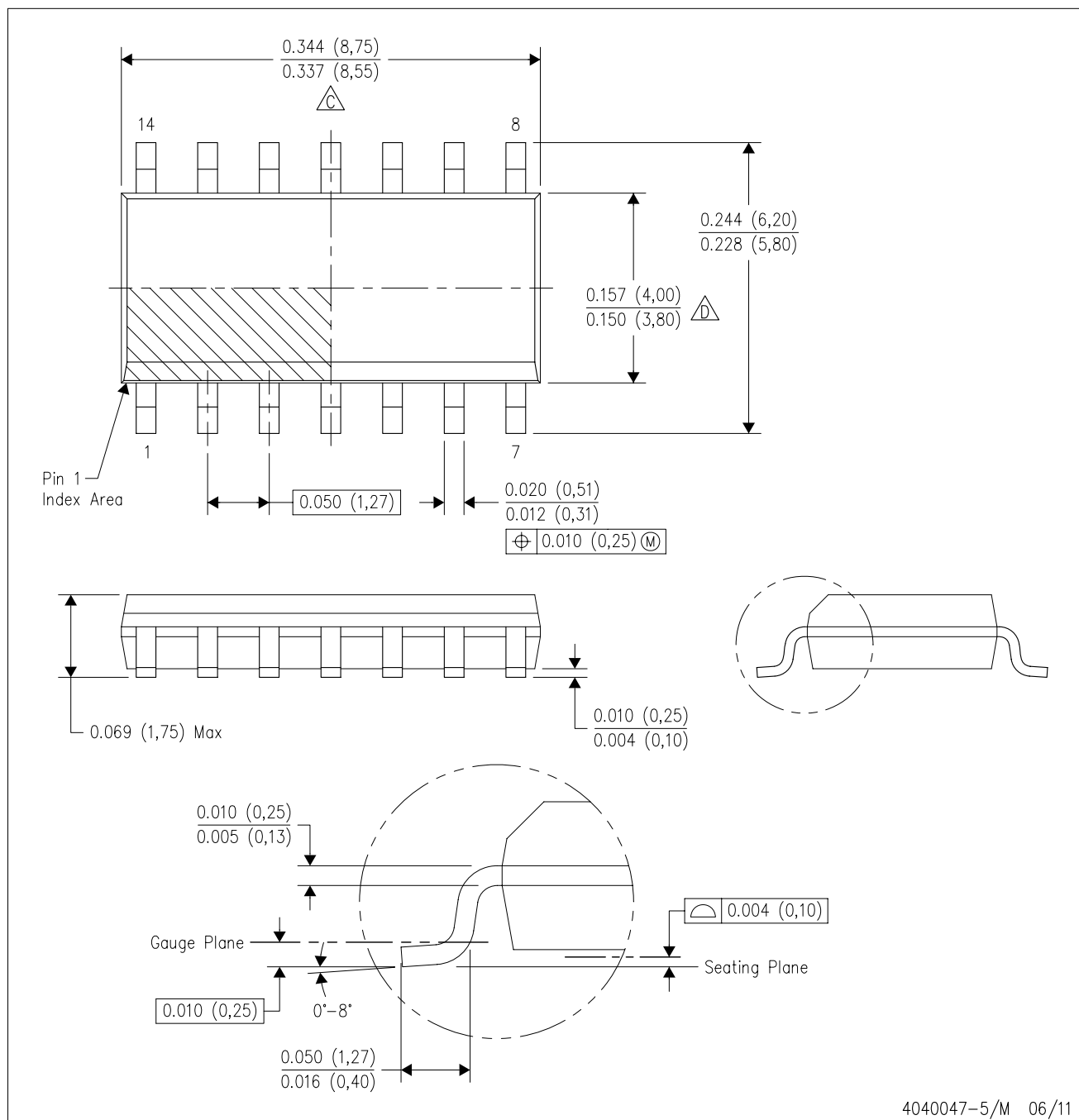
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



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D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

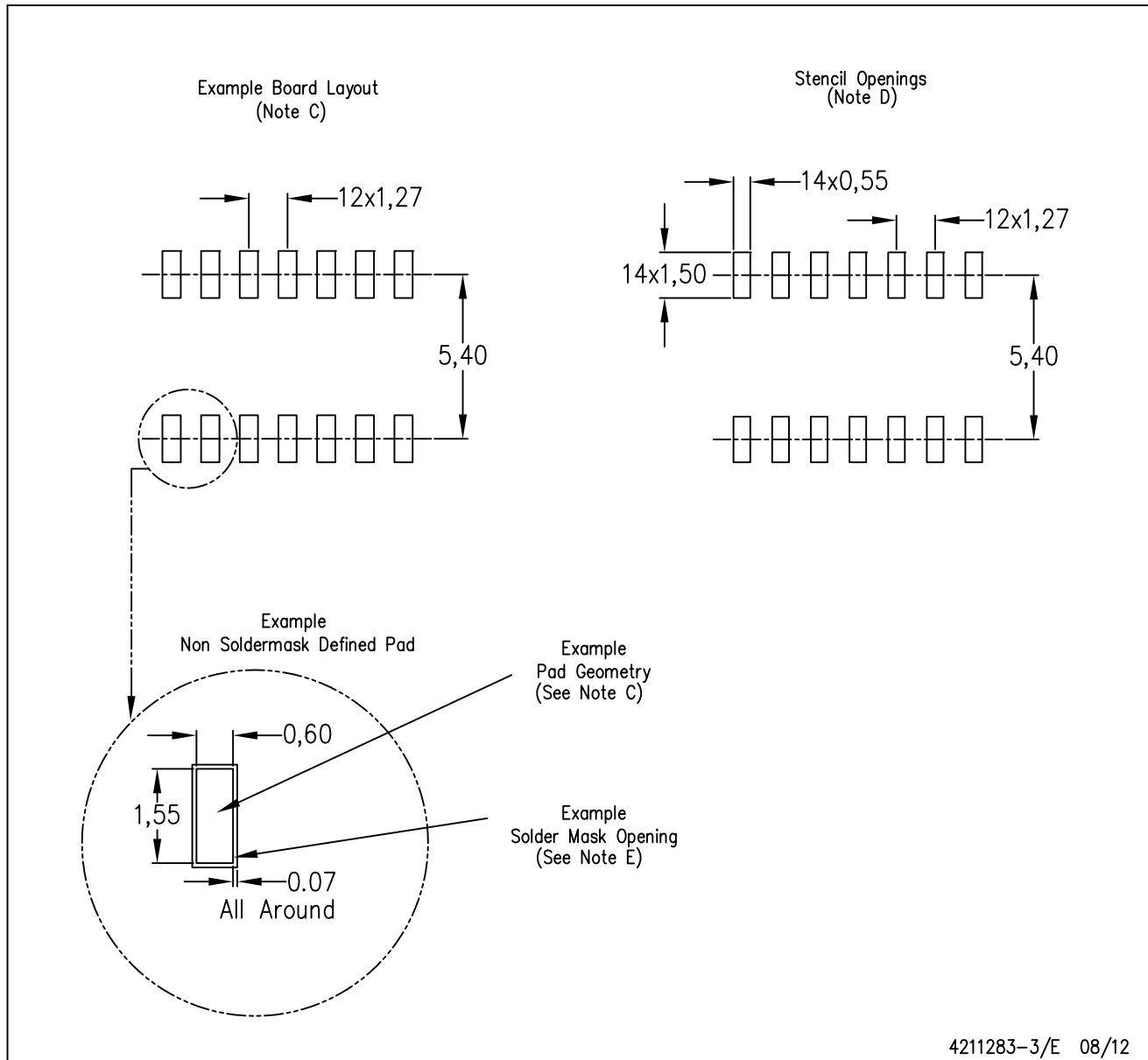


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

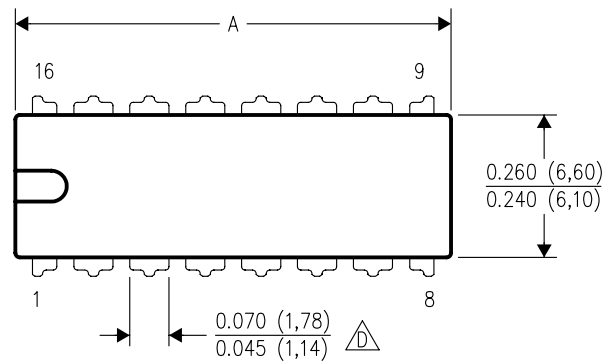


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

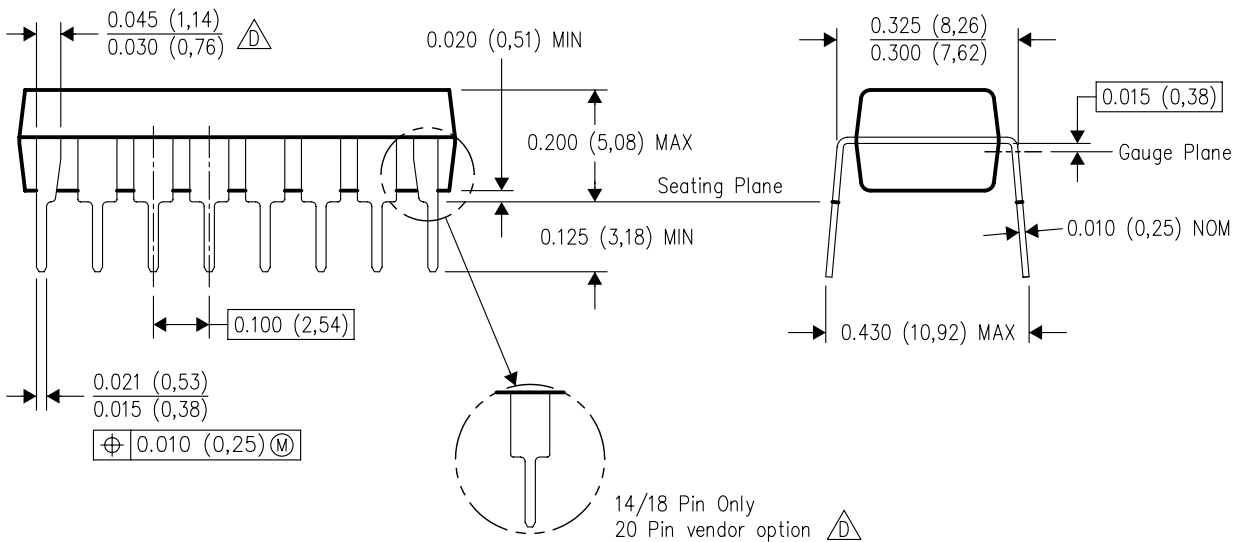
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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