

SNx4ACT573 具有三态输出的八路透明 D 类锁存器

1 特性

- 工作电压范围为 4.5V 至 5.5V V_{CC}
- 输入电压高达 5.5V
- 5V 时的 t_{pd} 最大值为 9.5ns
- 输入兼容 TTL 电压

2 应用

- 并行数据存储
- 数字总线缓冲器

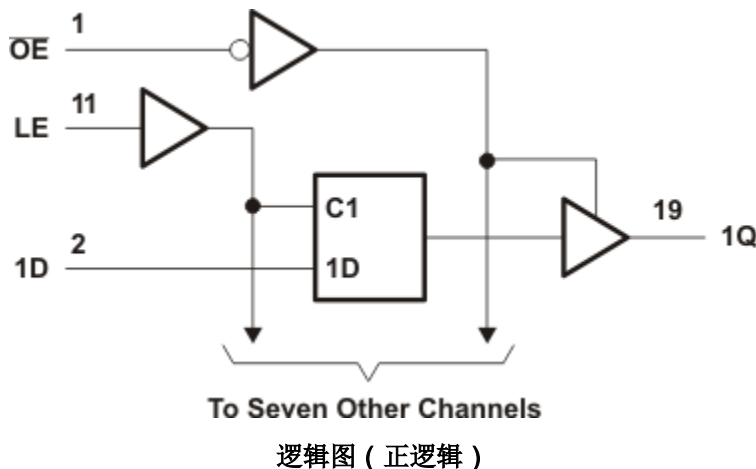
3 说明

这些 8 位锁存器具有专门设计用于驱动高电容或相对低阻抗负载的三态输出。这些器件特别适用于实现缓冲寄存器、I/O 端口、总线驱动器和寄存器。

器件信息

器件型号	等级	封装 ⁽¹⁾
SN54ACT573	军用	J (CDIP , 20)
		W (CFP , 20)
		FK (LCCC , 20)
SN74ACT573	目录	DB (SSOP , 20)
		DW (SOIC , 20)
		N (WQFN , 20)
		NS (SOP , 20)
		PW (TSSOP , 20)
		RKS (VQFN , 20)

(1) 如需了解更多信息，请参阅 节 11。



内容

1 特性.....	1	7.1 概述.....	9
2 应用.....	1	7.2 功能方框图.....	9
3 说明.....	1	7.3 器件功能模式.....	9
4 引脚配置和功能.....	3	8 应用和实施.....	10
5 规格.....	5	8.1 电源相关建议.....	10
5.1 绝对最大额定值.....	5	8.2 布局.....	10
5.2 建议运行条件.....	5	9 器件和文档支持.....	11
5.3 热性能信息.....	5	9.1 接收文档更新通知.....	11
5.4 电气特性.....	6	9.2 支持资源.....	11
5.5 时序要求.....	6	9.3 商标.....	11
5.6 开关特性.....	7	9.4 静电放电警告.....	11
5.7 工作特性.....	7	9.5 术语表.....	11
6 参数测量信息.....	8	10 修订历史记录.....	11
7 详细说明.....	9	11 机械、封装和可订购信息.....	11

4 引脚配置和功能

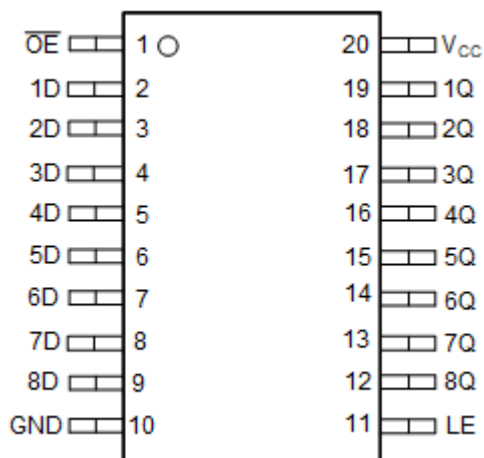


图 4-1. SN54ACT573 J 或 W 封装, SN74ACT573 DB、DW、N、NS 或 PW 封装 (顶视图)

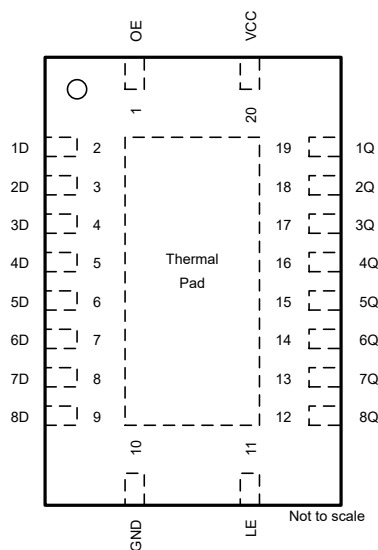


图 4-2. SNx4ACT573 RKS 封装, 20 引脚 VQFN (顶视图)

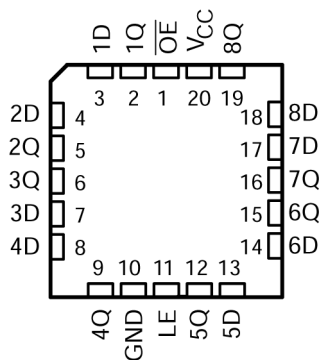


图 4-3. SN54ACT573 FK 封装, 20 引脚 LCCC (顶视图)

表 4-1. 引脚功能

引脚		类型 ⁽¹⁾	说明
名称	编号		
OE	1	I	输出使能测试点
1D	2	I	1D 输入
2D	3	I	2D 输入
3D	4	I	3D 输入
4D	5	I	4D 输入
5D	6	I	5D 输入
6D	7	I	6D 输入
7D	8	I	7D 输入
8D	9	I	8D 输入
GND	10	—	地
LE	11	I	锁存使能输入
8Q	12	O	8Q 输出
7Q	13	O	7Q 输出
6Q	14	O	6Q 输出
5Q	15	O	5Q 输出
4Q	16	O	4Q 输出
3Q	17	O	3Q 输出
2Q	18	O	2Q 输出
1Q	19	O	1Q 输出
V _{CC}	20	—	电源引脚
散热焊盘 ⁽²⁾		—	散热焊盘可连接到 GND 或悬空。请勿连接到任何其他信号或电源。

(1) I = 输入, O = 输出, I/O = 输入或输出, G = 接地, P = 电源。

(2) 仅限 RKS 封装。

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内 (除非另有说明) ¹

			最小值	最大值	单位
V _{CC}	电源电压范围		-0.5	7	V
V _I ⁽²⁾	输入电压范围		-0.5	V _{CC} +0.5	V
V _O ⁽²⁾	输出电压范围		-0.5	V _{CC} +0.5	V
I _{IK}	输入钳位电流	(V _I < 0 或 V _I > V _{CC})		±20	mA
I _{OK}	输出钳位电流	(V _O < 0 或 V _O > V _{CC})		±20	mA
I _O	持续输出电流	(V _O = 0 至 V _{CC})		±50	mA
通过 V _{CC} 或 GND 的持续电流				±200	mA
T _{stg}	贮存温度范围		-65	150	°C

- (1) 应力超出绝对最大额定值下列出的值可能会对器件造成损坏。这些仅为压力额定值，并不表示器件在这些条件下以及在建议的工作条件以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
- (2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

5.2 建议运行条件

在自然通风条件下的工作温度范围内 (除非另有说明) ¹

		SN54ACT573		SN74ACT573		单位
		最小值	最大值	最小值	最大值	
V _{CC}	电源电压	4.5	5.5	4.5	5.5	V
V _{IH}	高电平输入电压	2		2		V
V _{IL}	低电平输入电压		0.8		0.8	V
V _I	输入电压	0	V _{CC}	0	V _{CC}	V
V _O	输出电压	0	V _{CC}	0	V _{CC}	V
I _{OH}	高电平输出电流		- 24		- 24	mA
I _{OL}	低电平输出电流		24		24	mA
Δt/Δv	输入转换上升或下降速率		8		8	ns/V
T _A	自然通风条件下的工作温度范围	-55	125	- 40	85	°C

5.3 热性能信息

热性能指标		SN74ACT573						单位
		DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RKS (VQFN)	
		20 引脚	20 引脚	20 引脚	20 引脚	20 引脚	20 引脚	
R _{θJA}	结至环境热阻 ⁽¹⁾	101.2	70	69	60	126.2	67.7	°C/W

- (1) 有关新旧热性能指标的更多信息，请参阅 [半导体和 IC 封装热性能指标](#) 应用报告。

5.4 电气特性

在自然通风条件下的工作温度范围内测得（除非另有说明）

参数	测试条件	V _{CC}	T _A = 25°C			SN54ACT573		SN74ACT573		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V _{OH}	I _{OH} = -50μA	4.5V	4.4	4.49		4.4		4.4		V
		5.5V	5.4	5.49		5.4		5.4		
	I _{OH} = -24mA	4.5V	3.86			3.7		3.76		
		5.5V	4.86			4.7		4.76		
	I _{OH} = -50mA ⁽¹⁾	5.5V				3.85				
	I _{OH} = -75mA ⁽¹⁾	5.5V						3.85		
V _{OL}	I _{OL} = 50 μA	4.5V			0.1	0.1		0.1		V
		5.5V			0.1	0.1		0.1		
	I _{OL} = 24mA	4.5V			0.36	0.44		0.44		
		5.5V			0.36	0.44		0.44		
	I _{OL} = 50mA ⁽¹⁾	5.5V				1.65				
	I _{OL} = 75mA ⁽¹⁾	5.5V						1.65		
I _{OZ}	V _O = V _{CC} 或 GND	5.5V			±0.25	±5		±2.5		μA
I _I	V _I = V _{CC} 或 GND	5.5V			±0.1	±1		±1		μA
I _{CC}	V _I = V _{CC} 或 GND, I _O = 0	5.5V			4	80		40		μA
Δ I _{CC} ⁽²⁾	一个输入电压为 3.4V, 其他输入电压为 GND 或 V _{CC}	5.5V		0.6		1.5		1.5		mA
C _i	V _I = V _{CC} 或 GND	5V		5						pF

(1) 一次不应测试超过一个输出，且测试持续时间不应超过 2ms。

(2) 这是每个输入在指定 TTL 电压电平之一而不是 0V 或 V_{CC} 时电源电流的增加情况。

5.5 时序要求

在自然通风条件下的工作温度范围内测得，V_{CC} = 5V ± 0.5V（除非另有说明）（请参阅[负载电路和电压波形](#)）

		T _A = 25°C		SN54ACT573		SN74ACT573		单位
		最小值	最大值	最小值	最大值	最小值	最大值	
t _w	脉冲持续时间，LE 高电平	3.5		5		4		ns
t _{su}	设置时间，LE ↓ 前的数据	3		4.5		3.5		ns
t _h	保持时间，LE ↓ 后的数据	0		1		0		ns

5.6 开关特性

在自然通风条件下的工作温度范围内测得， $V_{CC} = 5V \pm 0.5V$ (除非另有说明) (请参阅[负载电路和电压波形](#))

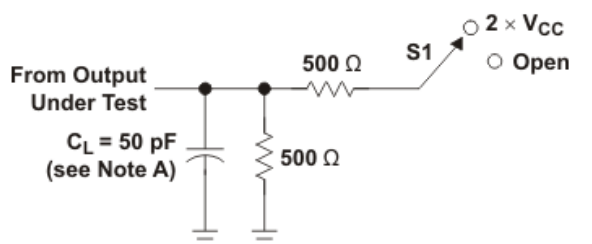
参数	从 (输入)	至 (输出)	$T_A = 25^\circ C$			SN54ACT573		SN74ACT573		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	D	Q	2.5	6	10.5	1.5	13.5	2	12	ns
t_{PHL}			2.5	6	10.5	1.5	13.5	2	12	
t_{PLH}	LE	Q)	3	6	10.5	1.5	13	2.5	12	ns
t_{PHL}			2.5	5.5	9.5	1.5	12	2	10.5	
t_{PZH}	OE	Q	2	5.5	10	1.5	11.5	1.5	11	ns
t_{PZL}			1.5	5.5	9.5	1.5	11	1.5	10.5	
t_{PHZ}	OE	Q)	2.5	6.5	11	1.5	13.5	1.5	12.5	ns
t_{PLZ}			1.5	5	8.5	1.5	10.5	1	9.5	

5.7 工作特性

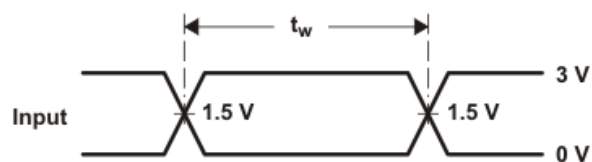
$V_{CC} = 5V$, $T_A = 25^\circ C$

参数	测试条件	典型值	单位
C_{pd} 功率耗散电容	$C_L = 50pF$, $f = 1MHz$	25	pF

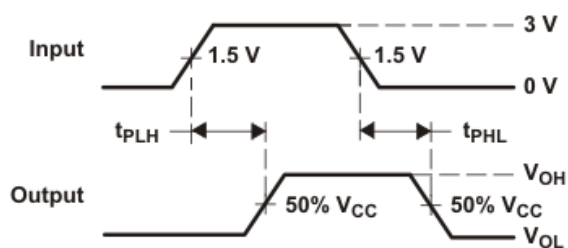
6 参数测量信息



LOAD CIRCUIT

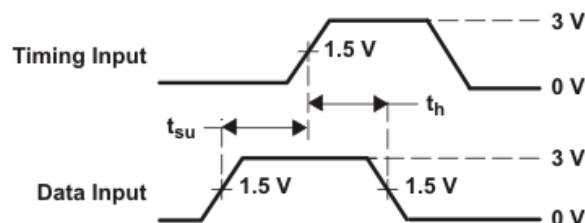


VOLTAGE WAVEFORMS

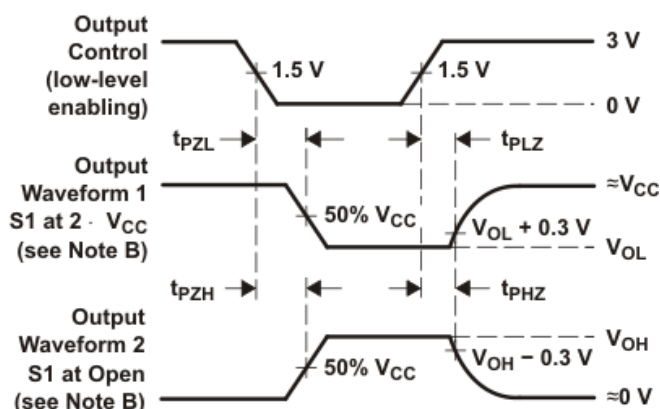


VOLTAGE WAVEFORMS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- A. C_L 包括探头和夹具电容。
- B. 波形 1 用于具有内部条件的输出，使得输出为低电平，除非被输出控制禁用。波形 2 用于具有内部条件的输出，使得输出为高电平，除非被输出控制禁用。
- C. 所有输入脉冲由具有以下特性的发生器提供： $PRR \leq 1\text{MHz}$ ， $Z_O = 50 \Omega$ ， $t_r \leq 2.5\text{ns}$ ， $t_f \leq 2.5\text{ns}$ 。
- D. 一次测量一个输出，每次测量一个输入转换。

图 6-1. 负载电路和电压波形

8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 电源相关建议

电源可以是 [节 5.2](#) 中最小和最大电源电压额定值之间的任意电压。

每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，TI 建议使用 $0.1\mu\text{F}$ 电容器；如果有多个 V_{CC} 端子，则 TI 建议为每个电源端子使用 $0.01\mu\text{F}$ 或 $0.022\mu\text{F}$ 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。 $0.1\mu\text{F}$ 和 $1\mu\text{F}$ 通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

8.2 布局

8.2.1 布局指南

当使用多位逻辑器件时，输入决不能悬空。

在许多情况下，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时，未使用数字逻辑器件的功能或部分功能。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的操作状态。以下指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。应应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，它们将连接到 GND 或 V_{CC} ，具体取决于哪种更合理或更方便。浮动输出通常是可以接受的，除非该器件是收发器。如果该收发器有一个输出使能引脚，它会在置为有效时禁用该器件的输出部分。这不会禁用 IO 的输入部分，因此它们在禁用后不能悬空。

8.2.2 布局示例

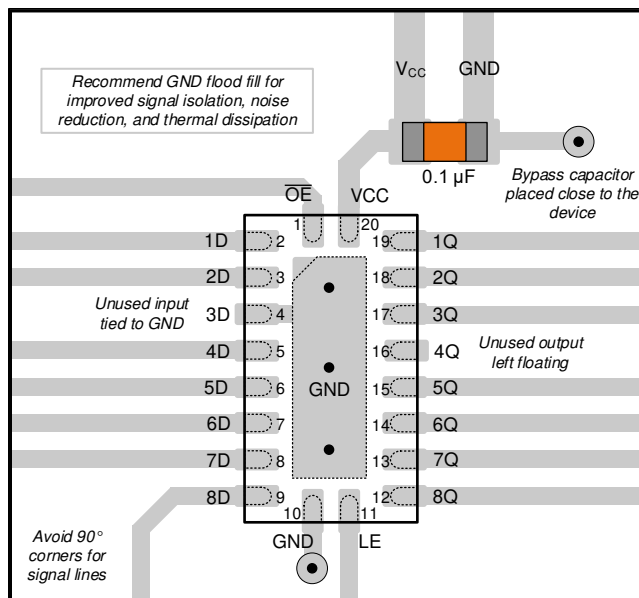


图 8-1. SNx4ACT573 的示例布局

9 器件和文档支持

9.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

9.3 商标

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (November 2023) to Revision G (March 2024)	Page
• 更新了 R _{θJA} 值：DW = 58 至 101.2，PW = 83 至 126.2，所有值均以 °C/W 为单位.....	5
• 添加了 <i>应用和实施</i> 部分.....	10

Changes from Revision E (August 2023) to Revision F (November 2023)	Page
• 添加了 <i>RKS</i> 封装信息.....	1
• 更新了 <i>器件信息</i> 表以包含额定值.....	1

11 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87664012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 87664012A SNJ54ACT 573FK	Samples
5962-8766401RA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8766401RA SNJ54ACT573J	Samples
5962-8766401SA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8766401SA SNJ54ACT573W	Samples
SN74ACT573DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD573	Samples
SN74ACT573DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	ACT573	
SN74ACT573DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT573	Samples
SN74ACT573N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ACT573N	Samples
SN74ACT573NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT573	Samples
SN74ACT573PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	AD573	
SN74ACT573PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD573	Samples
SN74ACT573RKSR	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ACT573	Samples
SNJ54ACT573FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 87664012A SNJ54ACT 573FK	Samples
SNJ54ACT573J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8766401RA SNJ54ACT573J	Samples
SNJ54ACT573W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8766401SA SNJ54ACT573W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ACT573, SN74ACT573 :

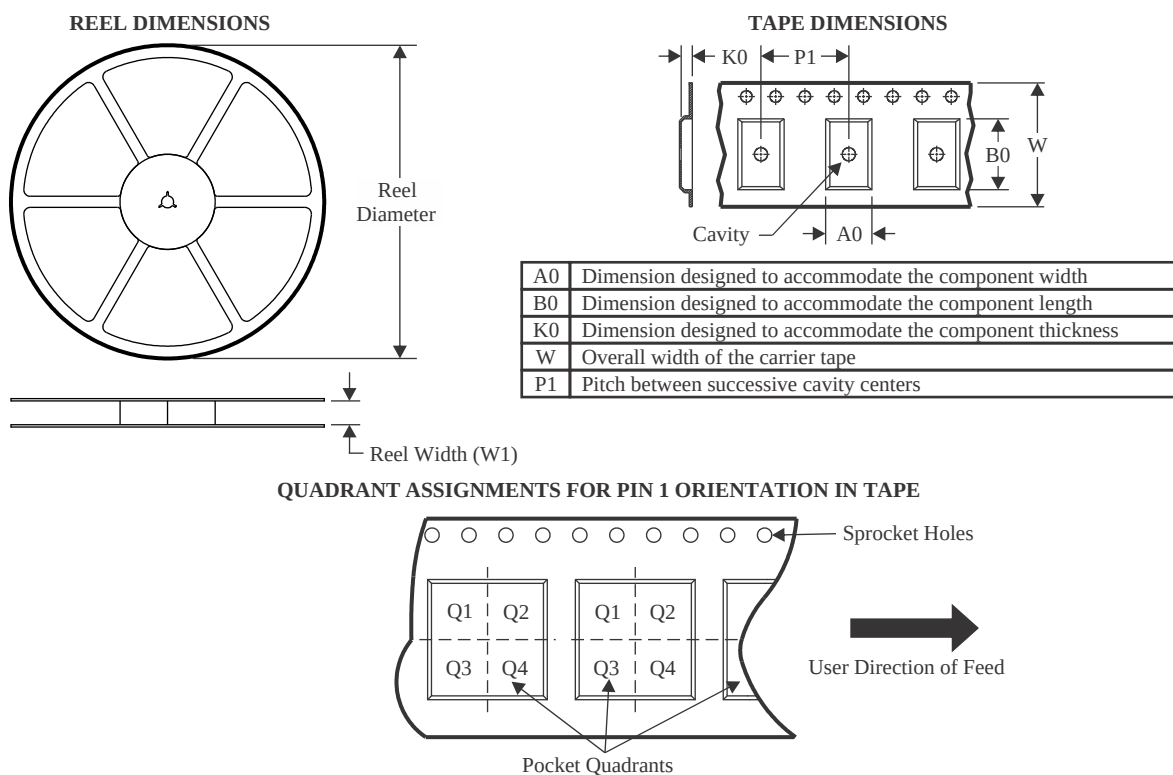
- Catalog : [SN74ACT573](#)
- Automotive : [SN74ACT573-Q1](#), [SN74ACT573-Q1](#)
- Military : [SN54ACT573](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

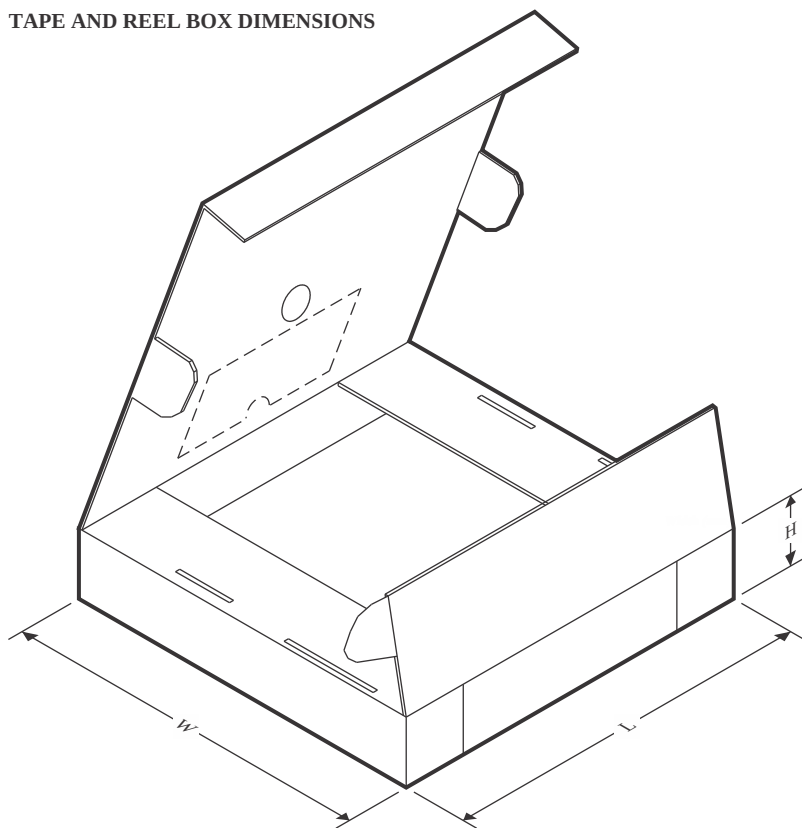
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT573DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ACT573DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74ACT573DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ACT573NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ACT573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74ACT573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74ACT573RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

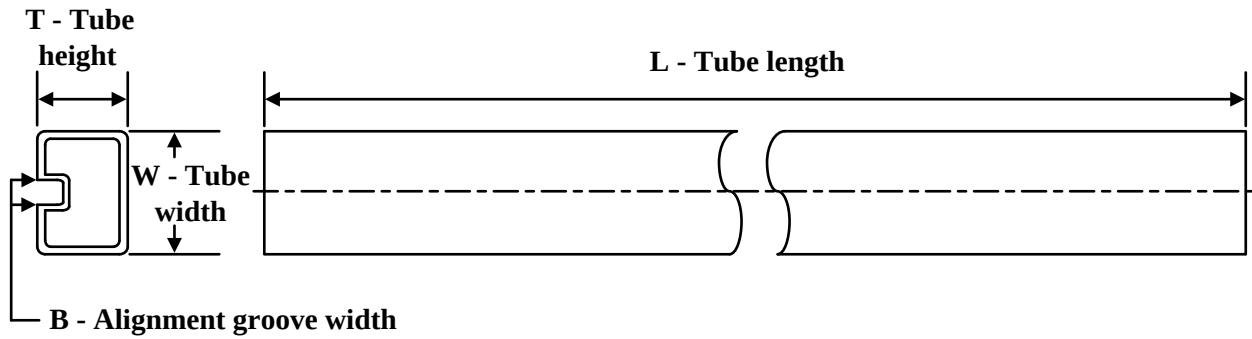
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT573DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74ACT573DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ACT573DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ACT573NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ACT573PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74ACT573PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74ACT573RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE

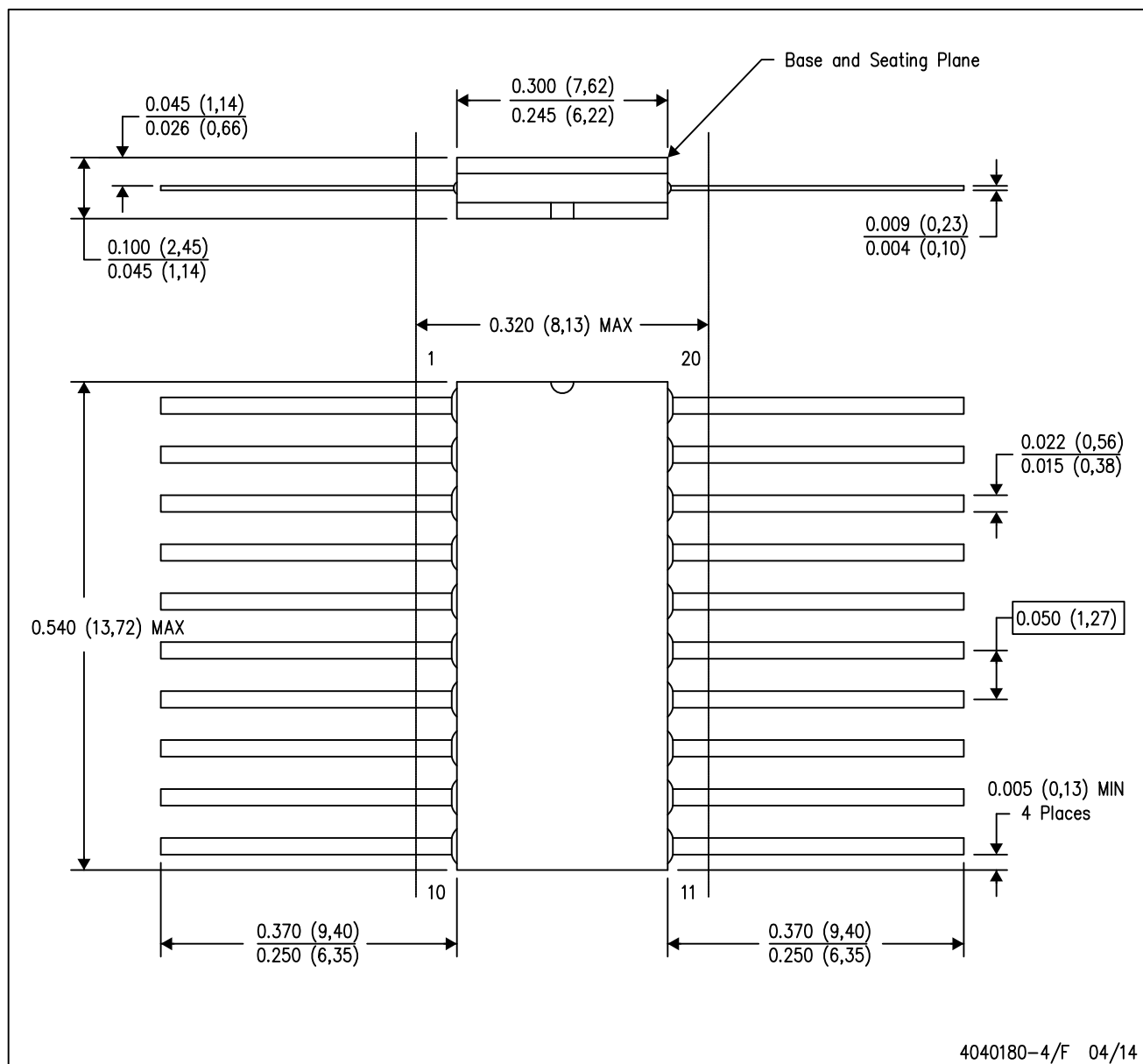


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-87664012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8766401SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ACT573N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ACT573FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT573W	W	CFP	20	25	506.98	26.16	6220	NA

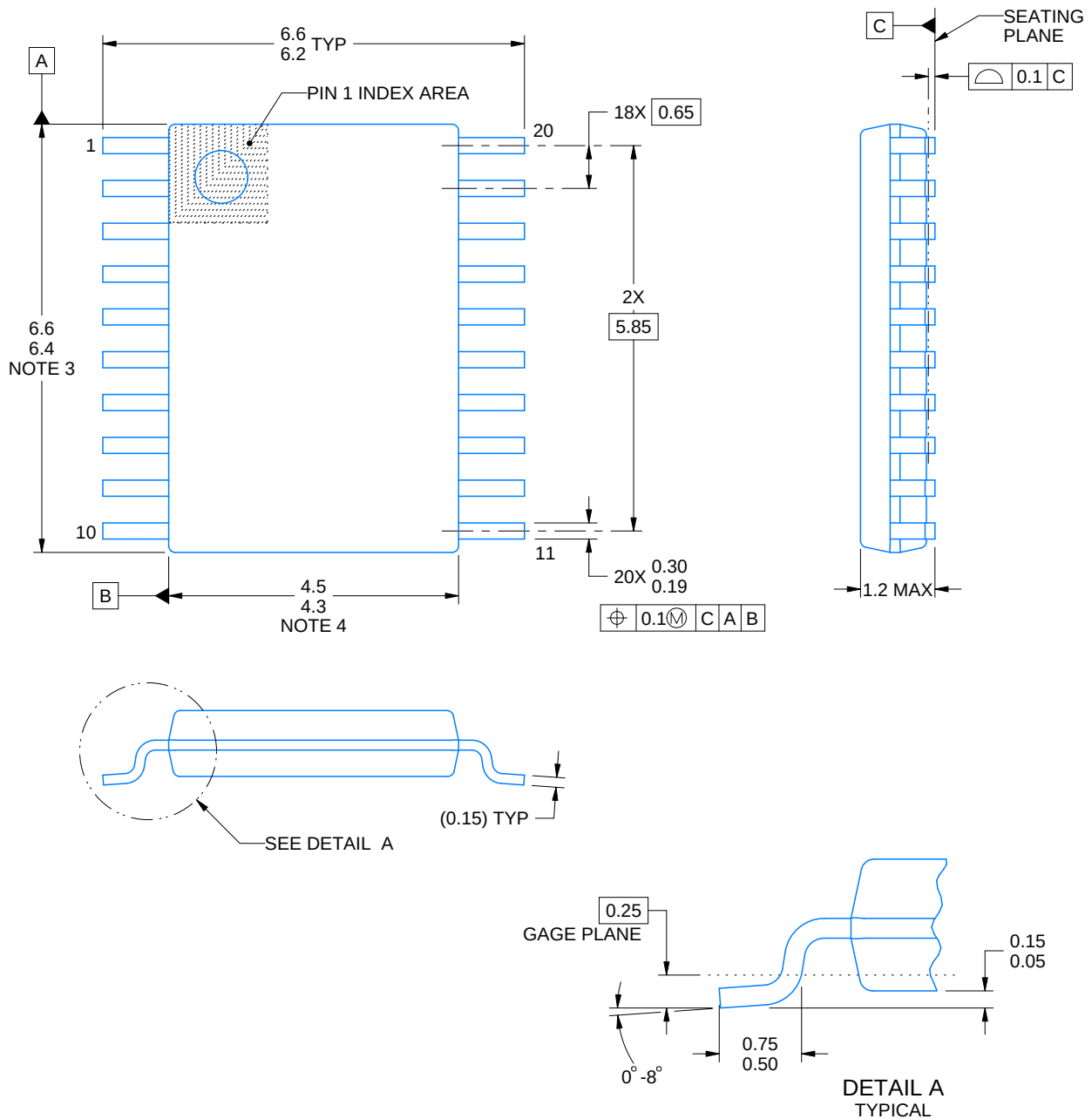
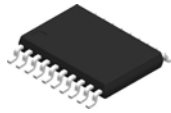
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



4220206/A 02/2017

NOTES:

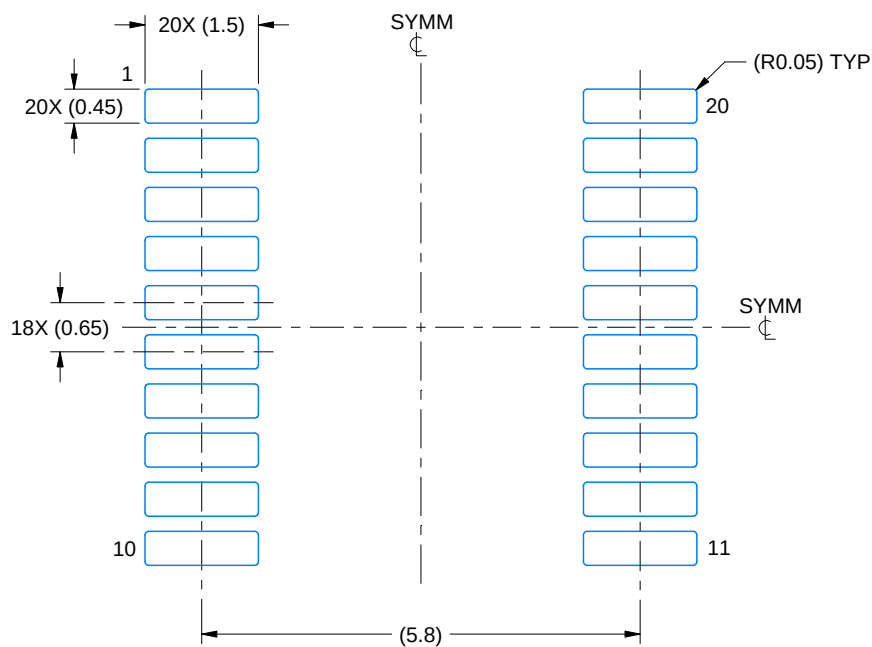
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

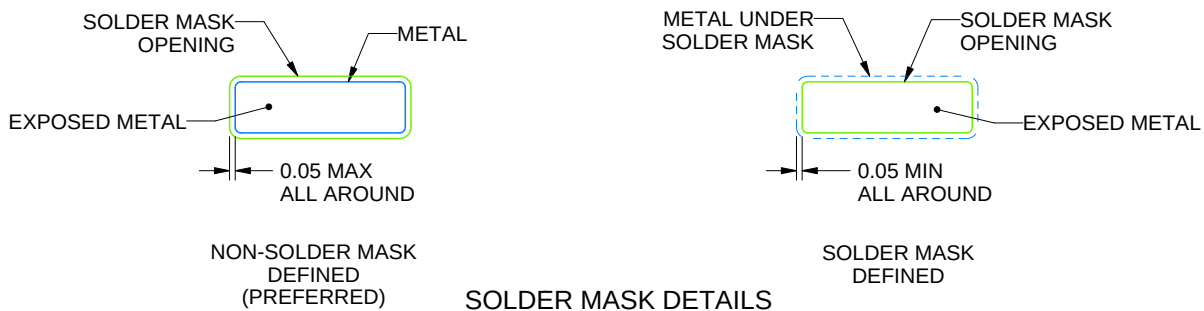
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

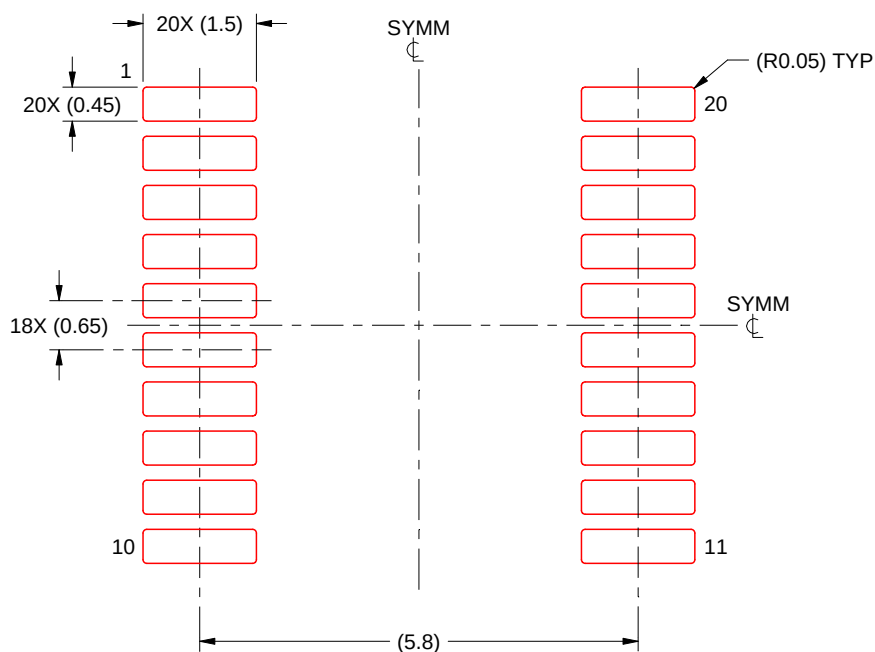
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

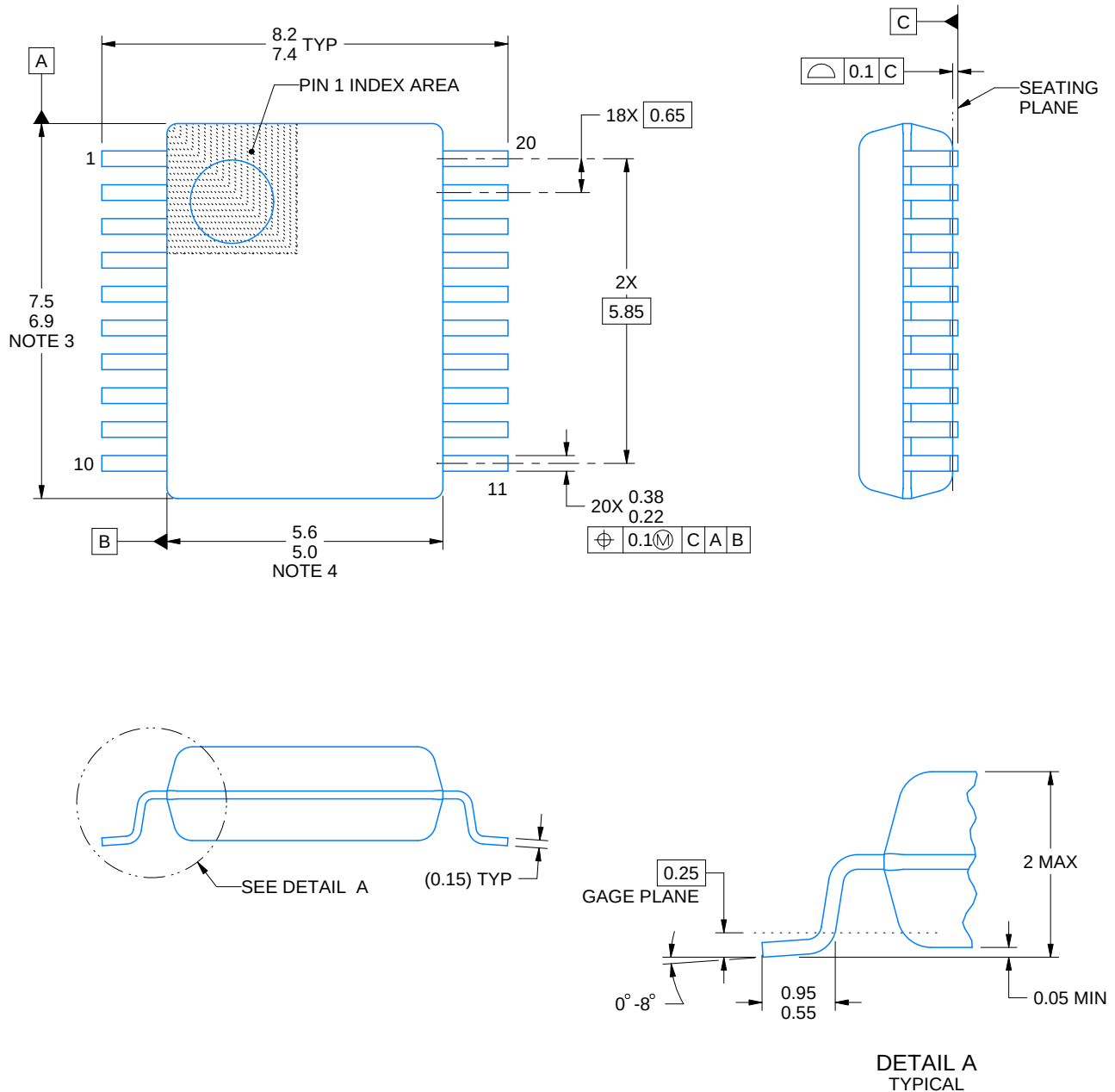
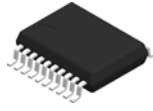


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

NOTES:

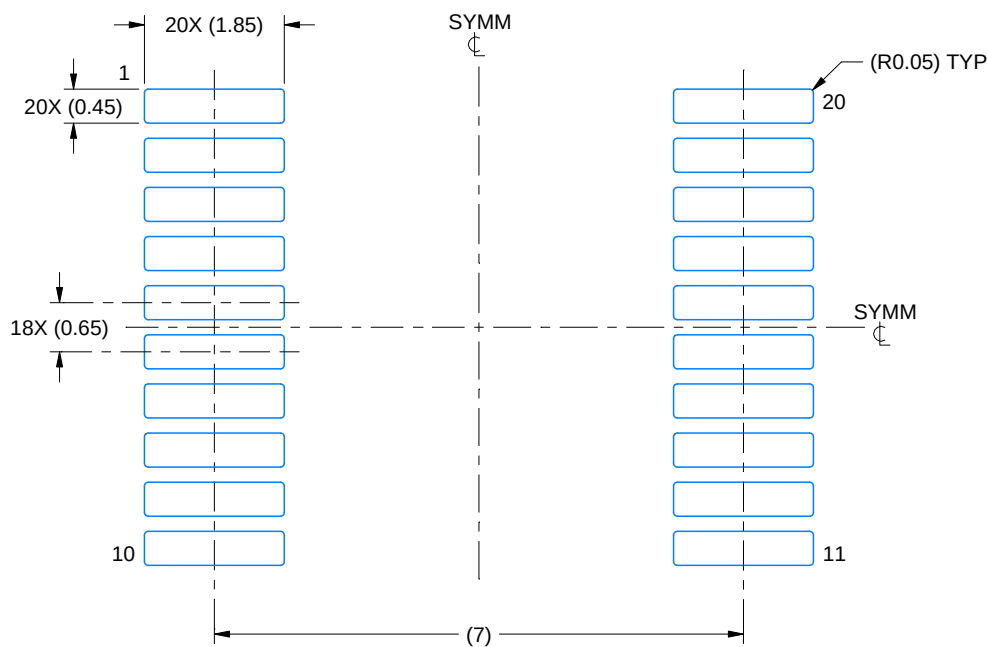
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

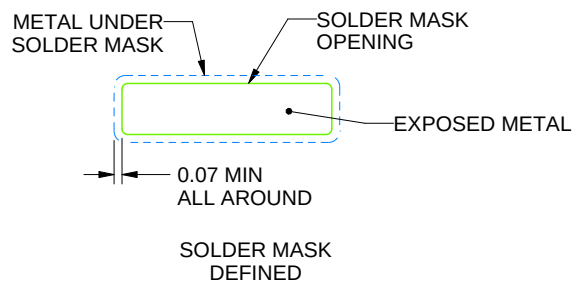
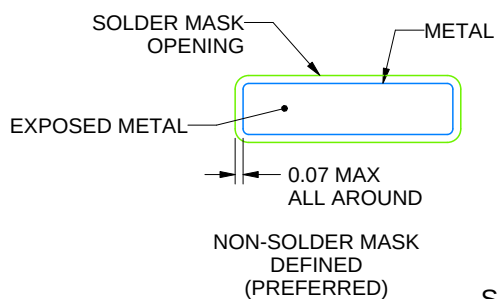
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

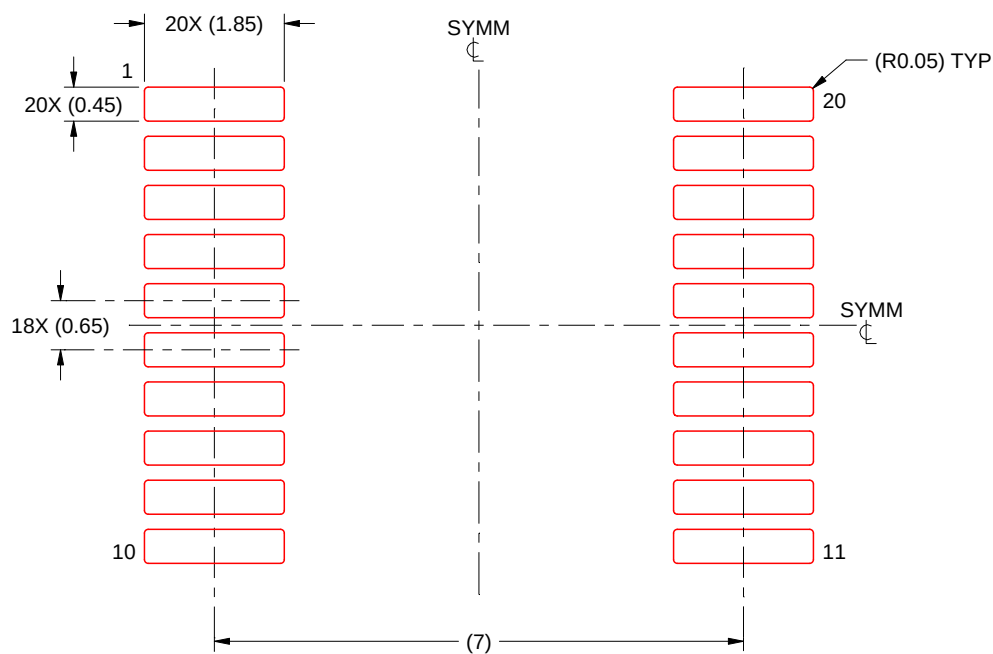
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

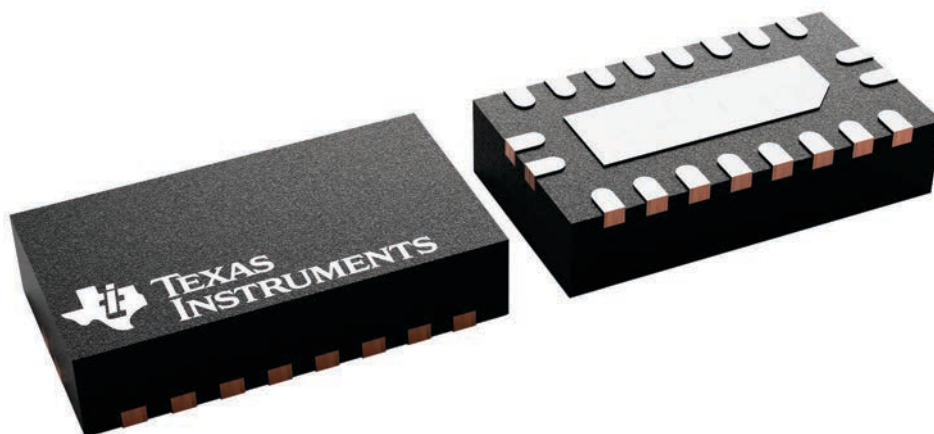
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

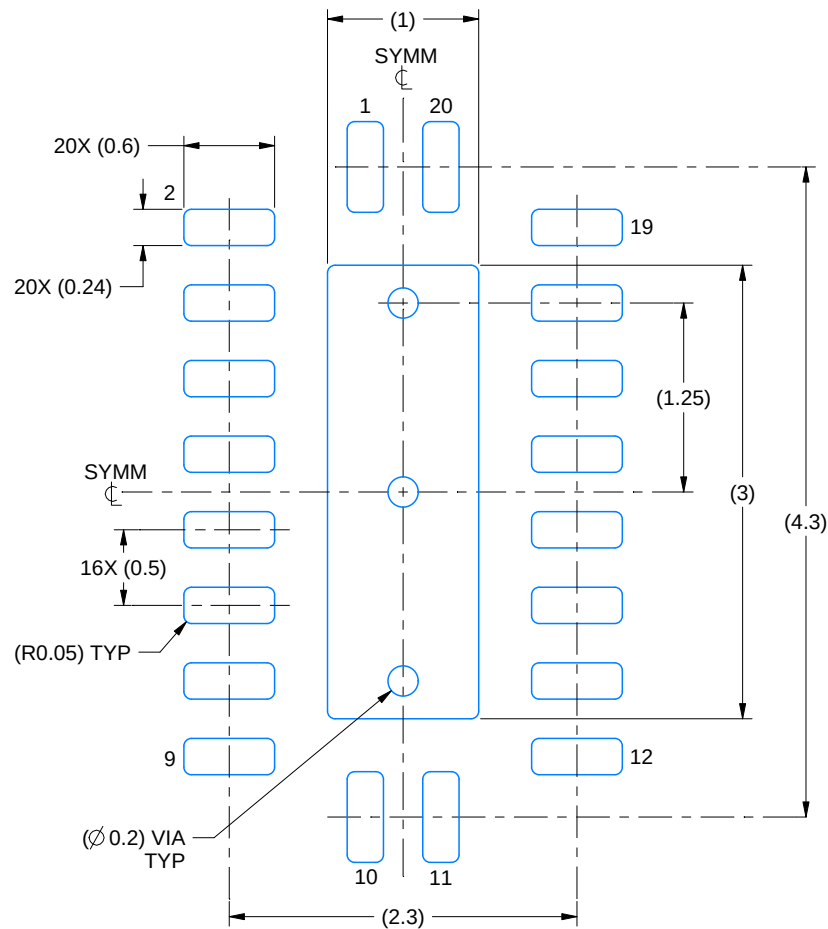


EXAMPLE BOARD LAYOUT

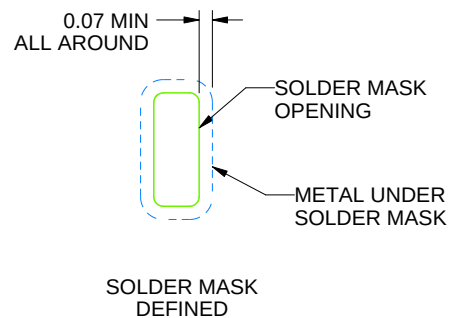
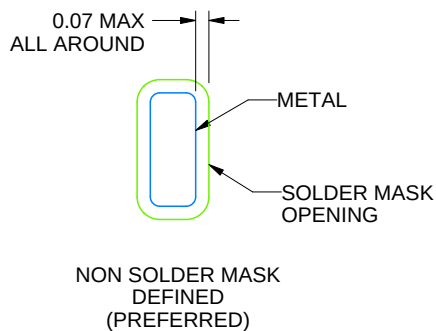
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

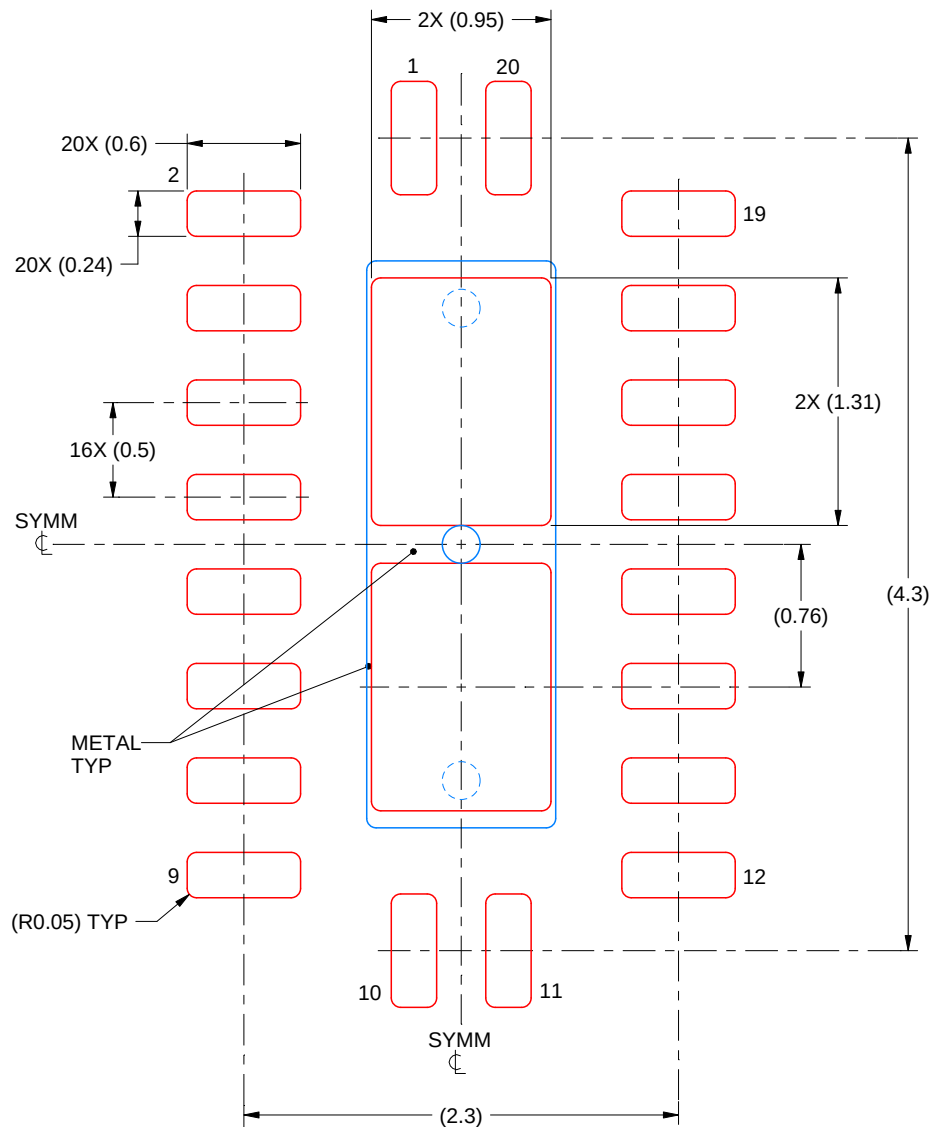
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

NOTES: (continued)

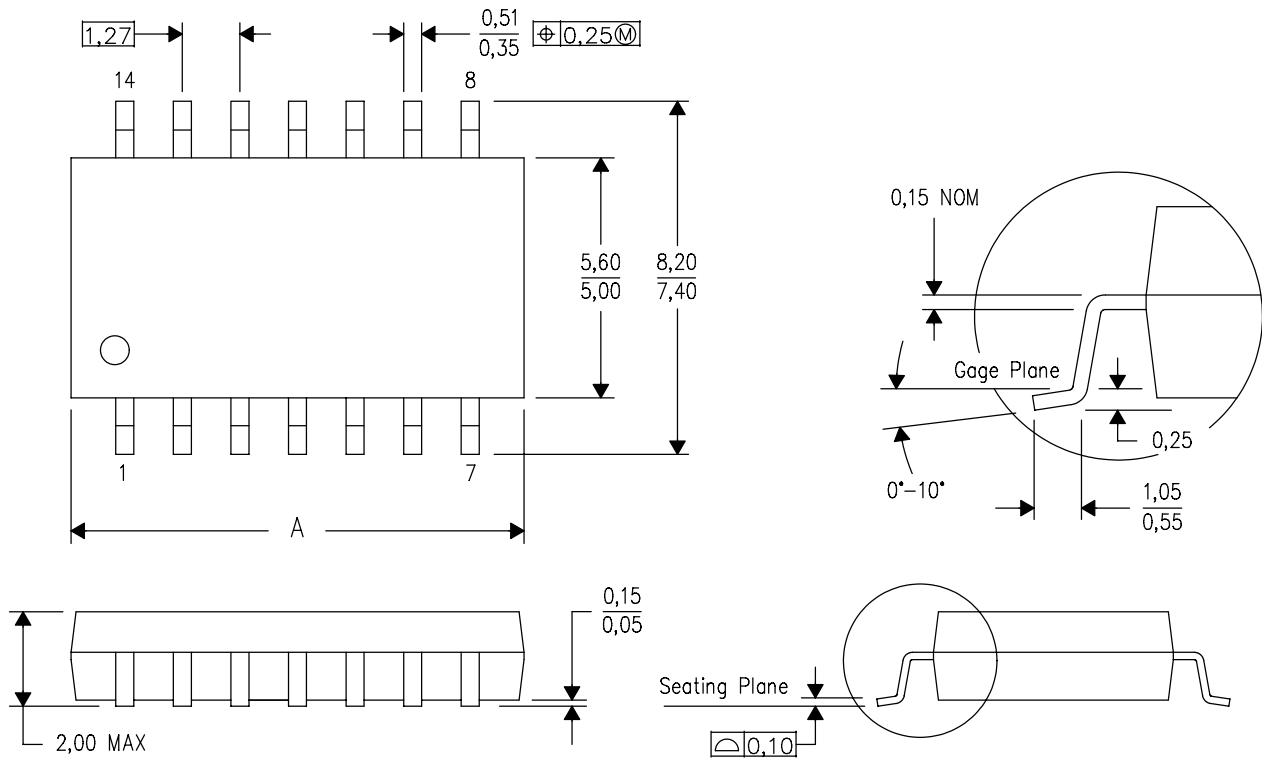
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

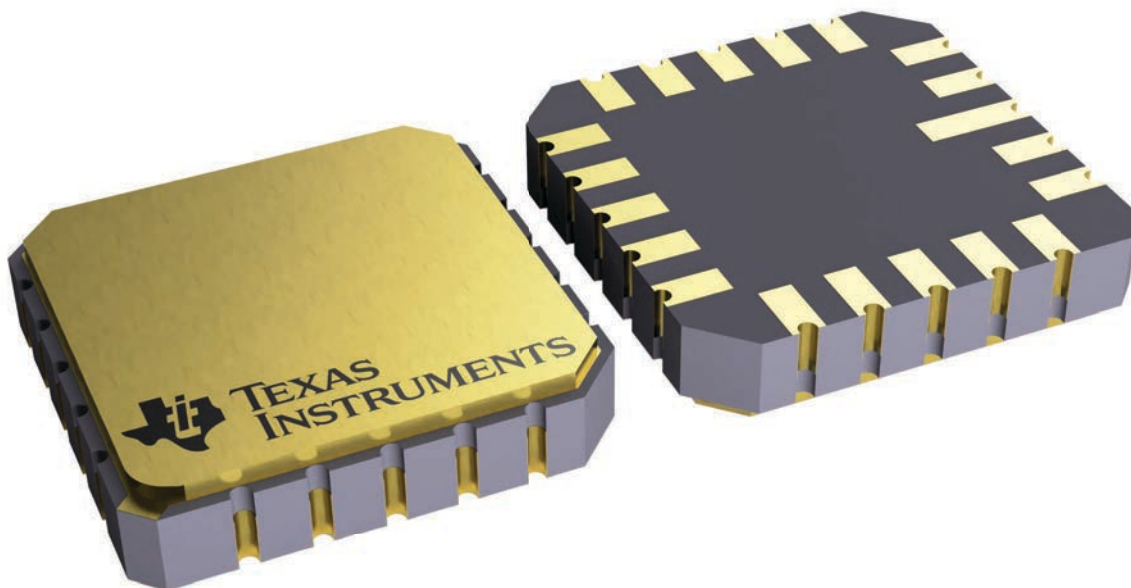
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

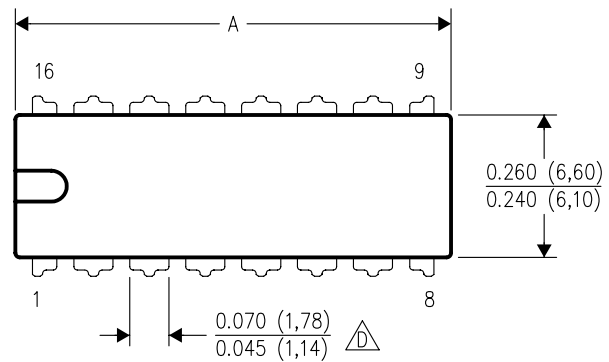


4229370VA\

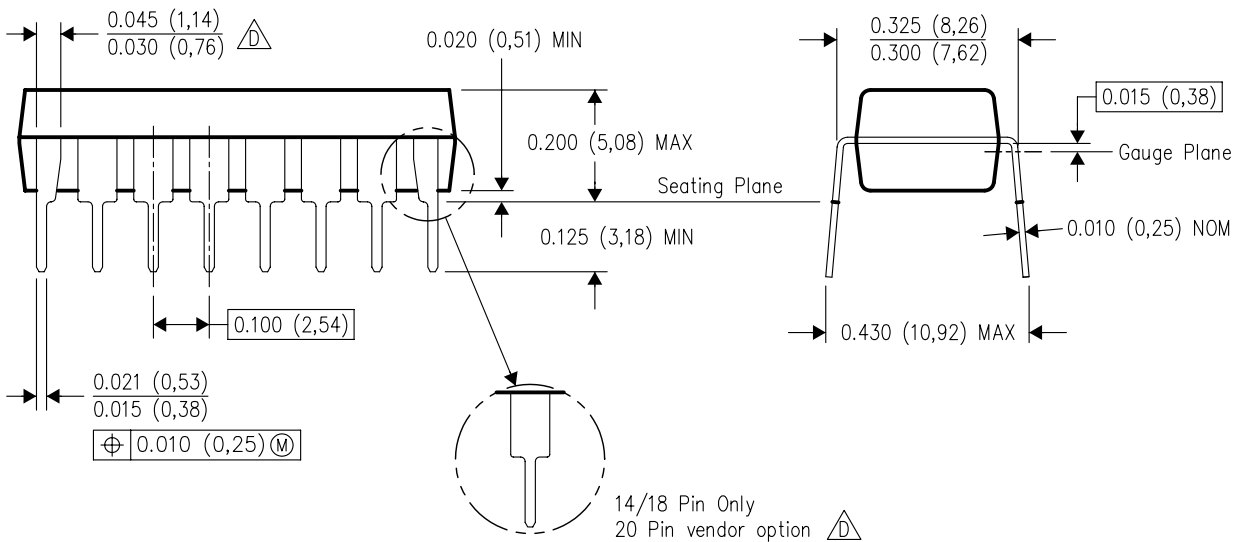
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

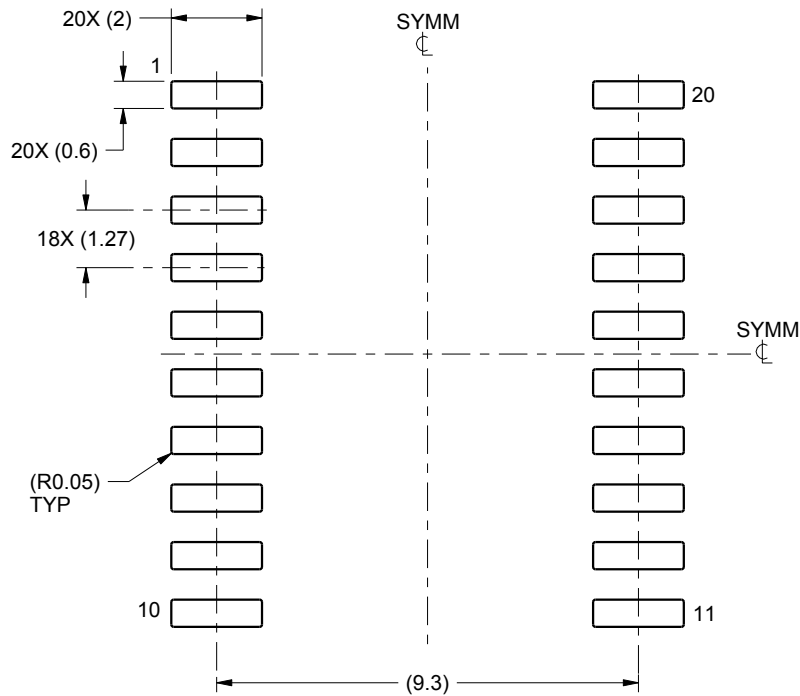
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

EXAMPLE BOARD LAYOUT

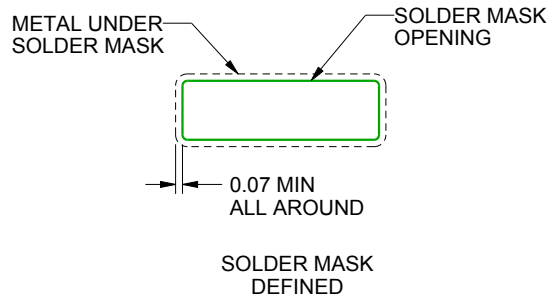
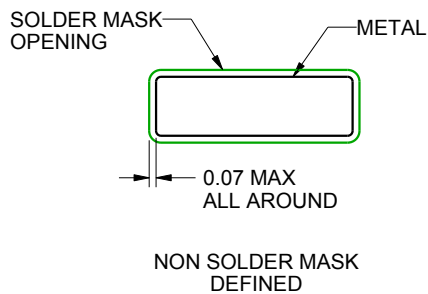
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

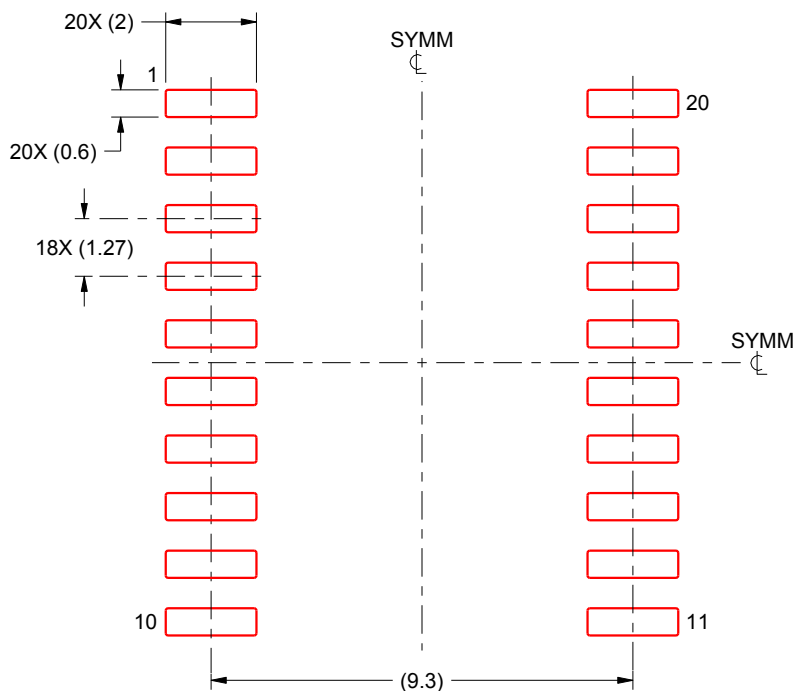
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

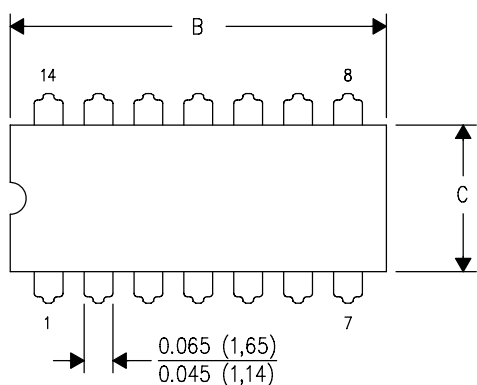
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

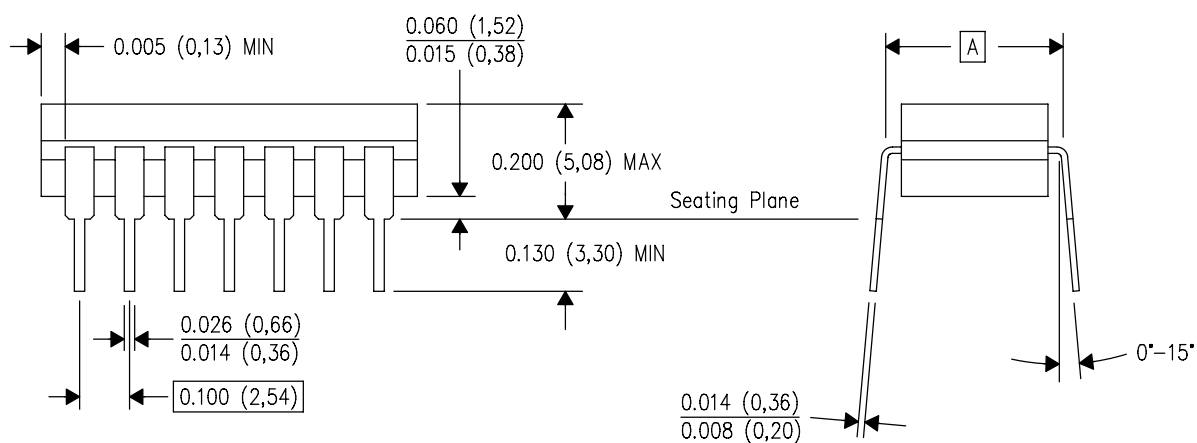
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024，德州仪器 (TI) 公司