

## AM69x 处理器，器件修订版本 1.0

### 1 特性

#### 处理器内核：

- 多达八核 64 位 Arm® Cortex®-A72 微处理器子系统，性能高达 2GHz
  - 每个四核 Cortex®-A72 集群具有 2MB L2 共享缓存
  - 每个 Cortex®-A72 内核具有 32KB L1 数据缓存和 48KB L1 指令缓存
- 多达四个深度学习加速器：
  - 每个加速器高达 8 万亿次每秒运算 (TOPS)
  - 总计 32 万亿次每秒运算 (32TOPS)
- 双核 Arm® Cortex®-R5F MCU，在具有 FFI 的通用计算分区中性能高达 1.0GHz
  - 16KB L1 数据缓存、16KB L1 指令缓存和 64KB L2 TCM
- 双核 Arm® Cortex®-R5F MCU，性能高达 1.0GHz，支持器件管理
  - 32K L1 数据缓存、32K 指令缓存和 64K L2 TCM，所有存储器上都有 SECDED ECC
- 最多两个具有图像信号处理器 (ISP) 和多个视觉辅助加速器的视觉处理加速器 (VPAC)
  - 4.8 亿像素/秒 ISP
  - 支持多达 16 位的输入 RAW 格式
  - 宽动态范围 (WDR)、镜头失真校正 (LDC)、视觉成像子系统 (VISS) 和多标量 (MSC) 支持
  - 输出颜色格式：8 位、12 位，以及 YUV 4:2:2、YUV 4:2:0，RGB，HSV/HSI
- 多媒体：
  - 显示子系统支持：
    - 最多 4 台显示器
    - 最多两个 DSI 4L TX (高达 2.5K)
    - 一个 eDP 4L
    - 一个 DPI 24 位 RGB 并行接口
    - OLDI/LVDS (4 通道 - 2 个) 和 24 位 RGB 并行接口
    - 定帧检测和 MISR 数据检查等安全功能
  - 3D 图形处理单元
    - IMG BXS-4-64，高达 800MHz
    - 50GFLOPS，4GTexel/s
    - >500 百万像素/秒，>8 个 GFLOP
    - 支持至少 2 个合成层
    - 支持高达 2048x1080 @60fps 的分辨率
    - 支持 ARGB32、RGB565 和 YUV 格式
    - 支持 2D 图形
    - OpenGL ES 3.1、Vulkan 1.2

- 三个 CSI2.0 4L 摄像头串行接口 RX (CSI-RX) 以及两个具有 DPHY 的 CSI2.0 4L TX (CSI-TX)
  - 符合 MIPI CSI 1.3 标准 + MIPI-DPHY 1.2
  - 支持高达 1.5Gbps 的 1、2、3 或 4 数据通道模式
  - ECC 验证/校正和 RAM 上的 CRC 校验 + ECC
  - 虚拟通道支持 (多达 16 个)
  - 能够通过 DMA 将流数据直接写入 DDR
- 两个视频编码器/解码器模块
  - 支持 5.1 级高阶的 HEVC (H.265) 主配置文件
  - 支持 5.2 级 H.264 基线/主/高配置文件
  - 每个模块支持高达 4K 超高清分辨率 (3840 × 2160)
  - 每个模块支持 4K60 H.264/H.265 编码/解码 (高达 480MP/s)

#### 存储器子系统：

- 高达 8MB 的片上 L3 RAM (具有 ECC 和一致性)
  - ECC 错误保护
  - 共享一致性缓存
  - 支持内部 DMA 引擎
- 多达四个具有 ECC 的外部存储器接口 (EMIF) 模块
  - 支持 LPDDR4 存储器类型
  - 支持高达 4266MT/s 的速度
  - 多达 4 个具有内联 ECC 的 32 位总线，速率高达 68GB/s
- 通用存储器控制器 (GPMC)
- MAIN 域中有 512KB 片上 SRAM，受 ECC 保护
- 符合 AEC-Q100 标准 (以 Q1 结尾的器件型号)

#### 器件安全：

- 安全启动，提供安全运行时支持
- 客户可编程的根密钥，级别高达 RSA-4K 或 ECC-512
- 嵌入式硬件安全模块
- 加密硬件加速器 - 带 ECC 的 PKA、AES、SHA、RNG、DES 和 3DES



**高速串行接口：**

- 集成以太网交换机，支持最多 8 个外部端口
  - 两个端口支持 5Gb、10Gb USXGMII 或 5Gb XFI
  - 所有端口均支持 1Gb、2.5Gb SGMII
  - 所有端口均可支持 QSGMII。最多可启用 2 个 QSGMII 并使用所有 8 个内部通道。1 个 QSGMII 接口使用 4 个内部通道。
- 多达 4 个 2L/2 个 4L PCI-Express® (PCIe) 第 3 代控制器
  - 第 1 代 (2.5GT/s)、第 2 代 (5.0GT/s) 和第 3 代 (8.0GT/s) 运行，具有自动协商功能
- 一个 USB 3.0 双重角色器件 (DRD) 子系统
  - 增强型超高速第一代端口
  - 支持 Type-C 开关
  - 可独立配置为 USB 主机、USB 外设或 USB DRD

**以太网**

- 两个 RGMII/RMII 接口

**汽车接口：****2 应用**

- 机器视觉摄像机和计算机
- 智能购物车
- 零售自动化
- 智能农业
- 视频监控
- 交通监控
- 自主移动机器人 (AMR)
- 无人机
- 工业运输
- 工业人机界面 (HMI)
- 工业 PC
- 单板计算机
- 患者监护和医疗设备

- 20 个模块化控制器局域网 (MCAN) 模块，具有完整 CAN-FD 支持

**音频接口：**

- 5 个多通道音频串行端口 (MCASP) 模块

**闪存接口：**

- 嵌入式多媒体卡接口 (eMMC™ 5.1)
- 一个安全数字® 3.0/安全数字输入输出 3.0 接口 (SD3.0/SDIO3.0)
- 具有 2 个通道的通用闪存 (UFS 2.1) 接口
- 两个独立闪存接口，配置为
  - 一个 OSPI 或 HyperBus™ 或 QSPI 闪存接口，以及
  - 一个 QSPI 闪存接口

**片上系统 (SoC) 架构：**

- 16nm FinFET 技术
- 31mm × 31mm、0.8mm 间距、1414 引脚 FCBGA (ALY)，可实现 IPC 3 级 PCB 布线

**TPS6594-Q1 配套电源管理 IC (PMIC)：**

- 等级高达 ASIL-D 的功能安全支持
- 灵活的映射，可支持不同的用例

### 3 说明

AM69 可扩展处理器系列采用不断发展的 Jacinto™ 7 架构，面向智能视觉摄像头应用，基于 TI 在视觉处理器市场上十多年所积累的广泛先进市场知识而构建。AM69x 系列专为工厂自动化、楼宇自动化和其他市场中广泛的成本敏感型高性能计算应用而构建。

AM69 以业界卓越的功耗/性能比为传统和深度学习算法提供高性能计算技术，并且系统集成度高，可为高级视觉摄像头应用实现可扩展性和更低的成本。关键内核包括用于常规计算的新款 Arm 和 GPU 处理器、具有标量和矢量内核的下一代 DSP、专用深度学习和传统算法加速器、集成的下一代成像子系统 (ISP)、视频编解码器和隔离式 MCU 岛。所有这些都由工业级安全硬件加速器提供保护。

**通用计算内核和集成概述：**Arm® Cortex®-A72 的两个四核集群配置（共 8 个内核）有助于实现多操作系统应用，且对软件管理程序的需求非常低。最多两个双核（共 4 个内核）Arm® Cortex®-R5F 子系统能够管理低级的时序关键型处理任务，使 Arm® Cortex®-A72 内核不受应用的影响。TI 的第 7 代 ISP 以现有出色的 ISP 为基础，能够灵活地处理更广泛的传感器套件，支持更高的位深度，并且具有面向分析应用的特性。集成的诊断和安全功能可支持高达 SIL-2 级别的运行，同时集成的安全功能可保护数据免受现代攻击。CSI2.0 端口支持多传感器输入。

**主要高性能内核概述：**C7000™ DSP 下一代内核（“C7x”）将 TI 先进的 DSP 和 EVE 内核整合到性能更高的单个内核中，并增加了浮点矢量计算功能，可实现对旧代码的向后兼容性，同时简化软件编程。即使在 105°C 和 125°C 的最坏情况结温下运行，四个“MMA”深度学习加速器也可在业界超低功率范围内实现高达 32 万亿次每秒运算 (TOPS) [每内核 8TOPS] 的性能。专用的视觉硬件加速器可提供视觉预处理，而不会影响系统性能。C7x/MMA 内核仅可用于 AM69 级处理器中的深度学习功能。

**封装信息**

| 器件型号    | 封装 <sup>(1)</sup> | 封装尺寸 <sup>(2)</sup> |
|---------|-------------------|---------------------|
| AM69x   | ALY (FCBGA, 1414) | 31mm x 31mm         |
| XJ784S4 | ALY (FCBGA, 1414) | 31mm x 31mm         |

- (1) 有关更多信息，请参阅[机械、封装和可订购信息](#)部分。  
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

#### 3.1 功能方框图

图 3-1 是器件的功能方框图。

#### 备注

要了解 TI 软件开发套件 (SDK) 目前支持哪些器件功能，请参阅 [AM69 软件构建表 \(PROCESSOR-SDK-AM69\)](#) 和 [AM69A 软件构建表 \(PROCESSOR-SDK-AM69A\)](#)。

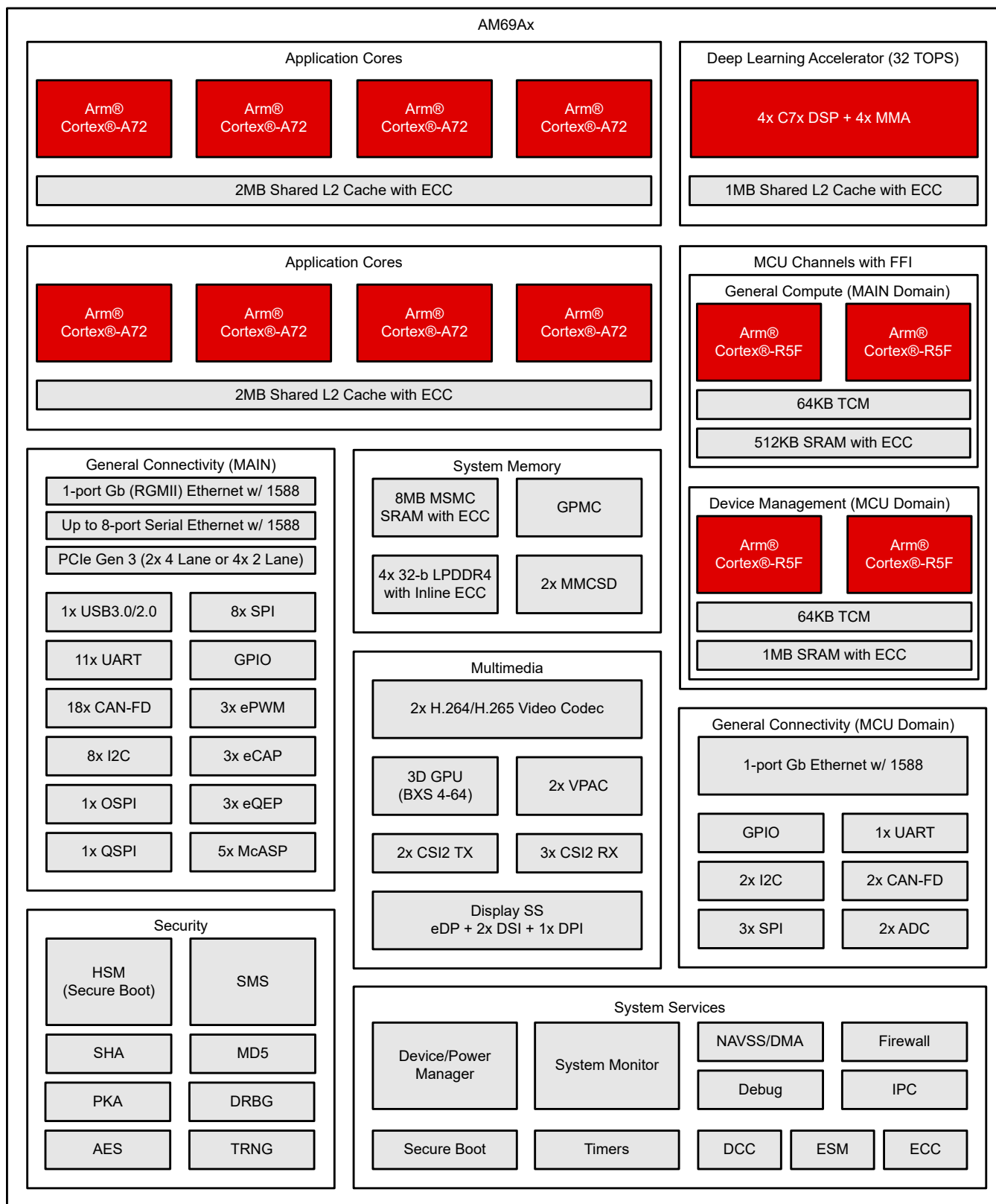


图 3-1. 功能方框图

## 内容

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## 4 Revision History

Changes from March 2, 2023 to August 18, 2023 (from Revision \* (MARCH 2023) to Revision A (AUGUST 2023))

|                                                                                                                                                                                   | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • 通篇：将文档标题从“AM69Ax”更新/更改为“AM69x”.....                                                                                                                                             | 0    |
| • 通篇：删除了所有 OLDI/LVDS 内容；不适用于此器件套件.....                                                                                                                                            | 1    |
| • 通篇：将 3D 图形处理单元 (GPU) 的“BSX”、“BSX-64-4”和“BXS-64-4”更新/更改为“IMG BXS-4-64”.....                                                                                                      | 1    |
| • (封装信息)：更新了表以与新的内容标准一致.....                                                                                                                                                      | 3    |
| • (Device Comparison): Added AM69 and AM69A part numbers to the table. Merged table cells to show commonality/differences and to improve readability.....                         | 7    |
| • (Device Comparison): Added software build sheet Note.....                                                                                                                       | 7    |
| • (Device Comparison): Added footnotes to clarify LPDDR instance usage for a) pin compatibility with 27 mm package, and b) requirements for using fewer than 4 DDR instances..... | 7    |
| • (DDRSS0 Signal Descriptions): Added "DDRSS incremental order" footnote.....                                                                                                     | 88   |
| • (DDRSS1 Signal Descriptions): Added "DDRSS incremental order" footnote.....                                                                                                     | 89   |
| • (DDRSS2 Signal Descriptions): Added "DDRSS incremental order" footnote.....                                                                                                     | 91   |
| • (DDRSS2 Signal Descriptions): Added DDRSS2, DDRSS3, and SERDES2 availability footnote.....                                                                                      | 91   |
| • (DDRSS3 Signal Descriptions): Added "DDRSS incremental order" footnote.....                                                                                                     | 92   |
| • (DDRSS3 Signal Descriptions): Added DDRSS2, DDRSS3, and SERDES2 availability footnote.....                                                                                      | 92   |
| • (SERDES2 Signal Descriptions): Added DDRSS2, DDRSS3, and SERDES2 availability footnote.....                                                                                     | 114  |

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- (Pin Connectivity Requirements) Updated ADC AIN recommendation to allow the tie-off of signals directly to ground..... [132](#)
  - (Pin Connectivity Requirements): Added requirement for DDR interfaces to be used in incrementing order [132](#)
  - (Recommended Operating Conditions): Added clarification to the "... supply inputs" footnote, specifically for VDD\_CORE, VDD\_MCU, and VDD\_CPU domains plus, added cross-references to the MIN/MAX values.. [139](#)
  - (Recommended Operating Conditions): Added vdda\_\* noise specification..... [139](#)
  - (USB VBUS Design Guidelines): Updated/Changed USB VBUS Detect Voltage Divider / Clamp Circuit figure..... [288](#)
-

## 5 Device Comparison

表 5-1 shows the features of the SoC.

### 备注

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the [AM69 Software Build Sheet \(PROCESSOR-SDK-AM69\)](#) and [AM69A Software Build Sheet \(PROCESSOR-SDK-AM69A\)](#).

表 5-1. Device Comparison

| FEATURES <sup>(9)</sup>                    | REFERENCE NAME            | AM69A98                                 | AM69A94   | AM69A78    | AM6958     | AM6934    |
|--------------------------------------------|---------------------------|-----------------------------------------|-----------|------------|------------|-----------|
| PROCESSORS AND ACCELERATORS                |                           |                                         |           |            |            |           |
| Speed Grades                               |                           | T                                       |           |            |            |           |
| Arm Cortex-A72 Microprocessor Subsystem    | Arm A72                   | Octal Core                              | Quad Core | Octal Core | Octal Core | Quad Core |
| Arm Cortex-R5F                             | Arm R5F Device Management | Dual Core <sup>(12)</sup>               |           |            |            |           |
|                                            | Arm R5F General Compute   | Dual Core <sup>(12)</sup>               |           |            |            |           |
| Security Management Subsystem              | SMS                       | Yes                                     |           |            |            |           |
| Security Accelerators                      | SA                        | Yes                                     |           |            |            |           |
| Deep Learning Accelerator (32 TOPS)        | C7x DSP + MMA             | Quad Core <sup>(13)</sup>               |           |            | No         |           |
| Graphics Accelerator IMG BXS-4-64          | GPU                       | Yes                                     |           | No         | Yes        | No        |
| Depth and Motion Processing Accelerators   | DMPAC                     | No                                      |           |            |            |           |
| Vision Processing Accelerators             | VPAC                      | Yes                                     |           |            | No         |           |
| Video Encoder/Decoder                      | VENC/VDEC                 | 2 × Encode/Decode                       |           |            |            | No        |
| SAFETY AND SECURITY                        |                           |                                         |           |            |            |           |
| Safety Targeted                            | Safety                    | No <sup>(1)</sup>                       |           |            |            |           |
| Device Security                            | Security                  | Optional <sup>(2)</sup>                 |           |            |            |           |
| AEC-Q100 Qualified                         | Q1                        | Optional <sup>(3)</sup>                 |           |            |            |           |
| PROGRAM AND DATA STORAGE                   |                           |                                         |           |            |            |           |
| On-Chip Shared Memory (RAM) in MAIN Domain | OCSRAM                    | 512KB SRAM                              |           |            |            |           |
| On-Chip Shared Memory (RAM) in MCU Domain  | MCU_MSRAM                 | 1MB SRAM                                |           |            |            |           |
| Multicore Shared Memory Controller         | MSMC                      | 8MB (On-Chip SRAM with ECC)             |           |            |            |           |
| LPDDR4 DDR Subsystem                       | DDRSS0 <sup>(5)</sup>     | Up to 8GB (32-bit data) with inline ECC |           |            |            |           |
|                                            | DDRSS1 <sup>(5)</sup>     | Up to 8GB (32-bit data) with inline ECC |           |            |            |           |
|                                            | DDRSS2 <sup>(4) (5)</sup> | Up to 8GB (32-bit data) with inline ECC |           |            |            |           |
|                                            | DDRSS3 <sup>(4) (5)</sup> | Up to 8GB (32-bit data) with inline ECC |           |            |            |           |
|                                            | SECEDED                   | Yes                                     |           |            |            |           |
| General-Purpose Memory Controller          | GPMC                      | Up to 1GB with ECC                      |           |            |            |           |



表 5-1. Device Comparison (continued)

| FEATURES <sup>(9)</sup>                                                           | REFERENCE NAME        | AM69A98                      | AM69A94 | AM69A78 | AM6958 | AM6934 |
|-----------------------------------------------------------------------------------|-----------------------|------------------------------|---------|---------|--------|--------|
| <b>PERIPHERALS</b>                                                                |                       |                              |         |         |        |        |
| Display Subsystem                                                                 | DSS                   | Yes                          |         |         |        |        |
|                                                                                   | DSI 4L TX             | 2                            |         |         |        |        |
|                                                                                   | eDP 4L                | 1                            |         |         |        |        |
|                                                                                   | DPI                   | 1                            |         |         |        |        |
| Modular Controller Area Network Interface with Full CAN-FD Support                | MCAN                  | 20                           |         |         |        |        |
| General-Purpose I/O                                                               | GPIO                  | 155                          |         |         |        |        |
| Inter-Integrated Circuit Interface                                                | I2C                   | 10                           |         |         |        |        |
| Improved Inter-Integrated Circuit Interface                                       | I3C                   | 1                            |         |         |        |        |
| Analog-to-Digital Converter                                                       | ADC                   | 2                            |         |         |        |        |
| Capture Subsystem with Camera Serial Interface (CSI2)                             | CSI2.0 4L RX          | 3                            |         |         |        |        |
|                                                                                   | CSI2.0 4L TX          | 2                            |         |         |        |        |
| Multichannel Serial Peripheral Interface                                          | MCSPi                 | 11                           |         |         |        |        |
| Multichannel Audio Serial Port                                                    | MCASP0                | 16 Serializers               |         |         |        |        |
|                                                                                   | MCASP1                | 5 Serializers                |         |         |        |        |
|                                                                                   | MCASP2                | 5 Serializers                |         |         |        |        |
|                                                                                   | MCASP3                | 3 Serializers                |         |         |        |        |
|                                                                                   | MCASP4                | 5 Serializers                |         |         |        |        |
| MultiMedia Card/ Secure Digital Interface                                         | MMCSD0                | eMMC (8-bits)                |         |         |        |        |
|                                                                                   | MMCSD1                | SD/SDIO (4-bits)             |         |         |        |        |
| Universal Flash Storage                                                           | UFS 2L                | No                           |         |         |        |        |
| Flash Subsystem (FSS)                                                             | OSPI0                 | 8-bits <sup>(8)</sup>        |         |         |        |        |
|                                                                                   | OSPI1 <sup>(10)</sup> | 4-bits                       |         |         |        |        |
|                                                                                   | HyperBus              | Yes <sup>(8)</sup>           |         |         |        |        |
| 4x PCI Express Port with Integrated PHY                                           | PCIE                  | 2x4L or 4x2L <sup>(6)</sup>  |         |         |        |        |
| Hyperlink                                                                         | HYP                   | No <sup>(11)</sup>           |         |         |        |        |
| Ethernet Interfaces                                                               | MCU CPSW2G            | RMII or RGMII <sup>(7)</sup> |         |         |        |        |
|                                                                                   | MAIN CPSW2G           | RMII or RGMII <sup>(7)</sup> |         |         |        |        |
|                                                                                   | CPSW9G                | 8 port SERDES <sup>(6)</sup> |         |         |        |        |
| General-Purpose Timers                                                            | TIMER                 | 30                           |         |         |        |        |
| Enhanced High Resolution Pulse-Width Modulator Module                             | eHRPWM                | 6                            |         |         |        |        |
| Enhanced Capture Module                                                           | eCAP                  | 3                            |         |         |        |        |
| Enhanced Quadrature Encoder Pulse Module                                          | eQEP                  | 3                            |         |         |        |        |
| Universal Asynchronous Receiver and Transmitter                                   | UART                  | 12                           |         |         |        |        |
| Universal Serial Bus (USB3.1) SuperSpeed Dual-Role-Device (DRD) Ports with SS PHY | USB0                  | Yes <sup>(6)</sup>           |         |         |        |        |

(1) Functional Safety is not supported on this device family, if interested in this feature, please see the [TDA4VH device family](#).



- (2) Device security features including Secure Boot and Customer Programmable Keys are applicable to select part number variants as indicated by the Device Type (Y) identifier in the [Nomenclature Description table](#)
- (3) AEC-Q100 qualification is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the [Nomenclature Description table](#)
- (4) DDRSS2 and DDRSS3 are not available on the 27mm package variant of this SoC. DDR2/DDR3 should not be used if software compatibility is desired with systems that use the 27mm package
- (5) DDRSS0, DDRSS1, DDRSS2 and DDRSS3 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to DDR0\_\* interface. When using two LPDDR components, they must be connected to DDR0\_\* and DDR1\_\* interfaces, and so forth.
- (6) DP, SGMII, USB3.0, and PCIE share total of 16 SerDes lanes.
- (7) AM69 CPSW supports up to 8 ports using the following instances and signals and modes of operation:
  - **PORT1 Signals:** SGMII1, **Modes:** One of 5Gb, 10Gb USXGMII/XFI, 2.5 Gb SGMII/XAUI, 1Gb SGMII, 5Gb QSGMII
  - **PORT2 Signals:** SGMII2, **Modes:** One of 5Gb, 10Gb USXGMII/XFI, 2.5 Gb SGMII/XAUI, 1Gb SGMII, 5Gb QSGMII
  - **PORTn (n=3 thru 8) Signals:** SGMII<sub>n</sub>, **Modes:** One of 2.5 Gb SGMII/XAUI, 1Gb SGMII, 5Gb QSGMII

If QSGMII is used on any SGMII Port 1 thru 4, then SGMII1/2/3/4 cannot be used for Ethernet functionality since all 4 internal CPSW ports map to the selected QSGMII SERDES port.  
 If QSGMII is used on any SGMII Port 5 thru 8, then SGMII5/6/7/8 cannot be used for Ethernet functionality since all 4 internal CPSW ports map to the selected QSGMII SERDES port.
- (8) Two simultaneous flash interfaces configured as OSPI0 and OSPI1, or HyperBus and OSPI1.
- (9) J784S4 is the base part number for the superset device. Software should constrain the features used to match the intended production device.
- (10) OSPI1 module only pins out 4 pins and is referred to as QSPI in some contexts.
- (11) Hyperlink is not supported on this SoC. System designs should not use the signals HYP\_\*, HYP0\_\*, HYP1\_\*.
- (12) MCU\_R5FSS0 includes Dual-Core R5F that provides Device Management functionality, and is reserved for executing TI provided code.  
 R5FSS1 is a Dual-Core R5F that provides Multimedia Control functionality, and is reserved for executing TI provided code.
- (13) The Deep Learning Accelerator C7x + MMA are reserved for executing TI provided code, and are not available for custom code.

## 6 Terminal Configuration and Functions

### 6.1 Pin Diagrams

#### 备注

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

For details on the pin diagram, see the [Mechanical, Packaging, and Orderable Information](#) section.

### 6.2 Pin Attributes

1. **Ball Number:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **Ball Name:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **Signal Name:** Signal name of all dedicated and pin multiplexed signal functions associated with a ball.

#### 备注

The *Pin Attributes* table, defines the SoC pin multiplexed signal function implemented at the pin and **does not** define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

4. **Mux Mode:** The MUXMODE value associated with each pin multiplexed signal function:
  - MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.
  - MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only valid values of MUXMODE can be used.
  - Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz\_OUT. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
  - An empty box or "-" means Not Applicable.

#### 备注

- The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when MCU\_PORz is deasserted.
- Configuring two pins to the same pin multiplexed signal function can yield unexpected results and is not supported. This can be prevented with proper software configuration.
- Configuring a pad to an undefined multiplexing mode results in undefined behavior and must be avoided.

5. **Signal Type:** Signal type and direction:

- I = Input
- O = Output
- OD = Output, with open-drain output function
- IO = Input, Output, or simultaneously Input and Output
- IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
- IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
- OZ = Output with three-state output function
- A = Analog
- CAP = LDO capacitor
- PWR = Power

- GND = Ground
6. **I/O VOLTAGE VALUE:** This column describes the IO voltage value (the corresponding power supply).  
An empty box means Not Applicable.
  7. **Ball State During Reset (RX/TX/PULL):** State of the terminal while MCU\_PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
    - RX (Input buffer)
      - Off: The input buffer is **disabled**.
      - On: The input buffer is **enabled**.
    - TX (Output buffer)
      - Off: The output buffer is **disabled**.
      - Low: The output buffer is **enabled** and drives V<sub>OL</sub>.
    - PULL (Internal pull resistors)
      - Off: Internal pull resistors are turned **off**.
      - Up: Internal **pull-up** resistor is turned on.
      - Down: Internal **pull-down** resistor is turned on.
      - NA: No internal pull resistor.
    - An empty box, or "-" means Not Applicable.
  8. **Ball State After Reset (RX/TX/PULL):** State of the terminal after MCU\_PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
    - RX (Input buffer)
      - Off: The input buffer is **disabled**.
      - On: The input buffer is **enabled**.
    - TX (Output buffer)
      - Off: The output buffer is **disabled**.
      - SS: The subsystem selected with MUXMODE determines the output buffer state.
    - PULL (Internal pull resistors)
      - Off: Internal pull resistors are turned **off**.
      - Up: Internal **pull-up resistor** is turned on.
      - Down: Internal **pull-down resistor** is turned on.
      - NA: No internal pull resistor.
    - An empty box, NA, or "-" means Not Applicable.
  9. **Mux Mode After Reset:** The value found in this column defines the **default** pin multiplexed signal function after MCU\_PORz is deasserted.
    - An empty box, NA, or "-" means Not Applicable.
  10. **PULL TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    - PU: Internal pull-up Only
    - PD: Internal pull-down Only
    - PU/PD: Internal pull-up and pull-down
    - An empty box, NA, or "-" means No internal pull.

## 备注

Configuring two pins to the same pin multiplexed signal function is not supported as this yields unexpected results. Issues can be easily prevented with the proper software configuration.

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This must be avoided.

- 
11. **Power:** The power supply of the associated I/O, when applicable.
    - An empty box, NA, or "-" means Not Applicable.
  12. **Hys:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: Hysteresis Support
    - No: **No** Hysteresis Support
    - An empty box, NA, or "-" means Not Applicable.

For more information, see the hysteresis values in [Electrical Characteristics](#) section.

13. **Voltage Buffer Type:** This column defines the buffer type associated with a terminal. This information can be used to determine the applicable Electrical Characteristics table.
  - An empty box, NA, or "-" means Not Applicable.

For electrical characteristics, refer to the appropriate buffer type table in [Electrical Characteristics](#) section.

14. **IO RET:** Yes means WKUP and IO retention supported.
15. **Pad Configuration Register Name:** This is the name of the device pad/pin configuration register.
16. **Pad Configuration Register Address:** This is the memory address of the device pad/pin configuration register.

表 6-1. Pin Attributes (ALY Package)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                       | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|--------------------------------------------------|----------|--------------------------|-------------|
| V29          | CAP_VDDS0                                                    | CAP_VDDS0       |              | CAP             |                 |                                          |                                         |                          |                |                                                  |          |                          |             |
| L27          | CAP_VDDS0_MCU                                                | CAP_VDDS0_MCU   |              | CAP             |                 |                                          |                                         |                          |                |                                                  |          |                          |             |
| L25          | CAP_VDDS1_MCU                                                | CAP_VDDS1_MCU   |              | CAP             |                 |                                          |                                         |                          |                |                                                  |          |                          |             |
| T29          | CAP_VDDS2                                                    | CAP_VDDS2       |              | CAP             |                 |                                          |                                         |                          |                |                                                  |          |                          |             |
| L26          | CAP_VDDS2_MCU                                                | CAP_VDDS2_MCU   |              | CAP             |                 |                                          |                                         |                          |                |                                                  |          |                          |             |
| P29          | CAP_VDDS5                                                    | CAP_VDDS5       |              | CAP             |                 |                                          |                                         |                          |                |                                                  |          |                          |             |
| AN30         | CSI0_RXCLKN                                                  | CSI0_RXCLKN     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AN29         | CSI0_RXCLKP                                                  | CSI0_RXCLKP     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AM28         | CSI0_RXRCALIB                                                | CSI0_RXRCALIB   |              | A               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AP32         | CSI1_RXCLKN                                                  | CSI1_RXCLKN     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AP31         | CSI1_RXCLKP                                                  | CSI1_RXCLKP     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AL28         | CSI1_RXRCALIB                                                | CSI1_RXRCALIB   |              | A               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AN32         | CSI2_RXCLKN                                                  | CSI2_RXCLKN     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AN33         | CSI2_RXCLKP                                                  | CSI2_RXCLKP     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AM31         | CSI2_RXRCALIB                                                | CSI2_RXRCALIB   |              | A               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AU33         | CSI0_RXN0                                                    | CSI0_RXN0       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                       | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|--------------------------------------------------|----------|--------------------------|-------------|
| AT32         | CSI0_RXN1                                                    | CSI0_RXN1       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AV31         | CSI0_RXN2                                                    | CSI0_RXN2       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AR30         | CSI0_RXN3                                                    | CSI0_RXN3       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AU32         | CSI0_RXP0                                                    | CSI0_RXP0       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AT31         | CSI0_RXP1                                                    | CSI0_RXP1       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AV30         | CSI0_RXP2                                                    | CSI0_RXP2       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AR29         | CSI0_RXP3                                                    | CSI0_RXP3       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AT35         | CSI1_RXN0                                                    | CSI1_RXN0       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AU36         | CSI1_RXN1                                                    | CSI1_RXN1       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AR33         | CSI1_RXN2                                                    | CSI1_RXN2       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AV34         | CSI1_RXN3                                                    | CSI1_RXN3       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AT34         | CSI1_RXP0                                                    | CSI1_RXP0       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                       | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|--------------------------------------------------|----------|--------------------------|-------------|
| AU35         | CSI1_RXP1                                                    | CSI1_RXP1       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AR32         | CSI1_RXP2                                                    | CSI1_RXP2       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AV33         | CSI1_RXP3                                                    | CSI1_RXP3       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX0_1 /<br>VDDA_1P8_C<br>SIRX0_1 |          | D-PHY                    |             |
| AR36         | CSI2_RXN0                                                    | CSI2_RXN0       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AT38         | CSI2_RXN1                                                    | CSI2_RXN1       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AP35         | CSI2_RXN2                                                    | CSI2_RXN2       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AV37         | CSI2_RXN3                                                    | CSI2_RXN3       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AR35         | CSI2_RXP0                                                    | CSI2_RXP0       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AT37         | CSI2_RXP1                                                    | CSI2_RXP1       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AP34         | CSI2_RXP2                                                    | CSI2_RXP2       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AV36         | CSI2_RXP3                                                    | CSI2_RXP3       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_C<br>SIRX2 /<br>VDDA_1P8_C<br>SIRX2     |          | D-PHY                    |             |
| AB2          | DDR0_CKN                                                     | DDR0_CKN        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDS_DDR /<br>VDDS_DDR_ C0                       |          | DDR                      |             |
| AC1          | DDR0_CKP                                                     | DDR0_CKP        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDS_DDR /<br>VDDS_DDR_ C0                       |          | DDR                      |             |



表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]               | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|--------------------------|----------|--------------------------|-------------|
| AD5          | DDR0_RESETh                                                  | DDR0_RESETh     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C0 |          | DDR                      |             |
| AC8          | DDR0_RET                                                     | DDR0_RET        |              | I               | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C0 |          | DDR                      |             |
| A11          | DDR1_CKN                                                     | DDR1_CKN        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1 |          | DDR                      |             |
| B10          | DDR1_CKP                                                     | DDR1_CKP        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1 |          | DDR                      |             |
| G10          | DDR1_RESETh                                                  | DDR1_RESETh     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1 |          | DDR                      |             |
| G8           | DDR1_RET                                                     | DDR1_RET        |              | I               | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C1 |          | DDR                      |             |
| K1           | DDR2_CKN                                                     | DDR2_CKN        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| L2           | DDR2_CKP                                                     | DDR2_CKP        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| J5           | DDR2_RESETh                                                  | DDR2_RESETh     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| L8           | DDR2_RET                                                     | DDR2_RET        |              | I               | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| B25          | DDR3_CKN                                                     | DDR3_CKN        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |
| A24          | DDR3_CKP                                                     | DDR3_CKP        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |
| C23          | DDR3_RESETh                                                  | DDR3_RESETh     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |
| G27          | DDR3_RET                                                     | DDR3_RET        |              | I               | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |
| AD2          | DDR0_CA0                                                     | DDR0_CA0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C0 |          | DDR                      |             |
| AC5          | DDR0_CA1                                                     | DDR0_CA1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C0 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| AB4          | DDR0_CA2                                                     | DDR0_CA2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AC4          | DDR0_CA3                                                     | DDR0_CA3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AB3          | DDR0_CA4                                                     | DDR0_CA4        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AC3          | DDR0_CA5                                                     | DDR0_CA5        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AE8          | DDR0_CAL0                                                    | DDR0_CAL0       |              | A               | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AB6          | DDR0_CKE0                                                    | DDR0_CKE0       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AD3          | DDR0_CKE1                                                    | DDR0_CKE1       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AD7          | DDR0_CS0_0                                                   | DDR0_CS0_0      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AC7          | DDR0_CS0_1                                                   | DDR0_CS0_1      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AB7          | DDR0_CS1_0                                                   | DDR0_CS1_0      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AD6          | DDR0_CS1_1                                                   | DDR0_CS1_1      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| V3           | DDR0_DM0                                                     | DDR0_DM0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AA4          | DDR0_DM1                                                     | DDR0_DM1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AG2          | DDR0_DM2                                                     | DDR0_DM2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AJ5          | DDR0_DM3                                                     | DDR0_DM3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| U2           | DDR0_DQ0                                                     | DDR0_DQ0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| U4           | DDR0_DQ1                                                     | DDR0_DQ1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| W6           | DDR0_DQ2                                                     | DDR0_DQ2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| W5           | DDR0_DQ3                                                     | DDR0_DQ3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| V4           | DDR0_DQ4                                                     | DDR0_DQ4        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| V7           | DDR0_DQ5                                                     | DDR0_DQ5        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| U5           | DDR0_DQ6                                                     | DDR0_DQ6        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| V6           | DDR0_DQ7                                                     | DDR0_DQ7        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| Y2           | DDR0_DQ8                                                     | DDR0_DQ8        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| W3           | DDR0_DQ9                                                     | DDR0_DQ9        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AA3          | DDR0_DQ10                                                    | DDR0_DQ10       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| W2           | DDR0_DQ11                                                    | DDR0_DQ11       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AA6          | DDR0_DQ12                                                    | DDR0_DQ12       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| Y4           | DDR0_DQ13                                                    | DDR0_DQ13       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| Y5           | DDR0_DQ14                                                    | DDR0_DQ14       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AA7          | DDR0_DQ15                                                    | DDR0_DQ15       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AF2          | DDR0_DQ16                                                    | DDR0_DQ16       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| AE7          | DDR0_DQ17                                                    | DDR0_DQ17       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AG3          | DDR0_DQ18                                                    | DDR0_DQ18       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AF5          | DDR0_DQ19                                                    | DDR0_DQ19       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AE6          | DDR0_DQ20                                                    | DDR0_DQ20       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AF4          | DDR0_DQ21                                                    | DDR0_DQ21       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AE3          | DDR0_DQ22                                                    | DDR0_DQ22       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AE4          | DDR0_DQ23                                                    | DDR0_DQ23       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AG5          | DDR0_DQ24                                                    | DDR0_DQ24       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AH3          | DDR0_DQ25                                                    | DDR0_DQ25       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AJ2          | DDR0_DQ26                                                    | DDR0_DQ26       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AH4          | DDR0_DQ27                                                    | DDR0_DQ27       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AJ4          | DDR0_DQ28                                                    | DDR0_DQ28       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AH6          | DDR0_DQ29                                                    | DDR0_DQ29       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AH7          | DDR0_DQ30                                                    | DDR0_DQ30       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AG6          | DDR0_DQ31                                                    | DDR0_DQ31       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| V1           | DDR0_QS0N                                                    | DDR0_QS0N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| U1           | DDR0_QS0P                                                    | DDR0_QS0P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| Y1           | DDR0_QS1N                                                    | DDR0_QS1N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AA1          | DDR0_QS1P                                                    | DDR0_QS1P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AE1          | DDR0_QS2N                                                    | DDR0_QS2N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AF1          | DDR0_QS2P                                                    | DDR0_QS2P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AH1          | DDR0_QS3N                                                    | DDR0_QS3N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| AJ1          | DDR0_QS3P                                                    | DDR0_QS3P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C0 |          | DDR                      |             |
| F12          | DDR1_CA0                                                     | DDR1_CA0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C12          | DDR1_CA1                                                     | DDR1_CA1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B12          | DDR1_CA2                                                     | DDR1_CA2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C11          | DDR1_CA3                                                     | DDR1_CA3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D12          | DDR1_CA4                                                     | DDR1_CA4        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E10          | DDR1_CA5                                                     | DDR1_CA5        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| G14          | DDR1_CAL0                                                    | DDR1_CAL0       |              | A               | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D11          | DDR1_CKE0                                                    | DDR1_CKE0       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C10          | DDR1_CKE1                                                    | DDR1_CKE1       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| E11          | DDR1_CS0_0                                                   | DDR1_CS0_0      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| G11          | DDR1_CS0_1                                                   | DDR1_CS0_1      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F10          | DDR1_CS1_0                                                   | DDR1_CS1_0      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| G12          | DDR1_CS1_1                                                   | DDR1_CS1_1      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E17          | DDR1_DM0                                                     | DDR1_DM0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C15          | DDR1_DM1                                                     | DDR1_DM1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D8           | DDR1_DM2                                                     | DDR1_DM2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C1           | DDR1_DM3                                                     | DDR1_DM3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F16          | DDR1_DQ0                                                     | DDR1_DQ0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| G16          | DDR1_DQ1                                                     | DDR1_DQ1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F15          | DDR1_DQ2                                                     | DDR1_DQ2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E15          | DDR1_DQ3                                                     | DDR1_DQ3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D16          | DDR1_DQ4                                                     | DDR1_DQ4        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C16          | DDR1_DQ5                                                     | DDR1_DQ5        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B17          | DDR1_DQ6                                                     | DDR1_DQ6        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D17          | DDR1_DQ7                                                     | DDR1_DQ7        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| B15          | DDR1_DQ8                                                     | DDR1_DQ8        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B14          | DDR1_DQ9                                                     | DDR1_DQ9        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C13          | DDR1_DQ10                                                    | DDR1_DQ10       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D13          | DDR1_DQ11                                                    | DDR1_DQ11       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F13          | DDR1_DQ12                                                    | DDR1_DQ12       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| G13          | DDR1_DQ13                                                    | DDR1_DQ13       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E14          | DDR1_DQ14                                                    | DDR1_DQ14       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D14          | DDR1_DQ15                                                    | DDR1_DQ15       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| E8           | DDR1_DQ16                                                    | DDR1_DQ16       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| G9           | DDR1_DQ17                                                    | DDR1_DQ17       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| F9           | DDR1_DQ18                                                    | DDR1_DQ18       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| D9           | DDR1_DQ19                                                    | DDR1_DQ19       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C9           | DDR1_DQ20                                                    | DDR1_DQ20       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B8           | DDR1_DQ21                                                    | DDR1_DQ21       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B7           | DDR1_DQ22                                                    | DDR1_DQ22       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C7           | DDR1_DQ23                                                    | DDR1_DQ23       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| B2           | DDR1_DQ24                                                    | DDR1_DQ24       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B3           | DDR1_DQ25                                                    | DDR1_DQ25       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B4           | DDR1_DQ26                                                    | DDR1_DQ26       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| B5           | DDR1_DQ27                                                    | DDR1_DQ27       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A6           | DDR1_DQ28                                                    | DDR1_DQ28       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C5           | DDR1_DQ29                                                    | DDR1_DQ29       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C6           | DDR1_DQ30                                                    | DDR1_DQ30       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| C3           | DDR1_DQ31                                                    | DDR1_DQ31       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A17          | DDR1_QS0N                                                    | DDR1_QS0N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A16          | DDR1_QS0P                                                    | DDR1_QS0P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A14          | DDR1_QS1N                                                    | DDR1_QS1N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A13          | DDR1_QS1P                                                    | DDR1_QS1P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A9           | DDR1_QS2N                                                    | DDR1_QS2N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A8           | DDR1_QS2P                                                    | DDR1_QS2P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A4           | DDR1_QS3N                                                    | DDR1_QS3N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |
| A3           | DDR1_QS3P                                                    | DDR1_QS3P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C1 |          | DDR                      |             |



表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| K3           | DDR2_CA0                                                     | DDR2_CA0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| L3           | DDR2_CA1                                                     | DDR2_CA1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| K5           | DDR2_CA2                                                     | DDR2_CA2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| L4           | DDR2_CA3                                                     | DDR2_CA3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| K4           | DDR2_CA4                                                     | DDR2_CA4        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| L7           | DDR2_CA5                                                     | DDR2_CA5        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| U7           | DDR2_CAL0                                                    | DDR2_CAL0       |              | A               | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| L6           | DDR2_CKE0                                                    | DDR2_CKE0       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| J2           | DDR2_CKE1                                                    | DDR2_CKE1       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| J3           | DDR2_CSn0_0                                                  | DDR2_CSn0_0     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| J6           | DDR2_CSn0_1                                                  | DDR2_CSn0_1     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| J7           | DDR2_CSn1_0                                                  | DDR2_CSn1_0     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| K7           | DDR2_CSn1_1                                                  | DDR2_CSn1_1     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| T2           | DDR2_DM0                                                     | DDR2_DM0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| M6           | DDR2_DM1                                                     | DDR2_DM1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| G4           | DDR2_DM2                                                     | DDR2_DM2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| D5           | DDR2_DM3                                                     | DDR2_DM3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| T4           | DDR2_DQ0                                                     | DDR2_DQ0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| R6           | DDR2_DQ1                                                     | DDR2_DQ1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| R3           | DDR2_DQ2                                                     | DDR2_DQ2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| R4           | DDR2_DQ3                                                     | DDR2_DQ3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| P6           | DDR2_DQ4                                                     | DDR2_DQ4        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| P5           | DDR2_DQ5                                                     | DDR2_DQ5        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| T5           | DDR2_DQ6                                                     | DDR2_DQ6        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| R7           | DDR2_DQ7                                                     | DDR2_DQ7        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| N2           | DDR2_DQ8                                                     | DDR2_DQ8        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| N4           | DDR2_DQ9                                                     | DDR2_DQ9        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| P2           | DDR2_DQ10                                                    | DDR2_DQ10       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| P3           | DDR2_DQ11                                                    | DDR2_DQ11       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| M7           | DDR2_DQ12                                                    | DDR2_DQ12       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| N5           | DDR2_DQ13                                                    | DDR2_DQ13       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| M4           | DDR2_DQ14                                                    | DDR2_DQ14       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| M3           | DDR2_DQ15                                                    | DDR2_DQ15       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| F3           | DDR2_DQ16                                                    | DDR2_DQ16       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| G7           | DDR2_DQ17                                                    | DDR2_DQ17       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| H6           | DDR2_DQ18                                                    | DDR2_DQ18       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| H4           | DDR2_DQ19                                                    | DDR2_DQ19       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| G2           | DDR2_DQ20                                                    | DDR2_DQ20       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| H3           | DDR2_DQ21                                                    | DDR2_DQ21       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| G5           | DDR2_DQ22                                                    | DDR2_DQ22       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| F2           | DDR2_DQ23                                                    | DDR2_DQ23       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| E4           | DDR2_DQ24                                                    | DDR2_DQ24       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| D2           | DDR2_DQ25                                                    | DDR2_DQ25       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| F6           | DDR2_DQ26                                                    | DDR2_DQ26       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| F5           | DDR2_DQ27                                                    | DDR2_DQ27       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| E3           | DDR2_DQ28                                                    | DDR2_DQ28       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| E7           | DDR2_DQ29                                                    | DDR2_DQ29       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |
| E6           | DDR2_DQ30                                                    | DDR2_DQ30       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C2 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]               | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|--------------------------|----------|--------------------------|-------------|
| D4           | DDR2_DQ31                                                    | DDR2_DQ31       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| R1           | DDR2_DQS0N                                                   | DDR2_DQS0N      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| T1           | DDR2_DQS0P                                                   | DDR2_DQS0P      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| M1           | DDR2_DQS1N                                                   | DDR2_DQS1N      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| N1           | DDR2_DQS1P                                                   | DDR2_DQS1P      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| G1           | DDR2_DQS2N                                                   | DDR2_DQS2N      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| H1           | DDR2_DQS2P                                                   | DDR2_DQS2P      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| D1           | DDR2_DQS3N                                                   | DDR2_DQS3N      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| E1           | DDR2_DQS3P                                                   | DDR2_DQS3P      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C2 |          | DDR                      |             |
| D25          | DDR3_CA0                                                     | DDR3_CA0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |
| B23          | DDR3_CA1                                                     | DDR3_CA1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |
| D24          | DDR3_CA2                                                     | DDR3_CA2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |
| C24          | DDR3_CA3                                                     | DDR3_CA3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |
| E23          | DDR3_CA4                                                     | DDR3_CA4        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |
| F23          | DDR3_CA5                                                     | DDR3_CA5        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |
| F18          | DDR3_CAL0                                                    | DDR3_CAL0       |              | A               | 1.1 V           |                                          |                                         |                          |                | VDDSD_DDR / VDDSD_DDR_C3 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| C25          | DDR3_CKE0                                                    | DDR3_CKE0       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| G24          | DDR3_CKE1                                                    | DDR3_CKE1       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| G23          | DDR3_CSn0_0                                                  | DDR3_CSn0_0     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| G25          | DDR3_CSn0_1                                                  | DDR3_CSn0_1     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| F25          | DDR3_CSn1_0                                                  | DDR3_CSn1_0     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| E24          | DDR3_CSn1_1                                                  | DDR3_CSn1_1     |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| E18          | DDR3_DM0                                                     | DDR3_DM0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| D21          | DDR3_DM1                                                     | DDR3_DM1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| C28          | DDR3_DM2                                                     | DDR3_DM2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| E30          | DDR3_DM3                                                     | DDR3_DM3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| D18          | DDR3_DQ0                                                     | DDR3_DQ0        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| B18          | DDR3_DQ1                                                     | DDR3_DQ1        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| C19          | DDR3_DQ2                                                     | DDR3_DQ2        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| D19          | DDR3_DQ3                                                     | DDR3_DQ3        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| F20          | DDR3_DQ4                                                     | DDR3_DQ4        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| E20          | DDR3_DQ5                                                     | DDR3_DQ5        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| G19          | DDR3_DQ6                                                     | DDR3_DQ6        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| F19          | DDR3_DQ7                                                     | DDR3_DQ7        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| E21          | DDR3_DQ8                                                     | DDR3_DQ8        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| G21          | DDR3_DQ9                                                     | DDR3_DQ9        |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| F22          | DDR3_DQ10                                                    | DDR3_DQ10       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| D22          | DDR3_DQ11                                                    | DDR3_DQ11       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| C22          | DDR3_DQ12                                                    | DDR3_DQ12       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| B21          | DDR3_DQ13                                                    | DDR3_DQ13       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| B20          | DDR3_DQ14                                                    | DDR3_DQ14       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| C20          | DDR3_DQ15                                                    | DDR3_DQ15       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| B28          | DDR3_DQ16                                                    | DDR3_DQ16       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| B27          | DDR3_DQ17                                                    | DDR3_DQ17       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| C26          | DDR3_DQ18                                                    | DDR3_DQ18       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| D26          | DDR3_DQ19                                                    | DDR3_DQ19       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| F26          | DDR3_DQ20                                                    | DDR3_DQ20       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| G26          | DDR3_DQ21                                                    | DDR3_DQ21       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------|----------|--------------------------|-------------|
| E27          | DDR3_DQ22                                                    | DDR3_DQ22       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| D27          | DDR3_DQ23                                                    | DDR3_DQ23       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| F29          | DDR3_DQ24                                                    | DDR3_DQ24       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| G29          | DDR3_DQ25                                                    | DDR3_DQ25       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| F28          | DDR3_DQ26                                                    | DDR3_DQ26       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| E28          | DDR3_DQ27                                                    | DDR3_DQ27       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| D29          | DDR3_DQ28                                                    | DDR3_DQ28       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| C29          | DDR3_DQ29                                                    | DDR3_DQ29       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| B30          | DDR3_DQ30                                                    | DDR3_DQ30       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| D30          | DDR3_DQ31                                                    | DDR3_DQ31       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| A19          | DDR3_QS0N                                                    | DDR3_QS0N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| A18          | DDR3_QS0P                                                    | DDR3_QS0P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| A22          | DDR3_QS1N                                                    | DDR3_QS1N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| A21          | DDR3_QS1P                                                    | DDR3_QS1P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| A27          | DDR3_QS2N                                                    | DDR3_QS2N       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |
| A26          | DDR3_QS2P                                                    | DDR3_QS2P       |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3 |          | DDR                      |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                      | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------|----------|--------------------------|-------------|
| A30          | DDR3_DQS3N                                                   | DDR3_DQS3N      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3                            |          | DDR                      |             |
| A29          | DDR3_DQS3P                                                   | DDR3_DQS3P      |              | IO              | 1.1 V           |                                          |                                         |                          |                | VDDSDDR / VDDSDDR_C3                            |          | DDR                      |             |
| AP22         | DP0_AUXN                                                     | DP0_AUXN        |              | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA1P8S ERDES2_4                               |          | AUX-PHY                  |             |
| AP23         | DP0_AUXP                                                     | DP0_AUXP        |              | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA1P8S ERDES2_4                               |          | AUX-PHY                  |             |
| AP26         | DSI0_TXCLKN                                                  | CSI0_TXCLKN     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA0P8D SITX / VDDA0P8D SITX_C / VDDA1P8D SITX |          | D-PHY                    |             |
|              |                                                              | DSI0_TXCLKN     |              | O               |                 |                                          |                                         |                          |                |                                                 |          |                          |             |
| AP25         | DSI0_TXCLKP                                                  | DSI0_TXCLKP     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA0P8D SITX / VDDA0P8D SITX_C / VDDA1P8D SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXCLKP     |              | O               |                 |                                          |                                         |                          |                |                                                 |          |                          |             |
| AM24         | DSI0_TXRCALIB                                                | DSI0_TXRCALIB   |              | A               | 1.8 V           |                                          |                                         |                          |                | VDDA0P8D SITX / VDDA0P8D SITX_C / VDDA1P8D SITX |          | D-PHY                    |             |
| AP29         | DSI1_TXCLKN                                                  | DSI1_TXCLKN     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA0P8D SITX / VDDA0P8D SITX_C / VDDA1P8D SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXCLKN     |              | O               |                 |                                          |                                         |                          |                |                                                 |          |                          |             |
| AP28         | DSI1_TXCLKP                                                  | DSI1_TXCLKP     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA0P8D SITX / VDDA0P8D SITX_C / VDDA1P8D SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXCLKP     |              | O               |                 |                                          |                                         |                          |                |                                                 |          |                          |             |
| AL22         | DSI1_TXRCALIB                                                | DSI1_TXRCALIB   |              | A               | 1.8 V           |                                          |                                         |                          |                | VDDA0P8D SITX / VDDA0P8D SITX_C / VDDA1P8D SITX |          | D-PHY                    |             |
| AU27         | DSI0_TXN0                                                    | CSI0_TXN0       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA0P8D SITX / VDDA0P8D SITX_C / VDDA1P8D SITX |          | D-PHY                    |             |
|              |                                                              | DSI0_TXN0       |              | IO              |                 |                                          |                                         |                          |                |                                                 |          |                          |             |



表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------------------------------------------------------|----------|--------------------------|-------------|
| AT26         | DSI0_TXN1                                                    | CSI0_TXN1       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | DSI0_TXN1       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AR27         | DSI0_TXN2                                                    | DSI0_TXN2       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXN2       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AN24         | DSI0_TXN3                                                    | DSI0_TXN3       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXN3       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AU26         | DSI0_TXP0                                                    | CSI0_TXP0       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | DSI0_TXP0       |              | IO              |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AT25         | DSI0_TXP1                                                    | CSI0_TXP1       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | DSI0_TXP1       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AR26         | DSI0_TXP2                                                    | DSI0_TXP2       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXP2       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AN23         | DSI0_TXP3                                                    | DSI0_TXP3       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI0_TXP3       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AT29         | DSI1_TXN0                                                    | CSI1_TXN0       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | DSI1_TXN0       |              | IO              |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                           | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------------------------------------------------------|----------|--------------------------|-------------|
| AN27         | DSI1_TXN1                                                    | CSI1_TXN1       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | DSI1_TXN1       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AV28         | DSI1_TXN2                                                    | CSI1_TXN2       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | DSI1_TXN2       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AU30         | DSI1_TXN3                                                    | CSI1_TXN3       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | DSI1_TXN3       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AT28         | DSI1_TXP0                                                    | DSI1_TXP0       |              | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXP0       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AN26         | DSI1_TXP1                                                    | CSI1_TXP1       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | DSI1_TXP1       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AV27         | DSI1_TXP2                                                    | DSI1_TXP2       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | CSI1_TXP2       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |
| AU29         | DSI1_TXP3                                                    | CSI1_TXP3       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_D<br>SITX /<br>VDDA_0P8_D<br>SITX_C /<br>VDDA_1P8_D<br>SITX |          | D-PHY                    |             |
|              |                                                              | DSI1_TXP3       |              | O               |                 |                                          |                                         |                          |                |                                                                      |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| AD36         | ECAP0_IN_APWM_OUT<br>PADCFG:<br>PADCONFIG_49<br>0x0011C0C4   | ECAP0_IN_APWM_OUT | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2     | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP4_AXR2       | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | CPTS0_RFT_CLK     | 2            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | HYP1_TXFLCLK      | 3            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCAN12_TX         | 4            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | VOUT0_DATA23      | 5            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | GPMC0_AD5         | 6            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | GPIO0_49          | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | SPI6_D0           | 8            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | SYNC0_OUT         | 9            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | TRC_DATA1         | 10           | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | UART2_CTSn        | 11           | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | CPTS0_HW1TSPUSH   | 12           | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | I2C1_SCL          | 13           | IOD             |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | UART3_RXD         | 14           | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| F35          | EMU0<br>PADCFG:<br>WKUP_PADCONFIG_75<br>0x4301C12C           | EMU0              | 0            | IO              | 1.8 V/3.3 V     | On / Off / Up                            | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | No          |
| H34          | EMU1<br>PADCFG:<br>WKUP_PADCONFIG_76<br>0x4301C130           | EMU1              | 0            | IO              | 1.8 V/3.3 V     | On / Off / Up                            | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_OBSCLK0       | 15           | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
| AN35         | EXTINTn<br>PADCFG:<br>PADCONFIG_0<br>0x0011C000              | EXTINTn           | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / SS / Off                          | 7                        |                | VDDSHV0     | Yes      | I2C OPEN DRAIN           | No          |
|              |                                                              | GPIO0_0           | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AJ32         | EXT_REFCLK1<br>PADCFG:<br>PADCONFIG_50<br>0x0011C0C8         | EXT_REFCLK1     | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP4_ACLKX    | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA16    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_TXFLDAT    | 3            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCAN1_RX        | 4            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD6       | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_50        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SYNC1_OUT       | 9            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_CLK         | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART2_RTSn      | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | CPTS0_HW2TSPUSH | 12           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C1_SDA        | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART3_TXD       | 14           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              |                 |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |
| AL32         | GPIO0_11<br>PADCFG:<br>PADCONFIG_11<br>0x0011C02C            | MCAN17_TX       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA18    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A14       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_11        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_CS3        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA25      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CSn2      | 12           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART7_RXD       | 13           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AK37         | GPIO0_12<br>PADCFG:<br>PADCONFIG_12<br>0x0011C030            | MCAN12_RX       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA17    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_RXFLDAT    | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA22    | 5            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD4       | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_12        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI6_CLK        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP1_I         | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA2       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_CTSn      | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_RXD       | 12           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AN36         | I2C0_SCL<br>PADCFG:<br>PADCONFIG_56<br>0x0011C0E0            | I2C0_SCL        | 0            | IOD             | 1.8 V/3.3 V     | Off / Off / Off                          | On / SS / Off                           | 7                        |                | VDDSHV0    | Yes      | I2C OPEN DRAIN           | No          |
|              |                                                              | GPIO0_56        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |

**表 6-1. Pin Attributes (ALY Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AP37         | I2C0_SDA<br>PADCFG:<br>PADCONFIG_57<br>0x0011C0E4            | I2C0_SDA        | 0            | IOD             | 1.8 V/3.3 V     | Off / Off / Off                          | On / SS / Off                           | 7                        |                | VDDSHV0    | Yes      | I2C OPEN DRAIN           | No          |
|              |                                                              | GPIO0_57        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
| AE38         | MCAN0_RX<br>PADCFG:<br>PADCONFIG_26<br>0x0011C068            | MCAN0_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP4_AXR1     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA3     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD15      | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_26        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_CS0        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_A       | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA16      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART2_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_RTSn      | 12           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_D0         | 13           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
| AF38         | MCAN0_TX<br>PADCFG:<br>PADCONFIG_25<br>0x0011C064            | MCAN0_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_AXR2     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA4     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD14      | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_25        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_CS1        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_B       | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA11      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART2_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_CTSn      | 12           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C3_SCL        | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AH38         | MCAN1_RX<br>PADCFG:<br>PADCONFIG_28<br>0x0011C070            | MCAN1_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP4_AXR3     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA1     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA19    | 5            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_BE0n_CLE  | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_28        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_D0         | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_SYNCI   | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA5       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART3_RTSn      | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AJ37         | MCAN1_TX<br>PADCFG:<br>PADCONFIG_27<br>0x0011C06C            | MCAN1_TX          | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP4_AFSX       | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_EXTCLKIN    | 2            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_TXPMCLK      | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DSS_FSYNCO        | 4            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD7         | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_27          | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN5    | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_CTL           | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_TXD         | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AH37         | MCAN2_RX<br>PADCFG:<br>PADCONFIG_30<br>0x0011C078            | MCAN2_RX          | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | AUDIO_EXT_REFCLK1 | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_PCLK        | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CSn1        | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_30          | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI6_CS1          | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM4_B         | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA17        | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART3_TXD         | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_DIR         | 12           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C5_SDA          | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AC33         | MCAN2_TX<br>PADCFG:<br>PADCONFIG_29<br>0x0011C074            | MCAN2_TX          | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_AXR3       | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA0       | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA18      | 5            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_WAIT0       | 6            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_29          | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI6_D1           | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM1_B         | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA3         | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART3_RXD         | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_DIR         | 12           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C5_SCL          | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AJ33         | MCAN12_RX<br>PADCFG:<br>PADCONFIG_2<br>0x0011C008            | MCAN12_RX       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | UART0_DCDn      | 1            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DSS_FSYNC1      | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A23       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_2         | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_CTL         | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CSn3      | 12           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AG36         | MCAN12_TX<br>PADCFG:<br>PADCONFIG_1<br>0x0011C004            | MCAN12_TX       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | DSS_FSYNC0      | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A24       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_1         | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_CLK         | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CLK       | 12           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
| AH33         | MCAN13_RX<br>PADCFG:<br>PADCONFIG_4<br>0x0011C010            | MCAN13_RX       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | UART0_DTRn      | 1            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DSS_FSYNC3      | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A21       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_4         | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C4_SDA        | 8            | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA1       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AF33         | MCAN13_TX<br>PADCFG:<br>PADCONFIG_3<br>0x0011C00C            | MCAN13_TX       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | UART0_DSRn      | 1            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DSS_FSYNC2      | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A22       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_3         | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA0       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_WAIT2     | 12           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AK36         | MCAN14_RX<br>PADCFG:<br>PADCONFIG_6<br>0x0011C018            | MCAN14_RX       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA23    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A19       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_6         | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C5_SDA        | 8            | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA3       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AG33         | MCAN14_TX<br>PADCFG:<br>PADCONFIG_5<br>0x0011C014            | MCAN14_TX       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | UART0_RIn       | 1            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A20       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_5         | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C4_SCL        | 8            | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA2       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AJ35         | MCAN15_RX<br>PADCFG:<br>PADCONFIG_8<br>0x0011C020            | MCAN15_RX       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA21    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A17       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_8         | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI0_CS2        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA22      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C1_SCL        | 12           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AG34         | MCAN15_TX<br>PADCFG:<br>PADCONFIG_7<br>0x0011C01C            | MCAN15_TX       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA22    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A18       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_7         | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C5_SCL        | 8            | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA21      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AE33         | MCAN16_RX<br>PADCFG:<br>PADCONFIG_10<br>0x0011C028           | MCAN16_RX       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA19    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A15       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_10        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI0_CS3        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA24      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_WAIT1     | 12           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |



**表 6-1. Pin Attributes (ALY Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AH34         | MCAN16_TX<br>PADCFG:<br>PADCONFIG_9<br>0x0011C024            | MCAN16_TX       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | VOUT0_DATA20    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A16       | 6            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_9         | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_CS3        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA23      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C1_SDA        | 12           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AK35         | MCASP0_ACLKX<br>PADCFG:<br>PADCONFIG_14<br>0x0011C038        | MCAN5_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_ACLKX    | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA15    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_RXFLCLK    | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD0       | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_14        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN2  | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AK38         | MCASP0_AFSX<br>PADCFG:<br>PADCONFIG_15<br>0x0011C03C         | UART8_RXD       | 11           | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCAN5_RX        | 0            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP0_AFSX     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA14    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_RXFLDAT    | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD1       | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_15        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
| AC34         | MCASP1_ACLKX<br>PADCFG:<br>PADCONFIG_46<br>0x0011C0B8        | EHRPWM2_B       | 9            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | UART8_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCAN10_RX       | 0            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP1_ACLKX    | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DP0_HPDP        | 3            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | PCIE0_CLKREQn   | 4            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A11       | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_RD0       | 6            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_46        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP0_S         | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RTSn      | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_CS3        | 12           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_RTSn      | 13           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AD33         | MCASP1_AFSX<br>PADCFG:<br>PADCONFIG_47<br>0x0011C0BC         | MCAN11_TX       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AFSX     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A12       | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MDIO0_MDIO      | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_47        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_CS0        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP0_I         | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART0_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AD37         | MCASP2_ACLKX<br>PADCFG:<br>PADCONFIG_21<br>0x0011C054        | MCAN8_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_ACLKX    | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA8     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_TXPMCLK    | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA20    | 5            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD10      | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_21        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_CS2        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP2_S         | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA4       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART1_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_CS1        | 13           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SYNC3_OUT       | 14           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              |                 |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |
| AE37         | MCASP2_AFSX<br>PADCFG:<br>PADCONFIG_22<br>0x0011C058         | MCAN9_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_AFSX     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA7     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_TXPMDAT    | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MDIO1_MDC       | 4            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD11      | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_22        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_CS3        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_SOCA     | 9            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA9       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART1_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_CS2        | 13           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AF37         | MCASP0_AXR0<br>PADCFG:<br>PADCONFIG_16<br>0x0011C040         | MCAN6_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR0     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOU0_DATA13     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_TXFLCLK    | 3            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD2       | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_16        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_CS2        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM2_A       | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA14      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_CLK        | 13           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART8_CTSn      | 14           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AG37         | MCASP0_AXR1<br>PADCFG:<br>PADCONFIG_17<br>0x0011C044         | MCAN6_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR1     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOU0_DATA12     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_TXFLDAT    | 3            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | OBCLK1          | 4            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD3       | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_17        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_CS3        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_SYNCO   | 9            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA12      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_CS0        | 13           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
| AK33         | MCASP0_AXR2<br>PADCFG:<br>PADCONFIG_18<br>0x0011C048         | MCAN7_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR2     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOU0_DATA11     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_RXFLCLK    | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_ADVn_ALE  | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_18        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP2_A         | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA10      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_CTSn      | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_WPn       | 12           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_CTSn      | 13           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AJ38         | MCASP0_AXR3<br>PADCFG:<br>PADCONFIG_31<br>0x0011C07C         | MCAN3_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR3     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA2     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_BE1n      | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_31        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_CLK        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN0  | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA7       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART3_CTSn      | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_CS1        | 12           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI7_D1         | 13           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
| AK34         | MCASP0_AXR4<br>PADCFG:<br>PADCONFIG_32<br>0x0011C080         | MCAN3_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR4     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_HSYNC     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_TXPMDAT    | 3            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP0_HSYNC | 4            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP2_HSYNC | 5            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_OEn_REn   | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_32        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI6_CS2        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM5_B       | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA18      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AG38         | MCASP0_AXR5<br>PADCFG:<br>PADCONFIG_33<br>0x0011C084         | I2C4_SDA        | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCAN4_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR5     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DE        | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP1_ACLKR    | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP0_DE    | 4            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP2_DE    | 5            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CS0n      | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_33        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI6_CS3        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM5_A       | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA19      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C4_SCL        | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AF36         | MCASP0_AXR6<br>PADCFG:<br>PADCONFIG_34<br>0x0011C088         | MCAN4_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR6     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VSYNC     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP1_AFSR     | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP0_VSYNC | 4            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_VP2_VSYNC | 5            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CLKOUT    | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_34        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_CS2        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN4  | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA20      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI5_D1         | 11           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_FCLK_MUX  | 12           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AE35         | MCASP0_AXR7<br>PADCFG:<br>PADCONFIG_35<br>0x0011C08C         | MCAN5_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR7     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP4_ACLKR    | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A0        | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_TD0       | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_35        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A14       | 8            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_A       | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_CSn2      | 12           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | USB0_DRVVBUS    | 14           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              |                 |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |
| AC35         | MCASP0_AXR8<br>PADCFG:<br>PADCONFIG_36<br>0x0011C090         | MCAN5_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR8     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP4_AFSR     | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A1        | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_TD1       | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_36        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_RXD0      | 8            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN3  | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AG35         | MCASP0_AXR9<br>PADCFG:<br>PADCONFIG_37<br>0x0011C094         | MCAN6_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR9     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP4_AXR4     | 2            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A2        | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_TD2       | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_37        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_RXD1      | 8            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_SYNC0   | 9            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_CTSn      | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AH36         | MCASP0_AXR10<br>PADCFG:<br>PADCONFIG_38<br>0x0011C098        | MCAN6_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR10    | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A3        | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_TD3       | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_38        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_CRS_DV    | 8            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_SYNCI   | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RTSn      | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AF35         | MCASP0_AXR11<br>PADCFG:<br>PADCONFIG_39<br>0x0011C09C        | MCAN7_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR11    | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DSS_FSYNC2      | 4            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A4        | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_TX_CTL    | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_39        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_RX_ER     | 8            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_B       | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_CS1        | 10           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |

**表 6-1. Pin Attributes (ALY Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AD34         | MCASP0_AXR12<br>PADCFG:<br>PADCONFIG_40<br>0x0011C0A0        | MCAN7_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR12    | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP2_ACLKR    | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | DSS_FSYNC3      | 4            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A5        | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_RD1       | 6            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_40        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_TXD0      | 8            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_SOCB     | 9            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_CLK        | 10           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AJ36         | MCASP0_AXR13<br>PADCFG:<br>PADCONFIG_41<br>0x0011C0A4        | MCAN8_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR13    | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP2_AFSR     | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A6        | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_RD2       | 6            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_41        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII_REF_CLK    | 8            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM4_A       | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_CS0        | 10           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_CTSn      | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART7_RXD       | 13           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AF34         | MCASP0_AXR14<br>PADCFG:<br>PADCONFIG_42<br>0x0011C0A8        | MCAN8_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR14    | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP2_AXR4     | 2            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP0_ACLKR    | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A7        | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_RD3       | 6            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_42        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | CLKOUT          | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP0_A         | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_D0         | 10           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_RTSn      | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART7_TXD       | 13           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AE34         | MCASP0_AXR15<br>PADCFG:<br>PADCONFIG_43<br>0x0011C0AC        | MCAN9_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP0_AXR15    | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCASP0_AFSR     | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A8        | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_RX_CTL    | 6            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_43        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_TX_EN     | 8            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP0_B         | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI2_D1         | 10           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART8_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C1_SCL        | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AD38         | MCASP1_AXR0<br>PADCFG:<br>PADCONFIG_48<br>0x0011C0C0         | MCAN11_RX       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AXR0     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A13       | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MDIO0_MDC       | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_48        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_CLK        | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP1_S         | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART0_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_WAIT3     | 12           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SYNC2_OUT       | 14           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              |                 |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |
| AC32         | MCASP1_AXR1<br>PADCFG:<br>PADCONFIG_19<br>0x0011C04C         | MCAN7_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AXR1     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA10    | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_RXPMCLK    | 3            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD8       | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_19        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_D0         | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM_TZn_IN1  | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA8       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART0_CTSn      | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_RXD       | 12           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C2_SCL        | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |



表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AC37         | MCASP1_AXR2<br>PADCFG:<br>PADCONFIG_20<br>0x0011C050         | MCAN8_TX        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AXR2     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA9     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP1_RXPMDAT    | 3            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA21    | 5            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD9       | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_20        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI3_D1         | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP2_B         | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA6       | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART0_RTSn      | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART9_TXD       | 12           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C2_SDA        | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AL33         | MCASP1_AXR3<br>PADCFG:<br>PADCONFIG_44<br>0x0011C0B0         | MCAN9_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AXR3     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | PCIE2_CLKREQn   | 4            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A9        | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI1_RXC       | 6            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_44        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RMII1_TXD1      | 8            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP1_A         | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART8_TXD       | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C1_SDA        | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AL34         | MCASP1_AXR4<br>PADCFG:<br>PADCONFIG_45<br>0x0011C0B4         | MCAN10_TX       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP1_AXR4     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | PCIE3_CLKREQn   | 4            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_A10       | 5            | OZ              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | RGMI11_TXC      | 6            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_45        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP1_B         | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RXD       | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |

**表 6-1. Pin Attributes (ALY Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AC36         | MCASP2_AXR0<br>PADCFG:<br>PADCONFIG_23<br>0x0011C05C         | MCAN9_RX        | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_AXR0     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA6     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_RXPMCLK    | 3            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MDIO1_MDIO      | 4            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD12      | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_23        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EQEP2_I         | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA15      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART1_CTSn      | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_RXD       | 12           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AE36         | MCASP2_AXR1<br>PADCFG:<br>PADCONFIG_24<br>0x0011C060         | MCAN17_RX       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2    | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCASP2_AXR1     | 1            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | VOUT0_DATA5     | 2            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | HYP0_RXPMDAT    | 3            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPMC0_AD13      | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_24        | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM1_A       | 9            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TRC_DATA13      | 10           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART1_RTSn      | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART6_TXD       | 12           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C3_SDA        | 13           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
| U35          | MCU_ADC0_REFN                                                | MCU_ADC0_REFN   |              | A               | 1.8 V           |                                          |                                         |                          |                | VDDA_ADC0  |          | ADC12B                   | No          |
| R35          | MCU_ADC0_REFP                                                | MCU_ADC0_REFP   |              | A               | 1.8 V           |                                          |                                         |                          |                | VDDA_ADC0  |          | ADC12B                   | No          |
| W35          | MCU_ADC1_REFN                                                | MCU_ADC1_REFN   |              | A               | 1.8 V           |                                          |                                         |                          |                | VDDA_ADC1  |          | ADC12B                   | No          |
| AA35         | MCU_ADC1_REFP                                                | MCU_ADC1_REFP   |              | A               | 1.8 V           |                                          |                                         |                          |                | VDDA_ADC1  |          | ADC12B                   | No          |
| P36          | MCU_ADC0_AIN0<br>PADCFG:<br>WKUP_PADCONFIG_77<br>0x4301C134  | MCU_ADC0_AIN0   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_71   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| V36          | MCU_ADC0_AIN1<br>PADCFG:<br>WKUP_PADCONFIG_78<br>0x4301C138  | MCU_ADC0_AIN1   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_72   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| T34          | MCU_ADC0_AIN2<br>PADCFG:<br>WKUP_PADCONFIG_79<br>0x4301C13C  | MCU_ADC0_AIN2   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_73   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| T36          | MCU_ADC0_AIN3<br>PADCFG:<br>WKUP_PADCONFIG_80<br>0x4301C140  | MCU_ADC0_AIN3   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_74   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| P34          | MCU_ADC0_AIN4<br>PADCFG:<br>WKUP_PADCONFIG_81<br>0x4301C144  | MCU_ADC0_AIN4   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_75   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| R37          | MCU_ADC0_AIN5<br>PADCFG:<br>WKUP_PADCONFIG_82<br>0x4301C148  | MCU_ADC0_AIN5   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_76   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| R33          | MCU_ADC0_AIN6<br>PADCFG:<br>WKUP_PADCONFIG_83<br>0x4301C14C  | MCU_ADC0_AIN6   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_77   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| V38          | MCU_ADC0_AIN7<br>PADCFG:<br>WKUP_PADCONFIG_84<br>0x4301C150  | MCU_ADC0_AIN7   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC0  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_78   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| Y38          | MCU_ADC1_AIN0<br>PADCFG:<br>WKUP_PADCONFIG_85<br>0x4301C154  | MCU_ADC1_AIN0   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC1  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_79   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| Y34          | MCU_ADC1_AIN1<br>PADCFG:<br>WKUP_PADCONFIG_86<br>0x4301C158  | MCU_ADC1_AIN1   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC1  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_80   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| V34          | MCU_ADC1_AIN2<br>PADCFG:<br>WKUP_PADCONFIG_87<br>0x4301C15C  | MCU_ADC1_AIN2   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC1  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_81   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| W37          | MCU_ADC1_AIN3<br>PADCFG:<br>WKUP_PADCONFIG_88<br>0x4301C160  | MCU_ADC1_AIN3   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC1  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_82   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AA37         | MCU_ADC1_AIN4<br>PADCFG:<br>WKUP_PADCONFIG_89<br>0x4301C164  | MCU_ADC1_AIN4   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC1  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_83   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| W33          | MCU_ADC1_AIN5<br>PADCFG:<br>WKUP_PADCONFIG_90<br>0x4301C168  | MCU_ADC1_AIN5   | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC1  |          | ADC12B                   | No          |
|              |                                                              | WKUP_GPIO0_84   | 7            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16]  | Signal Name [3]    | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|---------------------------------------------------------------|--------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| U33          | MCU_ADC1_AIN6<br>PADCFG:<br>WKUP_PADCONFIG_91<br>0x4301C16C   | MCU_ADC1_AIN6      | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC1   |          | ADC12B                   | No          |
|              |                                                               | WKUP_GPIO0_85      | 7            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| Y36          | MCU_ADC1_AIN7<br>PADCFG:<br>WKUP_PADCONFIG_92<br>0x4301C170   | MCU_ADC1_AIN7      | 0            | A               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_ADC1   |          | ADC12B                   | No          |
|              |                                                               | WKUP_GPIO0_86      | 7            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| M35          | MCU_I2C0_SCL<br>PADCFG:<br>WKUP_PADCONFIG_66<br>0x4301C108    | MCU_I2C0_SCL       | 0            | IOD             | 1.8 V/3.3 V     | Off / Off / Off                          | On / SS / Off                           | 0                        |                | VDDSHV0_MCU | Yes      | I2C OPEN DRAIN           | Yes         |
|              |                                                               | WKUP_GPIO0_65      | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| G34          | MCU_I2C0_SDA<br>PADCFG:<br>WKUP_PADCONFIG_67<br>0x4301C10C    | MCU_I2C0_SDA       | 0            | IOD             | 1.8 V/3.3 V     | Off / Off / Off                          | On / SS / Off                           | 0                        |                | VDDSHV0_MCU | Yes      | I2C OPEN DRAIN           | Yes         |
|              |                                                               | WKUP_GPIO0_87      | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| F38          | MCU_MCAN0_RX<br>PADCFG:<br>WKUP_PADCONFIG_47<br>0x4301C0BC    | MCU_MCAN0_RX       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                               | WKUP_GPIO0_61      | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| K33          | MCU_MCAN0_TX<br>PADCFG:<br>WKUP_PADCONFIG_46<br>0x4301C0B8    | MCU_MCAN0_TX       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                               | WKUP_GPIO0_60      | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| A36          | MCU_MDIO0_MDC<br>PADCFG:<br>WKUP_PADCONFIG_39<br>0x4301C09C   | MCU_MDIO0_MDC      | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_MCU | Yes      | LVCMOS                   | No          |
|              |                                                               | WKUP_GPIO0_53      | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| B35          | MCU_MDIO0_MDIO<br>PADCFG:<br>WKUP_PADCONFIG_38<br>0x4301C098  | MCU_MDIO0_MDIO     | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_MCU | Yes      | LVCMOS                   | No          |
|              |                                                               | WKUP_GPIO0_52      | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| E32          | MCU_OSPI0_CLK<br>PADCFG:<br>WKUP_PADCONFIG_0<br>0x4301C000    | MCU_OSPI0_CLK      | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                               | MCU_HYPERBUS0_CK   | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                               | WKUP_GPIO0_16      | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| C34          | MCU_OSPI0_DQS<br>PADCFG:<br>WKUP_PADCONFIG_2<br>0x4301C008    | MCU_OSPI0_DQS      | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                               | MCU_HYPERBUS0_RWDS | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                               | WKUP_GPIO0_18      | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| D32          | MCU_OSPI0_LBCLKO<br>PADCFG:<br>WKUP_PADCONFIG_1<br>0x4301C004 | MCU_OSPI0_LBCLKO   | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                               | MCU_HYPERBUS0_CKn  | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                               | WKUP_GPIO0_17      | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16]       | Signal Name [3]        | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------------|------------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| F32          | MCU_OSPi1_CLK<br><br>PADCFG:<br>WKUP_PADCONFIG_16<br>0x4301C040    | MCU_OSPi1_CLK          | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                    | WKUP_GPIO0_31          | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| F31          | MCU_OSPi1_DQS<br><br>PADCFG:<br>WKUP_PADCONFIG_18<br>0x4301C048    | MCU_OSPi1_DQS          | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                    | MCU_OSPi0_CSn3         | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_HYPERBUS0_INTn     | 2            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_OSPi0_ECC_FAIL     | 6            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| C31          | MCU_OSPi1_LBCLKO<br><br>PADCFG:<br>WKUP_PADCONFIG_17<br>0x4301C044 | WKUP_GPIO0_33          | 7            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                    | MCU_OSPi1_LBCLKO       | 0            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_OSPi0_CSn2         | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_HYPERBUS0_RESETO_n | 2            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| A32          | MCU_OSPi0_CSn0<br><br>PADCFG:<br>WKUP_PADCONFIG_11<br>0x4301C02C   | MCU_OSPi0_RESET_OUT0   | 6            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                    | WKUP_GPIO0_32          | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_OSPi0_CSn0         | 0            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
| A33          | MCU_OSPi0_CSn1<br><br>PADCFG:<br>WKUP_PADCONFIG_12<br>0x4301C030   | MCU_HYPERBUS0_CSn0     | 1            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                    | MCU_OSPi0_CSn1         | 0            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_HYPERBUS0_RESETO_n | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
| B34          | MCU_OSPi0_CSn2<br><br>PADCFG:<br>WKUP_PADCONFIG_14<br>0x4301C038   | WKUP_GPIO0_28          | 7            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                    | MCU_OSPi0_CSn2         | 0            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_OSPi0_CSn2         | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_HYPERBUS0_RESETO_n | 2            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_HYPERBUS0_WPn      | 3            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_HYPERBUS0_CSn1     | 4            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
| C32          | MCU_OSPi0_CSn3<br><br>PADCFG:<br>WKUP_PADCONFIG_15<br>0x4301C03C   | MCU_OSPi0_RESET_OUT0   | 6            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                    | WKUP_GPIO0_29          | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_OSPi0_CSn3         | 0            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_OSPi0_CSn3         | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_HYPERBUS0_INTn     | 2            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | MCU_HYPERBUS0_WPn      | 3            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
| C32          | MCU_OSPi0_CSn3<br><br>PADCFG:<br>WKUP_PADCONFIG_15<br>0x4301C03C   | MCU_OSPi0_RESET_OUT1   | 5            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                    | MCU_OSPi0_ECC_FAIL     | 6            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                    | WKUP_GPIO0_30          | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| B33          | MCU_OSPI0_D0<br>PADCFG:<br>WKUP_PADCONFIG_3<br>0x4301C00C    | MCU_OSPI0_D0      | 0            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_HYPERBUS0_DQ0 | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_19     | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | BOOTMODE00        | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| B32          | MCU_OSPI0_D1<br>PADCFG:<br>WKUP_PADCONFIG_4<br>0x4301C010    | MCU_OSPI0_D1      | 0            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_HYPERBUS0_DQ1 | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_20     | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | BOOTMODE01        | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| C33          | MCU_OSPI0_D2<br>PADCFG:<br>WKUP_PADCONFIG_5<br>0x4301C014    | MCU_OSPI0_D2      | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_HYPERBUS0_DQ2 | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_21     | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| C35          | MCU_OSPI0_D3<br>PADCFG:<br>WKUP_PADCONFIG_6<br>0x4301C018    | MCU_OSPI0_D3      | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_HYPERBUS0_DQ3 | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_22     | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| D33          | MCU_OSPI0_D4<br>PADCFG:<br>WKUP_PADCONFIG_7<br>0x4301C01C    | MCU_OSPI0_D4      | 0            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_HYPERBUS0_DQ4 | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_23     | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | BOOTMODE02        | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| D34          | MCU_OSPI0_D5<br>PADCFG:<br>WKUP_PADCONFIG_8<br>0x4301C020    | MCU_OSPI0_D5      | 0            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_HYPERBUS0_DQ5 | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_24     | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | BOOTMODE03        | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| E34          | MCU_OSPI0_D6<br>PADCFG:<br>WKUP_PADCONFIG_9<br>0x4301C024    | MCU_OSPI0_D6      | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_HYPERBUS0_DQ6 | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_25     | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| E33          | MCU_OSPI0_D7<br>PADCFG:<br>WKUP_PADCONFIG_10<br>0x4301C028   | MCU_OSPI0_D7      | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_HYPERBUS0_DQ7 | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_26     | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| G32          | MCU_OSPI1_CS0<br>PADCFG:<br>WKUP_PADCONFIG_23<br>0x4301C05C  | MCU_OSPI1_CS0     | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                              | WKUP_GPIO0_38     | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |

**表 6-1. Pin Attributes (ALY Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16]    | Signal Name [3]      | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|-----------------------------------------------------------------|----------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| G33          | MCU_OSPI1_CSn1<br>PADCFG:<br>WKUP_PADCONFIG_24<br>0x4301C060    | MCU_OSPI1_CSn1       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_HYPERBUS0_WPn    | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_TIMER_I00        | 2            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_HYPERBUS0_CSn1   | 3            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_UART0_RTSn       | 4            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_SPI0_CS2         | 5            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_OSPI0_RESET_OUT1 | 6            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | WKUP_GPIO0_39        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| E35          | MCU_OSPI1_D0<br>PADCFG:<br>WKUP_PADCONFIG_19<br>0x4301C04C      | MCU_OSPI1_D0         | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                 | WKUP_GPIO0_34        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| D31          | MCU_OSPI1_D1<br>PADCFG:<br>WKUP_PADCONFIG_20<br>0x4301C050      | MCU_OSPI1_D1         | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_UART0_RXD        | 4            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_SPI1_CS1         | 5            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | WKUP_GPIO0_35        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| G31          | MCU_OSPI1_D2<br>PADCFG:<br>WKUP_PADCONFIG_21<br>0x4301C054      | MCU_OSPI1_D2         | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_UART0_TXD        | 4            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_SPI1_CS2         | 5            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | WKUP_GPIO0_36        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| F33          | MCU_OSPI1_D3<br>PADCFG:<br>WKUP_PADCONFIG_22<br>0x4301C058      | MCU_OSPI1_D3         | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV1_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_UART0_CTSn       | 4            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | MCU_SPI0_CS1         | 5            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | WKUP_GPIO0_37        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| K32          | MCU_PORz                                                        | MCU_PORz             |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_WKUP   | Yes      | FS_RESET                 | No          |
| F36          | MCU_RESETSTATz<br>PADCFG:<br>WKUP_PADCONFIG_71<br>0x4301C11C    | MCU_RESETSTATz       | 0            | O               | 1.8 V/3.3 V     | Off / Low / Off                          | Off / SS / Off                          | 0                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                 | WKUP_GPIO0_68        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| G36          | MCU_RESETz<br>PADCFG:<br>WKUP_PADCONFIG_70<br>0x4301C118        | MCU_RESETz           | 0            | I               | 1.8 V/3.3 V     | On / NA / Up                             | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | No          |
| B37          | MCU_RGMII1_RXC<br>PADCFG:<br>WKUP_PADCONFIG_33<br>0x4301C084    | MCU_RGMII1_RXC       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_REF_CLK    | 1            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | WKUP_GPIO0_47        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| C37          | MCU_RGMII1_RX_CTL<br>PADCFG:<br>WKUP_PADCONFIG_27<br>0x4301C06C | MCU_RGMII1_RX_CTL    | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_MCU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_RX_ER      | 1            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                                 | WKUP_GPIO0_41        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16]    | Signal Name [3]      | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]      | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|-----------------------------------------------------------------|----------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-----------------|----------|--------------------------|-------------|
| E36          | MCU_RGMII1_TXC<br>PADCFG:<br>WKUP_PADCONFIG_32<br>0x4301C080    | MCU_RGMII1_TXC       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_TX_EN      | 1            | O               |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_46        | 7            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| C38          | MCU_RGMII1_TX_CTL<br>PADCFG:<br>WKUP_PADCONFIG_26<br>0x4301C068 | MCU_RGMII1_TX_CTL    | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_CRS_DV     | 1            | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_40        | 7            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| A35          | MCU_RGMII1_RD0<br>PADCFG:<br>WKUP_PADCONFIG_37<br>0x4301C094    | MCU_RGMII1_RD0       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_RXD0       | 1            | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_51        | 7            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| B36          | MCU_RGMII1_RD1<br>PADCFG:<br>WKUP_PADCONFIG_36<br>0x4301C090    | MCU_RGMII1_RD1       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_RXD1       | 1            | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_50        | 7            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| C36          | MCU_RGMII1_RD2<br>PADCFG:<br>WKUP_PADCONFIG_35<br>0x4301C08C    | MCU_RGMII1_RD2       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_TIMER_IO5        | 1            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_62        | 7            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| D36          | MCU_RGMII1_RD3<br>PADCFG:<br>WKUP_PADCONFIG_34<br>0x4301C088    | MCU_RGMII1_RD3       | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_TIMER_IO4        | 1            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_48        | 7            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| D37          | MCU_RGMII1_TD0<br>PADCFG:<br>WKUP_PADCONFIG_31<br>0x4301C07C    | MCU_RGMII1_TD0       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_TXD0       | 1            | O               |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_45        | 7            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| D38          | MCU_RGMII1_TD1<br>PADCFG:<br>WKUP_PADCONFIG_30<br>0x4301C078    | MCU_RGMII1_TD1       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_RMII1_TXD1       | 1            | O               |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_44        | 7            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| E37          | MCU_RGMII1_TD2<br>PADCFG:<br>WKUP_PADCONFIG_29<br>0x4301C074    | MCU_RGMII1_TD2       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_TIMER_IO3        | 1            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | MCU_ADC_EXT_TRIGGER1 | 3            | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_43        | 7            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| E38          | MCU_RGMII1_TD3<br>PADCFG:<br>WKUP_PADCONFIG_28<br>0x4301C070    | MCU_RGMII1_TD3       | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                                 | MCU_TIMER_IO2        | 1            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | MCU_ADC_EXT_TRIGGER0 | 3            | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                                 | WKUP_GPIO0_42        | 7            | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| N36          | MCU_SAFETY_ERRORn<br>PADCFG:<br>WKUP_PADCONFIG_69<br>0x4301C114 | MCU_SAFETY_ERRORn    | 0            | IO              | 1.8 V           | Off / Off / Down                         | On / SS / Down                          | 0                        | PU/PD          | VDDA_WKUP       | Yes      | LVCMOS                   | No          |



表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| G38          | MCU_SPI0_CLK<br>PADCFG:<br>WKUP_PADCONFIG_40<br>0x4301C0A0   | MCU_SPI0_CLK    | 0            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_GPIO0_54   | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_BOOTMODE00  | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| F37          | MCU_SPI0_CS0<br>PADCFG:<br>WKUP_PADCONFIG_43<br>0x4301C0AC   | MCU_SPI0_CS0    | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_TIMER_IO1   | 4            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_70   | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| H36          | MCU_SPI0_D0<br>PADCFG:<br>WKUP_PADCONFIG_41<br>0x4301C0A4    | MCU_SPI0_D0     | 0            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_GPIO0_55   | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_BOOTMODE01  | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| J38          | MCU_SPI0_D1<br>PADCFG:<br>WKUP_PADCONFIG_42<br>0x4301C0A8    | MCU_SPI0_D1     | 0            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_TIMER_IO0   | 4            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_69   | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_BOOTMODE02  | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| AJ7          | MMC0_CALPAD                                                  | MMC0_CALPAD     |              | A               | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDS_MMC0   |          | eMMC PHY                 | No          |
| AK5          | MMC0_CLK                                                     | MMC0_CLK        |              | O               | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDS_MMC0   |          | eMMC PHY                 | No          |
| AL8          | MMC0_CMD                                                     | MMC0_CMD        |              | IO              | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDS_MMC0   |          | eMMC PHY                 | No          |
| AK4          | MMC0_DS                                                      | MMC0_DS         |              | IO              | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDS_MMC0   |          | eMMC PHY                 | No          |
| AB38         | MMC1_CLK<br>PADCFG:<br>PADCONFIG_65<br>0x0011C104            | MMC1_CLK        | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5     | Yes      | SDIO                     | No          |
|              |                                                              | UART8_RXD       | 1            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | TIMER_IO6       | 3            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | EHRPWM2_B       | 4            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | UART4_CTSn      | 5            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | EHRPWM5_A       | 6            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | GPIO0_64        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | SPI1_CLK        | 8            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | UART0_RTSn      | 9            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | I2C6_SDA        | 10           | IOD             |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCAN15_TX       | 11           | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | PCIE2_CLKREQn   | 12           | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AB36         | MMC1_CMD<br>PADCFG:<br>PADCONFIG_66<br>0x0011C108            | MMC1_CMD          | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5    | Yes      | SDIO                     | No          |
|              |                                                              | UART8_TXD         | 1            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TIMER_IO7         | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM2_A         | 4            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RTSn        | 5            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_65          | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_D1           | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C6_SCL          | 10           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | MCAN15_RX         | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | PCIE3_CLKREQn     | 12           | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
| AK9          | MMC0_DAT0                                                    | MMC0_DAT0         |              | IO              | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDSD_MMC0 |          | eMMC PHY                 | No          |
| AL6          | MMC0_DAT1                                                    | MMC0_DAT1         |              | IO              | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDSD_MMC0 |          | eMMC PHY                 | No          |
| AK8          | MMC0_DAT2                                                    | MMC0_DAT2         |              | IO              | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDSD_MMC0 |          | eMMC PHY                 | No          |
| AK6          | MMC0_DAT3                                                    | MMC0_DAT3         |              | IO              | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDSD_MMC0 |          | eMMC PHY                 | No          |
| AK7          | MMC0_DAT4                                                    | MMC0_DAT4         |              | IO              | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDSD_MMC0 |          | eMMC PHY                 | No          |
| AL7          | MMC0_DAT5                                                    | MMC0_DAT5         |              | IO              | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDSD_MMC0 |          | eMMC PHY                 | No          |
| AL5          | MMC0_DAT6                                                    | MMC0_DAT6         |              | IO              | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDSD_MMC0 |          | eMMC PHY                 | No          |
| AK3          | MMC0_DAT7                                                    | MMC0_DAT7         |              | IO              | 1.8 V           |                                          |                                         |                          | PU/PD          | VDDSD_MMC0 |          | eMMC PHY                 | No          |
| AA33         | MMC1_DAT0<br>PADCFG:<br>PADCONFIG_63<br>0x0011C0FC           | MMC1_DAT0         | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5    | Yes      | SDIO                     | No          |
|              |                                                              | UART7_RTSn        | 1            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | ECAP1_IN_APWM_OUT | 2            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TIMER_IO5         | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM1_A         | 4            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_TXD         | 5            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_63          | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_D0           | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_RTSn        | 9            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C4_SCL          | 10           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART2_TXD         | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AB34         | MMC1_DAT1<br>PADCFG:<br>PADCONFIG_62<br>0x0011C0F8           | MMC1_DAT1         | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5    | Yes      | SDIO                     | No          |
|              |                                                              | UART7_CTSn        | 1            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | ECAP0_IN_APWM_OUT | 2            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TIMER_IO4         | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM1_B         | 4            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART4_RXD         | 5            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM4_A         | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_62          | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_CS2          | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_CTSn        | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C4_SDA          | 10           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART2_RXD         | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AA32         | MMC1_DAT2<br>PADCFG:<br>PADCONFIG_61<br>0x0011C0F4           | MMC1_DAT2         | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5    | Yes      | SDIO                     | No          |
|              |                                                              | UART7_TXD         | 1            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TIMER_IO3         | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_A         | 4            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_61          | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_CS1          | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | CPTS0_TS_SYNC     | 9            | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C3_SDA          | 10           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_TXD         | 11           | O               |                 |                                          |                                         |                          |                |            |          |                          |             |
| AC38         | MMC1_DAT3<br>PADCFG:<br>PADCONFIG_60<br>0x0011C0F0           | MMC1_DAT3         | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV5    | Yes      | SDIO                     | No          |
|              |                                                              | UART7_RXD         | 1            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | PCIE1_CLKREQn     | 2            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | TIMER_IO2         | 3            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM0_B         | 4            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | EHRPWM3_A         | 6            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | GPIO0_60          | 7            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | SPI1_CS0          | 8            | IO              |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART0_CTSn        | 9            | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | I2C3_SCL          | 10           | IOD             |                 |                                          |                                         |                          |                |            |          |                          |             |
|              |                                                              | UART5_RXD         | 11           | I               |                 |                                          |                                         |                          |                |            |          |                          |             |
| P38          | OSC1_XI                                                      | OSC1_XI           |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_OSC1  | Yes      | HFXOSC                   |             |
| N37          | OSC1_XO                                                      | OSC1_XO           |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_OSC1  | Yes      | HFXOSC                   |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]    | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|--------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AP4          | PCIE_REFCLK0_N_OUT                                           | PCIE_REFCLK0_N_OUT |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AP5          | PCIE_REFCLK0_P_OUT                                           | PCIE_REFCLK0_P_OUT |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AN8          | PCIE_REFCLK1_N_OUT                                           | PCIE_REFCLK1_N_OUT |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AN9          | PCIE_REFCLK1_P_OUT                                           | PCIE_REFCLK1_P_OUT |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AN5          | PCIE_REFCLK2_N_OUT                                           | PCIE_REFCLK2_N_OUT |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AN6          | PCIE_REFCLK2_P_OUT                                           | PCIE_REFCLK2_P_OUT |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AP7          | PCIE_REFCLK3_N_OUT                                           | PCIE_REFCLK3_N_OUT |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]    | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|--------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AP8          | PCIE_REFCLK3_P_OUT                                           | PCIE_REFCLK3_P_OUT |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| L38          | PMIC_POWER_EN1                                               | PMIC_POWER_EN1     | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_M<br>CU                                                                     | Yes      | LVCMOS                   | Yes         |
|              | PADCFG:<br>WKUP_PADCONFIG_68<br>0x4301C110                   | MCU_I3C0_SDAPULLEN | 5            | OD              |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | WKUP_GPIO0_88      | 7            | IO              |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AJ34         | PMIC_WAKE0n<br><br>PADCFG:<br>PADCONFIG_13<br>0x0011C034     | PMIC_WAKE0n        | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV2                                                                             | Yes      | LVCMOS                   | No          |
|              |                                                              | MCASP4_AXR0        | 1            | IO              |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | DSS_FSYNC1         | 4            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | MCAN17_RX          | 5            | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | GPMC0_WEn          | 6            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | GPIO0_13           | 7            | IO              |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | SPI6_CS0           | 8            | IO              |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | TRC_DATA0          | 10           | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | UART9_RTSn         | 11           | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| P33          | PORz                                                         | PORz               | 0            | I               | 1.8 V           |                                          |                                         | 0                        |                | VDDA_WKUP                                                                           | Yes      | FS_RESET                 | No          |
|              | PADCFG:<br>WKUP_PADCONFIG_94<br>0x4301C178                   |                    |              |                 |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              |                    |              |                 |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AL38         | RESETSTATz                                                   | RESETSTATz         | 0            | O               | 1.8 V/3.3 V     | Off / Low / Off                          | Off / SS / Off                          | 0                        | PU/PD          | VDDSHV0                                                                             | Yes      | LVCMOS                   | No          |
| F34          | RESET_REQz                                                   | RESET_REQz         | 0            | I               | 1.8 V/3.3 V     | On / Off / Up                            | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0_M<br>CU                                                                     | Yes      | LVCMOS                   | No          |
| AU9          | SERDES0_REFCLK_N                                             | SERDES0_REFCLK_N   |              | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]  | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AU8          | SERDES0_REFCLK_P                                             | SERDES0_REFCLK_P |              | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AN11         | SERDES0_REXT                                                 | SERDES0_REXT     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AV3          | SERDES1_REFCLK_N                                             | SERDES1_REFCLK_N | 0            | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AV4          | SERDES1_REFCLK_P                                             | SERDES1_REFCLK_P | 0            | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AL9          | SERDES1_REXT                                                 | SERDES1_REXT     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
| AV21         | SERDES2_REFCLK_N                                             | SERDES2_REFCLK_N |              | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2          |          | 4L_PHY                   |             |
| AV22         | SERDES2_REFCLK_P                                             | SERDES2_REFCLK_P |              | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2          |          | 4L_PHY                   |             |
| AL20         | SERDES2_REXT                                                 | SERDES2_REXT     | 0            | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2          |          | 4L_PHY                   |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]  | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AV16         | SERDES4_REFCLK_N                                             | SERDES4_REFCLK_N |              | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4          |          | 4L_PHY                   |             |
| AV15         | SERDES4_REFCLK_P                                             | SERDES4_REFCLK_P |              | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4          |          | 4L_PHY                   |             |
| AM19         | SERDES4_REXT                                                 | SERDES4_REXT     |              | IO              | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4          |          | 4L_PHY                   |             |
| AR8          | SERDES0_RX0_N                                                | HYP_RXN0         |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_RXN0       |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AR9          | SERDES0_RX0_P                                                | PCIE1_RXP0       | 1            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | HYP_RXP0         | 4            | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AT10         | SERDES0_RX1_N                                                | PCIE1_RXN1       | 1            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | HYP_RXN1         | 4            | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AT11         | SERDES0_RX1_P                                                | HYP_RXP1         |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_RXP1       |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AR11         | SERDES0_RX2_N                                                | PCIE1_RXN2       |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE3_RXN0       |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSRX1N      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_RXN2         |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AR12         | SERDES0_RX2_P                                                | PCIE3_RXP0      |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE1_RXP2      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSRX1P     |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_RXP2        |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AU11         | SERDES0_RX3_N                                                | HYP_RXN3        |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX2N     |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE3_RXN1      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE1_RXN3      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AU12         | SERDES0_RX3_P                                                | HYP_RXP3        |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE3_RXP1      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE1_RXP3      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | USB0_SSRX2P     |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AT7          | SERDES0_TX0_N                                                | PCIE1_TXN0      | 1            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | HYP_TXN0        | 4            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AT8          | SERDES0_TX0_P                                                | PCIE1_TXP0      | 1            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | HYP_TXP0        | 4            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AP10         | SERDES0_TX1_N                                                | PCIE1_TXN1      | 1            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | HYP_TXN1        | 4            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AP11         | SERDES0_TX1_P                                                | PCIE1_TXP1      | 1            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | HYP_TXP1        | 4            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |



表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AV9          | SERDES0_TX2_N                                                | PCIE1_TXN2      | 1            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSTX1N     | 2            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE3_TXN0      | 3            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXN2        | 4            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AV10         | SERDES0_TX2_P                                                | PCIE1_TXP2      | 1            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSTX1P     | 2            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE3_TXP0      | 3            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXP2        | 4            | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AV12         | SERDES0_TX3_N                                                | USB0_SSTX2N     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE3_TXN1      |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | HYP_TXN3        |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE1_TXN3      |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AV13         | SERDES0_TX3_P                                                | HYP_TXP3        |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSTX2P     |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE3_TXP1      |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE1_TXP3      |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AU5          | SERDES1_RX0_N                                                | PCIE0_RXN0      |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | SGMII3_RXN0     |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AU6          | SERDES1_RX0_P                                                | PCIE0_RXP0      |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | SGMII3_RXP0     |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AT4          | SERDES1_RX1_N                                                | SGMII4_RXN0     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE0_RXN1      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AT5          | SERDES1_RX1_P                                                | SGMII4_RXP0     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE0_RXP1      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AU2          | SERDES1_RX2_N                                                | PCIE2_RXN0      |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE0_RXN2      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | SGMII1_RXN0     |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AU3          | SERDES1_RX2_P                                                | SGMII1_RXP0     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE2_RXP0      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE0_RXP2      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AT1          | SERDES1_RX3_N                                                | PCIE0_RXN3      |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE2_RXN1      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | SGMII2_RXN0     |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AT2          | SERDES1_RX3_P                                                | PCIE0_RXP3      |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | SGMII2_RXP0     |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE2_RXP1      |              | I               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AV6          | SERDES1_TX0_N                                                | SGMII3_TXN0     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE0_TXN0      |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AV7          | SERDES1_TX0_P                                                | PCIE0_TXP0      |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | SGMII3_TXP0     |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                          | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------------------------------------------------------------|----------|--------------------------|-------------|
| AR5          | SERDES1_TX1_N                                                | PCIE0_TXN1      |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | SGMII4_TXN0     |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AR6          | SERDES1_TX1_P                                                | PCIE0_TXP1      |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | SGMII4_TXP0     |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AR2          | SERDES1_TX2_N                                                | PCIE0_TXN2      |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | SGMII1_TXN0     |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE2_TXN0      |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AR3          | SERDES1_TX2_P                                                | PCIE2_TXP0      |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | SGMII1_TXP0     |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE0_TXP2      |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AP1          | SERDES1_TX3_N                                                | PCIE2_TXN1      |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE0_TXN3      |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | SGMII2_TXN0     |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AP2          | SERDES1_TX3_P                                                | SGMII2_TXP0     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES0_1 /<br>VDDA_0P8_S<br>ERDES_C0_1<br>/<br>VDDA_1P8_S<br>ERDES0_1 |          | 4L_PHY                   |             |
|              |                                                              | PCIE0_TXP3      |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
|              |                                                              | PCIE2_TXP1      |              | O               |                 |                                          |                                         |                          |                |                                                                                     |          |                          |             |
| AU23         | SERDES2_RX0_N                                                | SGMII5_RXN0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2          |          | 4L_PHY                   |             |
| AU24         | SERDES2_RX0_P                                                | SGMII5_RXP0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2          |          | 4L_PHY                   |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                 | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------------------------------------------------------------|----------|--------------------------|-------------|
| AT22         | SERDES2_RX1_N                                                | SGMII6_RXN0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
| AT23         | SERDES2_RX1_P                                                | SGMII6_RXP0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
| AU20         | SERDES2_RX2_N                                                | SGMII7_RXN0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
|              |                                                              | SGMII1_RXN0     | 1            | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AU21         | SERDES2_RX2_P                                                | SGMII7_RXP0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
|              |                                                              | SGMII1_RXP0     | 1            | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AT19         | SERDES2_RX3_N                                                | SGMII8_RXN0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
|              |                                                              | SGMII2_RXN0     | 1            | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AT20         | SERDES2_RX3_P                                                | SGMII8_RXP0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
|              |                                                              | SGMII2_RXP0     | 1            | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AV24         | SERDES2_TX0_N                                                | SGMII5_TXN0     | 0            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
| AV25         | SERDES2_TX0_P                                                | SGMII5_TXP0     | 0            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                 | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------------------------------------------------------------|----------|--------------------------|-------------|
| AR23         | SERDES2_TX1_N                                                | SGMII6_TXN0     | 0            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
| AR24         | SERDES2_TX1_P                                                | SGMII6_TXP0     | 0            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
| AR20         | SERDES2_TX2_N                                                | SGMII7_TXN0     | 0            | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
|              |                                                              | SGMII1_TXN0     | 1            | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AR21         | SERDES2_TX2_P                                                | SGMII7_TXP0     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
|              |                                                              | SGMII1_TXP0     |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AP19         | SERDES2_TX3_N                                                | SGMII8_TXN0     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
|              |                                                              | SGMII2_TXN0     |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AP20         | SERDES2_TX3_P                                                | SGMII2_TXP0     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES2 /<br>VDDA_0P8_S<br>ERDES_C2 /<br>VDDA_1P8_S<br>ERDES2 |          | 4L_PHY                   |             |
|              |                                                              | SGMII8_TXP0     |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AR14         | SERDES4_RX0_N                                                | HYP_RXN0        |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | SGMII5_RXN0     |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AR15         | SERDES4_RX0_P                                                | SGMII5_RXP0     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | HYP_RXP0        |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                 | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------------------------------------------------------------|----------|--------------------------|-------------|
| AU14         | SERDES4_RX1_N                                                | SGMII6_RXN0     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | HYP_RXN1        |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AU15         | SERDES4_RX1_P                                                | HYP_RXP1        |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | SGMII6_RXP0     |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AR17         | SERDES4_RX2_N                                                | USB0_SSRX1N     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | HYP_RXN2        |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | SGMII7_RXN0     |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AR18         | SERDES4_RX2_P                                                | USB0_SSRX1P     |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | HYP_RXP2        |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | SGMII7_RXP0     |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AU17         | SERDES4_RX3_N                                                | HYP_RXN3        |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX2N     |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | SGMII8_RXN0     |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AU18         | SERDES4_RX3_P                                                | HYP_RXP3        |              | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSRX2P     |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | SGMII8_RXP0     |              | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AP13         | SERDES4_TX0_N                                                | DP0_TXN0        |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | SGMII5_TXN0     |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | HYP_TXN0        |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AP14         | SERDES4_TX0_P                                                | SGMII5_TXP0     |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | HYP_TXP0        |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | DP0_TXP0        |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                                 | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|----------------------------------------------------------------------------|----------|--------------------------|-------------|
| AT13         | SERDES4_TX1_N                                                | HYP_TXN1          |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | SGMII6_TXN0       |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | DP0_TXN1          |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AT14         | SERDES4_TX1_P                                                | HYP_TXP1          |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | DP0_TXP1          |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | SGMII6_TXP0       |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AT16         | SERDES4_TX2_N                                                | DP0_TXN2          |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | HYP_TXN2          |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | SGMII7_TXN0       |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | USB0_SSTX1N       |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AT17         | SERDES4_TX2_P                                                | SGMII7_TXP0       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | DP0_TXP2          |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | HYP_TXP2          |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | USB0_SSTX1P       |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AV18         | SERDES4_TX3_N                                                | SGMII8_TXN0       |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | USB0_SSTX2N       |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | DP0_TXN3          |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | HYP_TXN3          |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AV19         | SERDES4_TX3_P                                                | HYP_TXP3          |              | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_0P8_S<br>ERDES4 /<br>VDDA_0P8_S<br>ERDES_C4 /<br>VDDA_1P8_S<br>ERDES4 |          | 4L_PHY                   |             |
|              |                                                              | SGMII8_TXP0       |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | USB0_SSTX2P       |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | DP0_TXP3          |              | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
| AM34         | SOC_SAFETY_ERRORn<br>PADCFG:<br>PADCONFIG_68<br>0x0011C110   | SOC_SAFETY_ERRORn | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Down                         | On / SS / Down                          | 0                        | PU/PD          | VDDSHV0                                                                    | Yes      | LVC MOS                  | No          |
| AN38         | SPI0_CLK<br>PADCFG:<br>PADCONFIG_53<br>0x0011C0D4            | SPI0_CLK          | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0                                                                    | Yes      | LVC MOS                  | No          |
|              |                                                              | UART1_CTSn        | 1            | I               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | I2C2_SCL          | 2            | IOD             |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | MCASP3_AXR0       | 3            | IO              |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | EHRPWM2_A         | 5            | IO              |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | GPIO0_53          | 7            | IO              |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |
|              |                                                              | UART8_TXD         | 11           | O               |                 |                                          |                                         |                          |                |                                                                            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| AM37         | SPI0_CS0<br>PADCFG:<br>PADCONFIG_51<br>0x0011C0CC            | SPI0_CS0        | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0     | Yes      | LVCMOS                   | No          |
|              |                                                              | MCASP3_ACLKX    | 3            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCASP3_ACLKR    | 4            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | EHRPWM0_A       | 5            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | GPIO0_51        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCAN14_TX       | 9            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | DP0_HPD         | 12           | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| AP38         | SPI0_CS1<br>PADCFG:<br>PADCONFIG_52<br>0x0011C0D0            | SPI0_CS1        | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0     | Yes      | LVCMOS                   | No          |
|              |                                                              | CPTS0_TS_COMP   | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | UART0_RTSn      | 2            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCASP3_AFSX     | 3            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCASP3_AFSR     | 4            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | EHRPWM1_A       | 5            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | GPIO0_52        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCAN14_RX       | 9            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| AM35         | SPI0_D0<br>PADCFG:<br>PADCONFIG_54<br>0x0011C0D8             | UART8_RXD       | 11           | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0     | Yes      | LVCMOS                   | No          |
|              |                                                              | SPI0_D0         | 0            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | UART1_RTSn      | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | I2C2_SDA        | 2            | IOD             |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCASP3_AXR1     | 3            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | EHRPWM3_A       | 5            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | GPIO0_54        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| AM36         | SPI0_D1<br>PADCFG:<br>PADCONFIG_55<br>0x0011C0DC             | UART2_RXD       | 11           | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0     | Yes      | LVCMOS                   | No          |
|              |                                                              | SPI0_D1         | 0            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCASP3_AXR2     | 3            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | EHRPWM4_A       | 5            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | GPIO0_55        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| G35          | TCK<br>PADCFG:<br>WKUP_PADCONFIG_73<br>0x4301C124            | TCK             | 0            | I               | 1.8 V/3.3 V     | On / NA / Up                             | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | No          |
| AL37         | TDI<br>PADCFG:<br>PADCONFIG_69<br>0x0011C114                 | TDI             | 0            | I               | 1.8 V/3.3 V     | On / Off / Up                            | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0     | Yes      | LVCMOS                   | No          |



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**表 6-1. Pin Attributes (ALY Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                    | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------------------------|----------|--------------------------|-------------|
| AL35         | TDO<br>PADCFG:<br>PADCONFIG_70<br>0x0011C118                 | TDO               | 0            | OZ              | 1.8 V/3.3 V     | Off / Off / Up                           | Off / SS / Up                           | 0                        | PU/PD          | VDDSHV0                       | Yes      | LVC MOS                  | No          |
| AR38         | TIMER_IO0<br>PADCFG:<br>PADCONFIG_58<br>0x0011C0E8           | TIMER_IO0         | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0                       | Yes      | LVC MOS                  | No          |
|              |                                                              | ECAP1_IN_APWM_OUT | 1            | IO              |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | SYSClkOUT0        | 2            | O               |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | UART3_RXD         | 5            | I               |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | PCIE1_CLKREQn     | 6            | IO              |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | GPIO0_58          | 7            | IO              |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | MMC1_SD CD        | 8            | I               |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | MCAN13_TX         | 9            | O               |                 |                                          |                                         |                          |                |                               |          |                          |             |
| AN37         | TIMER_IO1<br>PADCFG:<br>PADCONFIG_59<br>0x0011C0EC           | I2C6_SDA          | 13           | IOD             | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0                       | Yes      | LVC MOS                  | No          |
|              |                                                              | TIMER_IO1         | 0            | IO              |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | ECAP2_IN_APWM_OUT | 1            | IO              |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | OBSClk0           | 2            | O               |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | UART3_TXD         | 5            | O               |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | USB0_DRVVBUS      | 6            | O               |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | GPIO0_59          | 7            | IO              |                 |                                          |                                         |                          |                |                               |          |                          |             |
|              |                                                              | MMC1_SD WP        | 8            | I               |                 |                                          |                                         |                          |                |                               |          |                          |             |
| AL36         | TMS<br>PADCFG:<br>PADCONFIG_71<br>0x0011C11C                 | MMC13_RX          | 9            | I               | 1.8 V/3.3 V     | On / Off / Up                            | On / Off / Up                           | 0                        | PU/PD          | VDDSHV0                       | Yes      | LVC MOS                  | No          |
|              |                                                              | I2C6_SCL          | 13           | IOD             |                 |                                          |                                         |                          |                |                               |          |                          |             |
| G37          | TRSTn<br>PADCFG:<br>WKUP_PADCONFIG_74<br>0x4301C128          | OBSClk0           | 15           | O               | 1.8 V/3.3 V     | On / Off / Down                          | On / Off / Down                         | 0                        | PU/PD          | VDDSHV0_M CU                  | Yes      | LVC MOS                  | No          |
|              |                                                              | TRSTn             | 0            | I               |                 |                                          |                                         |                          |                |                               |          |                          |             |
| AM7          | UFS0_REF_CLK                                                 | UFS0_REF_CLK      | 0            | I               | 1.2 V           |                                          |                                         |                          |                | VDDA_1p8_U FS / VDDA_0P8_U FS |          | M-PHY                    |             |
|              |                                                              | UFS0_REF_CLK      | 16           | I               |                 |                                          |                                         |                          |                |                               |          |                          |             |
| AM8          | UFS0_RSTn                                                    | UFS0_RSTn         | 0            | I               | 1.2 V           |                                          |                                         |                          |                | VDDA_1p8_U FS / VDDA_0P8_U FS |          | M-PHY                    |             |
|              |                                                              | UFS0_RSTn         | 16           | I               |                 |                                          |                                         |                          |                |                               |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                    | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-----------------------------------------------|----------|--------------------------|-------------|
| AM4          | UFS0_RX_DN0                                                  | UFS0_RX_DN0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_1p8_U FS / VDDA_0P8_U FS                 |          | M-PHY                    |             |
|              |                                                              | UFS0_RX_DN0     | 16           | I               |                 |                                          |                                         |                          |                |                                               |          |                          |             |
| AM1          | UFS0_RX_DN1                                                  | UFS0_RX_DN1     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_1p8_U FS / VDDA_0P8_U FS                 |          | M-PHY                    |             |
|              |                                                              | UFS0_RX_DN1     | 16           | I               |                 |                                          |                                         |                          |                |                                               |          |                          |             |
| AM5          | UFS0_RX_DP0                                                  | UFS0_RX_DP0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_1p8_U FS / VDDA_0P8_U FS                 |          | M-PHY                    |             |
|              |                                                              | UFS0_RX_DP0     | 16           | I               |                 |                                          |                                         |                          |                |                                               |          |                          |             |
| AM2          | UFS0_RX_DP1                                                  | UFS0_RX_DP1     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_1p8_U FS / VDDA_0P8_U FS                 |          | M-PHY                    |             |
|              |                                                              | UFS0_RX_DP1     | 16           | I               |                 |                                          |                                         |                          |                |                                               |          |                          |             |
| AL2          | UFS0_TX_DN0                                                  | UFS0_TX_DN0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_1p8_U FS / VDDA_0P8_U FS                 |          | M-PHY                    |             |
|              |                                                              | UFS0_TX_DN0     | 16           | I               |                 |                                          |                                         |                          |                |                                               |          |                          |             |
| AN2          | UFS0_TX_DN1                                                  | UFS0_TX_DN1     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_1p8_U FS / VDDA_0P8_U FS                 |          | M-PHY                    |             |
|              |                                                              | UFS0_TX_DN1     | 16           | I               |                 |                                          |                                         |                          |                |                                               |          |                          |             |
| AL3          | UFS0_TX_DP0                                                  | UFS0_TX_DP0     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_1p8_U FS / VDDA_0P8_U FS                 |          | M-PHY                    |             |
|              |                                                              | UFS0_TX_DP0     | 16           | I               |                 |                                          |                                         |                          |                |                                               |          |                          |             |
| AN3          | UFS0_TX_DP1                                                  | UFS0_TX_DP1     | 0            | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_1p8_U FS / VDDA_0P8_U FS                 |          | M-PHY                    |             |
|              |                                                              | UFS0_TX_DP1     | 16           | I               |                 |                                          |                                         |                          |                |                                               |          |                          |             |
| AP16         | USB0_DM                                                      | USB0_DM         |              | IO              | 3.3 V           |                                          |                                         |                          |                | VDDA_0P8_U SB / VDDA_1P8_U SB / VDDA_3P3_U SB |          | USB2PHY                  |             |
| AP17         | USB0_DP                                                      | USB0_DP         |              | IO              | 3.3 V           |                                          |                                         |                          |                | VDDA_0P8_U SB / VDDA_1P8_U SB / VDDA_3P3_U SB |          | USB2PHY                  |             |
| AN17         | USB0_ID                                                      | USB0_ID         |              | A               | 3.3 V           |                                          |                                         |                          |                | VDDA_0P8_U SB / VDDA_1P8_U SB / VDDA_3P3_U SB |          | USB2PHY                  |             |

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**表 6-1. Pin Attributes (ALY Package) (continued)**

| Ball Num [1]                                                                                 | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]                    | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]                                                   | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|----------------------------------------------------------------------------------------------|--------------------------------------------------------------|------------------------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|--------------------------------------------------------------|----------|--------------------------|-------------|
| AN18                                                                                         | USB0_RCALIB                                                  | <a href="#">USB0_RCALIB</a>        |              | A               | 3.3 V           |                                          |                                         |                          |                | VDDA_0P8_U<br>SB /<br>VDDA_1P8_U<br>SB /<br>VDDA_3P3_U<br>SB |          | USB2PHY                  |             |
| AN15                                                                                         | USB0_VBUS                                                    | <a href="#">USB0_VBUS</a>          |              | A               | 5.0 V           |                                          |                                         |                          |                | VDDA_0P8_U<br>SB /<br>VDDA_1P8_U<br>SB /<br>VDDA_3P3_U<br>SB |          | DDR                      |             |
| AB27,<br>AC24, AF15,<br>AF18, AF21,<br>AG11,<br>AG28, T25                                    | VDDAR_CORE                                                   | <a href="#">VDDAR_CORE</a>         |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AB13,<br>AC16,<br>AC18,<br>AC20,<br>AE12, M21,<br>N23, T15,<br>U20, W14,<br>W21, Y11,<br>Y19 | VDDAR_CPU                                                    | <a href="#">VDDAR_CPU</a>          |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| M27, N24                                                                                     | VDDAR_MCU                                                    | <a href="#">VDDAR_MCU</a>          |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AJ24                                                                                         | VDDA_0P8_DSITX                                               | <a href="#">VDDA_0P8_DSITX</a>     |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AJ25                                                                                         | VDDA_0P8_DSITX_C                                             | <a href="#">VDDA_0P8_DSITX_C</a>   |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AH11                                                                                         | VDDA_0P8_UFS                                                 | <a href="#">VDDA_0P8_UFS</a>       |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AK20                                                                                         | VDDA_0P8_USB                                                 | <a href="#">VDDA_0P8_USB</a>       |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AJ28                                                                                         | VDDA_0P8_CSIRX2                                              | <a href="#">VDDA_0P8_CSIRX2</a>    |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AJ26, AK26                                                                                   | VDDA_0P8_CSIRX0_1                                            | <a href="#">VDDA_0P8_CSIRX0_1</a>  |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AE9                                                                                          | VDDA_0P8_DLL_MMC0                                            | <a href="#">VDDA_0P8_DLL_MMC0</a>  |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| U11                                                                                          | VDDA_0P8_PLL_DDR0                                            | <a href="#">VDDA_0P8_PLL_DDR0</a>  |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| M14                                                                                          | VDDA_0P8_PLL_DDR1                                            | <a href="#">VDDA_0P8_PLL_DDR1</a>  |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| N11                                                                                          | VDDA_0P8_PLL_DDR2                                            | <a href="#">VDDA_0P8_PLL_DDR2</a>  |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| M18                                                                                          | VDDA_0P8_PLL_DDR3                                            | <a href="#">VDDA_0P8_PLL_DDR3</a>  |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AJ20, AJ21                                                                                   | VDDA_0P8_SERDES2                                             | <a href="#">VDDA_0P8_SERDES2</a>   |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AJ17, AJ18                                                                                   | VDDA_0P8_SERDES4                                             | <a href="#">VDDA_0P8_SERDES4</a>   |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AJ12, AJ15,<br>AK13, AK14                                                                    | VDDA_0P8_SERDES0_1                                           | <a href="#">VDDA_0P8_SERDES0_1</a> |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AG21, AH20                                                                                   | VDDA_0P8_SERDES_C2                                           | <a href="#">VDDA_0P8_SERDES_C2</a> |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |
| AG17, AH18                                                                                   | VDDA_0P8_SERDES_C4                                           | <a href="#">VDDA_0P8_SERDES_C4</a> |              | PWR             |                 |                                          |                                         |                          |                |                                                              |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1]           | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]      | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|------------------------|--------------------------------------------------------------|----------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AH12, AH13, AH15, AH16 | VDDA_0P8_SERDES_C0_1                                         | VDDA_0P8_SERDES_C0_1 |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AH24, AH25             | VDDA_1P8_DSITX                                               | VDDA_1P8_DSITX       |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AJ10                   | VDDA_1P8_UFS                                                 | VDDA_1P8_UFS         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AK21                   | VDDA_1P8_USB                                                 | VDDA_1P8_USB         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AH29, AJ29             | VDDA_1P8_CSIRX2                                              | VDDA_1P8_CSIRX2      |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AH27, AH28             | VDDA_1P8_CSIRX0_1                                            | VDDA_1P8_CSIRX0_1    |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AH21                   | VDDA_1P8_SERDES2                                             | VDDA_1P8_SERDES2     |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AH17                   | VDDA_1P8_SERDES4                                             | VDDA_1P8_SERDES4     |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AJ13, AJ14             | VDDA_1P8_SERDES0_1                                           | VDDA_1P8_SERDES0_1   |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AJ23                   | VDDA_1P8_SERDES2_4                                           | VDDA_1P8_SERDES2_4   |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AJ19                   | VDDA_3P3_USB                                                 | VDDA_3P3_USB         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| M31                    | VDDA_ADC0                                                    | VDDA_ADC0            |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| N30                    | VDDA_ADC1                                                    | VDDA_ADC1            |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| M28                    | VDDA_MCU_PLLGRP0                                             | VDDA_MCU_PLLGRP0     |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| M26                    | VDDA_MCU_TEMP                                                | VDDA_MCU_TEMP        |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| N29                    | VDDA_OSC1                                                    | VDDA_OSC1            |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AA27                   | VDDA_PLLGRP0                                                 | VDDA_PLLGRP0         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| Y28                    | VDDA_PLLGRP1                                                 | VDDA_PLLGRP1         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AG13                   | VDDA_PLLGRP2                                                 | VDDA_PLLGRP2         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| V14                    | VDDA_PLLGRP5                                                 | VDDA_PLLGRP5         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| R21                    | VDDA_PLLGRP6                                                 | VDDA_PLLGRP6         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| P12                    | VDDA_PLLGRP7                                                 | VDDA_PLLGRP7         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| P15                    | VDDA_PLLGRP8                                                 | VDDA_PLLGRP8         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| Y26                    | VDDA_PLLGRP9                                                 | VDDA_PLLGRP9         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AG23                   | VDDA_PLLGRP10                                                | VDDA_PLLGRP10        |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AA23                   | VDDA_PLLGRP12                                                | VDDA_PLLGRP12        |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AB26                   | VDDA_PLLGRP13                                                | VDDA_PLLGRP13        |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| N28                    | VDDA_POR_WKUP                                                | VDDA_POR_WKUP        |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| Y27                    | VDDA_TEMP0                                                   | VDDA_TEMP0           |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| M12                    | VDDA_TEMP1                                                   | VDDA_TEMP1           |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| W23                    | VDDA_TEMP2                                                   | VDDA_TEMP2           |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AE13                   | VDDA_TEMP3                                                   | VDDA_TEMP3           |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AD18                   | VDDA_TEMP4                                                   | VDDA_TEMP4           |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| K31, L32               | VDDA_WKUP                                                    | VDDA_WKUP            |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| V30, V32, W31          | VDDSHV0                                                      | VDDSHV0              |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1]                                                                                                                                                        | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| H29, J28, K29                                                                                                                                                       | VDDSHV0_MCU                                                  | VDDSHV0_MCU     |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| H25, J24, K25                                                                                                                                                       | VDDSHV1_MCU                                                  | VDDSHV1_MCU     |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| T30, T32, U31                                                                                                                                                       | VDDSHV2                                                      | VDDSHV2         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| H27, J26, K27                                                                                                                                                       | VDDSHV2_MCU                                                  | VDDSHV2_MCU     |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| P31, R30, R31                                                                                                                                                       | VDDSHV5                                                      | VDDSHV5         |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| A31, AK1, B1, H11, H13, H15, H17, H19, H9, J10, J12, J14, J16, J18, J8, K11, K13, K15, K17, K19, K9, L10, L12, L14, L16, L18, M9, N10, N8, P9, R10, R8, T9, U10, U8 | VDDS_DDR                                                     | VDDS_DDR        |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| T10                                                                                                                                                                 | VDDS_DDR_C0                                                  | VDDS_DDR_C0     |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| L15                                                                                                                                                                 | VDDS_DDR_C1                                                  | VDDS_DDR_C1     |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| M10                                                                                                                                                                 | VDDS_DDR_C2                                                  | VDDS_DDR_C2     |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| L17                                                                                                                                                                 | VDDS_DDR_C3                                                  | VDDS_DDR_C3     |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| AF9, AG10, AG8, AH9                                                                                                                                                 | VDDS_MMC0                                                    | VDDS_MMC0       |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AA24, AA26,<br>AA28, AA30,<br>AB25, AB29,<br>AB31,<br>AC26,<br>AC28,<br>AC30,<br>AD25,<br>AD27,<br>AD29,<br>AD31,<br>AE24, AE26,<br>AE28, AE30,<br>AE32, AF13,<br>AF17, AF19,<br>AF23, AF25,<br>AF27, AF29,<br>AF31,<br>AG12,<br>AG14,<br>AG16,<br>AG18,<br>AG20,<br>AG22,<br>AG24,<br>AG26,<br>AG30,<br>AG32,<br>AH31, AJ30,<br>M11, M13,<br>M15, M17,<br>M19, N12,<br>N16, N18,<br>P11, P17,<br>P19, R12,<br>R14, R16,<br>R18, R24,<br>R26, R28,<br>T11, T13,<br>T27, U12,<br>U24, U26,<br>U28, V25,<br>V27, W24,<br>W26, W28,<br>W30, W32,<br>Y25, Y29,<br>Y31 | VDD_CORE                                                     | VDD_CORE        |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |

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**表 6-1. Pin Attributes (ALY Package) (continued)**

| Ball Num [1]                                                                                                                                                                                                                                                                                                                                           | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]  | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| AA10, AA12, AA14, AA20, AA22, AA8, AB11, AB19, AB21, AB23, AB9, AC10, AC12, AC14, AC22, AD11, AD13, AD15, AD17, AD19, AD21, AD23, AD9, AE10, AE14, AE16, AE18, AE20, AE22, AF11, H21, H23, J20, J22, K21, K23, L20, L22, N20, N22, P21, R20, R22, T17, T19, T21, T23, U14, U22, V11, V13, V19, V21, V23, V9, W10, W12, W20, W22, W8, Y13, Y21, Y23, Y9 | VDD_CPU                                                      | VDD_CPU          |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| L24, M23, M25, N26, P23, P25, P27                                                                                                                                                                                                                                                                                                                      | VDD_MCU                                                      | VDD_MCU          |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| L28                                                                                                                                                                                                                                                                                                                                                    | VDD_MCU_WAKE1                                                | VDD_MCU_WAKE1    |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| U29                                                                                                                                                                                                                                                                                                                                                    | VDD_WAKE0                                                    | VDD_WAKE0        |              | PWR             |                 |                                          |                                         |                          |                |            |          |                          |             |
| K28                                                                                                                                                                                                                                                                                                                                                    | VMON1_ER_VSYS                                                | VMON1_ER_VSYS    |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |
| N27                                                                                                                                                                                                                                                                                                                                                    | VMON2_IR_VCPU                                                | VMON2_IR_VCPU    |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |
| J30                                                                                                                                                                                                                                                                                                                                                    | VMON3_IR_VEXT1P8                                             | VMON3_IR_VEXT1P8 |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |
| P28                                                                                                                                                                                                                                                                                                                                                    | VMON4_IR_VEXT1P8                                             | VMON4_IR_VEXT1P8 |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |
| R29                                                                                                                                                                                                                                                                                                                                                    | VMON5_IR_VEXT3P3                                             | VMON5_IR_VEXT3P3 |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |
| AA31                                                                                                                                                                                                                                                                                                                                                   | VPP_CORE                                                     | VPP_CORE         |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |
| L29                                                                                                                                                                                                                                                                                                                                                    | VPP_MCU                                                      | VPP_MCU          |              |                 |                 |                                          |                                         |                          |                |            |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11] | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|------------|----------|--------------------------|-------------|
| A1, A10,<br>A12, A15,<br>A2, A20,<br>A23, A25,<br>A28, A34,<br>A37, A5, A7,<br>AA11, AA13,<br>AA19, AA2,<br>AA21, AA25,<br>AA29, AA34,<br>AA36, AA38,<br>AA5, AA9,<br>AB1, AB10,<br>AB12, AB14,<br>AB20, AB22,<br>AB24, AB28,<br>AB30, AB32,<br>AB33, AB35,<br>AB37, AB5,<br>AB8, AC11,<br>AC13,<br>AC15,<br>AC17,<br>AC19, AC2,<br>AC21,<br>AC23,<br>AC25,<br>AC27,<br>AC29,<br>AC31, AC6,<br>AC9, AD1,<br>AD10,<br>AD12,<br>AD14,<br>AD16,<br>AD20,<br>AD22,<br>AD24,<br>AD26,<br>AD28,<br>AD30,<br>AD32,<br>AD35, AD4,<br>AD8, AE11,<br>AE15, AE17,<br>AE19, AE2,<br>AE21, AE23,<br>AE25, AE27,<br>AE29, AE31,<br>AE5, AF10,<br>AF12, AF14,<br>AF16, AF20,<br>AF22, AF24,<br>AF26, AF28,<br>AF3, AF30,<br>AF32, AF6,<br>AF8, AG1,<br>AG15, | VSS                                                          | VSS             |              | GND             |                 |                                          |                                         |                          |                |            |          |                          |             |

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**表 6-1. Pin Attributes (ALY Package) (continued)**

| Ball<br>Num [1]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Ball<br>Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal<br>Name [3] | Mux<br>Mode<br>[4] | Signal<br>Type [5] | I/O<br>Voltage [6] | Ball State<br>DURING<br>Reset<br>(RX/TX/PULL)<br>[7] | Ball State<br>AFTER<br>Reset<br>(RX/TX/PULL)<br>[8] | Mux<br>Mode<br>AFTER<br>Reset [9] | Pull<br>Type<br>[10] | Power [11] | Hys<br>[12] | Voltage<br>Buffer<br>Type [13] | IO<br>RET [14] |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|--------------------|--------------------|--------------------|--------------------|------------------------------------------------------|-----------------------------------------------------|-----------------------------------|----------------------|------------|-------------|--------------------------------|----------------|
| AG19,<br>AG25,<br>AG27,<br>AG29,<br>AG31, AG4,<br>AG7, AG9,<br>AH10,<br>AH14,<br>AH19, AH2,<br>AH22,<br>AH23,<br>AH26,<br>AH30,<br>AH32,<br>AH35, AH5,<br>AH8, AJ11,<br>AJ16, AJ22,<br>AJ27, AJ3,<br>AJ31, AJ6,<br>AJ8, AJ9,<br>AK10, AK11,<br>AK12, AK15,<br>AK16, AK17,<br>AK18, AK19,<br>AK22, AK23,<br>AK24, AK25,<br>AK27, AK28,<br>AK30, AK32,<br>AL1, AL10,<br>AL12, AL13,<br>AL14, AL15,<br>AL16, AL17,<br>AL18, AL19,<br>AL21, AL26,<br>AL29, AL31,<br>AL4, AM11,<br>AM13,<br>AM15,<br>AM18,<br>AM20,<br>AM23,<br>AM25,<br>AM27, AM3,<br>AM30,<br>AM32,<br>AM38, AM6,<br>AN1, AN10,<br>AN12,<br>AN14,<br>AN16,<br>AN19,<br>AN22,<br>AN25,<br>AN28,<br>AN31,<br>AN34, AN4,<br>AN7, AP12,<br>AP15, AP18, |                                                                 |                    |                    |                    |                    |                                                      |                                                     |                                   |                      |            |             |                                |                |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball<br>Num [1]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Ball<br>Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal<br>Name [3] | Mux<br>Mode<br>[4] | Signal<br>Type [5] | I/O<br>Voltage [6] | Ball State<br>DURING<br>Reset<br>(RX/TX/PULL)<br>[7] | Ball State<br>AFTER<br>Reset<br>(RX/TX/PULL)<br>[8] | Mux<br>Mode<br>AFTER<br>Reset [9] | Pull<br>Type<br>[10] | Power [11] | Hys<br>[12] | Voltage<br>Buffer<br>Type [13] | IO<br>RET [14] |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|--------------------|--------------------|--------------------|--------------------|------------------------------------------------------|-----------------------------------------------------|-----------------------------------|----------------------|------------|-------------|--------------------------------|----------------|
| AP21, AP24,<br>AP27, AP3,<br>AP30, AP33,<br>AP36, AP6,<br>AP9, AR1,<br>AR10,<br>AR13,<br>AR16,<br>AR19,<br>AR22,<br>AR25,<br>AR28,<br>AR31,<br>AR34,<br>AR37, AR4,<br>AR7, AT12,<br>AT15, AT18,<br>AT21, AT24,<br>AT27, AT3,<br>AT30, AT33,<br>AT36, AT6,<br>AT9, AU1,<br>AU10,<br>AU13,<br>AU16,<br>AU19,<br>AU22,<br>AU25,<br>AU28,<br>AU31,<br>AU34,<br>AU37,<br>AU38, AU4,<br>AU7, AV1,<br>AV11, AV14,<br>AV17, AV2,<br>AV20, AV23,<br>AV26, AV29,<br>AV32, AV35,<br>AV5, AV8,<br>B11, B13,<br>B16, B19,<br>B22, B24,<br>B26, B29,<br>B31, B38,<br>B6, B9, C14,<br>C17, C18,<br>C2, C21,<br>C27, C30,<br>C4, C8,<br>D10, D15,<br>D20, D23,<br>D28, D3,<br>D35, D6,<br>D7, E12,<br>E13, E16,<br>E19, E2,<br>E22, E25, |                                                                 |                    |                    |                    |                    |                                                      |                                                     |                                   |                      |            |             |                                |                |

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表 6-1. Pin Attributes (ALY Package) (continued)

| Ball<br>Num [1]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Ball<br>Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal<br>Name [3] | Mux<br>Mode<br>[4] | Signal<br>Type [5] | I/O<br>Voltage [6] | Ball State<br>DURING<br>Reset<br>(RX/TX/PULL)<br>[7] | Ball State<br>AFTER<br>Reset<br>(RX/TX/PULL)<br>[8] | Mux<br>Mode<br>AFTER<br>Reset [9] | Pull<br>Type<br>[10] | Power [11] | Hys<br>[12] | Voltage<br>Buffer<br>Type [13] | IO<br>RET [14] |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|--------------------|--------------------|--------------------|--------------------|------------------------------------------------------|-----------------------------------------------------|-----------------------------------|----------------------|------------|-------------|--------------------------------|----------------|
| E26, E29,<br>E31, E5, E9,<br>F1, F11,<br>F14, F17,<br>F21, F24,<br>F27, F30,<br>F4, F7, F8,<br>G15, G18,<br>G20, G28,<br>G3, G6,<br>H10, H16,<br>H18, H2,<br>H20, H22,<br>H24, H26,<br>H28, H30,<br>H31, H5,<br>H7, H8, J1,<br>J11, J13,<br>J15, J17,<br>J19, J21,<br>J23, J25,<br>J27, J29,<br>J32, J4, J9,<br>K10, K12,<br>K14, K16,<br>K18, K2,<br>K20, K22,<br>K24, K26,<br>K6, K8, L1,<br>L11, L13,<br>L19, L21,<br>L23, L31,<br>L5, L9, M16,<br>M2, M20,<br>M22, M24,<br>M29, M30,<br>M32, M5,<br>M8, N15,<br>N17, N19,<br>N21, N25,<br>N3, N31,<br>N32, N38,<br>N6, N9, P1,<br>P10, P16,<br>P18, P20,<br>P22, P24,<br>P26, P30,<br>P32, P35,<br>P37, P4, P7,<br>P8, R11,<br>R13, R15,<br>R17, R19,<br>R2, R23,<br>R25, R27,<br>R32, R34,<br>R36, R38,<br>R5, R9, T12,<br>T14, T16, |                                                                 |                    |                    |                    |                    |                                                      |                                                     |                                   |                      |            |             |                                |                |

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表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1]                                                                                                                                                                                                                                                                                                                       | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3] | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| T18, T20, T22, T24, T26, T28, T3, T31, T33, T35, T37, T6, T8, U13, U19, U21, U23, U25, U27, U3, U30, U32, U34, U36, U38, U6, U9, V10, V12, V2, V20, V22, V24, V26, V28, V31, V33, V35, V37, V5, V8, W1, W11, W13, W19, W25, W27, W29, W34, W36, W38, W4, W7, W9, Y10, Y12, Y14, Y20, Y22, Y24, Y3, Y30, Y32, Y33, Y35, Y37, Y6, Y8 |                                                              |                 |              |                 |                 |                                          |                                         |                          |                |             |          |                          |             |
| H38                                                                                                                                                                                                                                                                                                                                | WKUP_GPIO0_0<br>PADCFG:<br>WKUP_PADCONFIG_48<br>0x4301C0C0   | MCU_SPI1_CLK    | 0            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|                                                                                                                                                                                                                                                                                                                                    |                                                              | MCU_SPI1_CLK    | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|                                                                                                                                                                                                                                                                                                                                    |                                                              | WKUP_GPIO0_0    | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|                                                                                                                                                                                                                                                                                                                                    |                                                              | MCU_BOOTMODE03  | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| J34                                                                                                                                                                                                                                                                                                                                | WKUP_GPIO0_1<br>PADCFG:<br>WKUP_PADCONFIG_49<br>0x4301C0C4   | MCU_SPI1_D0     | 0            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|                                                                                                                                                                                                                                                                                                                                    |                                                              | MCU_SPI1_D0     | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|                                                                                                                                                                                                                                                                                                                                    |                                                              | WKUP_GPIO0_1    | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|                                                                                                                                                                                                                                                                                                                                    |                                                              | MCU_BOOTMODE04  | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| J35                                                                                                                                                                                                                                                                                                                                | WKUP_GPIO0_2<br>PADCFG:<br>WKUP_PADCONFIG_50<br>0x4301C0C8   | MCU_SPI1_D1     | 0            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|                                                                                                                                                                                                                                                                                                                                    |                                                              | MCU_SPI1_D1     | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|                                                                                                                                                                                                                                                                                                                                    |                                                              | WKUP_GPIO0_2    | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|                                                                                                                                                                                                                                                                                                                                    |                                                              | MCU_BOOTMODE05  | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]      | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|----------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| J36          | WKUP_GPIO0_3<br>PADCFG:<br>WKUP_PADCONFIG_51<br>0x4301C0CC   | MCU_SPI1_CS0         | 0            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_SPI1_CS0         | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_3         | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| H35          | WKUP_GPIO0_4<br>PADCFG:<br>WKUP_PADCONFIG_52<br>0x4301C0D0   | MCU_MCAN1_TX         | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_MCAN1_TX         | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_SPI0_CS3         | 2            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_ADC_EXT_TRIGGER0 | 3            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| K36          | WKUP_GPIO0_5<br>PADCFG:<br>WKUP_PADCONFIG_53<br>0x4301C0D4   | WKUP_GPIO0_4         | 7            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_MCAN1_RX         | 0            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_MCAN1_RX         | 1            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_SPI1_CS3         | 2            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_ADC_EXT_TRIGGER1 | 3            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
| L37          | WKUP_GPIO0_6<br>PADCFG:<br>WKUP_PADCONFIG_54<br>0x4301C0D8   | WKUP_GPIO0_5         | 7            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_UART0_CTSn      | 0            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_UART0_CTSn      | 1            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_CPTS0_HW1TSPUSH  | 2            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_I2C1_SCL         | 3            | IOD             |                 |                                          |                                         |                          |                |             |          |                          |             |
| L36          | WKUP_GPIO0_7<br>PADCFG:<br>WKUP_PADCONFIG_55<br>0x4301C0DC   | WKUP_UART0_CTSn      | 7            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_UART0_RTSn      | 0            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_UART0_RTSn      | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_CPTS0_HW2TSPUSH  | 2            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_I2C1_SDA         | 3            | IOD             |                 |                                          |                                         |                          |                |             |          |                          |             |
| L35          | WKUP_GPIO0_8<br>PADCFG:<br>WKUP_PADCONFIG_56<br>0x4301C0E0   | WKUP_GPIO0_7         | 7            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_I2C1_SCL         | 0            | IOD             |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_I2C1_SCL         | 1            | IOD             |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_CPTS0_TS_SYNC    | 2            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_I3C0_SCL         | 3            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_TIMER_IO6        | 4            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| L34          | WKUP_GPIO0_9<br>PADCFG:<br>WKUP_PADCONFIG_57<br>0x4301C0E4   | WKUP_GPIO0_8         | 7            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_I2C1_SDA         | 0            | IOD             |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_I2C1_SDA         | 1            | IOD             |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_CPTS0_TS_COMP    | 2            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_I3C0_SDA         | 3            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_TIMER_IO7        | 4            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| L34          | WKUP_GPIO0_9<br>PADCFG:<br>WKUP_PADCONFIG_57<br>0x4301C0E4   | WKUP_GPIO0_9         | 7            | IO              | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_I2C1_SDA         | 0            | IOD             |                 |                                          |                                         |                          |                |             |          |                          |             |

表 6-1. Pin Attributes (ALY Package) (continued)

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]      | Mux Mode [4] | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]  | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|----------------------|--------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-------------|----------|--------------------------|-------------|
| L33          | WKUP_GPIO0_10<br>PADCFG:<br>WKUP_PADCONFIG_58<br>0x4301C0E8  | MCU_EXT_REFCLK0      | 0            | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_EXT_REFCLK0      | 1            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_UART0_TXD        | 2            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_ADC_EXT_TRIGGER0 | 3            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_CPTS0_RFT_CLK    | 4            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_SYSCLKOUT0       | 5            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_10        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| M38          | WKUP_GPIO0_11<br>PADCFG:<br>WKUP_PADCONFIG_59<br>0x4301C0EC  | MCU_OBSCCLK0         | 0            | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_OBSCCLK0         | 1            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_UART0_RXD        | 2            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_ADC_EXT_TRIGGER1 | 3            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_TIMER_IO1        | 4            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_I3C0_SDAPULLEN   | 5            | OD              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_CLKOUT0          | 6            | OZ              |                 |                                          |                                         |                          |                |             |          |                          |             |
| J37          | WKUP_GPIO0_12<br>PADCFG:<br>WKUP_PADCONFIG_60<br>0x4301C0F0  | WKUP_GPIO0_11        | 7            | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_UART0_TXD        | 0            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_SPI0_CS1         | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_12        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| K38          | WKUP_GPIO0_13<br>PADCFG:<br>WKUP_PADCONFIG_61<br>0x4301C0F4  | MCU_BOOTMODE08       | BOOTS TRAP   | I               | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_UART0_RXD        | 0            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_SPI1_CS1         | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_13        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| H37          | WKUP_GPIO0_14<br>PADCFG:<br>WKUP_PADCONFIG_62<br>0x4301C0F8  | MCU_BOOTMODE09       | BOOTS TRAP   | I               | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_UART0_CTSn       | 0            | I               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_SPI0_CS2         | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_TIMER_IO8        | 4            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_14        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
| K37          | WKUP_GPIO0_15<br>PADCFG:<br>WKUP_PADCONFIG_63<br>0x4301C0FC  | MCU_BOOTMODE06       | BOOTS TRAP   | I               | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_MCU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | MCU_UART0_RTSn       | 0            | O               |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_SPI1_CS2         | 1            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_TIMER_IO9        | 4            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | WKUP_GPIO0_15        | 7            | IO              |                 |                                          |                                         |                          |                |             |          |                          |             |
|              |                                                              | MCU_BOOTMODE07       | BOOTS TRAP   | I               |                 |                                          |                                         |                          |                |             |          |                          |             |

**表 6-1. Pin Attributes (ALY Package) (continued)**

| Ball Num [1] | Ball Name [2]<br>PADCFG Register [15]<br>PADCFG Address [16] | Signal Name [3]   | Mux Mode [4]  | Signal Type [5] | I/O Voltage [6] | Ball State DURING Reset (RX/TX/PULL) [7] | Ball State AFTER Reset (RX/TX/PULL) [8] | Mux Mode AFTER Reset [9] | Pull Type [10] | Power [11]      | Hys [12] | Voltage Buffer Type [13] | IO RET [14] |
|--------------|--------------------------------------------------------------|-------------------|---------------|-----------------|-----------------|------------------------------------------|-----------------------------------------|--------------------------|----------------|-----------------|----------|--------------------------|-------------|
| M33          | WKUP_GPIO0_49<br>PADCFG:<br>WKUP_PADCONFIG_100<br>0x4301C190 | PMIC_WAKE1n       | 0             | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | MCU_EXT_REFCLK0   | 1             | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | MCU_CPTS0_RFT_CLK | 2             | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | WKUP_GPIO0_49     | 7             | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| M37          | WKUP_GPIO0_56<br>PADCFG:<br>WKUP_PADCONFIG_72<br>0x4301C120  | MCU_TIMER_I06     | 4             | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | WKUP_GPIO0_56     | 7             | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | BOOTMODE04        | BOOTS<br>TRAP | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
| M36          | WKUP_GPIO0_57<br>PADCFG:<br>WKUP_PADCONFIG_95<br>0x4301C17C  | MCU_TIMER_I07     | 4             | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | No          |
|              |                                                              | WKUP_GPIO0_57     | 7             | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | BOOTMODE05        | BOOTS<br>TRAP | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
| N34          | WKUP_GPIO0_66<br>PADCFG:<br>WKUP_PADCONFIG_96<br>0x4301C180  | WKUP_GPIO0_66     | 7             | IO              | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | BOOTMODE06        | BOOTS<br>TRAP | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
| M34          | WKUP_GPIO0_67<br>PADCFG:<br>WKUP_PADCONFIG_97<br>0x4301C184  | WKUP_LF_CLKIN     | 1             | I               | 1.8 V/3.3 V     | On / Off / Off                           | On / Off / Off                          | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_GPIO0_67     | 7             | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
|              |                                                              | BOOTMODE07        | BOOTS<br>TRAP | I               |                 |                                          |                                         |                          |                |                 |          |                          |             |
| N33          | WKUP_I2C0_SCL<br>PADCFG:<br>WKUP_PADCONFIG_64<br>0x4301C100  | WKUP_I2C0_SCL     | 0             | IOD             | 1.8 V/3.3 V     | Off / Off / Off                          | On / SS / Off                           | 0                        |                | VDDSHV0_M<br>CU | Yes      | I2C OPEN<br>DRAIN        | Yes         |
|              |                                                              | WKUP_GPIO0_63     | 7             | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| N35          | WKUP_I2C0_SDA<br>PADCFG:<br>WKUP_PADCONFIG_65<br>0x4301C104  | WKUP_I2C0_SDA     | 0             | IOD             | 1.8 V/3.3 V     | Off / Off / Off                          | On / SS / Off                           | 0                        |                | VDDSHV0_M<br>CU | Yes      | I2C OPEN<br>DRAIN        | Yes         |
|              |                                                              | WKUP_GPIO0_64     | 7             | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| T38          | WKUP_OSC0_XI                                                 | WKUP_OSC0_XI      |               | I               | 1.8 V           |                                          |                                         |                          |                | VDDA_WKUP       | Yes      | HFXOSC                   | No          |
| U37          | WKUP_OSC0_XO                                                 | WKUP_OSC0_XO      |               | O               | 1.8 V           |                                          |                                         |                          |                | VDDA_WKUP       | Yes      | HFXOSC                   | No          |
| K35          | WKUP_UART0_RXD<br>PADCFG:<br>WKUP_PADCONFIG_44<br>0x4301C0B0 | WKUP_UART0_RXD    | 0             | I               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_GPIO0_58     | 7             | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |
| K34          | WKUP_UART0_TXD<br>PADCFG:<br>WKUP_PADCONFIG_45<br>0x4301C0B4 | WKUP_UART0_TXD    | 0             | O               | 1.8 V/3.3 V     | Off / Off / Off                          | Off / Off / Off                         | 7                        | PU/PD          | VDDSHV0_M<br>CU | Yes      | LVCMOS                   | Yes         |
|              |                                                              | WKUP_GPIO0_59     | 7             | IO              |                 |                                          |                                         |                          |                |                 |          |                          |             |

## 6.3 Signal Descriptions

1. **SIGNAL NAME:** The name of the signal passing through the pin.

### 备注

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via PADCONFIG registers. Device subsystems may provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:

- I = Input
- O = Output
- OD = Output, with open-drain output function
- IO = Input, Output, or simultaneously Input and Output
- IOD = Input, Output, or simultaneously Input and Output with open-drain output function
- IOZ = Input, Output, or simultaneously Input and Output with three-state output function
- OZ = Output with three-state output function
- A = Analog
- PWR = Power
- GND = Ground
- CAP = LDO Capacitor

3. **DESCRIPTION:** Description of the signal

4. **BALL:** Ball number(s) associated with signal

For more information on the IO cell configurations, see the *Pad Configuration Registers* section in *Device Configuration* chapter of the device TRM.

### 6.3.1 ADC

#### 6.3.1.1 MCU Domain

表 6-2. MCU\_ADC Signal Descriptions

| SIGNAL NAME [1]      | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4]   |
|----------------------|--------------|-------------------|---------------|
| MCU_ADC_EXT_TRIGGER0 | I            | ADC Trigger Input | E38, H35, L33 |
| MCU_ADC_EXT_TRIGGER1 | I            | ADC Trigger Input | E37, K36, M38 |

表 6-3. MCU\_ADC0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]          | ALY PIN [4] |
|-----------------|--------------|--------------------------|-------------|
| MCU_ADC0_REFN   | A            | ADC Reference (Negative) | U35         |
| MCU_ADC0_REFP   | A            | ADC Reference (Positive) | R35         |
| MCU_ADC0_AIN0   | A            | ADC Input 0              | P36         |
| MCU_ADC0_AIN1   | A            | ADC Input 1              | V36         |
| MCU_ADC0_AIN2   | A            | ADC Input 2              | T34         |
| MCU_ADC0_AIN3   | A            | ADC Input 3              | T36         |
| MCU_ADC0_AIN4   | A            | ADC Input 4              | P34         |
| MCU_ADC0_AIN5   | A            | ADC Input 5              | R37         |
| MCU_ADC0_AIN6   | A            | ADC Input 6              | R33         |
| MCU_ADC0_AIN7   | A            | ADC Input 7              | V38         |



表 6-4. MCU\_ADC1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]          | ALY PIN [4] |
|-----------------|--------------|--------------------------|-------------|
| MCU_ADC1_REFN   | A            | ADC Reference (Negative) | W35         |
| MCU_ADC1_REFP   | A            | ADC Reference (Positive) | AA35        |
| MCU_ADC1_AIN0   | A            | ADC Input 0              | Y38         |
| MCU_ADC1_AIN1   | A            | ADC Input 1              | Y34         |
| MCU_ADC1_AIN2   | A            | ADC Input 2              | V34         |
| MCU_ADC1_AIN3   | A            | ADC Input 3              | W37         |
| MCU_ADC1_AIN4   | A            | ADC Input 4              | AA37        |
| MCU_ADC1_AIN5   | A            | ADC Input 5              | W33         |
| MCU_ADC1_AIN6   | A            | ADC Input 6              | U33         |
| MCU_ADC1_AIN7   | A            | ADC Input 7              | Y36         |

### 6.3.2 DDRSS

#### 6.3.2.1 MAIN Domain

表 6-5. DDRSS0 Signal Descriptions

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]                     | ALY PIN [4] |
|--------------------------------|--------------|-------------------------------------|-------------|
| DDR0_CKN                       | IO           | DDRSS Differential Clock (negative) | AB2         |
| DDR0_CKP                       | IO           | DDRSS Differential Clock (positive) | AC1         |
| DDR0_RESETn                    | IO           | DDRSS Reset                         | AD5         |
| DDR0_RET                       | I            | DDR Retention Enable                | AC8         |
| DDR0_CA0                       | IO           | DDRSS Command Address               | AD2         |
| DDR0_CA1                       | IO           | DDRSS Command Address               | AC5         |
| DDR0_CA2                       | IO           | DDRSS Command Address               | AB4         |
| DDR0_CA3                       | IO           | DDRSS Command Address               | AC4         |
| DDR0_CA4                       | IO           | DDRSS Command Address               | AB3         |
| DDR0_CA5                       | IO           | DDRSS Command Address               | AC3         |
| DDR0_CAL0 <sup>(1)</sup>       | A            | IO Pad Calibration Resistor         | AE8         |
| DDR0_CKE0                      | IO           | DDRSS Clock Enable                  | AB6         |
| DDR0_CKE1                      | IO           | DDRSS Clock Enable                  | AD3         |
| DDR0_CSn0_0                    | IO           | DDRSS Chip Select                   | AD7         |
| DDR0_CSn0_1                    | IO           | DDRSS Chip Select                   | AC7         |
| DDR0_CSn1_0                    | IO           | DDRSS Chip Select                   | AB7         |
| DDR0_CSn1_1                    | IO           | DDRSS Chip Select                   | AD6         |
| DDR0_DM0                       | IO           | DDRSS Data Mask                     | V3          |
| DDR0_DM1                       | IO           | DDRSS Data Mask                     | AA4         |
| DDR0_DM2                       | IO           | DDRSS Data Mask                     | AG2         |
| DDR0_DM3                       | IO           | DDRSS Data Mask                     | AJ5         |
| DDR0_DQ0                       | IO           | DDRSS Data                          | U2          |
| DDR0_DQ1                       | IO           | DDRSS Data                          | U4          |
| DDR0_DQ2                       | IO           | DDRSS Data                          | W6          |
| DDR0_DQ3                       | IO           | DDRSS Data                          | W5          |
| DDR0_DQ4                       | IO           | DDRSS Data                          | V4          |
| DDR0_DQ5                       | IO           | DDRSS Data                          | V7          |
| DDR0_DQ6                       | IO           | DDRSS Data                          | U5          |
| DDR0_DQ7                       | IO           | DDRSS Data                          | V6          |
| DDR0_DQ8                       | IO           | DDRSS Data                          | Y2          |

**表 6-5. DDRSS0 Signal Descriptions (continued)**

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]                 | ALY PIN [4] |
|--------------------------------|--------------|---------------------------------|-------------|
| DDR0_DQ9                       | IO           | DDRSS Data                      | W3          |
| DDR0_DQ10                      | IO           | DDRSS Data                      | AA3         |
| DDR0_DQ11                      | IO           | DDRSS Data                      | W2          |
| DDR0_DQ12                      | IO           | DDRSS Data                      | AA6         |
| DDR0_DQ13                      | IO           | DDRSS Data                      | Y4          |
| DDR0_DQ14                      | IO           | DDRSS Data                      | Y5          |
| DDR0_DQ15                      | IO           | DDRSS Data                      | AA7         |
| DDR0_DQ16                      | IO           | DDRSS Data                      | AF2         |
| DDR0_DQ17                      | IO           | DDRSS Data                      | AE7         |
| DDR0_DQ18                      | IO           | DDRSS Data                      | AG3         |
| DDR0_DQ19                      | IO           | DDRSS Data                      | AF5         |
| DDR0_DQ20                      | IO           | DDRSS Data                      | AE6         |
| DDR0_DQ21                      | IO           | DDRSS Data                      | AF4         |
| DDR0_DQ22                      | IO           | DDRSS Data                      | AE3         |
| DDR0_DQ23                      | IO           | DDRSS Data                      | AE4         |
| DDR0_DQ24                      | IO           | DDRSS Data                      | AG5         |
| DDR0_DQ25                      | IO           | DDRSS Data                      | AH3         |
| DDR0_DQ26                      | IO           | DDRSS Data                      | AJ2         |
| DDR0_DQ27                      | IO           | DDRSS Data                      | AH4         |
| DDR0_DQ28                      | IO           | DDRSS Data                      | AJ4         |
| DDR0_DQ29                      | IO           | DDRSS Data                      | AH6         |
| DDR0_DQ30                      | IO           | DDRSS Data                      | AH7         |
| DDR0_DQ31                      | IO           | DDRSS Data                      | AG6         |
| DDR0_QS0N                      | IO           | DDRSS Complimentary Data Strobe | V1          |
| DDR0_QS0P                      | IO           | DDRSS Data Strobe               | U1          |
| DDR0_QS1N                      | IO           | DDRSS Complimentary Data Strobe | Y1          |
| DDR0_QS1P                      | IO           | DDRSS Data Strobe               | AA1         |
| DDR0_QS2N                      | IO           | DDRSS Complimentary Data Strobe | AE1         |
| DDR0_QS2P                      | IO           | DDRSS Data Strobe               | AF1         |
| DDR0_QS3N                      | IO           | DDRSS Complimentary Data Strobe | AH1         |
| DDR0_QS3P                      | IO           | DDRSS Data Strobe               | AJ1         |

- (1) An external 240  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.  
 (2) DDRSS0, DDRSS1, DDRSS2, and DDRSS3 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0\_\* interface. When using two LPDDR components, they must be connected to DDR0\_\* and DDR1\_\* interfaces, and so forth.

**表 6-6. DDRSS1 Signal Descriptions**

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]                     | ALY PIN [4] |
|--------------------------------|--------------|-------------------------------------|-------------|
| DDR1_CKN                       | IO           | DDRSS Differential Clock (negative) | A11         |
| DDR1_CKP                       | IO           | DDRSS Differential Clock (positive) | B10         |
| DDR1_RESETh                    | IO           | DDRSS Reset                         | G10         |
| DDR1_RET                       | I            | DDR Retention Enable                | G8          |
| DDR1_CA0                       | IO           | DDRSS Command Address               | F12         |
| DDR1_CA1                       | IO           | DDRSS Command Address               | C12         |
| DDR1_CA2                       | IO           | DDRSS Command Address               | B12         |
| DDR1_CA3                       | IO           | DDRSS Command Address               | C11         |

表 6-6. DDRSS1 Signal Descriptions (continued)

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]             | ALY PIN [4] |
|--------------------------------|--------------|-----------------------------|-------------|
| DDR1_CA4                       | IO           | DDRSS Command Address       | D12         |
| DDR1_CA5                       | IO           | DDRSS Command Address       | E10         |
| DDR1_CAL0 <sup>(1)</sup>       | A            | IO Pad Calibration Resistor | G14         |
| DDR1_CKE0                      | IO           | DDRSS Clock Enable          | D11         |
| DDR1_CKE1                      | IO           | DDRSS Clock Enable          | C10         |
| DDR1_CSn0_0                    | IO           | DDRSS Chip Select           | E11         |
| DDR1_CSn0_1                    | IO           | DDRSS Chip Select           | G11         |
| DDR1_CSn1_0                    | IO           | DDRSS Chip Select           | F10         |
| DDR1_CSn1_1                    | IO           | DDRSS Chip Select           | G12         |
| DDR1_DM0                       | IO           | DDRSS Data Mask             | E17         |
| DDR1_DM1                       | IO           | DDRSS Data Mask             | C15         |
| DDR1_DM2                       | IO           | DDRSS Data Mask             | D8          |
| DDR1_DM3                       | IO           | DDRSS Data Mask             | C1          |
| DDR1_DQ0                       | IO           | DDRSS Data                  | F16         |
| DDR1_DQ1                       | IO           | DDRSS Data                  | G16         |
| DDR1_DQ2                       | IO           | DDRSS Data                  | F15         |
| DDR1_DQ3                       | IO           | DDRSS Data                  | E15         |
| DDR1_DQ4                       | IO           | DDRSS Data                  | D16         |
| DDR1_DQ5                       | IO           | DDRSS Data                  | C16         |
| DDR1_DQ6                       | IO           | DDRSS Data                  | B17         |
| DDR1_DQ7                       | IO           | DDRSS Data                  | D17         |
| DDR1_DQ8                       | IO           | DDRSS Data                  | B15         |
| DDR1_DQ9                       | IO           | DDRSS Data                  | B14         |
| DDR1_DQ10                      | IO           | DDRSS Data                  | C13         |
| DDR1_DQ11                      | IO           | DDRSS Data                  | D13         |
| DDR1_DQ12                      | IO           | DDRSS Data                  | F13         |
| DDR1_DQ13                      | IO           | DDRSS Data                  | G13         |
| DDR1_DQ14                      | IO           | DDRSS Data                  | E14         |
| DDR1_DQ15                      | IO           | DDRSS Data                  | D14         |
| DDR1_DQ16                      | IO           | DDRSS Data                  | E8          |
| DDR1_DQ17                      | IO           | DDRSS Data                  | G9          |
| DDR1_DQ18                      | IO           | DDRSS Data                  | F9          |
| DDR1_DQ19                      | IO           | DDRSS Data                  | D9          |
| DDR1_DQ20                      | IO           | DDRSS Data                  | C9          |
| DDR1_DQ21                      | IO           | DDRSS Data                  | B8          |
| DDR1_DQ22                      | IO           | DDRSS Data                  | B7          |
| DDR1_DQ23                      | IO           | DDRSS Data                  | C7          |
| DDR1_DQ24                      | IO           | DDRSS Data                  | B2          |
| DDR1_DQ25                      | IO           | DDRSS Data                  | B3          |
| DDR1_DQ26                      | IO           | DDRSS Data                  | B4          |
| DDR1_DQ27                      | IO           | DDRSS Data                  | B5          |
| DDR1_DQ28                      | IO           | DDRSS Data                  | A6          |
| DDR1_DQ29                      | IO           | DDRSS Data                  | C5          |
| DDR1_DQ30                      | IO           | DDRSS Data                  | C6          |
| DDR1_DQ31                      | IO           | DDRSS Data                  | C3          |

**表 6-6. DDRSS1 Signal Descriptions (continued)**

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]                 | ALY PIN [4] |
|--------------------------------|--------------|---------------------------------|-------------|
| DDR1_DQS0N                     | IO           | DDRSS Complimentary Data Strobe | A17         |
| DDR1_DQS0P                     | IO           | DDRSS Data Strobe               | A16         |
| DDR1_DQS1N                     | IO           | DDRSS Complimentary Data Strobe | A14         |
| DDR1_DQS1P                     | IO           | DDRSS Data Strobe               | A13         |
| DDR1_DQS2N                     | IO           | DDRSS Complimentary Data Strobe | A9          |
| DDR1_DQS2P                     | IO           | DDRSS Data Strobe               | A8          |
| DDR1_DQS3N                     | IO           | DDRSS Complimentary Data Strobe | A4          |
| DDR1_DQS3P                     | IO           | DDRSS Data Strobe               | A3          |

- (1) An external 240  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.  
 (2) DDRSS0, DDRSS1, DDRSS2, and DDRSS3 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0\_\* interface. When using two LPDDR components, they must be connected to DDR0\_\* and DDR1\_\* interfaces, and so forth.

**表 6-7. DDRSS2 Signal Descriptions**

| SIGNAL NAME [1] <sup>(2)</sup> <sup>(3)</sup> | PIN TYPE [2] | DESCRIPTION [3]                     | ALY PIN [4] |
|-----------------------------------------------|--------------|-------------------------------------|-------------|
| DDR2_CKN                                      | IO           | DDRSS Differential Clock (negative) | K1          |
| DDR2_CKP                                      | IO           | DDRSS Differential Clock (positive) | L2          |
| DDR2_RESETn                                   | IO           | DDRSS Reset                         | J5          |
| DDR2_RET                                      | I            | DDR Retention Enable                | L8          |
| DDR2_CA0                                      | IO           | DDRS Command Address                | K3          |
| DDR2_CA1                                      | IO           | DDRS Command Address                | L3          |
| DDR2_CA2                                      | IO           | DDRS Command Address                | K5          |
| DDR2_CA3                                      | IO           | DDRS Command Address                | L4          |
| DDR2_CA4                                      | IO           | DDRS Command Address                | K4          |
| DDR2_CA5                                      | IO           | DDRS Command Address                | L7          |
| DDR2_CAL0 <sup>(1)</sup>                      | A            | DDRSS IO Pad Calibration Resistor   | U7          |
| DDR2_CKE0                                     | IO           | DDR Clock Enable                    | L6          |
| DDR2_CKE1                                     | IO           | DDR Clock Enable                    | J2          |
| DDR2_CSn0_0                                   | IO           | DDRSS Chip Select                   | J3          |
| DDR2_CSn0_1                                   | IO           | DDRSS Chip Select                   | J6          |
| DDR2_CSn1_0                                   | IO           | DDRSS Chip Select                   | J7          |
| DDR2_CSn1_1                                   | IO           | DDRSS Chip Select                   | K7          |
| DDR2_DM0                                      | IO           | DDRSS Data Mask                     | T2          |
| DDR2_DM1                                      | IO           | DDRSS Data Mask                     | M6          |
| DDR2_DM2                                      | IO           | DDRSS Data Mask                     | G4          |
| DDR2_DM3                                      | IO           | DDRSS Data Mask                     | D5          |
| DDR2_DQ0                                      | IO           | DDRSS Data                          | T4          |
| DDR2_DQ1                                      | IO           | DDRSS Data                          | R6          |
| DDR2_DQ2                                      | IO           | DDRSS Data                          | R3          |
| DDR2_DQ3                                      | IO           | DDRSS Data                          | R4          |
| DDR2_DQ4                                      | IO           | DDRSS Data                          | P6          |
| DDR2_DQ5                                      | IO           | DDRSS Data                          | P5          |
| DDR2_DQ6                                      | IO           | DDRSS Data                          | T5          |
| DDR2_DQ7                                      | IO           | DDRSS Data                          | R7          |
| DDR2_DQ8                                      | IO           | DDRSS Data                          | N2          |
| DDR2_DQ9                                      | IO           | DDRSS Data                          | N4          |

表 6-7. DDRSS2 Signal Descriptions (continued)

| SIGNAL NAME [1] <sup>(2)</sup> <sup>(3)</sup> | PIN TYPE [2] | DESCRIPTION [3]                | ALY PIN [4] |
|-----------------------------------------------|--------------|--------------------------------|-------------|
| DDR2_DQ10                                     | IO           | DDRSS Data                     | P2          |
| DDR2_DQ11                                     | IO           | DDRSS Data                     | P3          |
| DDR2_DQ12                                     | IO           | DDRSS Data                     | M7          |
| DDR2_DQ13                                     | IO           | DDRSS Data                     | N5          |
| DDR2_DQ14                                     | IO           | DDRSS Data                     | M4          |
| DDR2_DQ15                                     | IO           | DDRSS Data                     | M3          |
| DDR2_DQ16                                     | IO           | DDRSS Data                     | F3          |
| DDR2_DQ17                                     | IO           | DDRSS Data                     | G7          |
| DDR2_DQ18                                     | IO           | DDRSS Data                     | H6          |
| DDR2_DQ19                                     | IO           | DDRSS Data                     | H4          |
| DDR2_DQ20                                     | IO           | DDRSS Data                     | G2          |
| DDR2_DQ21                                     | IO           | DDRSS Data                     | H3          |
| DDR2_DQ22                                     | IO           | DDRSS Data                     | G5          |
| DDR2_DQ23                                     | IO           | DDRSS Data                     | F2          |
| DDR2_DQ24                                     | IO           | DDRSS Data                     | E4          |
| DDR2_DQ25                                     | IO           | DDRSS Data                     | D2          |
| DDR2_DQ26                                     | IO           | DDRSS Data                     | F6          |
| DDR2_DQ27                                     | IO           | DDRSS Data                     | F5          |
| DDR2_DQ28                                     | IO           | DDRSS Data                     | E3          |
| DDR2_DQ29                                     | IO           | DDRSS Data                     | E7          |
| DDR2_DQ30                                     | IO           | DDRSS Data                     | E6          |
| DDR2_DQ31                                     | IO           | DDRSS Data                     | D4          |
| DDR2_QS0N                                     | IO           | DDRS Complimentary Data Strobe | R1          |
| DDR2_QS0P                                     | IO           | DDRS Data Strobe               | T1          |
| DDR2_QS1N                                     | IO           | DDRS Complimentary Data Strobe | M1          |
| DDR2_QS1P                                     | IO           | DDRS Data Strobe               | N1          |
| DDR2_QS2N                                     | IO           | DDRS Complimentary Data Strobe | G1          |
| DDR2_QS2P                                     | IO           | DDRS Data Strobe               | H1          |
| DDR2_QS3N                                     | IO           | DDRS Complimentary Data Strobe | D1          |
| DDR2_QS3P                                     | IO           | DDRS Data Strobe               | E1          |

- (1) An external  $240\ \Omega \pm 1\%$  resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.
- (2) DDRSS0, DDRSS1, DDRSS2, and DDRSS3 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0\_\* interface. When using two LPDDR components, they must be connected to DDR0\_\* and DDR1\_\* interfaces, and so forth.
- (3) DDRSS2, DDRSS3, and SERDES2 are not available on the 27mm package variant of this SoC. DDRSS2/DDRSS3/SERDES2 should be avoided if software compatibility is desired with systems that use the 27mm package.

表 6-8. DDRSS3 Signal Descriptions

| SIGNAL NAME [1] <sup>(2)</sup> <sup>(3)</sup> | PIN TYPE [2] | DESCRIPTION [3]                     | ALY PIN [4] |
|-----------------------------------------------|--------------|-------------------------------------|-------------|
| DDR3_CKN                                      | IO           | DDRSS Differential Clock (negative) | B25         |
| DDR3_CKP                                      | IO           | DDRSS Differential Clock (positive) | A24         |
| DDR3_RESETh                                   | IO           | DDRSS Reset                         | C23         |
| DDR3_RET                                      | I            | DDR Retention Enable                | G27         |
| DDR3_CA0                                      | IO           | DDRSS Command Address               | D25         |
| DDR3_CA1                                      | IO           | DDRSS Command Address               | B23         |
| DDR3_CA2                                      | IO           | DDRSS Command Address               | D24         |
| DDR3_CA3                                      | IO           | DDRSS Command Address               | C24         |

**表 6-8. DDRSS3 Signal Descriptions (continued)**

| SIGNAL NAME [1] <sup>(2)</sup> <sup>(3)</sup> | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4] |
|-----------------------------------------------|--------------|-----------------------------------|-------------|
| DDR3_CA4                                      | IO           | DDRSS Command Address             | E23         |
| DDR3_CA5                                      | IO           | DDRSS Command Address             | F23         |
| DDR3_CAL0 <sup>(1)</sup>                      | A            | DDRSS IO Pad Calibration Resistor | F18         |
| DDR3_CKE0                                     | IO           | DDRSS Clock Enable                | C25         |
| DDR3_CKE1                                     | IO           | DDRSS Clock Enable                | G24         |
| DDR3_CSn0_0                                   | IO           | DDRSS Chip Select                 | G23         |
| DDR3_CSn0_1                                   | IO           | DDRSS Chip Select                 | G25         |
| DDR3_CSn1_0                                   | IO           | DDRSS Chip Select                 | F25         |
| DDR3_CSn1_1                                   | IO           | DDRSS Chip Select                 | E24         |
| DDR3_DM0                                      | IO           | DDRSS Data Mask                   | E18         |
| DDR3_DM1                                      | IO           | DDRSS Data Mask                   | D21         |
| DDR3_DM2                                      | IO           | DDRSS Data Mask                   | C28         |
| DDR3_DM3                                      | IO           | DDRSS Data Mask                   | E30         |
| DDR3_DQ0                                      | IO           | DDRSS Data                        | D18         |
| DDR3_DQ1                                      | IO           | DDRSS Data                        | B18         |
| DDR3_DQ2                                      | IO           | DDRSS Data                        | C19         |
| DDR3_DQ3                                      | IO           | DDRSS Data                        | D19         |
| DDR3_DQ4                                      | IO           | DDRSS Data                        | F20         |
| DDR3_DQ5                                      | IO           | DDRSS Data                        | E20         |
| DDR3_DQ6                                      | IO           | DDRSS Data                        | G19         |
| DDR3_DQ7                                      | IO           | DDRSS Data                        | F19         |
| DDR3_DQ8                                      | IO           | DDRSS Data                        | E21         |
| DDR3_DQ9                                      | IO           | DDRSS Data                        | G21         |
| DDR3_DQ10                                     | IO           | DDRSS Data                        | F22         |
| DDR3_DQ11                                     | IO           | DDRSS Data                        | D22         |
| DDR3_DQ12                                     | IO           | DDRSS Data                        | C22         |
| DDR3_DQ13                                     | IO           | DDRSS Data                        | B21         |
| DDR3_DQ14                                     | IO           | DDRSS Data                        | B20         |
| DDR3_DQ15                                     | IO           | DDRSS Data                        | C20         |
| DDR3_DQ16                                     | IO           | DDRSS Data                        | B28         |
| DDR3_DQ17                                     | IO           | DDRSS Data                        | B27         |
| DDR3_DQ18                                     | IO           | DDRSS Data                        | C26         |
| DDR3_DQ19                                     | IO           | DDRSS Data                        | D26         |
| DDR3_DQ20                                     | IO           | DDRSS Data                        | F26         |
| DDR3_DQ21                                     | IO           | DDRSS Data                        | G26         |
| DDR3_DQ22                                     | IO           | DDRSS Data                        | E27         |
| DDR3_DQ23                                     | IO           | DDRSS Data                        | D27         |
| DDR3_DQ24                                     | IO           | DDRSS Data                        | F29         |
| DDR3_DQ25                                     | IO           | DDRSS Data                        | G29         |
| DDR3_DQ26                                     | IO           | DDRSS Data                        | F28         |
| DDR3_DQ27                                     | IO           | DDRSS Data                        | E28         |
| DDR3_DQ28                                     | IO           | DDRSS Data                        | D29         |
| DDR3_DQ29                                     | IO           | DDRSS Data                        | C29         |
| DDR3_DQ30                                     | IO           | DDRSS Data                        | B30         |
| DDR3_DQ31                                     | IO           | DDRSS Data                        | D30         |

表 6-8. DDRSS3 Signal Descriptions (continued)

| SIGNAL NAME [1] <sup>(2)</sup> <sup>(3)</sup> | PIN TYPE [2] | DESCRIPTION [3]                 | ALY PIN [4] |
|-----------------------------------------------|--------------|---------------------------------|-------------|
| DDR3_DQS0N                                    | IO           | DDRSS Complimentary Data Strobe | A19         |
| DDR3_DQS0P                                    | IO           | DDRSS Data Strobe               | A18         |
| DDR3_DQS1N                                    | IO           | DDRSS Complimentary Data Strobe | A22         |
| DDR3_DQS1P                                    | IO           | DDRSS Data Strobe               | A21         |
| DDR3_DQS2N                                    | IO           | DDRSS Complimentary Data Strobe | A27         |
| DDR3_DQS2P                                    | IO           | DDRSS Data Strobe               | A26         |
| DDR3_DQS3N                                    | IO           | DDRSS Complimentary Data Strobe | A30         |
| DDR3_DQS3P                                    | IO           | DDRSS Data Strobe               | A29         |

- (1) An external  $240\ \Omega \pm 1\%$  resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.
- (2) DDRSS0, DDRSS1, DDRSS2, and DDRSS3 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0\_\* interface. When using two LPDDR components, they must be connected to DDR0\_\* and DDR1\_\* interfaces, and so forth.
- (3) DDRSS2, DDRSS3, and SERDES2 are not available on the 27mm package variant of this SoC. DDRSS2/DDRSS3/SERDES2 should be avoided if software compatibility is desired with systems that use the 27mm package.

### 6.3.3 GPIO

#### 6.3.3.1 MAIN Domain

表 6-9. GPIO0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALY PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO0_0         | IO           | General Purpose Input/Output | AN35        |
| GPIO0_1         | IO           | General Purpose Input/Output | AG36        |
| GPIO0_2         | IO           | General Purpose Input/Output | AJ33        |
| GPIO0_3         | IO           | General Purpose Input/Output | AF33        |
| GPIO0_4         | IO           | General Purpose Input/Output | AH33        |
| GPIO0_5         | IO           | General Purpose Input/Output | AG33        |
| GPIO0_6         | IO           | General Purpose Input/Output | AK36        |
| GPIO0_7         | IO           | General Purpose Input/Output | AG34        |
| GPIO0_8         | IO           | General Purpose Input/Output | AJ35        |
| GPIO0_9         | IO           | General Purpose Input/Output | AH34        |
| GPIO0_10        | IO           | General Purpose Input/Output | AE33        |
| GPIO0_11        | IO           | General Purpose Input/Output | AL32        |
| GPIO0_12        | IO           | General Purpose Input/Output | AK37        |
| GPIO0_13        | IO           | General Purpose Input/Output | AJ34        |
| GPIO0_14        | IO           | General Purpose Input/Output | AK35        |
| GPIO0_15        | IO           | General Purpose Input/Output | AK38        |
| GPIO0_16        | IO           | General Purpose Input/Output | AF37        |
| GPIO0_17        | IO           | General Purpose Input/Output | AG37        |
| GPIO0_18        | IO           | General Purpose Input/Output | AK33        |
| GPIO0_19        | IO           | General Purpose Input/Output | AC32        |
| GPIO0_20        | IO           | General Purpose Input/Output | AC37        |
| GPIO0_21        | IO           | General Purpose Input/Output | AD37        |
| GPIO0_22        | IO           | General Purpose Input/Output | AE37        |
| GPIO0_23        | IO           | General Purpose Input/Output | AC36        |
| GPIO0_24        | IO           | General Purpose Input/Output | AE36        |
| GPIO0_25        | IO           | General Purpose Input/Output | AF38        |
| GPIO0_26        | IO           | General Purpose Input/Output | AE38        |

**表 6-9. GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALY PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| GPIO0_27        | IO           | General Purpose Input/Output | AJ37        |
| GPIO0_28        | IO           | General Purpose Input/Output | AH38        |
| GPIO0_29        | IO           | General Purpose Input/Output | AC33        |
| GPIO0_30        | IO           | General Purpose Input/Output | AH37        |
| GPIO0_31        | IO           | General Purpose Input/Output | AJ38        |
| GPIO0_32        | IO           | General Purpose Input/Output | AK34        |
| GPIO0_33        | IO           | General Purpose Input/Output | AG38        |
| GPIO0_34        | IO           | General Purpose Input/Output | AF36        |
| GPIO0_35        | IO           | General Purpose Input/Output | AE35        |
| GPIO0_36        | IO           | General Purpose Input/Output | AC35        |
| GPIO0_37        | IO           | General Purpose Input/Output | AG35        |
| GPIO0_38        | IO           | General Purpose Input/Output | AH36        |
| GPIO0_39        | IO           | General Purpose Input/Output | AF35        |
| GPIO0_40        | IO           | General Purpose Input/Output | AD34        |
| GPIO0_41        | IO           | General Purpose Input/Output | AJ36        |
| GPIO0_42        | IO           | General Purpose Input/Output | AF34        |
| GPIO0_43        | IO           | General Purpose Input/Output | AE34        |
| GPIO0_44        | IO           | General Purpose Input/Output | AL33        |
| GPIO0_45        | IO           | General Purpose Input/Output | AL34        |
| GPIO0_46        | IO           | General Purpose Input/Output | AC34        |
| GPIO0_47        | IO           | General Purpose Input/Output | AD33        |
| GPIO0_48        | IO           | General Purpose Input/Output | AD38        |
| GPIO0_49        | IO           | General Purpose Input/Output | AD36        |
| GPIO0_50        | IO           | General Purpose Input/Output | AJ32        |
| GPIO0_51        | IO           | General Purpose Input/Output | AM37        |
| GPIO0_52        | IO           | General Purpose Input/Output | AP38        |
| GPIO0_53        | IO           | General Purpose Input/Output | AN38        |
| GPIO0_54        | IO           | General Purpose Input/Output | AM35        |
| GPIO0_55        | IO           | General Purpose Input/Output | AM36        |
| GPIO0_56        | IO           | General Purpose Input/Output | AN36        |
| GPIO0_57        | IO           | General Purpose Input/Output | AP37        |
| GPIO0_58        | IO           | General Purpose Input/Output | AR38        |
| GPIO0_59        | IO           | General Purpose Input/Output | AN37        |
| GPIO0_60        | IO           | General Purpose Input/Output | AC38        |
| GPIO0_61        | IO           | General Purpose Input/Output | AA32        |
| GPIO0_62        | IO           | General Purpose Input/Output | AB34        |
| GPIO0_63        | IO           | General Purpose Input/Output | AA33        |
| GPIO0_64        | IO           | General Purpose Input/Output | AB38        |
| GPIO0_65        | IO           | General Purpose Input/Output | AB36        |

### 6.3.3.2 WKUP Domain

**表 6-10. WKUP\_GPIO0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALY PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| WKUP_GPIO0_0    | IO           | General Purpose Input/Output | H38         |
| WKUP_GPIO0_1    | IO           | General Purpose Input/Output | J34         |



表 6-10. WKUP\_GPIO0 Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALY PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| WKUP_GPIO0_2    | IO           | General Purpose Input/Output | J35         |
| WKUP_GPIO0_3    | IO           | General Purpose Input/Output | J36         |
| WKUP_GPIO0_4    | IO           | General Purpose Input/Output | H35         |
| WKUP_GPIO0_5    | IO           | General Purpose Input/Output | K36         |
| WKUP_GPIO0_6    | IO           | General Purpose Input/Output | L37         |
| WKUP_GPIO0_7    | IO           | General Purpose Input/Output | L36         |
| WKUP_GPIO0_8    | IO           | General Purpose Input/Output | L35         |
| WKUP_GPIO0_9    | IO           | General Purpose Input/Output | L34         |
| WKUP_GPIO0_10   | IO           | General Purpose Input/Output | L33         |
| WKUP_GPIO0_11   | IO           | General Purpose Input/Output | M38         |
| WKUP_GPIO0_12   | IO           | General Purpose Input/Output | J37         |
| WKUP_GPIO0_13   | IO           | General Purpose Input/Output | K38         |
| WKUP_GPIO0_14   | IO           | General Purpose Input/Output | H37         |
| WKUP_GPIO0_15   | IO           | General Purpose Input/Output | K37         |
| WKUP_GPIO0_16   | IO           | General Purpose Input/Output | E32         |
| WKUP_GPIO0_17   | IO           | General Purpose Input/Output | D32         |
| WKUP_GPIO0_18   | IO           | General Purpose Input/Output | C34         |
| WKUP_GPIO0_19   | IO           | General Purpose Input/Output | B33         |
| WKUP_GPIO0_20   | IO           | General Purpose Input/Output | B32         |
| WKUP_GPIO0_21   | IO           | General Purpose Input/Output | C33         |
| WKUP_GPIO0_22   | IO           | General Purpose Input/Output | C35         |
| WKUP_GPIO0_23   | IO           | General Purpose Input/Output | D33         |
| WKUP_GPIO0_24   | IO           | General Purpose Input/Output | D34         |
| WKUP_GPIO0_25   | IO           | General Purpose Input/Output | E34         |
| WKUP_GPIO0_26   | IO           | General Purpose Input/Output | E33         |
| WKUP_GPIO0_27   | IO           | General Purpose Input/Output | A32         |
| WKUP_GPIO0_28   | IO           | General Purpose Input/Output | A33         |
| WKUP_GPIO0_29   | IO           | General Purpose Input/Output | B34         |
| WKUP_GPIO0_30   | IO           | General Purpose Input/Output | C32         |
| WKUP_GPIO0_31   | IO           | General Purpose Input/Output | F32         |
| WKUP_GPIO0_32   | IO           | General Purpose Input/Output | C31         |
| WKUP_GPIO0_33   | IO           | General Purpose Input/Output | F31         |
| WKUP_GPIO0_34   | IO           | General Purpose Input/Output | E35         |
| WKUP_GPIO0_35   | IO           | General Purpose Input/Output | D31         |
| WKUP_GPIO0_36   | IO           | General Purpose Input/Output | G31         |
| WKUP_GPIO0_37   | IO           | General Purpose Input/Output | F33         |
| WKUP_GPIO0_38   | IO           | General Purpose Input/Output | G32         |
| WKUP_GPIO0_39   | IO           | General Purpose Input/Output | G33         |
| WKUP_GPIO0_40   | IO           | General Purpose Input/Output | C38         |
| WKUP_GPIO0_41   | IO           | General Purpose Input/Output | C37         |
| WKUP_GPIO0_42   | IO           | General Purpose Input/Output | E38         |
| WKUP_GPIO0_43   | IO           | General Purpose Input/Output | E37         |
| WKUP_GPIO0_44   | IO           | General Purpose Input/Output | D38         |
| WKUP_GPIO0_45   | IO           | General Purpose Input/Output | D37         |
| WKUP_GPIO0_46   | IO           | General Purpose Input/Output | E36         |

**表 6-10. WKUP\_GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALY PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| WKUP_GPIO0_47   | IO           | General Purpose Input/Output | B37         |
| WKUP_GPIO0_48   | IO           | General Purpose Input/Output | D36         |
| WKUP_GPIO0_49   | IO           | General Purpose Input/Output | M33         |
| WKUP_GPIO0_50   | IO           | General Purpose Input/Output | B36         |
| WKUP_GPIO0_51   | IO           | General Purpose Input/Output | A35         |
| WKUP_GPIO0_52   | IO           | General Purpose Input/Output | B35         |
| WKUP_GPIO0_53   | IO           | General Purpose Input/Output | A36         |
| WKUP_GPIO0_54   | IO           | General Purpose Input/Output | G38         |
| WKUP_GPIO0_55   | IO           | General Purpose Input/Output | H36         |
| WKUP_GPIO0_56   | IO           | General Purpose Input/Output | M37         |
| WKUP_GPIO0_57   | IO           | General Purpose Input/Output | M36         |
| WKUP_GPIO0_58   | IO           | General Purpose Input/Output | K35         |
| WKUP_GPIO0_59   | IO           | General Purpose Input/Output | K34         |
| WKUP_GPIO0_60   | IO           | General Purpose Input/Output | K33         |
| WKUP_GPIO0_61   | IO           | General Purpose Input/Output | F38         |
| WKUP_GPIO0_62   | IO           | General Purpose Input/Output | C36         |
| WKUP_GPIO0_63   | IO           | General Purpose Input/Output | N33         |
| WKUP_GPIO0_64   | IO           | General Purpose Input/Output | N35         |
| WKUP_GPIO0_65   | IO           | General Purpose Input/Output | M35         |
| WKUP_GPIO0_66   | IO           | General Purpose Input/Output | N34         |
| WKUP_GPIO0_67   | IO           | General Purpose Input/Output | M34         |
| WKUP_GPIO0_68   | IO           | General Purpose Input/Output | F36         |
| WKUP_GPIO0_69   | IO           | General Purpose Input/Output | J38         |
| WKUP_GPIO0_70   | IO           | General Purpose Input/Output | F37         |
| WKUP_GPIO0_71   | I            | General Purpose Input/Output | P36         |
| WKUP_GPIO0_72   | I            | General Purpose Input/Output | V36         |
| WKUP_GPIO0_73   | I            | General Purpose Input/Output | T34         |
| WKUP_GPIO0_74   | I            | General Purpose Input/Output | T36         |
| WKUP_GPIO0_75   | I            | General Purpose Input/Output | P34         |
| WKUP_GPIO0_76   | I            | General Purpose Input/Output | R37         |
| WKUP_GPIO0_77   | I            | General Purpose Input/Output | R33         |
| WKUP_GPIO0_78   | I            | General Purpose Input/Output | V38         |
| WKUP_GPIO0_79   | I            | General Purpose Input/Output | Y38         |
| WKUP_GPIO0_80   | I            | General Purpose Input/Output | Y34         |
| WKUP_GPIO0_81   | I            | General Purpose Input/Output | V34         |
| WKUP_GPIO0_82   | I            | General Purpose Input/Output | W37         |
| WKUP_GPIO0_83   | I            | General Purpose Input/Output | AA37        |
| WKUP_GPIO0_84   | I            | General Purpose Input/Output | W33         |
| WKUP_GPIO0_85   | I            | General Purpose Input/Output | U33         |
| WKUP_GPIO0_86   | I            | General Purpose Input/Output | Y36         |
| WKUP_GPIO0_87   | IO           | General Purpose Input/Output | G34         |
| WKUP_GPIO0_88   | IO           | General Purpose Input/Output | L38         |

### 6.3.4 I2C

#### 6.3.4.1 MAIN Domain

表 6-11. I2C0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C0_SCL        | IOD          | I2C Clock       | AN36        |
| I2C0_SDA        | IOD          | I2C Data        | AP37        |

表 6-12. I2C1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4]      |
|-----------------|--------------|-----------------|------------------|
| I2C1_SCL        | IOD          | I2C Clock       | AD36, AE34, AJ35 |
| I2C1_SDA        | IOD          | I2C Data        | AH34, AJ32, AL33 |

表 6-13. I2C2 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C2_SCL        | IOD          | I2C Clock       | AC32, AN38  |
| I2C2_SDA        | IOD          | I2C Data        | AC37, AM35  |

表 6-14. I2C3 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C3_SCL        | IOD          | I2C Clock       | AC38, AF38  |
| I2C3_SDA        | IOD          | I2C Data        | AA32, AE36  |

表 6-15. I2C4 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4]      |
|-----------------|--------------|-----------------|------------------|
| I2C4_SCL        | IOD          | I2C Clock       | AA33, AG33, AG38 |
| I2C4_SDA        | IOD          | I2C Data        | AB34, AH33, AK34 |

表 6-16. I2C5 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C5_SCL        | IOD          | I2C Clock       | AC33, AG34  |
| I2C5_SDA        | IOD          | I2C Data        | AH37, AK36  |

表 6-17. I2C6 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| I2C6_SCL        | IOD          | I2C Clock       | AB36, AN37  |
| I2C6_SDA        | IOD          | I2C Data        | AB38, AR38  |

#### 6.3.4.2 MCU Domain

表 6-18. MCU\_I2C0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_I2C0_SCL    | IOD          | I2C Clock       | M35         |
| MCU_I2C0_SDA    | IOD          | I2C Data        | G34         |

表 6-19. MCU\_I2C1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_I2C1_SCL    | IOD          | I2C Clock       | L35, L37    |

**表 6-19. MCU\_I2C1 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_I2C1_SDA    | IOD          | I2C Data        | L34, L36    |

### 6.3.4.3 WKUP Domain

**表 6-20. WKUP\_I2C0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| WKUP_I2C0_SCL   | IOD          | I2C Clock       | N33         |
| WKUP_I2C0_SDA   | IOD          | I2C Data        | N35         |

## 6.3.5 I3C

### 6.3.5.1 MCU Domain

**表 6-21. MCU\_I3C0 Signal Descriptions**

| SIGNAL NAME [1]    | PIN TYPE [2] | DESCRIPTION [3]      | ALY PIN [4] |
|--------------------|--------------|----------------------|-------------|
| MCU_I3C0_SCL       | IO           | I3C Clock            | L35         |
| MCU_I3C0_SDA       | IO           | I3C Data             | L34         |
| MCU_I3C0_SDAPULLEN | OD           | I3C Data Pull Enable | L38, M38    |

## 6.3.6 MCAN

### 6.3.6.1 MAIN Domain

**表 6-22. MCAN0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN0_RX        | I            | MCAN Receive Data  | AE38        |
| MCAN0_TX        | O            | MCAN Transmit Data | AF38        |

**表 6-23. MCAN1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN1_RX        | I            | MCAN Receive Data  | AH38, AJ32  |
| MCAN1_TX        | O            | MCAN Transmit Data | AJ37        |

**表 6-24. MCAN2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN2_RX        | I            | MCAN Receive Data  | AH37        |
| MCAN2_TX        | O            | MCAN Transmit Data | AC33        |

**表 6-25. MCAN3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN3_RX        | I            | MCAN Receive Data  | AK34        |
| MCAN3_TX        | O            | MCAN Transmit Data | AJ38        |

**表 6-26. MCAN4 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN4_RX        | I            | MCAN Receive Data  | AF36        |
| MCAN4_TX        | O            | MCAN Transmit Data | AG38        |

表 6-27. MCAN5 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN5_RX        | I            | MCAN Receive Data  | AC35, AK38  |
| MCAN5_TX        | O            | MCAN Transmit Data | AE35, AK35  |

表 6-28. MCAN6 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN6_RX        | I            | MCAN Receive Data  | AG37, AH36  |
| MCAN6_TX        | O            | MCAN Transmit Data | AF37, AG35  |

表 6-29. MCAN7 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN7_RX        | I            | MCAN Receive Data  | AC32, AD34  |
| MCAN7_TX        | O            | MCAN Transmit Data | AF35, AK33  |

表 6-30. MCAN8 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN8_RX        | I            | MCAN Receive Data  | AD37, AF34  |
| MCAN8_TX        | O            | MCAN Transmit Data | AC37, AJ36  |

表 6-31. MCAN9 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN9_RX        | I            | MCAN Receive Data  | AC36, AL33  |
| MCAN9_TX        | O            | MCAN Transmit Data | AE34, AE37  |

表 6-32. MCAN10 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN10_RX       | I            | MCAN Receive Data  | AC34        |
| MCAN10_TX       | O            | MCAN Transmit Data | AL34        |

表 6-33. MCAN11 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN11_RX       | I            | MCAN Receive Data  | AD38        |
| MCAN11_TX       | O            | MCAN Transmit Data | AD33        |

表 6-34. MCAN12 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN12_RX       | I            | MCAN Receive Data  | AJ33, AK37  |
| MCAN12_TX       | O            | MCAN Transmit Data | AD36, AG36  |

表 6-35. MCAN13 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN13_RX       | I            | MCAN Receive Data  | AH33, AN37  |
| MCAN13_TX       | O            | MCAN Transmit Data | AF33, AR38  |

**表 6-36. MCAN14 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN14_RX       | I            | MCAN Receive Data  | AK36, AP38  |
| MCAN14_TX       | O            | MCAN Transmit Data | AG33, AM37  |

**表 6-37. MCAN15 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN15_RX       | I            | MCAN Receive Data  | AB36, AJ35  |
| MCAN15_TX       | O            | MCAN Transmit Data | AB38, AG34  |

**表 6-38. MCAN16 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN16_RX       | I            | MCAN Receive Data  | AE33        |
| MCAN16_TX       | O            | MCAN Transmit Data | AH34        |

**表 6-39. MCAN17 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCAN17_RX       | I            | MCAN Receive Data  | AE36, AJ34  |
| MCAN17_TX       | O            | MCAN Transmit Data | AL32        |

### 6.3.6.2 MCU Domain

**表 6-40. MCU\_MCAN0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCU_MCAN0_RX    | I            | MCAN Receive Data  | F38         |
| MCU_MCAN0_TX    | O            | MCAN Transmit Data | K33         |

**表 6-41. MCU\_MCAN1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| MCU_MCAN1_RX    | I            | MCAN Receive Data  | K36         |
| MCU_MCAN1_TX    | O            | MCAN Transmit Data | H35         |

### 6.3.7 MCSPI

#### 6.3.7.1 MAIN Domain

**表 6-42. MCSPI0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI0_CLK        | IO           | SPI Clock         | AN38        |
| SPI0_CS0        | IO           | SPI Chip Select 0 | AM37        |
| SPI0_CS1        | IO           | SPI Chip Select 1 | AP38        |
| SPI0_CS2        | IO           | SPI Chip Select 2 | AJ35        |
| SPI0_CS3        | IO           | SPI Chip Select 3 | AE33        |
| SPI0_D0         | IO           | SPI Data 0        | AM35        |
| SPI0_D1         | IO           | SPI Data 1        | AM36        |

**表 6-43. MCSPI1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI1_CLK        | IO           | SPI Clock         | AB38        |
| SPI1_CS0        | IO           | SPI Chip Select 0 | AC38        |

表 6-43. MCSPI1 Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI1_CS1        | IO           | SPI Chip Select 1 | AA32        |
| SPI1_CS2        | IO           | SPI Chip Select 2 | AB34        |
| SPI1_CS3        | IO           | SPI Chip Select 3 | AH34        |
| SPI1_D0         | IO           | SPI Data 0        | AA33        |
| SPI1_D1         | IO           | SPI Data 1        | AB36        |

表 6-44. MCSPI2 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI2_CLK        | IO           | SPI Clock         | AD34        |
| SPI2_CS0        | IO           | SPI Chip Select 0 | AJ36        |
| SPI2_CS1        | IO           | SPI Chip Select 1 | AF35        |
| SPI2_CS2        | IO           | SPI Chip Select 2 | AF37        |
| SPI2_CS3        | IO           | SPI Chip Select 3 | AG37        |
| SPI2_D0         | IO           | SPI Data 0        | AF34        |
| SPI2_D1         | IO           | SPI Data 1        | AE34        |

表 6-45. MCSPI3 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI3_CLK        | IO           | SPI Clock         | AD38        |
| SPI3_CS0        | IO           | SPI Chip Select 0 | AD33        |
| SPI3_CS1        | IO           | SPI Chip Select 1 | AJ38        |
| SPI3_CS2        | IO           | SPI Chip Select 2 | AF36        |
| SPI3_CS3        | IO           | SPI Chip Select 3 | AC34        |
| SPI3_D0         | IO           | SPI Data 0        | AC32        |
| SPI3_D1         | IO           | SPI Data 1        | AC37        |

表 6-46. MCSPI5 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI5_CLK        | IO           | SPI Clock         | AJ38        |
| SPI5_CS0        | IO           | SPI Chip Select 0 | AE38        |
| SPI5_CS1        | IO           | SPI Chip Select 1 | AF38        |
| SPI5_CS2        | IO           | SPI Chip Select 2 | AD37        |
| SPI5_CS3        | IO           | SPI Chip Select 3 | AE37        |
| SPI5_D0         | IO           | SPI Data 0        | AH38        |
| SPI5_D1         | IO           | SPI Data 1        | AF36        |

表 6-47. MCSPI6 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI6_CLK        | IO           | SPI Clock         | AK37        |
| SPI6_CS0        | IO           | SPI Chip Select 0 | AJ34        |
| SPI6_CS1        | IO           | SPI Chip Select 1 | AH37        |
| SPI6_CS2        | IO           | SPI Chip Select 2 | AK34        |
| SPI6_CS3        | IO           | SPI Chip Select 3 | AG38        |
| SPI6_D0         | IO           | SPI Data 0        | AD36        |

**表 6-47. MCSPI6 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| SPI6_D1         | IO           | SPI Data 1      | AC33        |

**表 6-48. MCSPI7 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4] |
|-----------------|--------------|-------------------|-------------|
| SPI7_CLK        | IO           | SPI Clock         | AF37        |
| SPI7_CS0        | IO           | SPI Chip Select 0 | AG37        |
| SPI7_CS1        | IO           | SPI Chip Select 1 | AD37        |
| SPI7_CS2        | IO           | SPI Chip Select 2 | AE37        |
| SPI7_CS3        | IO           | SPI Chip Select 3 | AL32        |
| SPI7_D0         | IO           | SPI Data 0        | AE38        |
| SPI7_D1         | IO           | SPI Data 1        | AJ38        |

### 6.3.7.2 MCU Domain

**表 6-49. MCU\_MCSPI0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4] |
|-----------------|--------------|-------------------|-------------|
| MCU_SPI0_CLK    | IO           | SPI Clock         | G38         |
| MCU_SPI0_CS0    | IO           | SPI Chip Select 0 | F37         |
| MCU_SPI0_CS1    | IO           | SPI Chip Select 1 | F33, J37    |
| MCU_SPI0_CS2    | IO           | SPI Chip Select 2 | G33, H37    |
| MCU_SPI0_CS3    | IO           | SPI Chip Select 3 | H35         |
| MCU_SPI0_D0     | IO           | SPI Data 0        | H36         |
| MCU_SPI0_D1     | IO           | SPI Data 1        | J38         |

**表 6-50. MCU\_MCSPI1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]   | ALY PIN [4] |
|-----------------|--------------|-------------------|-------------|
| MCU_SPI1_CLK    | IO           | SPI Clock         | H38         |
| MCU_SPI1_CS0    | IO           | SPI Chip Select 0 | J36         |
| MCU_SPI1_CS1    | IO           | SPI Chip Select 1 | D31, K38    |
| MCU_SPI1_CS2    | IO           | SPI Chip Select 2 | G31, K37    |
| MCU_SPI1_CS3    | IO           | SPI Chip Select 3 | K36         |
| MCU_SPI1_D0     | IO           | SPI Data 0        | J34         |
| MCU_SPI1_D1     | IO           | SPI Data 1        | J35         |

### 6.3.8 UART

#### 6.3.8.1 MAIN Domain

**表 6-51. UART0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                       | ALY PIN [4]      |
|-----------------|--------------|---------------------------------------|------------------|
| UART0_CTSn      | I            | UART Clear to Send (active low)       | AC32, AC38       |
| UART0_DCDn      | I            | UART Data Carrier Detect (active low) | AJ33             |
| UART0_DSRn      | I            | UART Data Set Ready (active low)      | AF33             |
| UART0_DTRn      | O            | UART Data Terminal Ready (active low) | AH33             |
| UART0_RIn       | I            | UART Ring Indicator                   | AG33             |
| UART0_RTSn      | O            | UART Request to Send (active low)     | AB38, AC37, AP38 |
| UART0_RXD       | I            | UART Receive Data                     | AD33             |



表 6-51. UART0 Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| UART0_TXD       | O            | UART Transmit Data | AD38        |

表 6-52. UART1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| UART1_CTSn      | I            | UART Clear to Send (active low)   | AC36, AN38  |
| UART1_RTSn      | O            | UART Request to Send (active low) | AE36, AM35  |
| UART1_RXD       | I            | UART Receive Data                 | AD37        |
| UART1_TXD       | O            | UART Transmit Data                | AE37        |

表 6-53. UART2 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4]      |
|-----------------|--------------|-----------------------------------|------------------|
| UART2_CTSn      | I            | UART Clear to Send (active low)   | AD36             |
| UART2_RTSn      | O            | UART Request to Send (active low) | AJ32             |
| UART2_RXD       | I            | UART Receive Data                 | AB34, AF38, AM35 |
| UART2_TXD       | O            | UART Transmit Data                | AA33, AE38, AM36 |

表 6-54. UART3 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4]      |
|-----------------|--------------|-----------------------------------|------------------|
| UART3_CTSn      | I            | UART Clear to Send (active low)   | AJ38             |
| UART3_RTSn      | O            | UART Request to Send (active low) | AH38             |
| UART3_RXD       | I            | UART Receive Data                 | AC33, AD36, AR38 |
| UART3_TXD       | O            | UART Transmit Data                | AH37, AJ32, AN37 |

表 6-55. UART4 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4]            |
|-----------------|--------------|-----------------------------------|------------------------|
| UART4_CTSn      | I            | UART Clear to Send (active low)   | AB38, AG35, AK33       |
| UART4_RTSn      | O            | UART Request to Send (active low) | AB36, AC34, AH36       |
| UART4_RXD       | I            | UART Receive Data                 | AB34, AE35, AF37, AL34 |
| UART4_TXD       | O            | UART Transmit Data                | AA33, AC35, AF33, AG37 |

表 6-56. UART5 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4]      |
|-----------------|--------------|-----------------------------------|------------------|
| UART5_CTSn      | I            | UART Clear to Send (active low)   | AB34, AJ36       |
| UART5_RTSn      | O            | UART Request to Send (active low) | AA33, AF34       |
| UART5_RXD       | I            | UART Receive Data                 | AC38, AF35, AJ33 |
| UART5_TXD       | O            | UART Transmit Data                | AA32, AD34, AG36 |

表 6-57. UART6 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4]      |
|-----------------|--------------|-----------------------------------|------------------|
| UART6_CTSn      | I            | UART Clear to Send (active low)   | AF38             |
| UART6_RTSn      | O            | UART Request to Send (active low) | AE38             |
| UART6_RXD       | I            | UART Receive Data                 | AC36, AG33, AK37 |
| UART6_TXD       | O            | UART Transmit Data                | AE36, AH33, AJ37 |

**表 6-58. UART7 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4]      |
|-----------------|--------------|-----------------------------------|------------------|
| UART7_CTSn      | I            | UART Clear to Send (active low)   | AB34             |
| UART7_RTSn      | O            | UART Request to Send (active low) | AA33             |
| UART7_RXD       | I            | UART Receive Data                 | AC38, AJ36, AL32 |
| UART7_TXD       | O            | UART Transmit Data                | AA32, AF34, AJ34 |

**表 6-59. UART8 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4]            |
|-----------------|--------------|-----------------------------------|------------------------|
| UART8_CTSn      | I            | UART Clear to Send (active low)   | AF37                   |
| UART8_RTSn      | O            | UART Request to Send (active low) | AG37                   |
| UART8_RXD       | I            | UART Receive Data                 | AB38, AE34, AK35, AP38 |
| UART8_TXD       | O            | UART Transmit Data                | AB36, AK38, AL33, AN38 |

**表 6-60. UART9 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| UART9_CTSn      | I            | UART Clear to Send (active low)   | AK33, AK37  |
| UART9_RTSn      | O            | UART Request to Send (active low) | AC34, AJ34  |
| UART9_RXD       | I            | UART Receive Data                 | AC32, AG34  |
| UART9_TXD       | O            | UART Transmit Data                | AC37, AK36  |

### 6.3.8.2 MCU Domain

**表 6-61. MCU\_UART0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4]   |
|-----------------|--------------|-----------------------------------|---------------|
| MCU_UART0_CTSn  | I            | UART Clear to Send (active low)   | F33, H37      |
| MCU_UART0_RTSn  | O            | UART Request to Send (active low) | G33, K37      |
| MCU_UART0_RXD   | I            | UART Receive Data                 | D31, K38, M38 |
| MCU_UART0_TXD   | O            | UART Transmit Data                | G31, J37, L33 |

### 6.3.8.3 WKUP Domain

**表 6-62. WKUP\_UART0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| WKUP_UART0_CTSn | I            | UART Clear to Send (active low)   | L37         |
| WKUP_UART0_RTSn | O            | UART Request to Send (active low) | L36         |
| WKUP_UART0_RXD  | I            | UART Receive Data                 | K35         |
| WKUP_UART0_TXD  | O            | UART Transmit Data                | K34         |

## 6.3.9 MDIO

### 6.3.9.1 MAIN Domain

**表 6-63. MDIO0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MDIO0_MDC       | O            | MDIO Clock      | AD38        |
| MDIO0_MDIO      | IO           | MDIO Data       | AD33        |

表 6-64. MDIO1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MDIO1_MDC       | O            | MDIO Clock      | AE37        |
| MDIO1_MDIO      | IO           | MDIO Data       | AC36        |

## 6.3.9.2 MCU Domain

表 6-65. MCU\_MDIO0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| MCU_MDIO0_MDC   | O            | MDIO Clock      | A36         |
| MCU_MDIO0_MDIO  | IO           | MDIO Data       | B35         |

## 6.3.10 UFS

## 6.3.10.1 MAIN Domain

表 6-66. UFS0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]              | ALY PIN [4] |
|-----------------|--------------|------------------------------|-------------|
| UFS0_REF_CLK    | I            | UFS Reference Clock          | AM7         |
| UFS0_RSTn       | I            | UFS Reset                    | AM8         |
| UFS0_RX_DN0     | I            | UFS Receive Data (negative)  | AM4         |
| UFS0_RX_DN1     | I            | UFS Receive Data (negative)  | AM1         |
| UFS0_RX_DP0     | I            | UFS Receive Data (positive)  | AM5         |
| UFS0_RX_DP1     | I            | UFS Receive Data (positive)  | AM2         |
| UFS0_TX_DN0     | I            | UFS Transmit Data (negative) | AL2         |
| UFS0_TX_DN1     | I            | UFS Transmit Data (negative) | AN2         |
| UFS0_TX_DP0     | I            | UFS Transmit Data (positive) | AL3         |
| UFS0_TX_DP1     | I            | UFS Transmit Data (positive) | AN3         |

## 6.3.11 CPSW2G

## 6.3.11.1 MAIN Domain

表 6-67. CPSW2G0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                 | ALY PIN [4] |
|-----------------|--------------|---------------------------------|-------------|
| CLKOUT          | IO           | RMII Clock Output               | AF34        |
| RGMII1_RXC      | I            | RGMII Receive Clock             | AL33        |
| RGMII1_RX_CTL   | I            | RGMII Receive Control           | AE34        |
| RGMII1_TXC      | O            | RGMII Transmit Clock            | AL34        |
| RGMII1_TX_CTL   | O            | RGMII Transmit Control          | AF35        |
| RGMII1_RD0      | I            | RGMII Receive Data 0            | AC34        |
| RGMII1_RD1      | I            | RGMII Receive Data 1            | AD34        |
| RGMII1_RD2      | I            | RGMII Receive Data 2            | AJ36        |
| RGMII1_RD3      | I            | RGMII Receive Data 3            | AF34        |
| RGMII1_TD0      | O            | RGMII Transmit Data 0           | AE35        |
| RGMII1_TD1      | O            | RGMII Transmit Data 1           | AC35        |
| RGMII1_TD2      | O            | RGMII Transmit Data 2           | AG35        |
| RGMII1_TD3      | O            | RGMII Transmit Data 3           | AH36        |
| RMII1_CRD_DV    | I            | RMII Carrier Sense / Data Valid | AH36        |
| RMII1_RX_ER     | I            | RMII Receive Data Error         | AF35        |
| RMII1_TX_EN     | O            | RMII Transmit Enable            | AE34        |

**表 6-67. CPSW2G0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]      | ALY PIN [4] |
|-----------------|--------------|----------------------|-------------|
| RMII1_RXD0      | I            | RMII Receive Data 0  | AC35        |
| RMII1_RXD1      | I            | RMII Receive Data 1  | AG35        |
| RMII1_TXD0      | O            | RMII Transmit Data 0 | AD34        |
| RMII1_TXD1      | O            | RMII Transmit Data 1 | AL33        |
| RMII_REF_CLK    | I            | RMII Reference Clock | AJ36        |

### 6.3.11.2 MCU Domain

**表 6-68. MCU\_CPSW2G0 Signal Descriptions**

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                 | ALY PIN [4] |
|-------------------|--------------|---------------------------------|-------------|
| MCU_RGMII1_RXC    | I            | RGMII Receive Clock             | B37         |
| MCU_RGMII1_RX_CTL | I            | RGMII Receive Control           | C37         |
| MCU_RGMII1_TXC    | O            | RGMII Transmit Clock            | E36         |
| MCU_RGMII1_TX_CTL | O            | RGMII Transmit Control          | C38         |
| MCU_RGMII1_RD0    | I            | RGMII Receive Data 0            | A35         |
| MCU_RGMII1_RD1    | I            | RGMII Receive Data 1            | B36         |
| MCU_RGMII1_RD2    | I            | RGMII Receive Data 2            | C36         |
| MCU_RGMII1_RD3    | I            | RGMII Receive Data 3            | D36         |
| MCU_RGMII1_TD0    | O            | RGMII Transmit Data 0           | D37         |
| MCU_RGMII1_TD1    | O            | RGMII Transmit Data 1           | D38         |
| MCU_RGMII1_TD2    | O            | RGMII Transmit Data 2           | E37         |
| MCU_RGMII1_TD3    | O            | RGMII Transmit Data 3           | E38         |
| MCU_RMII1_CRD_DV  | I            | RMII Carrier Sense / Data Valid | C38         |
| MCU_RMII1_REF_CLK | I            | RMII Reference Clock            | B37         |
| MCU_RMII1_RX_ER   | I            | RMII Receive Data Error         | C37         |
| MCU_RMII1_TX_EN   | O            | RMII Transmit Enable            | E36         |
| MCU_RMII1_RXD0    | I            | RMII Receive Data 0             | A35         |
| MCU_RMII1_RXD1    | I            | RMII Receive Data 1             | B36         |
| MCU_RMII1_TXD0    | O            | RMII Transmit Data 0            | D37         |
| MCU_RMII1_TXD1    | O            | RMII Transmit Data 1            | D38         |

### 6.3.12 SGMII

#### 6.3.12.1 MAIN Domain

**表 6-69. CPSW9X0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]           | ALY PIN [4] |
|-----------------|--------------|---------------------------|-------------|
| SGMII1_RXN0     | I            | SGMII Receive (negative)  | AU2, AU20   |
| SGMII1_RXP0     | I            | SGMII Receive (positive)  | AU21, AU3   |
| SGMII1_TXN0     | O            | SGMII Transmit (negative) | AR2, AR20   |
| SGMII1_TXP0     | O            | SGMII Transmit (positive) | AR21, AR3   |
| SGMII2_RXN0     | I            | SGMII Receive (negative)  | AT1, AT19   |
| SGMII2_RXP0     | I            | SGMII Receive (positive)  | AT2, AT20   |
| SGMII2_TXN0     | O            | SGMII Transmit (negative) | AP1, AP19   |
| SGMII2_TXP0     | O            | SGMII Transmit (positive) | AP2, AP20   |
| SGMII3_RXN0     | I            | SGMII Receive (negative)  | AU5         |
| SGMII3_RXP0     | I            | SGMII Receive (positive)  | AU6         |
| SGMII3_TXN0     | O            | SGMII Transmit (negative) | AV6         |

表 6-69. CPSW9X0 Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]           | ALY PIN [4] |
|-----------------|--------------|---------------------------|-------------|
| SGMII3_TXP0     | O            | SGMII Transmit (positive) | AV7         |
| SGMII4_RXN0     | I            | SGMII Receive (negative)  | AT4         |
| SGMII4_RXP0     | I            | SGMII Receive (positive)  | AT5         |
| SGMII4_TXN0     | O            | SGMII Transmit (negative) | AR5         |
| SGMII4_TXP0     | O            | SGMII Transmit (positive) | AR6         |
| SGMII5_RXN0     | I            | SGMII Receive (negative)  | AR14, AU23  |
| SGMII5_RXP0     | I            | SGMII Receive (positive)  | AR15, AU24  |
| SGMII5_TXN0     | O            | SGMII Transmit (negative) | AP13, AV24  |
| SGMII5_TXP0     | O            | SGMII Transmit (positive) | AP14, AV25  |
| SGMII6_RXN0     | I            | SGMII Receive (negative)  | AT22, AU14  |
| SGMII6_RXP0     | I            | SGMII Receive (positive)  | AT23, AU15  |
| SGMII6_TXN0     | O            | SGMII Transmit (negative) | AR23, AT13  |
| SGMII6_TXP0     | O            | SGMII Transmit (positive) | AR24, AT14  |
| SGMII7_RXN0     | I            | SGMII Receive (negative)  | AR17, AU20  |
| SGMII7_RXP0     | I            | SGMII Receive (positive)  | AR18, AU21  |
| SGMII7_TXN0     | O            | SGMII Transmit (negative) | AR20, AT16  |
| SGMII7_TXP0     | O            | SGMII Transmit (positive) | AR21, AT17  |
| SGMII8_RXN0     | I            | SGMII Receive (negative)  | AT19, AU17  |
| SGMII8_RXP0     | I            | SGMII Receive (positive)  | AT20, AU18  |
| SGMII8_TXN0     | O            | SGMII Transmit (negative) | AP19, AV18  |
| SGMII8_TXP0     | O            | SGMII Transmit (positive) | AP20, AV19  |

### 6.3.13 ECAP

#### 6.3.13.1 MAIN Domain

表 6-70. ECAP0 Signal Descriptions

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                              | ALY PIN [4] |
|-------------------|--------------|--------------------------------------------------------------|-------------|
| ECAP0_IN_APWM_OUT | IO           | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | AB34, AD36  |

表 6-71. ECAP1 Signal Descriptions

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                              | ALY PIN [4] |
|-------------------|--------------|--------------------------------------------------------------|-------------|
| ECAP1_IN_APWM_OUT | IO           | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | AA33, AR38  |

表 6-72. ECAP2 Signal Descriptions

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                              | ALY PIN [4] |
|-------------------|--------------|--------------------------------------------------------------|-------------|
| ECAP2_IN_APWM_OUT | IO           | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | AN37        |

### 6.3.14 EQEP

#### 6.3.14.1 MAIN Domain

表 6-73. EQEP0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]         | ALY PIN [4] |
|-----------------|--------------|-------------------------|-------------|
| EQEP0_A         | I            | EQEP Quadrature Input A | AF34        |
| EQEP0_B         | I            | EQEP Quadrature Input B | AE34        |

**表 6-73. EQEP0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EQEP0_I         | IO           | EQEP Index      | AD33        |
| EQEP0_S         | IO           | EQEP Strobe     | AC34        |

**表 6-74. EQEP1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]         | ALY PIN [4] |
|-----------------|--------------|-------------------------|-------------|
| EQEP1_A         | I            | EQEP Quadrature Input A | AL33        |
| EQEP1_B         | I            | EQEP Quadrature Input B | AL34        |
| EQEP1_I         | IO           | EQEP Index              | AK37        |
| EQEP1_S         | IO           | EQEP Strobe             | AD38        |

**表 6-75. EQEP2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]         | ALY PIN [4] |
|-----------------|--------------|-------------------------|-------------|
| EQEP2_A         | I            | EQEP Quadrature Input A | AK33        |
| EQEP2_B         | I            | EQEP Quadrature Input B | AC37        |
| EQEP2_I         | IO           | EQEP Index              | AC36        |
| EQEP2_S         | IO           | EQEP Strobe             | AD37        |

### 6.3.15 EPWM

#### 6.3.15.1 MAIN Domain

**表 6-76. EPWM Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                       | ALY PIN [4] |
|-----------------|--------------|---------------------------------------|-------------|
| EHRPWM_SOCA     | O            | EHRPWM Start of Conversion A          | AE37        |
| EHRPWM_SOCB     | O            | EHRPWM Start of Conversion B          | AD34        |
| EHRPWM_TZn_IN0  | I            | EHRPWM Trip Zone Input 0 (active low) | AJ38        |
| EHRPWM_TZn_IN1  | I            | EHRPWM Trip Zone Input 1 (active low) | AC32        |
| EHRPWM_TZn_IN2  | I            | EHRPWM Trip Zone Input 2 (active low) | AK35        |
| EHRPWM_TZn_IN3  | I            | EHRPWM Trip Zone Input 3 (active low) | AC35        |
| EHRPWM_TZn_IN4  | I            | EHRPWM Trip Zone Input 4 (active low) | AF36        |
| EHRPWM_TZn_IN5  | I            | EHRPWM Trip Zone Input 5 (active low) | AJ37        |

**表 6-77. EPWM0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                  | ALY PIN [4]      |
|-----------------|--------------|--------------------------------------------------|------------------|
| EHRPWM0_A       | IO           | EHRPWM Output A                                  | AA32, AE38, AM37 |
| EHRPWM0_B       | IO           | EHRPWM Output B                                  | AC38, AF38       |
| EHRPWM0_SYNCI   | I            | Sync Input to EHRPWM module from an external pin | AH38             |
| EHRPWM0_SYNCO   | O            | Sync Output to EHRPWM module to an external pin  | AG37             |

**表 6-78. EPWM1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4]      |
|-----------------|--------------|-----------------|------------------|
| EHRPWM1_A       | IO           | EHRPWM Output A | AA33, AE36, AP38 |
| EHRPWM1_B       | IO           | EHRPWM Output B | AB34, AC33       |

**表 6-79. EPWM2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4]      |
|-----------------|--------------|-----------------|------------------|
| EHRPWM2_A       | IO           | EHRPWM Output A | AB36, AF37, AN38 |

表 6-79. EPWM2 Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EHRPWM2_B       | IO           | EHRPWM Output B | AB38, AK38  |

表 6-80. EPWM3 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                  | ALY PIN [4]      |
|-----------------|--------------|--------------------------------------------------|------------------|
| EHRPWM3_A       | IO           | EHRPWM Output A                                  | AC38, AE35, AM35 |
| EHRPWM3_B       | IO           | EHRPWM Output B                                  | AF35             |
| EHRPWM3_SYNCI   | I            | Sync Input to EHRPWM module from an external pin | AH36             |
| EHRPWM3_SYNCO   | O            | Sync Output to EHRPWM module to an external pin  | AG35             |

表 6-81. EPWM4 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4]      |
|-----------------|--------------|-----------------|------------------|
| EHRPWM4_A       | IO           | EHRPWM Output A | AB34, AJ36, AM36 |
| EHRPWM4_B       | IO           | EHRPWM Output B | AH37             |

表 6-82. EPWM5 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| EHRPWM5_A       | IO           | EHRPWM Output A | AB38, AG38  |
| EHRPWM5_B       | IO           | EHRPWM Output B | AK34        |

### 6.3.16 USB

#### 6.3.16.1 MAIN Domain

表 6-83. USB0 Signal Descriptions

| SIGNAL NAME [1]            | PIN TYPE [2] | DESCRIPTION [3]                                  | ALY PIN [4]      |
|----------------------------|--------------|--------------------------------------------------|------------------|
| USB0_DM                    | IO           | USB 2.0 Differential Data (negative)             | AP16             |
| USB0_DP                    | IO           | USB 2.0 Differential Data (positive)             | AP17             |
| USB0_DRVVBUS               | O            | USB VBUS Control Output (active high)            | AE35, AL32, AN37 |
| USB0_ID                    | A            | USB 2.0 Dual-Role Device Role Select             | AN17             |
| USB0_RCALIB <sup>(1)</sup> | A            | Pin to connect to calibration resistor           | AN18             |
| USB0_VBUS <sup>(2)</sup>   | A            | USB Level-shifted VBUS Detector                  | AN15             |
| USB0_SSRX1N                | I            | SERDES_USB Differential Receive Data (negative)  | AR11, AR17       |
| USB0_SSRX1P                | I            | SERDES_USB Differential Receive Data (positive)  | AR12, AR18       |
| USB0_SSRX2N                | I            | SERDES_USB Differential Receive Data (negative)  | AU11, AU17       |
| USB0_SSRX2P                | I            | SERDES_USB Differential Receive Data (positive)  | AU12, AU18       |
| USB0_SSTX1N                | O            | SERDES_USB Differential Transmit Data (negative) | AT16, AV9        |
| USB0_SSTX1P                | O            | SERDES_USB Differential Transmit Data (positive) | AT17, AV10       |
| USB0_SSTX2N                | O            | SERDES_USB Differential Transmit Data (negative) | AV12, AV18       |
| USB0_SSTX2P                | O            | SERDES_USB Differential Transmit Data (positive) | AV13, AV19       |

(1) An external 500  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS, even when the pin is unused

(2) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see *USB VBUS Design Guidelines*.

### 6.3.17 Display Port

#### 6.3.17.1 MAIN Domain

**表 6-84. DP0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                     | ALY PIN [4]      |
|-----------------|--------------|-----------------------------------------------------|------------------|
| DP0_AUXN        | IO           | Display Port Differential Auxiliary Data (negative) | AP22             |
| DP0_AUXP        | IO           | Display Port Differential Auxiliary Data (positive) | AP23             |
| DP0_HPD         | I            | Display Port Hot Plug Detection                     | AC34, AG33, AM37 |
| DP0_TXN0        | O            | Display Port Differential Transmit (negative)       | AP13             |
| DP0_TXN1        | O            | Display Port Differential Transmit (negative)       | AT13             |
| DP0_TXN2        | O            | Display Port Differential Transmit (negative)       | AT16             |
| DP0_TXN3        | O            | Display Port Differential Transmit (negative)       | AV18             |
| DP0_TXP0        | O            | Display Port Differential Transmit (positive)       | AP14             |
| DP0_TXP1        | O            | Display Port Differential Transmit (positive)       | AT14             |
| DP0_TXP2        | O            | Display Port Differential Transmit (positive)       | AT17             |
| DP0_TXP3        | O            | Display Port Differential Transmit (positive)       | AV19             |

### 6.3.18 Hyperlink

#### 6.3.18.1 MAIN Domain

**表 6-85. Hyperlink Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]          | ALY PIN [4] |
|-----------------|--------------|--------------------------|-------------|
| HYP_RXN0        | I            | Hyperlink RX (negative)  | AR14, AR8   |
| HYP_RXN1        | I            | Hyperlink RX (negative)  | AT10, AU14  |
| HYP_RXN2        | I            | Hyperlink RX (negative)  | AR11, AR17  |
| HYP_RXN3        | I            | Hyperlink RX (negative)  | AU11, AU17  |
| HYP_RXP0        | I            | Hyperlink RX (positive)  | AR15, AR9   |
| HYP_RXP1        | I            | Hyperlink RX (positive)  | AT11, AU15  |
| HYP_RXP2        | I            | Hyperlink RX (positive)  | AR12, AR18  |
| HYP_RXP3        | I            | Hyperlink RX (positive)  | AU12, AU18  |
| HYP_TXN0        | O            | Hyperlink TX0 (negative) | AP13, AT7   |
| HYP_TXN1        | O            | Hyperlink TX0 (negative) | AP10, AT13  |
| HYP_TXN2        | O            | Hyperlink TX0 (negative) | AT16, AV9   |
| HYP_TXN3        | O            | Hyperlink TX0 (negative) | AV12, AV18  |
| HYP_TXP0        | O            | Hyperlink TX0 (positive) | AP14, AT8   |
| HYP_TXP1        | O            | Hyperlink TX0 (positive) | AP11, AT14  |
| HYP_TXP2        | O            | Hyperlink TX0 (positive) | AT17, AV10  |
| HYP_TXP3        | O            | Hyperlink TX0 (positive) | AV13, AV19  |

**表 6-86. Hyperlink0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                           | ALY PIN [4] |
|-----------------|--------------|-------------------------------------------|-------------|
| HYP0_RXFLCLK    | O            | Hyperlink Flow Management Receive Clock   | AK35        |
| HYP0_RXFLDAT    | O            | Hyperlink Flow Management Receive Data    | AK38        |
| HYP0_RXPMCLK    | I            | Hyperlink Power Management Receive Clock  | AC36        |
| HYP0_RXPMDAT    | I            | Hyperlink Power Management Receive Data   | AE36        |
| HYP0_TXFLCLK    | I            | Hyperlink Flow Management Transmit Clock  | AF37        |
| HYP0_TXFLDAT    | I            | Hyperlink Flow Management Transmit Data   | AG37        |
| HYP0_TXPMCLK    | O            | Hyperlink Power Management Transmit Clock | AD37        |



表 6-86. Hyperlink0 Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                          | ALY PIN [4] |
|-----------------|--------------|------------------------------------------|-------------|
| HYP0_TXPMDAT    | O            | Hyperlink Power Management Transmit Data | AE37        |

表 6-87. Hyperlink1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                           | ALY PIN [4] |
|-----------------|--------------|-------------------------------------------|-------------|
| HYP1_RXFLCLK    | O            | Hyperlink Flow Management Receive Clock   | AK33        |
| HYP1_RXFLDAT    | O            | Hyperlink Flow Management Receive Data    | AK37        |
| HYP1_RXPMCLK    | I            | Hyperlink Power Management Receive Clock  | AC32        |
| HYP1_RXPMDAT    | I            | Hyperlink Power Management Receive Data   | AC37        |
| HYP1_TXFLCLK    | I            | Hyperlink Flow Management Transmit Clock  | AD36        |
| HYP1_TXFLDAT    | I            | Hyperlink Flow Management Transmit Data   | AJ32        |
| HYP1_TXPMCLK    | O            | Hyperlink Power Management Transmit Clock | AJ37        |
| HYP1_TXPMDAT    | O            | Hyperlink Power Management Transmit Data  | AK34        |

### 6.3.19 PCIE

#### 6.3.19.1 MAIN Domain

表 6-88. PCIE Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                   | ALY PIN [4] |
|-----------------|--------------|---------------------------------------------------|-------------|
| PCIE0_CLKREQn   | IO           | PCIE Clock Request Signal                         | AC34        |
| PCIE1_CLKREQn   | IO           | PCIE Clock Request Signal                         | AC38, AR38  |
| PCIE2_CLKREQn   | IO           | PCIE Clock Request Signal                         | AB38, AL33  |
| PCIE3_CLKREQn   | IO           | PCIE Clock Request Signal                         | AB36, AL34  |
| PCIE0_RXN0      | I            | SERDES_PCIE Differential Receive Data (negative)  | AU5         |
| PCIE0_RXN1      | I            | SERDES_PCIE Differential Receive Data (negative)  | AT4         |
| PCIE0_RXN2      | I            | SERDES_PCIE Differential Receive Data (negative)  | AU2         |
| PCIE0_RXN3      | I            | SERDES_PCIE Differential Receive Data (negative)  | AT1         |
| PCIE0_RXP0      | I            | SERDES_PCIE Differential Receive Data (positive)  | AU6         |
| PCIE0_RXP1      | I            | SERDES_PCIE Differential Receive Data (positive)  | AT5         |
| PCIE0_RXP2      | I            | SERDES_PCIE Differential Receive Data (positive)  | AU3         |
| PCIE0_RXP3      | I            | SERDES_PCIE Differential Receive Data (positive)  | AT2         |
| PCIE0_TXN0      | O            | SERDES_PCIE Differential Transmit Data (negative) | AV6         |
| PCIE0_TXN1      | O            | SERDES_PCIE Differential Transmit Data (negative) | AR5         |
| PCIE0_TXN2      | O            | SERDES_PCIE Differential Transmit Data (negative) | AR2         |
| PCIE0_TXN3      | O            | SERDES_PCIE Differential Transmit Data (positive) | AP1         |
| PCIE0_TXP0      | O            | SERDES_PCIE Differential Transmit Data (positive) | AV7         |
| PCIE0_TXP1      | O            | SERDES_PCIE Differential Transmit Data (positive) | AR6         |
| PCIE0_TXP2      | O            | SERDES_PCIE Differential Transmit Data (positive) | AR3         |
| PCIE0_TXP3      | O            | SERDES_PCIE Differential Transmit Data (positive) | AP2         |
| PCIE1_RXN0      | I            | SERDES_PCIE Differential Receive Data (negative)  | AR8         |
| PCIE1_RXN1      | I            | SERDES_PCIE Differential Receive Data (negative)  | AT10        |
| PCIE1_RXN2      | I            | SERDES_PCIE Differential Receive Data (negative)  | AR11        |
| PCIE1_RXN3      | I            | SERDES_PCIE Differential Receive Data (negative)  | AU11        |
| PCIE1_RXP0      | I            | SERDES_PCIE Differential Receive Data (positive)  | AR9         |
| PCIE1_RXP1      | I            | SERDES_PCIE Differential Receive Data (positive)  | AT11        |
| PCIE1_RXP2      | I            | SERDES_PCIE Differential Receive Data (positive)  | AR12        |
| PCIE1_RXP3      | I            | SERDES_PCIE Differential Receive Data (positive)  | AU12        |

**表 6-88. PCIe Signal Descriptions (continued)**

| SIGNAL NAME [1]    | PIN TYPE [2] | DESCRIPTION [3]                                   | ALY PIN [4] |
|--------------------|--------------|---------------------------------------------------|-------------|
| PCIE1_TXN0         | O            | SERDES_PCIE Differential Transmit Data (negative) | AT7         |
| PCIE1_TXN1         | O            | SERDES_PCIE Differential Transmit Data (negative) | AP10        |
| PCIE1_TXN2         | O            | SERDES_PCIE Differential Transmit Data (negative) | AV9         |
| PCIE1_TXN3         | O            | SERDES_PCIE Differential Transmit Data (negative) | AV12        |
| PCIE1_TXP0         | O            | SERDES_PCIE Differential Transmit Data (positive) | AT8         |
| PCIE1_TXP1         | O            | SERDES_PCIE Differential Transmit Data (positive) | AP11        |
| PCIE1_TXP2         | O            | SERDES_PCIE Differential Transmit Data (positive) | AV10        |
| PCIE1_TXP3         | O            | SERDES_PCIE Differential Transmit Data (positive) | AV13        |
| PCIE2_RXN0         | I            | SERDES_PCIE Differential Receive Data (negative)  | AU2         |
| PCIE2_RXN1         | I            | SERDES_PCIE Differential Receive Data (negative)  | AT1         |
| PCIE2_RXP0         | I            | SERDES_PCIE Differential Receive Data (positive)  | AU3         |
| PCIE2_RXP1         | I            | SERDES_PCIE Differential Receive Data (positive)  | AT2         |
| PCIE2_TXN0         | O            | SERDES_PCIE Differential Transmit Data (negative) | AR2         |
| PCIE2_TXN1         | O            | SERDES_PCIE Differential Transmit Data (negative) | AP1         |
| PCIE2_TXP0         | O            | SERDES_PCIE Differential Transmit Data (negative) | AR3         |
| PCIE2_TXP1         | O            | SERDES_PCIE Differential Transmit Data (positive) | AP2         |
| PCIE3_RXN0         | I            | SERDES_PCIE Differential Receive Data (negative)  | AR11        |
| PCIE3_RXN1         | I            | SERDES_PCIE Differential Receive Data (negative)  | AU11        |
| PCIE3_RXP0         | I            | SERDES_PCIE Differential Receive Data (positive)  | AR12        |
| PCIE3_RXP1         | I            | SERDES_PCIE Differential Receive Data (positive)  | AU12        |
| PCIE3_TXN0         | O            | SERDES_PCIE Differential Transmit Data (negative) | AV9         |
| PCIE3_TXN1         | O            | SERDES_PCIE Differential Transmit Data (negative) | AV12        |
| PCIE3_TXP0         | O            | SERDES_PCIE Differential Transmit Data (positive) | AV10        |
| PCIE3_TXP1         | O            | SERDES_PCIE Differential Transmit Data (positive) | AV13        |
| PCIE_REFCLK0_N_OUT | O            | SERDES_PCIE Reference Clock Negative              | AP4         |
| PCIE_REFCLK0_P_OUT | O            | SERDES_PCIE Reference Clock Positive              | AP5         |
| PCIE_REFCLK1_N_OUT | O            | SERDES_PCIE Reference Clock Out Negative          | AN8         |
| PCIE_REFCLK1_P_OUT | O            | SERDES_PCIE Reference Clock Out Positive          | AN9         |
| PCIE_REFCLK2_N_OUT | O            | SERDES_PCIE Reference Clock Out Negative          | AN5         |
| PCIE_REFCLK2_P_OUT | O            | SERDES_PCIE Reference Clock Out Positive          | AN6         |
| PCIE_REFCLK3_N_OUT | O            | SERDES_PCIE Reference Clock Out Negative          | AP7         |
| PCIE_REFCLK3_P_OUT | O            | SERDES_PCIE Reference Clock Out Positive          | AP8         |

## 6.3.20 SERDES

### 6.3.20.1 MAIN Domain

**表 6-89. SERDES0 Signal Descriptions**

| SIGNAL NAME [1]             | PIN TYPE [2] | DESCRIPTION [3]                                | ALY PIN [4] |
|-----------------------------|--------------|------------------------------------------------|-------------|
| SERDES0_REFCLK_N            | IO           | Serdes Reference Clock Input/Output (negative) | AU9         |
| SERDES0_REFCLK_P            | IO           | Serdes Reference Clock Input/Output (positive) | AU8         |
| SERDES0_REXT <sup>(1)</sup> | I            | External Calibration Resistor                  | AN11        |

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

**表 6-90. SERDES1 Signal Descriptions**

| SIGNAL NAME [1]  | PIN TYPE [2] | DESCRIPTION [3]                                | ALY PIN [4] |
|------------------|--------------|------------------------------------------------|-------------|
| SERDES1_REFCLK_N | IO           | Serdes Reference Clock Input/Output (negative) | AV3         |

表 6-90. SERDES1 Signal Descriptions (continued)

| SIGNAL NAME [1]             | PIN TYPE [2] | DESCRIPTION [3]                                | ALY PIN [4] |
|-----------------------------|--------------|------------------------------------------------|-------------|
| SERDES1_REFCLK_P            | IO           | Serdes Reference Clock Input/Output (positive) | AV4         |
| SERDES1_REXT <sup>(1)</sup> | I            | External Calibration Resistor                  | AL9         |

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

表 6-91. SERDES2 Signal Descriptions

| SIGNAL NAME [1] <sup>(2)</sup> | PIN TYPE [2] | DESCRIPTION [3]                                | ALY PIN [4] |
|--------------------------------|--------------|------------------------------------------------|-------------|
| SERDES2_REFCLK_N               | IO           | Serdes Reference Clock Input/Output (negative) | AV21        |
| SERDES2_REFCLK_P               | IO           | Serdes Reference Clock Input/Output (positive) | AV22        |
| SERDES2_REXT <sup>(1)</sup>    | IO           | External Calibration Resistor                  | AL20        |

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

(2) DDRSS2, DDRSS3, and SERDES2 are not available on the 27mm package variant of this SoC. DDRSS2/DDRSS3/SERDES2 should be avoided if software compatibility is desired with systems that use the 27mm package.

表 6-92. SERDES4 Signal Descriptions

| SIGNAL NAME [1]             | PIN TYPE [2] | DESCRIPTION [3]                                | ALY PIN [4] |
|-----------------------------|--------------|------------------------------------------------|-------------|
| SERDES4_REFCLK_N            | IO           | Serdes Reference Clock Input/Output (negative) | AV16        |
| SERDES4_REFCLK_P            | IO           | Serdes Reference Clock Input/Output (positive) | AV15        |
| SERDES4_REXT <sup>(1)</sup> | IO           | External Calibration Resistor                  | AM19        |

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

### 6.3.21 DSI

#### 6.3.21.1 MAIN Domain

表 6-93. DSI0 Signal Descriptions

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                                   | ALY PIN [4] |
|------------------------------|--------------|---------------------------------------------------|-------------|
| CSI0_TXCLKN                  | O            | CSI Differential Transmit Clock Output (negative) | AP26        |
| CSI0_TXCLKP                  | O            | CSI Differential Transmit Clock Output (positive) | AP25        |
| CSI0_TXN0                    | O            | CSI Differential Transmit Output (negative)       | AU27        |
| CSI0_TXN1                    | O            | CSI Differential Transmit Output (negative)       | AT26        |
| CSI0_TXN2                    | O            | CSI Differential Transmit Output (negative)       | AR27        |
| CSI0_TXN3                    | O            | CSI Differential Transmit Output (negative)       | AN24        |
| CSI0_TXP0                    | O            | CSI Differential Transmit Output (positive)       | AU26        |
| CSI0_TXP1                    | O            | CSI Differential Transmit Output (positive)       | AT25        |
| CSI0_TXP2                    | O            | CSI Differential Transmit Output (positive)       | AR26        |
| CSI0_TXP3                    | O            | CSI Differential Transmit Output (positive)       | AN23        |
| DSI0_TXCLKN                  | O            | DSI Transmit clock (negative)                     | AP26        |
| DSI0_TXCLKP                  | O            | DSI Transmit clock (positive)                     | AP25        |
| DSI0_TXRCALIB <sup>(1)</sup> | A            | DSI Transmit Calibration Resistor                 | AM24        |
| DSI0_TXN0                    | IO           | DSI Transmit (negative)                           | AU27        |
| DSI0_TXN1                    | O            | DSI Transmit (negative)                           | AT26        |
| DSI0_TXN2                    | O            | DSI Transmit (negative)                           | AR27        |
| DSI0_TXN3                    | O            | DSI Transmit (negative)                           | AN24        |
| DSI0_TXP0                    | IO           | DSI Transmit (positive)                           | AU26        |
| DSI0_TXP1                    | O            | DSI Transmit (positive)                           | AT25        |
| DSI0_TXP2                    | O            | DSI Transmit (positive)                           | AR26        |

**表 6-93. DSI0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]         | ALY PIN [4] |
|-----------------|--------------|-------------------------|-------------|
| DSI0_TXP3       | O            | DSI Transmit (positive) | AN23        |

(1) An external 500  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS, even when the pin is unused.

**表 6-94. DSI1 Signal Descriptions**

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                                   | ALY PIN [4] |
|------------------------------|--------------|---------------------------------------------------|-------------|
| CSI1_TXCLKN                  | O            | CSI Differential Transmit Clock Output (negative) | AP29        |
| CSI1_TXCLKP                  | O            | CSI Differential Transmit Clock Output (positive) | AP28        |
| CSI1_TXN0                    | O            | CSI Differential Transmit Output (negative)       | AT29        |
| CSI1_TXN1                    | O            | CSI Differential Transmit Output (negative)       | AN27        |
| CSI1_TXN2                    | O            | CSI Differential Transmit Output (negative)       | AV28        |
| CSI1_TXN3                    | O            | CSI Differential Transmit Output (negative)       | AU30        |
| CSI1_TXP0                    | O            | CSI Differential Transmit Output (positive)       | AT28        |
| CSI1_TXP1                    | O            | CSI Differential Transmit Output (positive)       | AN26        |
| CSI1_TXP2                    | O            | CSI Differential Transmit Output (positive)       | AV27        |
| CSI1_TXP3                    | O            | CSI Differential Transmit Output (positive)       | AU29        |
| DSI1_TXCLKN                  | O            | DSI Transmit clock (negative)                     | AP29        |
| DSI1_TXCLKP                  | O            | DSI Transmit clock (positive)                     | AP28        |
| DSI1_TXRCALIB <sup>(1)</sup> | A            | DSI Transmit Calibration Resistor                 | AL22        |
| DSI1_TXN0                    | IO           | DSI Transmit (negative)                           | AT29        |
| DSI1_TXN1                    | O            | DSI Transmit (negative)                           | AN27        |
| DSI1_TXN2                    | O            | DSI Transmit (negative)                           | AV28        |
| DSI1_TXN3                    | O            | DSI Transmit (negative)                           | AU30        |
| DSI1_TXP0                    | IO           | DSI Transmit (positive)                           | AT28        |
| DSI1_TXP1                    | O            | DSI Transmit (positive)                           | AN26        |
| DSI1_TXP2                    | O            | DSI Transmit (positive)                           | AV27        |
| DSI1_TXP3                    | O            | DSI Transmit (positive)                           | AU29        |

(1) An external 500  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS, even when the pin is unused.

## 6.3.22 CSI

### 6.3.22.1 MAIN Domain

**表 6-95. CSI0 Signal Descriptions**

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                                                         | ALY PIN [4] |
|------------------------------|--------------|-------------------------------------------------------------------------|-------------|
| CSI0_RXCLKN                  | I            | CSI Differential Receive Clock Input (negative)                         | AN30        |
| CSI0_RXCLKP                  | I            | CSI Differential Receive Clock Input (positive)                         | AN29        |
| CSI0_RXRCALIB <sup>(1)</sup> | A            | CSI Pin connected to external resistor for on-chip resistor calibration | AM28        |
| CSI0_RXN0                    | I            | CSI Differential Receive Input (negative)                               | AU33        |
| CSI0_RXN1                    | I            | CSI Differential Receive Input (negative)                               | AT32        |
| CSI0_RXN2                    | I            | CSI Differential Receive Input (negative)                               | AV31        |
| CSI0_RXN3                    | I            | CSI Differential Receive Input (negative)                               | AR30        |
| CSI0_RXP0                    | I            | CSI Differential Receive Input (positive)                               | AU32        |
| CSI0_RXP1                    | I            | CSI Differential Receive Input (positive)                               | AT31        |
| CSI0_RXP2                    | I            | CSI Differential Receive Input (positive)                               | AV30        |
| CSI0_RXP3                    | I            | CSI Differential Receive Input (positive)                               | AR29        |

(1) An external 500  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS, even when the pin is unused.

表 6-96. CSI1 Signal Descriptions

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                                                         | ALY PIN [4] |
|------------------------------|--------------|-------------------------------------------------------------------------|-------------|
| CSI1_RXCLKN                  | I            | CSI Differential Receive Clock Input (negative)                         | AP32        |
| CSI1_RXCLKP                  | I            | CSI Differential Receive Clock Input (positive)                         | AP31        |
| CSI1_RXRCALIB <sup>(1)</sup> | A            | CSI pin connected to external resistor for on-chip resistor calibration | AL28        |
| CSI1_RXN0                    | I            | CSI Differential Receive Input (negative)                               | AT35        |
| CSI1_RXN1                    | I            | CSI Differential Receive Input (negative)                               | AU36        |
| CSI1_RXN2                    | I            | CSI Differential Receive Input (negative)                               | AR33        |
| CSI1_RXN3                    | I            | CSI Differential Receive Input (negative)                               | AV34        |
| CSI1_RXP0                    | I            | CSI Differential Receive Input (positive)                               | AT34        |
| CSI1_RXP1                    | I            | CSI Differential Receive Input (positive)                               | AU35        |
| CSI1_RXP2                    | I            | CSI Differential Receive Input (positive)                               | AR32        |
| CSI1_RXP3                    | I            | CSI Differential Receive Input (positive)                               | AV33        |

(1) An external 500  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS, even when the pin is unused.

表 6-97. CSI2 Signal Descriptions

| SIGNAL NAME [1]              | PIN TYPE [2] | DESCRIPTION [3]                                                         | ALY PIN [4] |
|------------------------------|--------------|-------------------------------------------------------------------------|-------------|
| CSI2_RXCLKN                  | I            | CSI Differential Receive Clock Input (negative)                         | AN32        |
| CSI2_RXCLKP                  | I            | CSI Differential Receive Clock Input (positive)                         | AN33        |
| CSI2_RXRCALIB <sup>(1)</sup> | A            | CSI Pin connected to external resistor for on-chip resistor calibration | AM31        |
| CSI2_RXN0                    | I            | CSI Differential Receive Input (negative)                               | AR36        |
| CSI2_RXN1                    | I            | CSI Differential Receive Input (negative)                               | AT38        |
| CSI2_RXN2                    | I            | CSI Differential Receive Input (negative)                               | AP35        |
| CSI2_RXN3                    | I            | CSI Differential Receive Input (negative)                               | AV37        |
| CSI2_RXP0                    | I            | CSI Differential Receive Input (positive)                               | AR35        |
| CSI2_RXP1                    | I            | CSI Differential Receive Input (positive)                               | AT37        |
| CSI2_RXP2                    | I            | CSI Differential Receive Input (positive)                               | AP34        |
| CSI2_RXP3                    | I            | CSI Differential Receive Input (positive)                               | AV36        |

(1) An external 500  $\Omega$   $\pm$ 1% resistor must be connected between this pin and VSS, even when the pin is unused.

### 6.3.23 MCASP

#### 6.3.23.1 MAIN Domain

表 6-98. MCASP0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALY PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| MCASP0_ACLKR    | IO           | MCASP Receive Bit Clock          | AF34        |
| MCASP0_ACLKX    | IO           | MCASP Transmit Bit Clock         | AK35        |
| MCASP0_AFSR     | IO           | MCASP Receive Frame Sync         | AE34        |
| MCASP0_AFSX     | IO           | MCASP Transmit Frame Sync        | AK38        |
| MCASP0_AXR0     | IO           | MCASP Serial Data (Input/Output) | AF37        |
| MCASP0_AXR1     | IO           | MCASP Serial Data (Input/Output) | AG37        |
| MCASP0_AXR2     | IO           | MCASP Serial Data (Input/Output) | AK33        |
| MCASP0_AXR3     | IO           | MCASP Serial Data (Input/Output) | AJ38        |
| MCASP0_AXR4     | IO           | MCASP Serial Data (Input/Output) | AK34        |
| MCASP0_AXR5     | IO           | MCASP Serial Data (Input/Output) | AG38        |
| MCASP0_AXR6     | IO           | MCASP Serial Data (Input/Output) | AF36        |
| MCASP0_AXR7     | IO           | MCASP Serial Data (Input/Output) | AE35        |

**表 6-98. MCASP0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALY PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| MCASP0_AXR8     | IO           | MCASP Serial Data (Input/Output) | AC35        |
| MCASP0_AXR9     | IO           | MCASP Serial Data (Input/Output) | AG35        |
| MCASP0_AXR10    | IO           | MCASP Serial Data (Input/Output) | AH36        |
| MCASP0_AXR11    | IO           | MCASP Serial Data (Input/Output) | AF35        |
| MCASP0_AXR12    | IO           | MCASP Serial Data (Input/Output) | AD34        |
| MCASP0_AXR13    | IO           | MCASP Serial Data (Input/Output) | AJ36        |
| MCASP0_AXR14    | IO           | MCASP Serial Data (Input/Output) | AF34        |
| MCASP0_AXR15    | IO           | MCASP Serial Data (Input/Output) | AE34        |

**表 6-99. MCASP1 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALY PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| MCASP1_ACLKR    | IO           | MCASP Receive Bit Clock          | AG38        |
| MCASP1_ACLKX    | IO           | MCASP Transmit Bit Clock         | AC34        |
| MCASP1_AFSR     | IO           | MCASP Receive Frame Sync         | AF36        |
| MCASP1_AFSX     | IO           | MCASP Transmit Frame Sync        | AD33        |
| MCASP1_AXR0     | IO           | MCASP Serial Data (Input/Output) | AD38        |
| MCASP1_AXR1     | IO           | MCASP Serial Data (Input/Output) | AC32        |
| MCASP1_AXR2     | IO           | MCASP Serial Data (Input/Output) | AC37        |
| MCASP1_AXR3     | IO           | MCASP Serial Data (Input/Output) | AL33        |
| MCASP1_AXR4     | IO           | MCASP Serial Data (Input/Output) | AL34        |

**表 6-100. MCASP2 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALY PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| MCASP2_ACLKR    | IO           | MCASP Receive Bit Clock          | AD34        |
| MCASP2_ACLKX    | IO           | MCASP Transmit Bit Clock         | AD37        |
| MCASP2_AFSR     | IO           | MCASP Receive Frame Sync         | AJ36        |
| MCASP2_AFSX     | IO           | MCASP Transmit Frame Sync        | AE37        |
| MCASP2_AXR0     | IO           | MCASP Serial Data (Input/Output) | AC36        |
| MCASP2_AXR1     | IO           | MCASP Serial Data (Input/Output) | AE36        |
| MCASP2_AXR2     | IO           | MCASP Serial Data (Input/Output) | AF38        |
| MCASP2_AXR3     | IO           | MCASP Serial Data (Input/Output) | AC33        |
| MCASP2_AXR4     | IO           | MCASP Serial Data (Input/Output) | AF34        |

**表 6-101. MCASP3 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALY PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| MCASP3_ACLKR    | IO           | MCASP Receive Bit Clock          | AM37        |
| MCASP3_ACLKX    | IO           | MCASP Transmit Bit Clock         | AM37        |
| MCASP3_AFSR     | IO           | MCASP Receive Frame Sync         | AP38        |
| MCASP3_AFSX     | IO           | MCASP Transmit Frame Sync        | AP38        |
| MCASP3_AXR0     | IO           | MCASP Serial Data (Input/Output) | AN38        |
| MCASP3_AXR1     | IO           | MCASP Serial Data (Input/Output) | AM35        |
| MCASP3_AXR2     | IO           | MCASP Serial Data (Input/Output) | AM36        |

表 6-102. MCASP4 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                   | ALY PIN [4] |
|-----------------|--------------|-----------------------------------|-------------|
| MCASP4_ACLKR    | IO           | MCASP Receive Bit Clock           | AE35        |
| MCASP4_ACLKX    | IO           | MCASP Transmit Bit Clock          | AJ32        |
| MCASP4_AFSR     | IO           | MCASP Receive Frame Sync          | AC35        |
| MCASP4_AFSX     | IO           | MCASP Transmit Frame Sync         | AJ37        |
| MCASP4_AXR0     | IO           | MCASP Serial Data (Input/Output)  | AJ34        |
| MCASP4_AXR1     | IO           | MCASP Serial Data (Input/Output)  | AE38        |
| MCASP4_AXR2     | IO           | MCASP Serial Data (Input/Output)  | AD36        |
| MCASP4_AXR3     | IO           | MCASP Serial Data (Input/Output)  | AH38        |
| MCASP4_AXR4     | IO           | MCASPI Serial Data (Input/Output) | AG35        |

## 6.3.24 DMTIMER

## 6.3.24.1 MAIN Domain

表 6-103. DMTIMER Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                            | ALY PIN [4] |
|-----------------|--------------|----------------------------------------------------------------------------|-------------|
| TIMER_IO0       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | AR38        |
| TIMER_IO1       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | AN37        |
| TIMER_IO2       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | AC38        |
| TIMER_IO3       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | AA32        |
| TIMER_IO4       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | AB34        |
| TIMER_IO5       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | AA33        |
| TIMER_IO6       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | AB38        |
| TIMER_IO7       | IO           | Timer Inputs and Outputs (Can be used with any MAIN domain timer instance) | AB36        |

## 6.3.24.2 MCU Domain

表 6-104. MCU\_DMTIMER Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                            | ALY PIN [4] |
|-----------------|--------------|----------------------------------------------------------------------------|-------------|
| MCU_TIMER_IO0   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | G33, J38    |
| MCU_TIMER_IO1   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | F37, M38    |
| MCU_TIMER_IO2   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | E38         |
| MCU_TIMER_IO3   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | E37         |
| MCU_TIMER_IO4   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | D36         |
| MCU_TIMER_IO5   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | C36         |
| MCU_TIMER_IO6   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | L35, M37    |
| MCU_TIMER_IO7   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | L34, M36    |



**表 6-104. MCU\_DMTIMER Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                            | ALY PIN [4] |
|-----------------|--------------|----------------------------------------------------------------------------|-------------|
| MCU_TIMER_IO8   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | H37         |
| MCU_TIMER_IO9   | IO           | Timer Inputs and Outputs (Can be used with any MCU domain timer instance.) | K37         |

### 6.3.25 CPTS

#### 6.3.25.1 MAIN Domain

**表 6-105. CPTS0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                 | ALY PIN [4] |
|-----------------|--------------|---------------------------------|-------------|
| CPTS0_RFT_CLK   | I            | CPTS Reference Clock            | AD36        |
| CPTS0_TS_COMP   | O            | CPTS Time Stamp Counter Compare | AP38        |
| CPTS0_TS_SYNC   | O            | CPTS Time Stamp Counter Bit     | AA32        |
| CPTS0_HW1TSPUSH | I            | CPTS Hardware Time Stamp Push 1 | AD36        |
| CPTS0_HW2TSPUSH | I            | CPTS Hardware Time Stamp Push 2 | AJ32        |

#### 6.3.25.2 MCU Domain

**表 6-106. MCU\_CPTS0 Signal Descriptions**

| SIGNAL NAME [1]     | PIN TYPE [2] | DESCRIPTION [3]                 | ALY PIN [4] |
|---------------------|--------------|---------------------------------|-------------|
| MCU_CPTS0_RFT_CLK   | I            | CPTS Reference Clock            | L33, M33    |
| MCU_CPTS0_TS_COMP   | O            | CPTS Time Stamp Counter Compare | L34         |
| MCU_CPTS0_TS_SYNC   | O            | CPTS Time Stamp Counter Bit     | L35         |
| MCU_CPTS0_HW1TSPUSH | I            | CPTS Hardware Time Stamp Push 1 | L37         |
| MCU_CPTS0_HW2TSPUSH | I            | CPTS Hardware Time Stamp Push 2 | L36         |

### 6.3.26 DSS

#### 6.3.26.1 MAIN Domain

**表 6-107. DSS0 Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                         | ALY PIN [4] |
|-----------------|--------------|-----------------------------------------|-------------|
| DSS_FSYNC0      | O            | Video Output Frame Sync                 | AG36, AJ37  |
| DSS_FSYNC1      | O            | Video Output Frame Sync                 | AJ33, AJ34  |
| DSS_FSYNC2      | O            | Video Output Frame Sync                 | AF33, AF35  |
| DSS_FSYNC3      | O            | Video Output Frame Sync                 | AD34, AH33  |
| VOUT0_DE        | O            | Video Output Data Enable                | AG38        |
| VOUT0_EXTCLKIN  | I            | Video Output External Pixel Clock Input | AJ37        |
| VOUT0_HSYNC     | O            | Video Output Horizontal Sync            | AK34        |
| VOUT0_PCLK      | O            | Video Output Pixel Clock Output         | AH37        |
| VOUT0_VSYNC     | O            | Video Output Vertical Sync              | AF36        |
| VOUT0_DATA0     | O            | Video Output Data 0                     | AC33        |
| VOUT0_DATA1     | O            | Video Output Data 1                     | AH38        |
| VOUT0_DATA2     | O            | Video Output Data 2                     | AJ38        |
| VOUT0_DATA3     | O            | Video Output Data 3                     | AE38        |
| VOUT0_DATA4     | O            | Video Output Data 4                     | AF38        |
| VOUT0_DATA5     | O            | Video Output Data 5                     | AE36        |
| VOUT0_DATA6     | O            | Video Output Data 6                     | AC36        |
| VOUT0_DATA7     | O            | Video Output Data 7                     | AE37        |



表 6-107. DSS0 Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                    | ALY PIN [4] |
|-----------------|--------------|------------------------------------|-------------|
| VOUT0_DATA8     | O            | Video Output Data 8                | AD37        |
| VOUT0_DATA9     | O            | Video Output Data 9                | AC37        |
| VOUT0_DATA10    | O            | Video Output Data 10               | AC32        |
| VOUT0_DATA11    | O            | Video Output Data 11               | AK33        |
| VOUT0_DATA12    | O            | Video Output Data 12               | AG37        |
| VOUT0_DATA13    | O            | Video Output Data 13               | AF37        |
| VOUT0_DATA14    | O            | Video Output Data 14               | AK38        |
| VOUT0_DATA15    | O            | Video Output Data 15               | AK35        |
| VOUT0_DATA16    | O            | Video Output Data 16               | AJ32        |
| VOUT0_DATA17    | O            | Video Output Data 17               | AK37        |
| VOUT0_DATA18    | O            | Video Output Data 18               | AC33, AL32  |
| VOUT0_DATA19    | O            | Video Output Data 19               | AE33, AH38  |
| VOUT0_DATA20    | O            | Video Output Data 20               | AD37, AH34  |
| VOUT0_DATA21    | O            | Video Output Data 21               | AC37, AJ35  |
| VOUT0_DATA22    | O            | Video Output Data 22               | AG34, AK37  |
| VOUT0_DATA23    | O            | Video Output Data 23               | AD36, AK36  |
| VOUT0_VP0_DE    | O            | Alternative Output Data Enable     | AG38        |
| VOUT0_VP0_HSYNC | O            | Alternative Output Horizontal Sync | AK34        |
| VOUT0_VP0_VSYNC | O            | Alternative Output Vertical Sync   | AF36        |
| VOUT0_VP2_DE    | O            | Alternative Output Data Enable     | AG38        |
| VOUT0_VP2_HSYNC | O            | Alternative Output Horizontal Sync | AK34        |
| VOUT0_VP2_VSYNC | O            | Alternative Output Vertical Sync   | AF36        |

### 6.3.27 GPMC

#### 6.3.27.1 MAIN Domain

表 6-108. GPMC0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                             | ALY PIN [4] |
|-----------------|--------------|---------------------------------------------------------------------------------------------|-------------|
| GPMC0_ADVn_ALE  | O            | GPMC Address Valid (active low) or Address Latch Enable                                     | AK33        |
| GPMC0_CLK       | IO           | GPMC clock                                                                                  | AG36        |
| GPMC0_CLKOUT    | O            | GPMC clock generated for external synchronization                                           | AF36        |
| GPMC0_DIR       | O            | GPMC Data Bus Signal Direction Control                                                      | AC33, AH37  |
| GPMC0_OEn_REn   | O            | GPMC Output Enable (active low) or Read Enable (active low)                                 | AK34        |
| GPMC0_WEn       | O            | GPMC Write Enable (active low)                                                              | AJ34        |
| GPMC0_WPn       | O            | GPMC Flash Write Protect (active low)                                                       | AK33        |
| GPMC0_A0        | OZ           | GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories | AE35        |
| GPMC0_A1        | OZ           | GPMC Address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode    | AC35        |
| GPMC0_A2        | OZ           | GPMC Address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode    | AG35        |
| GPMC0_A3        | OZ           | GPMC Address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode    | AH36        |
| GPMC0_A4        | OZ           | GPMC Address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode    | AF35        |

**表 6-108. GPMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                | ALY PIN [4] |
|-----------------|--------------|----------------------------------------------------------------------------------------------------------------|-------------|
| GPMC0_A5        | OZ           | GPMC Address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode                       | AD34        |
| GPMC0_A6        | OZ           | GPMC Address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode                       | AJ36        |
| GPMC0_A7        | OZ           | GPMC Address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode                       | AF34        |
| GPMC0_A8        | OZ           | GPMC Address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode                       | AE34        |
| GPMC0_A9        | OZ           | GPMC Address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode                       | AL33        |
| GPMC0_A10       | OZ           | GPMC Address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode                      | AL34        |
| GPMC0_A11       | OZ           | GPMC Address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AC34        |
| GPMC0_A12       | OZ           | GPMC Address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AD33        |
| GPMC0_A13       | OZ           | GPMC Address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AD38        |
| GPMC0_A14       | OZ           | GPMC Address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AE35, AL32  |
| GPMC0_A15       | OZ           | GPMC Address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AE33        |
| GPMC0_A16       | OZ           | GPMC Address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AH34        |
| GPMC0_A17       | OZ           | GPMC Address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AJ35        |
| GPMC0_A18       | OZ           | GPMC Address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AG34        |
| GPMC0_A19       | OZ           | GPMC Address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AK36        |
| GPMC0_A20       | OZ           | GPMC Address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AG33        |
| GPMC0_A21       | OZ           | GPMC Address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AH33        |
| GPMC0_A22       | OZ           | GPMC Address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AF33        |
| GPMC0_A23       | OZ           | GPMC Address 23 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AJ33        |
| GPMC0_A24       | OZ           | GPMC Address 24 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                          | AG36        |
| GPMC0_AD0       | IO           | GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode | AK35        |
| GPMC0_AD1       | IO           | GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode | AK38        |
| GPMC0_AD2       | IO           | GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode | AF37        |
| GPMC0_AD3       | IO           | GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode | AG37        |

表 6-108. GPMC0 Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                                                                                                  | ALY PIN [4] |
|-----------------|--------------|------------------------------------------------------------------------------------------------------------------|-------------|
| GPMC0_AD4       | IO           | GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode   | AK37        |
| GPMC0_AD5       | IO           | GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode   | AD36        |
| GPMC0_AD6       | IO           | GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode   | AJ32        |
| GPMC0_AD7       | IO           | GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode   | AJ37        |
| GPMC0_AD8       | IO           | GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode   | AC32        |
| GPMC0_AD9       | IO           | GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode  | AC37        |
| GPMC0_AD10      | IO           | GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode | AD37        |
| GPMC0_AD11      | IO           | GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode | AE37        |
| GPMC0_AD12      | IO           | GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode | AC36        |
| GPMC0_AD13      | IO           | GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode | AE36        |
| GPMC0_AD14      | IO           | GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode | AF38        |
| GPMC0_AD15      | IO           | GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode | AE38        |
| GPMC0_BE0n_CLE  | O            | GPMC Lower-Byte Enable (active low) or Command Latch Enable                                                      | AH38        |
| GPMC0_BE1n      | O            | GPMC Upper-Byte Enable (active low)                                                                              | AJ38        |
| GPMC0_CSn0      | O            | GPMC Chip Select 0 (active low)                                                                                  | AG38        |
| GPMC0_CSn1      | O            | GPMC Chip Select 1 (active low)                                                                                  | AH37        |
| GPMC0_CSn2      | O            | GPMC Chip Select 2 (active low)                                                                                  | AE35, AL32  |
| GPMC0_CSn3      | O            | GPMC Chip Select 3 (active low)                                                                                  | AJ33        |
| GPMC0_WAIT0     | I            | GPMC External Indication of Wait                                                                                 | AC33        |
| GPMC0_WAIT1     | I            | GPMC External Indication of Wait                                                                                 | AE33        |
| GPMC0_WAIT2     | I            | GPMC External Indication of Wait                                                                                 | AF33        |
| GPMC0_WAIT3     | I            | GPMC External Indication of Wait                                                                                 | AD38        |

### 6.3.28 MMC

#### 6.3.28.1 MAIN Domain

表 6-109. MMC0 Signal Descriptions

| SIGNAL NAME [1]            | PIN TYPE [2] | DESCRIPTION [3]                  | ALY PIN [4] |
|----------------------------|--------------|----------------------------------|-------------|
| MMC0_CALPAD <sup>(1)</sup> | A            | MMC/SD/SDIO Calibration Resistor | AJ7         |

**表 6-109. MMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]     | ALY PIN [4] |
|-----------------|--------------|---------------------|-------------|
| MMC0_CLK        | O            | MMC/SD/SDIO Clock   | AK5         |
| MMC0_CMD        | IO           | MMC/SD/SDIO Command | AL8         |
| MMC0_DS         | IO           | MMC Data Strobe     | AK4         |
| MMC0_DAT0       | IO           | MMC/SD/SDIO Data    | AK9         |
| MMC0_DAT1       | IO           | MMC/SD/SDIO Data    | AL6         |
| MMC0_DAT2       | IO           | MMC/SD/SDIO Data    | AK8         |
| MMC0_DAT3       | IO           | MMC/SD/SDIO Data    | AK6         |
| MMC0_DAT4       | IO           | MMC/SD/SDIO Data    | AK7         |
| MMC0_DAT5       | IO           | MMC/SD/SDIO Data    | AL7         |
| MMC0_DAT6       | IO           | MMC/SD/SDIO Data    | AL5         |
| MMC0_DAT7       | IO           | MMC/SD/SDIO Data    | AK3         |

(1) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

**表 6-110. MMC1 Signal Descriptions**

| SIGNAL NAME [1]          | PIN TYPE [2] | DESCRIPTION [3]     | ALY PIN [4] |
|--------------------------|--------------|---------------------|-------------|
| MMC1_CLK <sup>(2)</sup>  | IO           | MMC/SD/SDIO Clock   | AB38        |
| MMC1_CMD                 | IO           | MMC/SD/SDIO Command | AB36        |
| MMC1_SDCD <sup>(1)</sup> | I            | SD Card Detect      | AR38        |
| MMC1_SDWP                | I            | SD Write Protect    | AN37        |
| MMC1_DAT0                | IO           | MMC/SD/SDIO Data    | AA33        |
| MMC1_DAT1                | IO           | MMC/SD/SDIO Data    | AB34        |
| MMC1_DAT2                | IO           | MMC/SD/SDIO Data    | AA32        |
| MMC1_DAT3                | IO           | MMC/SD/SDIO Data    | AC38        |

- (1) For ROM boot from MMC1 interface to work properly, the MMC1\_SDCD pin should be pulled low externally with a resistor to indicate an SD Card/Memory device is present.
- (2) For MMC1\_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR\_PADCONFIG171 register should be set to 0x1 because of retiming purposes.

## 6.3.29 OSPI

### 6.3.29.1 MCU Domain

**表 6-111. MCU\_OSPI0 Signal Descriptions**

| SIGNAL NAME [1]    | PIN TYPE [2] | DESCRIPTION [3]                                | ALY PIN [4] |
|--------------------|--------------|------------------------------------------------|-------------|
| MCU_OSPI0_CLK      | O            | OSPI Clock                                     | E32         |
| MCU_OSPI0_DQS      | I            | OSPI Data Strobe (DQS) or Loopback Clock Input | C34         |
| MCU_OSPI0_ECC_FAIL | I            | OSPI ECC Status                                | C32, F31    |
| MCU_OSPI0_LBCLKO   | IO           | OSPI Loopback Clock Output                     | D32         |
| MCU_OSPI0_CSn0     | O            | OSPI Chip Select 0 (active low)                | A32         |
| MCU_OSPI0_CSn1     | O            | OSPI Chip Select 1 (active low)                | A33         |
| MCU_OSPI0_CSn2     | O            | OSPI Chip Select 2 (active low)                | B34, C31    |
| MCU_OSPI0_CSn3     | O            | OSPI Chip Select 3 (active low)                | C32, F31    |
| MCU_OSPI0_D0       | IO           | OSPI Data 0                                    | B33         |
| MCU_OSPI0_D1       | IO           | OSPI Data 1                                    | B32         |
| MCU_OSPI0_D2       | IO           | OSPI Data 2                                    | C33         |
| MCU_OSPI0_D3       | IO           | OSPI Data 3                                    | C35         |
| MCU_OSPI0_D4       | IO           | OSPI Data 4                                    | D33         |
| MCU_OSPI0_D5       | IO           | OSPI Data 5                                    | D34         |

表 6-111. MCU\_OSPI0 Signal Descriptions (continued)

| SIGNAL NAME [1]      | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|----------------------|--------------|-----------------|-------------|
| MCU_OSPI0_D6         | IO           | OSPI Data 6     | E34         |
| MCU_OSPI0_D7         | IO           | OSPI Data 7     | E33         |
| MCU_OSPI0_RESET_OUT0 | O            | OSPI Reset      | B34, C31    |
| MCU_OSPI0_RESET_OUT1 | O            | OSPI Reset      | C32, G33    |

表 6-112. MCU\_OSPI1 Signal Descriptions

| SIGNAL NAME [1]  | PIN TYPE [2] | DESCRIPTION [3]                                | ALY PIN [4] |
|------------------|--------------|------------------------------------------------|-------------|
| MCU_OSPI1_CLK    | O            | OSPI Clock                                     | F32         |
| MCU_OSPI1_DQS    | I            | OSPI Data Strobe (DQS) or Loopback Clock Input | F31         |
| MCU_OSPI1_LBCLKO | IO           | OSPI Loopback Clock Output                     | C31         |
| MCU_OSPI1_CSn0   | O            | OSPI Chip Select 0 (active low)                | G32         |
| MCU_OSPI1_CSn1   | O            | OSPI Chip Select 1 (active low)                | G33         |
| MCU_OSPI1_D0     | IO           | OSPI Data 0                                    | E35         |
| MCU_OSPI1_D1     | IO           | OSPI Data 1                                    | D31         |
| MCU_OSPI1_D2     | IO           | OSPI Data 2                                    | G31         |
| MCU_OSPI1_D3     | IO           | OSPI Data 3                                    | F33         |

### 6.3.30 Hyperbus

#### 6.3.30.1 MCU Domain

表 6-113. MCU\_HYPERBUS0 Signal Descriptions

| SIGNAL NAME [1]        | PIN TYPE [2] | DESCRIPTION [3]                                                   | ALY PIN [4]   |
|------------------------|--------------|-------------------------------------------------------------------|---------------|
| MCU_HYPERBUS0_CK       | O            | Hyperbus Differential Clock (positive)                            | E32           |
| MCU_HYPERBUS0_CKn      | O            | Hyperbus Differential Clock (negative)                            | D32           |
| MCU_HYPERBUS0_INTn     | I            | Hyperbus Interrupt (active low)                                   | C32, F31      |
| MCU_HYPERBUS0_RESETh   | O            | Hyperbus Reset (active low) Output                                | A33           |
| MCU_HYPERBUS0_RESEThOn | I            | Hyperbus Reset Status Indicator (active low) from Hyperbus Memory | B34, C31      |
| MCU_HYPERBUS0_RWDS     | IO           | Hyperbus Read-Write Data Strobe                                   | C34           |
| MCU_HYPERBUS0_WPn      | O            | Hyperbus Write Protect (Not in use)                               | B34, C32, G33 |
| MCU_HYPERBUS0_CSn0     | O            | Hyperbus Chip Select 0                                            | A32           |
| MCU_HYPERBUS0_CSn1     | O            | Hyperbus Chip Select 1                                            | B34, G33      |
| MCU_HYPERBUS0_DQ0      | IO           | Hyperbus Data 0                                                   | B33           |
| MCU_HYPERBUS0_DQ1      | IO           | Hyperbus Data 1                                                   | B32           |
| MCU_HYPERBUS0_DQ2      | IO           | Hyperbus Data 2                                                   | C33           |
| MCU_HYPERBUS0_DQ3      | IO           | Hyperbus Data 3                                                   | C35           |
| MCU_HYPERBUS0_DQ4      | IO           | Hyperbus Data 4                                                   | D33           |
| MCU_HYPERBUS0_DQ5      | IO           | Hyperbus Data 5                                                   | D34           |
| MCU_HYPERBUS0_DQ6      | IO           | Hyperbus Data 6                                                   | E34           |
| MCU_HYPERBUS0_DQ7      | IO           | Hyperbus Data 7                                                   | E33           |

### 6.3.31 Emulation and Debug

#### 6.3.31.1 MAIN Domain

表 6-114. JTAG Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]     | ALY PIN [4] |
|-----------------|--------------|---------------------|-------------|
| EMU0            | IO           | Emulation Control 0 | F35         |

**表 6-114. JTAG Signal Descriptions (continued)**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]             | ALY PIN [4] |
|-----------------|--------------|-----------------------------|-------------|
| EMU1            | IO           | Emulation Control 1         | H34         |
| TCK             | I            | JTAG Test Clock Input       | G35         |
| TDI             | I            | JTAG Test Data Input        | AL37        |
| TDO             | OZ           | JTAG Test Data Output       | AL35        |
| TMS             | I            | JTAG Test Mode Select Input | AL36        |
| TRSTn           | I            | JTAG Reset                  | G37         |

**表 6-115. Trace Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| TRC_CLK         | O            | Trace Clock     | AG36, AJ32  |
| TRC_CTL         | O            | Trace Control   | AJ33, AJ37  |
| TRC_DATA0       | O            | Trace Data 0    | AF33, AJ34  |
| TRC_DATA1       | O            | Trace Data 1    | AD36, AH33  |
| TRC_DATA2       | O            | Trace Data 2    | AG33, AK37  |
| TRC_DATA3       | O            | Trace Data 3    | AC33, AK36  |
| TRC_DATA4       | O            | Trace Data 4    | AD37        |
| TRC_DATA5       | O            | Trace Data 5    | AH38        |
| TRC_DATA6       | O            | Trace Data 6    | AC37        |
| TRC_DATA7       | O            | Trace Data 7    | AJ38        |
| TRC_DATA8       | O            | Trace Data 8    | AC32        |
| TRC_DATA9       | O            | Trace Data 9    | AE37        |
| TRC_DATA10      | O            | Trace Data 10   | AK33        |
| TRC_DATA11      | O            | Trace Data 11   | AF38        |
| TRC_DATA12      | O            | Trace Data 12   | AG37        |
| TRC_DATA13      | O            | Trace Data 13   | AE36        |
| TRC_DATA14      | O            | Trace Data 14   | AF37        |
| TRC_DATA15      | O            | Trace Data 15   | AC36        |
| TRC_DATA16      | O            | Trace Data 16   | AE38        |
| TRC_DATA17      | O            | Trace Data 17   | AH37        |
| TRC_DATA18      | O            | Trace Data 18   | AK34        |
| TRC_DATA19      | O            | Trace Data 19   | AG38        |
| TRC_DATA20      | O            | Trace Data 20   | AF36        |
| TRC_DATA21      | O            | Trace Data 21   | AG34        |
| TRC_DATA22      | O            | Trace Data 22   | AJ35        |
| TRC_DATA23      | O            | Trace Data 23   | AH34        |
| TRC_DATA24      | O            | Trace Data 24   | AE33        |
| TRC_DATA25      | O            | Trace Data 25   | AL32        |

## 6.3.32 System and Miscellaneous

### 6.3.32.1 Boot Mode configuration

**表 6-116. Sysboot Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4] |
|-----------------|--------------|-----------------|-------------|
| BOOTMODE00      | I            | Bootmode Pin 0  | B33         |
| BOOTMODE01      | I            | Bootmode Pin 1  | B32         |
| BOOTMODE02      | I            | Bootmode Pin 2  | D33         |

表 6-116. Sysboot Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]    | ALY PIN [4] |
|-----------------|--------------|--------------------|-------------|
| BOOTMODE03      | I            | Bootmode Pin 3     | D34         |
| BOOTMODE04      | I            | Bootmode Pin 4     | M37         |
| BOOTMODE05      | I            | Bootmode Pin 5     | M36         |
| BOOTMODE06      | I            | Bootmode Pin 6     | N34         |
| BOOTMODE07      | I            | Bootmode Pin 7     | M34         |
| MCU_BOOTMODE00  | I            | MCU Bootmode Pin 0 | G38         |
| MCU_BOOTMODE01  | I            | MCU Bootmode Pin 1 | H36         |
| MCU_BOOTMODE02  | I            | MCU Bootmode Pin 2 | J38         |
| MCU_BOOTMODE03  | I            | MCU Bootmode Pin 3 | H38         |
| MCU_BOOTMODE04  | I            | MCU Bootmode Pin 4 | J34         |
| MCU_BOOTMODE05  | I            | MCU Bootmode Pin 5 | J35         |
| MCU_BOOTMODE06  | I            | MCU Bootmode Pin 6 | H37         |
| MCU_BOOTMODE07  | I            | MCU Bootmode Pin 7 | K37         |
| MCU_BOOTMODE08  | I            | MCU Bootmode Pin 8 | J37         |
| MCU_BOOTMODE09  | I            | MCU Bootmode Pin 9 | K38         |

## 6.3.32.2 Clock

表 6-117. Clock0 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                             | ALY PIN [4] |
|-----------------|--------------|---------------------------------------------|-------------|
| WKUP_LF_CLKIN   | I            | Low Frequency (32.768 KHz) Oscillator Input | M34         |
| WKUP_OSC0_XI    | I            | High Frequency Oscillator Input             | T38         |
| WKUP_OSC0_XO    | O            | High Frequency Oscillator Output            | U37         |

表 6-118. Clock1 Signal Descriptions

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                  | ALY PIN [4] |
|-----------------|--------------|----------------------------------|-------------|
| OSC1_XI         | I            | High Frequency Oscillator Input  | P38         |
| OSC1_XO         | O            | High Frequency Oscillator Output | N37         |

## 6.3.32.3 System

表 6-119. MCU System Signal Descriptions

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                                 | ALY PIN [4] |
|-------------------|--------------|-----------------------------------------------------------------|-------------|
| MCU_CLKOUT0       | OZ           | Reference clock output for Ethernet PHYs (50MHz or 25MHz)       | M38         |
| MCU_EXT_REFCLK0   | I            | External system clock input                                     | L33, M33    |
| MCU_OBSCLK0       | O            | Observation clock output for test and debug purposes only       | H34, M38    |
| MCU_PORz          | I            | MCU Domain Cold Reset                                           | K32         |
| MCU_RESETSTATz    | O            | MCU Domain Warm Reset status output                             | F36         |
| MCU_RESETz        | I            | MCU Domain Warm Reset                                           | G36         |
| MCU_SAFETY_ERRORn | IO           | Error signal output from MCU Domain ESM                         | N36         |
| MCU_SYSCLKOUT0    | O            | MCU Domain system clock output for test and debug purposes only | L33         |



**表 6-120. System Signal Descriptions**

| SIGNAL NAME [1]   | PIN TYPE [2] | DESCRIPTION [3]                                                                                                                                                                    | ALY PIN [4] |
|-------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| AUDIO_EXT_REFCLK0 | IO           | External clock routed to ATL or McASP as one of the selectable input clock sources, or as a output clock output for ATL or McASP                                                   | AJ34        |
| AUDIO_EXT_REFCLK1 | IO           | External clock routed to ATL or McASP as one of the selectable input clock sources, or as a output clock output for ATL or McASP                                                   | AH37        |
| EXTINTn           | I            | External Interrupt                                                                                                                                                                 | AN35        |
| EXT_REFCLK1       | I            | External clock input to Main Domain, routed to Timer clock muxes as one of the selectable input clock sources for Timer/WDT modules, or as reference clock to MAIN_PLL2 (PER1 PLL) | AJ32        |
| GPMC0_FCLK_MUX    | O            | GPMC functional clock output selected through a mux logic                                                                                                                          | AF36        |
| OBSCLK0           | O            | Observation clock output for test and debug purposes only                                                                                                                          | AN37        |
| OBSCLK1           | O            | Observation clock output for test and debug purposes only                                                                                                                          | AG37        |
| PMIC_POWER_EN1    | O            | Power enable output for MAIN Domain supplies                                                                                                                                       | L38         |
| PMIC_WAKE0n       | O            | PMIC WakeUp                                                                                                                                                                        | AJ34        |
| PMIC_WAKE1n       | O            | PMIC WakeUp                                                                                                                                                                        | M33         |
| PORz              | I            | SoC PORz Reset Signal                                                                                                                                                              | P33         |
| RESETSTATz        | O            | Main Domain Warm Reset status output                                                                                                                                               | AL38        |
| RESET_REQz        | I            | Main Domain external Warm Reset request input                                                                                                                                      | F34         |
| SOC_SAFETY_ERRORn | IO           | Error signal output from Main Domain ESM                                                                                                                                           | AM34        |
| SYNC0_OUT         | O            | CPTS Time Stamp Generator Bit 0                                                                                                                                                    | AD36        |
| SYNC1_OUT         | O            | CPTS Time Stamp Generator Bit 1                                                                                                                                                    | AJ32        |
| SYNC2_OUT         | O            | CPTS Time Stamp Generator Bit 2                                                                                                                                                    | AD38        |
| SYNC3_OUT         | O            | CPTS Time Stamp Generator Bit 3                                                                                                                                                    | AD37        |
| SYSCLKOUT0        | O            | SYSCLK0 output from Main PLL controller (divided by 6) for test and debug purposes only                                                                                            | AR38        |

#### 6.3.32.4 EFUSE

**表 6-121. EFUSE Signal Descriptions**

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                            | ALY PIN [4] |
|-----------------|--------------|--------------------------------------------|-------------|
| VPP_CORE        |              | Programming Voltage for MAIN Domain Efuses | AA31        |
| VPP_MCU         |              | Programming Voltage for MCU Domain Efuses  | L29         |

#### 6.3.32.5 VMON

**表 6-122. VMON Signal Descriptions**

| SIGNAL NAME [1]  | PIN TYPE [2] | DESCRIPTION [3]                                                                                                                                             | ALY PIN [4] |
|------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| VMON1_ER_VSYS    |              | Voltage Monitor, fixed 0.45V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply. | K28         |
| VMON2_IR_VCPU    |              | Must be externally connected directly to VDD_CPU                                                                                                            | N27         |
| VMON3_IR_VEXT1P8 |              | General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor divider.                                                      | J30         |
| VMON4_IR_VEXT1P8 |              | General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor divider.                                                      | P28         |



表 6-122. VMON Signal Descriptions (continued)

| SIGNAL NAME [1]  | PIN TYPE [2] | DESCRIPTION [3]                                                                                        | ALY PIN [4] |
|------------------|--------------|--------------------------------------------------------------------------------------------------------|-------------|
| VMON5_IR_VEXT3P3 |              | General purpose voltage monitor for external supplies, 3.3V threshold. With internal resistor divider. | R29         |

## 6.3.33 Power

表 6-123. Power Supply Signal Descriptions

| SIGNAL NAME [1]               | PIN TYPE [2] | DESCRIPTION [3]               | ALY PIN [4]                                                          |
|-------------------------------|--------------|-------------------------------|----------------------------------------------------------------------|
| CAP_VDDSO <sup>(1)</sup>      | CAP          | External Capacitor Connection | V29                                                                  |
| CAP_VDDSO_MCU <sup>(1)</sup>  | CAP          | External Capacitor Connection | L27                                                                  |
| CAP_VDDSO1_MCU <sup>(1)</sup> | CAP          | External Capacitor Connection | L25                                                                  |
| CAP_VDDSO2 <sup>(1)</sup>     | CAP          | External Capacitor Connection | T29                                                                  |
| CAP_VDDSO2_MCU <sup>(1)</sup> | CAP          | External Capacitor Connection | L26                                                                  |
| CAP_VDDSO5 <sup>(1)</sup>     | CAP          | External Capacitor Connection | P29                                                                  |
| VDDAR_CORE                    | PWR          | Core RAM Supply               | AB27, AC24, AF15, AF18, AF21, AG11, AG28, T25                        |
| VDDAR_CPU                     | PWR          | CPU RAM Supply                | AB13, AC16, AC18, AC20, AE12, M21, N23, T15, U20, W14, W21, Y11, Y19 |
| VDDAR_MCU                     | PWR          | MCU RAM Supply                | M27, N24                                                             |
| VDDA_0P8_DSITX                | PWR          | Analog Supply for DSITX       | AJ24                                                                 |
| VDDA_0P8_DSITX_C              | PWR          | DSITX Clock Supply            | AJ25                                                                 |
| VDDA_0P8_UFS                  | PWR          | UFS 0.8V Supply               | AH11                                                                 |
| VDDA_0P8_USB                  | PWR          | USB 0.8V Supply               | AK20                                                                 |
| VDDA_0P8_CSIRX2               | PWR          | Analog Supply for CSIRX       | AJ28                                                                 |
| VDDA_0P8_CSIRX0_1             | PWR          | Analog Supply for CSIRX       | AJ26, AK26                                                           |
| VDDA_0P8_DLL_MMC0             | PWR          | MMC DLL Analog Supply         | AE9                                                                  |
| VDDA_0P8_PLL_DDR0             | PWR          | DDR de-skew PLL Analog Supply | U11                                                                  |
| VDDA_0P8_PLL_DDR1             | PWR          | DDR de-skew PLL Analog Supply | M14                                                                  |
| VDDA_0P8_PLL_DDR2             | PWR          | DDR de-skew PLL Analog Supply | N11                                                                  |
| VDDA_0P8_PLL_DDR3             | PWR          | DDR de-skew PLL Analog Supply | M18                                                                  |
| VDDA_0P8_SERDES2              | PWR          | SERDES 0.8V Supply            | AJ20, AJ21                                                           |
| VDDA_0P8_SERDES4              | PWR          | SERDES 0.8V Supply            | AJ17, AJ18                                                           |
| VDDA_0P8_SERDES0_1            | PWR          | SERDES 0.8V Supply            | AJ12, AJ15, AK13, AK14                                               |
| VDDA_0P8_SERDES_C2            | PWR          | SERDES 0.8V Clock Supply      | AG21, AH20                                                           |
| VDDA_0P8_SERDES_C4            | PWR          | SERDES 0.8V Clock Supply      | AG17, AH18                                                           |
| VDDA_0P8_SERDES_C0_1          | PWR          | SERDES 0.8V Clock Supply      | AH12, AH13, AH15, AH16                                               |
| VDDA_1P8_DSITX                | PWR          | Analog Supply for DSITX       | AH24, AH25                                                           |
| VDDA_1P8_UFS                  | PWR          | UFS 1.8V Supply               | AJ10                                                                 |
| VDDA_1P8_USB                  | PWR          | USB 1.8V Supply               | AK21                                                                 |
| VDDA_1P8_CSIRX2               | PWR          | Analog Supply for CSIRX       | AH29, AJ29                                                           |
| VDDA_1P8_CSIRX0_1             | PWR          | Analog Supply for CSIRX       | AH27, AH28                                                           |
| VDDA_1P8_SERDES2              | PWR          | SERDES 1.8V Supply            | AH21                                                                 |
| VDDA_1P8_SERDES4              | PWR          | SERDES 1.8V Supply            | AH17                                                                 |
| VDDA_1P8_SERDES0_1            | PWR          | SERDES 1.8V Supply            | AJ13, AJ14                                                           |
| VDDA_1P8_SERDES2_4            | PWR          | SERDES 1.8V Supply            | AJ23                                                                 |
| VDDA_3P3_USB                  | PWR          | USB 3.3V Supply               | AJ19                                                                 |
| VDDA_ADC0                     | PWR          | ADC0 Analog Supply            | M31                                                                  |

**表 6-123. Power Supply Signal Descriptions (continued)**

| SIGNAL NAME [1]  | PIN TYPE [2] | DESCRIPTION [3]                          | ALY PIN [4]                                                                                                                                                         |
|------------------|--------------|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDDA_ADC1        | PWR          | ADC1 Analog Supply                       | N30                                                                                                                                                                 |
| VDDA_MCU_PLLGRP0 | PWR          | Analog Supply for MCU PLL Group 0        | M28                                                                                                                                                                 |
| VDDA_MCU_TEMP    | PWR          | Analog Supply for MCU temperature sensor | M26                                                                                                                                                                 |
| VDDA_OSC1        | PWR          | HFOSC1 Supply                            | N29                                                                                                                                                                 |
| VDDA_PLLGRP0     | PWR          | Analog Supply for MAIN PLL Group 0       | AA27                                                                                                                                                                |
| VDDA_PLLGRP1     | PWR          | Analog Supply for MAIN PLL Group 1       | Y28                                                                                                                                                                 |
| VDDA_PLLGRP2     | PWR          | Analog Supply for MAIN PLL Group 2       | AG13                                                                                                                                                                |
| VDDA_PLLGRP5     | PWR          | Analog Supply for MAIN PLL Group 5       | V14                                                                                                                                                                 |
| VDDA_PLLGRP6     | PWR          | Analog Supply for MAIN PLL Group 6       | R21                                                                                                                                                                 |
| VDDA_PLLGRP7     | PWR          | Analog Supply for MAIN PLL Group 7       | P12                                                                                                                                                                 |
| VDDA_PLLGRP8     | PWR          | Analog Supply for MAIN PLL Group 8       | P15                                                                                                                                                                 |
| VDDA_PLLGRP9     | PWR          | Analog Supply for MAIN PLL Group 9       | Y26                                                                                                                                                                 |
| VDDA_PLLGRP10    | PWR          | Analog Supply for MAIN PLL Group 10      | AG23                                                                                                                                                                |
| VDDA_PLLGRP12    | PWR          | Analog Supply for MAIN PLL Group 12      | AA23                                                                                                                                                                |
| VDDA_PLLGRP13    | PWR          | Analog Supply for MAIN PLL Group 13      | AB26                                                                                                                                                                |
| VDDA_POR_WKUP    | PWR          | WKUP domain Analog Supply                | N28                                                                                                                                                                 |
| VDDA_TEMP0       | PWR          | Analog Supply for temperature sensor 0   | Y27                                                                                                                                                                 |
| VDDA_TEMP1       | PWR          | Analog Supply for temperature sensor 1   | M12                                                                                                                                                                 |
| VDDA_TEMP2       | PWR          | Analog Supply for temperature sensor 2   | W23                                                                                                                                                                 |
| VDDA_TEMP3       | PWR          | Analog Supply for temperature sensor 3   | AE13                                                                                                                                                                |
| VDDA_TEMP4       | PWR          | Analog Supply for temperature sensor 4   | AD18                                                                                                                                                                |
| VDDA_WKUP        | PWR          | Oscillator Supply for WKUP domain        | K31, L32                                                                                                                                                            |
| VDDSHV0          | PWR          | IO Power Supply                          | V30, V32, W31                                                                                                                                                       |
| VDDSHV0_MCU      | PWR          | IO Power Supply                          | H29, J28, K29                                                                                                                                                       |
| VDDSHV1_MCU      | PWR          | IO Power Supply                          | H25, J24, K25                                                                                                                                                       |
| VDDSHV2          | PWR          | IO Power Supply                          | T30, T32, U31                                                                                                                                                       |
| VDDSHV2_MCU      | PWR          | IO Power Supply                          | H27, J26, K27                                                                                                                                                       |
| VDDSHV5          | PWR          | IO Power Supply                          | P31, R30, R31                                                                                                                                                       |
| VDDS_DDR         | PWR          | DDR PHY IO Supply                        | A31, AK1, B1, H11, H13, H15, H17, H19, H9, J10, J12, J14, J16, J18, J8, K11, K13, K15, K17, K19, K9, L10, L12, L14, L16, L18, M9, N10, N8, P9, R10, R8, T9, U10, U8 |
| VDDS_DDR_C0      | PWR          | IO Power Supply for DDR Clock            | T10                                                                                                                                                                 |
| VDDS_DDR_C1      | PWR          | IO Power Supply for DDR Clock            | L15                                                                                                                                                                 |
| VDDS_DDR_C2      | PWR          | IO Power Supply for DDR Clock            | M10                                                                                                                                                                 |
| VDDS_DDR_C3      | PWR          | IO Power Supply for DDR Clock            | L17                                                                                                                                                                 |
| VDDS_MMC0        | PWR          | MMC0 PHY IO Supply                       | AF9, AG10, AG8, AH9                                                                                                                                                 |

表 6-123. Power Supply Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3]                         | ALY PIN [4]                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------------|--------------|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD_CORE        | PWR          | MAIN domain core Supply                 | AA24, AA26, AA28, AA30, AB25, AB29, AB31, AC26, AC28, AC30, AD25, AD27, AD29, AD31, AE24, AE26, AE28, AE30, AE32, AF13, AF17, AF19, AF23, AF25, AF27, AF29, AF31, AG12, AG14, AG16, AG18, AG20, AG22, AG24, AG26, AG30, AG32, AH31, AJ30, M11, M13, M15, M17, M19, N12, N16, N18, P11, P17, P19, R12, R14, R16, R18, R24, R26, R28, T11, T13, T27, U12, U24, U26, U28, V25, V27, W24, W26, W28, W30, W32, Y25, Y29, Y31 |
| VDD_CPU         | PWR          | CPU core Supply                         | AA10, AA12, AA14, AA20, AA22, AA8, AB11, AB19, AB21, AB23, AB9, AC10, AC12, AC14, AC22, AD11, AD13, AD15, AD17, AD19, AD21, AD23, AD9, AE10, AE14, AE16, AE18, AE20, AE22, AF11, H21, H23, J20, J22, K21, K23, L20, L22, N20, N22, P21, R20, R22, T17, T19, T21, T23, U14, U22, V11, V13, V19, V21, V23, V9, W10, W12, W20, W22, W8, Y13, Y21, Y23, Y9                                                                  |
| VDD_MCU         | PWR          | MCU core Supply                         | L24, M23, M25, N26, P23, P25, P27                                                                                                                                                                                                                                                                                                                                                                                       |
| VDD_MCU_WAKE1   | PWR          | Core Supply for MCU daisy chain         | L28                                                                                                                                                                                                                                                                                                                                                                                                                     |
| VDD_WAKE0       | PWR          | Core Supply for MAIN domain daisy chain | U29                                                                                                                                                                                                                                                                                                                                                                                                                     |

表 6-123. Power Supply Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----------------|--------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VSS             | GND          | Ground          | <p>A1, A10, A12, A15, A2, A20, A23, A25, A28, A34, A37, A5, A7, AA11, AA13, AA19, AA2, AA21, AA25, AA29, AA34, AA36, AA38, AA5, AA9, AB1, AB10, AB12, AB14, AB20, AB22, AB24, AB28, AB30, AB32, AB33, AB35, AB37, AB5, AB8, AC11, AC13, AC15, AC17, AC19, AC2, AC21, AC23, AC25, AC27, AC29, AC31, AC6, AC9, AD1, AD10, AD12, AD14, AD16, AD20, AD22, AD24, AD26, AD28, AD30, AD32, AD35, AD4, AD8, AE11, AE15, AE17, AE19, AE2, AE21, AE23, AE25, AE27, AE29, AE31, AE5, AF10, AF12, AF14, AF16, AF20, AF22, AF24, AF26, AF28, AF3, AF30, AF32, AF6, AF8, AG1, AG15, AG19, AG25, AG27, AG29, AG31, AG4, AG7, AG9, AH10, AH14, AH19, AH2, AH22, AH23, AH26, AH30, AH32, AH35, AH5, AH8, AJ11, AJ16, AJ22, AJ27, AJ3, AJ31, AJ6, AJ8, AJ9, AK10, AK11, AK12, AK15, AK16, AK17, AK18, AK19, AK22, AK23, AK24, AK25, AK27, AK28, AK30, AK32, AL1, AL10, AL12, AL13, AL14, AL15, AL16, AL17, AL18, AL19, AL21, AL26, AL29, AL31, AL4, AM11, AM13, AM15, AM18, AM20, AM23, AM25, AM27, AM3, AM30, AM32, AM38, AM6, AN1, AN10, AN12, AN14, AN16, AN19, AN22, AN25, AN28, AN31, AN34, AN4, AN7, AP12, AP15, AP18, AP21, AP24, AP27, AP3, AP30, AP33, AP36, AP6, AP9, AR1, AR10, AR13, AR16, AR19, AR22, AR25, AR28, AR31, AR34, AR37, AR4, AR7, AT12, AT15, AT18, AT21, AT24, AT27, AT3, AT30, AT33, AT36, AT6, AT9, AU1, AU10, AU13, AU16, AU19, AU22, AU25, AU28, AU31, AU34, AU37, AU38, AU4, AU7, AV1, AV11, AV14, AV17, AV2, AV20, AV23, AV26, AV29, AV32, AV35, AV5, AV8, B11, B13, B16, B19,</p> |

表 6-123. Power Supply Signal Descriptions (continued)

| SIGNAL NAME [1] | PIN TYPE [2] | DESCRIPTION [3] | ALY PIN [4]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----------------|--------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                 |              |                 | B22, B24, B26, B29, B31,<br>B38, B6, B9, C14, C17,<br>C18, C2, C21, C27, C30,<br>C4, C8, D10, D15, D20,<br>D23, D28, D3, D35, D6,<br>D7, E12, E13, E16, E19,<br>E2, E22, E25, E26, E29,<br>E31, E5, E9, F1, F11, F14,<br>F17, F21, F24, F27, F30,<br>F4, F7, F8, G15, G18,<br>G20, G28, G3, G6, H10,<br>H16, H18, H2, H20, H22,<br>H24, H26, H28, H30, H31,<br>H5, H7, H8, J1, J11, J13,<br>J15, J17, J19, J21, J23,<br>J25, J27, J29, J32, J4, J9,<br>K10, K12, K14, K16, K18,<br>K2, K20, K22, K24, K26,<br>K6, K8, L1, L11, L13, L19,<br>L21, L23, L31, L5, L9,<br>M16, M2, M20, M22, M24,<br>M29, M30, M32, M5, M8,<br>N15, N17, N19, N21, N25,<br>N3, N31, N32, N38, N6,<br>N9, P1, P10, P16, P18,<br>P20, P22, P24, P26, P30,<br>P32, P35, P37, P4, P7,<br>P8, R11, R13, R15, R17,<br>R19, R2, R23, R25, R27,<br>R32, R34, R36, R38, R5,<br>R9, T12, T14, T16, T18,<br>T20, T22, T24, T26, T28,<br>T3, T31, T33, T35, T37,<br>T6, T8, U13, U19, U21,<br>U23, U25, U27, U3, U30,<br>U32, U34, U36, U38, U6,<br>U9, V10, V12, V2, V20,<br>V22, V24, V26, V28, V31,<br>V33, V35, V37, V5, V8,<br>W1, W11, W13, W19,<br>W25, W27, W29, W34,<br>W36, W38, W4, W7, W9,<br>Y10, Y12, Y14, Y20, Y22,<br>Y24, Y3, Y30, Y32, Y33,<br>Y35, Y37, Y6, Y8 |

(1) This pin must always be connected via a 1-  $\mu$ F  $\pm 10\%$  capacitor to VSS.

## 6.4 Pin Connectivity Requirements

This section describes connectivity requirements for package balls that have specific connectivity requirements and unused package balls.

### 备注

All power balls must be supplied with the voltages specified in the [Recommended Operating Conditions](#) section, unless otherwise specified in [Signal Descriptions](#).

### 备注

For additional clarification, "leave unconnected" or "no connect" (NC) means no signal traces can be connected to these device ball number.

表 6-124 shows the connectivity requirements for specific signals by ball name and ball number.

**表 6-124. Connectivity Requirements**

| BALL<br>NUMBER | BALL NAME        | CONNECTION REQUIREMENT                                                                                                                                       |
|----------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P38            | OSC1_XI          | Each of these balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low-level, if unused. |
| T38            | WKUP_OSC0_XI     |                                                                                                                                                              |
| G37            | TRSTN            |                                                                                                                                                              |
| U1             | DDR0_DQS0P       |                                                                                                                                                              |
| AA1            | DDR0_DQS1P       |                                                                                                                                                              |
| AF1            | DDR0_DQS2P       |                                                                                                                                                              |
| AJ1            | DDR0_DQS3P       |                                                                                                                                                              |
| A16            | DDR1_DQS0P       |                                                                                                                                                              |
| A13            | DDR1_DQS1P       |                                                                                                                                                              |
| A8             | DDR1_DQS2P       |                                                                                                                                                              |
| A3             | DDR1_DQS3P       |                                                                                                                                                              |
| T1             | DDR2_DQS0P       |                                                                                                                                                              |
| N1             | DDR2_DQS1P       |                                                                                                                                                              |
| H1             | DDR2_DQS2P       |                                                                                                                                                              |
| E1             | DDR2_DQS3P       |                                                                                                                                                              |
| A18            | DDR3_DQS0P       |                                                                                                                                                              |
| A21            | DDR3_DQS1P       |                                                                                                                                                              |
| A26            | DDR3_DQS2P       |                                                                                                                                                              |
| A29            | DDR3_DQS3P       |                                                                                                                                                              |
| AC8            | DDR0_RET         |                                                                                                                                                              |
| G8             | DDR1_RET         |                                                                                                                                                              |
| L8             | DDR2_RET         |                                                                                                                                                              |
| G27            | DDR3_RET         |                                                                                                                                                              |
| K28            | VMON1_ER_VSYS    |                                                                                                                                                              |
| N27            | VMON2_IR_VCPU    |                                                                                                                                                              |
| J30            | VMON3_IR_VEXT1P8 |                                                                                                                                                              |
| P28            | VMON4_IR_VEXT1P8 |                                                                                                                                                              |
| R29            | VMON5_IR_VEXT3P3 |                                                                                                                                                              |

表 6-124. Connectivity Requirements (continued)

| BALL<br>NUMBER | BALL NAME     | CONNECTION REQUIREMENT                                                                                                                                                                                                                                                      |
|----------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| P36            | MCU_ADC0_AIN0 | Each of these balls can be connected to VSS through a separate external pull resistor or can be connected directly to VSS to ensure these balls are held to a valid logic low-level, if unused.                                                                             |
| V36            | MCU_ADC0_AIN1 |                                                                                                                                                                                                                                                                             |
| T34            | MCU_ADC0_AIN2 |                                                                                                                                                                                                                                                                             |
| T36            | MCU_ADC0_AIN3 |                                                                                                                                                                                                                                                                             |
| P34            | MCU_ADC0_AIN4 |                                                                                                                                                                                                                                                                             |
| R37            | MCU_ADC0_AIN5 |                                                                                                                                                                                                                                                                             |
| R33            | MCU_ADC0_AIN6 |                                                                                                                                                                                                                                                                             |
| V38            | MCU_ADC0_AIN7 |                                                                                                                                                                                                                                                                             |
| Y38            | MCU_ADC1_AIN0 |                                                                                                                                                                                                                                                                             |
| Y34            | MCU_ADC1_AIN1 |                                                                                                                                                                                                                                                                             |
| V34            | MCU_ADC1_AIN2 |                                                                                                                                                                                                                                                                             |
| W37            | MCU_ADC1_AIN3 |                                                                                                                                                                                                                                                                             |
| AA37           | MCU_ADC1_AIN4 |                                                                                                                                                                                                                                                                             |
| W33            | MCU_ADC1_AIN5 |                                                                                                                                                                                                                                                                             |
| U33            | MCU_ADC1_AIN6 |                                                                                                                                                                                                                                                                             |
| Y36            | MCU_ADC1_AIN7 |                                                                                                                                                                                                                                                                             |
| AN11           | SERDES0_REXT  | Each of these balls must be connected to VSS through appropriate external pull resistor to ensure these balls are held to a valid logic low level, if unused. Refer to <a href="#">Signal Descriptions</a> footnote for appropriate value of pull-resistor for each signal. |
| AL9            | SERDES1_REXT  |                                                                                                                                                                                                                                                                             |
| AL20           | SERDES2_REXT  |                                                                                                                                                                                                                                                                             |
| AM19           | SERDES4_REXT  |                                                                                                                                                                                                                                                                             |
| AM28           | CSI0_RXRCALIB |                                                                                                                                                                                                                                                                             |
| AL28           | CSI1_RXRCALIB |                                                                                                                                                                                                                                                                             |
| AM31           | CSI2_RXRCALIB |                                                                                                                                                                                                                                                                             |
| AE8            | DDR0_CAL0     |                                                                                                                                                                                                                                                                             |
| G14            | DDR1_CAL0     |                                                                                                                                                                                                                                                                             |
| U7             | DDR2_CAL0     |                                                                                                                                                                                                                                                                             |
| F18            | DDR3_CAL0     |                                                                                                                                                                                                                                                                             |
| AM24           | DSI0_TXRCALIB |                                                                                                                                                                                                                                                                             |
| AL22           | DSI1_TXRCALIB |                                                                                                                                                                                                                                                                             |
| AN18           | USB0_RCALIB   |                                                                                                                                                                                                                                                                             |

**表 6-124. Connectivity Requirements (continued)**

| BALL<br>NUMBER | BALL NAME     | CONNECTION REQUIREMENT                                                                                                                                                                                                                                                              |
|----------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| G36            | MCU_RESETZ    | Each of these balls must be connected to the corresponding power supply through a separate external pull resistor to ensure these balls are held to a valid logic high level, if unused.                                                                                            |
| K32            | MCU_PORZ      |                                                                                                                                                                                                                                                                                     |
| P33            | PORZ          |                                                                                                                                                                                                                                                                                     |
| F34            | RESET_REQZ    |                                                                                                                                                                                                                                                                                     |
| G35            | TCK           |                                                                                                                                                                                                                                                                                     |
| AL36           | TMS           |                                                                                                                                                                                                                                                                                     |
| G34            | MCU_I2C0_SDA  |                                                                                                                                                                                                                                                                                     |
| M35            | MCU_I2C0_SCL  |                                                                                                                                                                                                                                                                                     |
| N33            | WKUP_I2C0_SCL |                                                                                                                                                                                                                                                                                     |
| N35            | WKUP_I2C0_SDA |                                                                                                                                                                                                                                                                                     |
| AN36           | I2C0_SCL      |                                                                                                                                                                                                                                                                                     |
| AP37           | I2C0_SDA      |                                                                                                                                                                                                                                                                                     |
| AN35           | EXTINTN       |                                                                                                                                                                                                                                                                                     |
| AL37           | TDI           |                                                                                                                                                                                                                                                                                     |
| AL35           | TDO           |                                                                                                                                                                                                                                                                                     |
| F35            | EMU0          |                                                                                                                                                                                                                                                                                     |
| H34            | EMU1          |                                                                                                                                                                                                                                                                                     |
| V1             | DDR0_DQS0N    |                                                                                                                                                                                                                                                                                     |
| Y1             | DDR0_DQS1N    |                                                                                                                                                                                                                                                                                     |
| AE1            | DDR0_DQS2N    |                                                                                                                                                                                                                                                                                     |
| AH1            | DDR0_DQS3N    |                                                                                                                                                                                                                                                                                     |
| A17            | DDR1_DQS0N    |                                                                                                                                                                                                                                                                                     |
| A14            | DDR1_DQS1N    |                                                                                                                                                                                                                                                                                     |
| A9             | DDR1_DQS2N    |                                                                                                                                                                                                                                                                                     |
| A4             | DDR1_DQS3N    |                                                                                                                                                                                                                                                                                     |
| R1             | DDR2_DQS0N    |                                                                                                                                                                                                                                                                                     |
| M1             | DDR2_DQS1N    |                                                                                                                                                                                                                                                                                     |
| G1             | DDR2_DQS2N    |                                                                                                                                                                                                                                                                                     |
| D1             | DDR2_DQS3N    |                                                                                                                                                                                                                                                                                     |
| A19            | DDR3_DQS0N    |                                                                                                                                                                                                                                                                                     |
| A22            | DDR3_DQS1N    |                                                                                                                                                                                                                                                                                     |
| A27            | DDR3_DQS2N    |                                                                                                                                                                                                                                                                                     |
| A30            | DDR3_DQS3N    |                                                                                                                                                                                                                                                                                     |
| R35            | MCU_ADC0_REFP | If the MCU_ADCn interface is not used, these signals should be connected to the same power supply as the VDDA_ADCn supply input.                                                                                                                                                    |
| AA35           | MCU_ADC1_REFP |                                                                                                                                                                                                                                                                                     |
| U35            | MCU_ADC0_REFN | If the MCU_ADCn interface is not used, these signals should be connected to VSS.                                                                                                                                                                                                    |
| W35            | MCU_ADC1_REFN |                                                                                                                                                                                                                                                                                     |
| L29            | VPP_MCU       | Each of these balls must be left unconnected, if unused.                                                                                                                                                                                                                            |
| AA31           | VPP_CORE      |                                                                                                                                                                                                                                                                                     |
| AJ7            | MMC0_CALPAD   |                                                                                                                                                                                                                                                                                     |
|                | DDR0_*        | DDRSS0, DDRSS1, DDRSS2 and DDRSS3 must always be used in incremental order. For instance, when using a single LPDDR component, it must be connected to the DDR0_* interface. When using two LPDDR components, they must be connected to DDR0_* and DDR1_* interfaces, and so forth. |
|                | DDR1_*        |                                                                                                                                                                                                                                                                                     |
|                | DDR2_*        |                                                                                                                                                                                                                                                                                     |
|                | DDR3_*        |                                                                                                                                                                                                                                                                                     |



表 6-125 shows the specific connection requirements for the RESERVED ball numbers on the device.

备注

For additional clarification, "left unconnected" or "no connect" (NC) means **no** signal traces can be connected to these device ball numbers.

表 6-125. Reserved Balls Specific Connection Requirements (AHP)

| BALL NUMBERS                                                                                                                                                                                                                                        | CONNECTION REQUIREMENTS                            |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|
| AF7 / AK2 / AK29 / AK31 / AL11 / AL23 / AL24 / AL25 / AL27 / AL30 / AM10 / AM12 / AM14 / AM16 / AM17 / AM21 / AM22 / AM26 / AM29 / AM33 / AM9 / AN13 / AN20 / AN21 / G17 / G22 / G30 / H12 / H14 / H32 / H33 / J31 / J33 / K30 / L30 / N7 / T7 / Y7 | RESERVED.<br>These balls must be left unconnected. |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free – air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                                                  |                                              |                                                                                                                   | MIN                           | MAX          | UNIT |
|------------------------------------------------------------|----------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-------------------------------|--------------|------|
| VDD_*(3)                                                   | Core supplies                                |                                                                                                                   | – 0.3                         | 1.05         | V    |
| VDDAR_*(3)                                                 | RAM supplies                                 |                                                                                                                   | – 0.3                         | 1.05         | V    |
| VDDA_0P8_*(3)                                              | Analog supplies for 0.8V domains             |                                                                                                                   | – 0.3                         | 1.05         | V    |
| VDDA_1P8_*(3)                                              | Analog supplies for 1.8 V PHY domains        |                                                                                                                   | – 0.3                         | 2.2          | V    |
| VDDA_3P3_USB                                               | Analog supply for 3.3V USB domain            |                                                                                                                   | – 0.3                         | 3.8          | V    |
| VDDA_*(3)                                                  | Analog supply for 1.8V PLL and other domains |                                                                                                                   | – 0.3                         | 2.2          | V    |
| VDDS_DDR_*(3)                                              | DDR interface power supplies                 |                                                                                                                   | – 0.3                         | 1.2          | V    |
| VDDS_MMC0                                                  | MMC0 IO supply                               |                                                                                                                   | – 0.3                         | 2.2          | V    |
| VDDSHV*(3)                                                 | Dual Voltage LVCMOS IO supplies              | 1.8 V                                                                                                             | – 0.3                         | 2.2          | V    |
|                                                            |                                              | 3.3 V                                                                                                             | – 0.3                         | 3.8          |      |
| VPP_CORE VPP MCU                                           | Supply voltage range for EFUSE domains       |                                                                                                                   | – 0.3                         | 1.89         | V    |
| USB0_VBUS(9)                                               | Voltage range for USB VBUS comparator input  |                                                                                                                   | – 0.3                         | 3.6          | V    |
| Steady State Max. Voltage at all fail – safe IO pins       |                                              | I2C0_SCL,<br>I2C0_SDA,<br>WKUP_I2C0_SC<br>L,<br>WKUP_I2C0_SD<br>A,<br>MCU_I2C0_SCL,<br>MCU_I2C0_SDA,<br>EXTINTn   | – 0.3                         | 3.8          | V    |
|                                                            |                                              | MCU_PORz,<br>PORz                                                                                                 | – 0.3                         | 3.8          | V    |
| Steady State Max. Voltage at all other IO pins(4)          |                                              | VMON1_ER_VSY<br>S(8),<br>VMON3_IR_VEX<br>T1P8,<br>VMON4_IR_VEX<br>T1P8                                            | – 0.3                         | 2.2          | V    |
|                                                            |                                              | VMON2_IR_VCP<br>U                                                                                                 | – 0.3                         | 1.05         | V    |
|                                                            |                                              | VMON5_IR_VEX<br>T3P3                                                                                              | – 0.3                         | 3.8          | V    |
|                                                            |                                              | All other IO pins                                                                                                 | – 0.3 IO supply voltage + 0.3 |              | V    |
| Transient Overshoot and Undershoot specification at IO pin |                                              | 20% of IO supply<br>voltage for up to<br>20% of signal<br>period<br>图 7-1 (see IO<br>Transient Voltage<br>Ranges) | 0.2 × VDD(7)                  |              | V    |
| Latch – up Performance, Class II (125°C)(5)                |                                              | I – Test                                                                                                          | – 100                         | 100          | mA   |
|                                                            |                                              | Over – Voltage<br>(OV) Test                                                                                       | NA                            | 1.5 × VDD(7) | V    |
| TSTG(6)                                                    | Storage<br>temperature                       |                                                                                                                   | – 55                          | +150         | °C   |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under [Recommended Operating Conditions](#). If

used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltage values are with respect to their associated VSS or VSSA\_x, unless otherwise noted.

(3) **VDD** \* includes: VDD\_CORE, VDD\_CPU, VDD\_MCU, VDD\_MCU\_WAKE1, VDD\_WAKE0

**VDDAR** \* includes: VDDAR\_CORE, VDDAR\_CPU, VDDAR\_MCU

**VDDA\_0P8** \* includes: VDDA\_0P8\_CSIRX0\_1, VDDA\_0P8\_CSIRX2, VDDA\_0P8\_DLL\_MMC0, VDDA\_0P8\_DSITX, VDDA\_0P8\_DSITX\_C, VDDA\_0P8\_PLL\_DDR0, VDDA\_0P8\_PLL\_DDR1, VDDA\_0P8\_PLL\_DDR2, VDDA\_0P8\_PLL\_DDR3, VDDA\_0P8\_SERDES\_C0\_1, VDDA\_0P8\_SERDES\_C2, VDDA\_0P8\_SERDES\_C4, VDDA\_0P8\_SERDES0\_1, VDDA\_0P8\_SERDES2, VDDA\_0P8\_SERDES4, VDDA\_0P8\_UFS, VDDA\_0P8\_USB

**VDDA\_1P8** \* includes: VDDA\_1P8\_CSIRX0\_1, VDDA\_1P8\_CSIRX2, VDDA\_1P8\_DSITX, VDDA\_1P8\_SERDES0\_1, VDDA\_1P8\_SERDES2, VDDA\_1P8\_SERDES2\_4, VDDA\_1P8\_SERDES4, VDDA\_1P8\_UFS, VDDA\_1P8\_USB

**VDDA** \* includes: VDDA\_ADC0, VDDA\_ADC1, VDDA\_MCU\_PLLGRP0, VDDA\_MCU\_TEMP, VDDA\_OSC1, VDDA\_PLLGRP0, VDDA\_PLLGRP1, VDDA\_PLLGRP10, VDDA\_PLLGRP12, VDDA\_PLLGRP13, VDDA\_PLLGRP2, VDDA\_PLLGRP5, VDDA\_PLLGRP6, VDDA\_PLLGRP7, VDDA\_PLLGRP8, VDDA\_PLLGRP9, VDDA\_POR\_WKUP, VDDA\_TEMP0, VDDA\_TEMP1, VDDA\_TEMP2, VDDA\_TEMP3, VDDA\_TEMP4, VDDA\_WKUP

**VDDS\_DDR** \* includes: VDDS\_DDR, VDDS\_DDR\_C0, VDDS\_DDR\_C1, VDDS\_DDR\_C2, VDDS\_DDR\_C3

**VDDSHV** \* includes: VDDSHV0, VDDSHV0\_MCU, VDDSHV1\_MCU, VDDSHV2, VDDSHV2\_MCU, VDDSHV5

(4) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be - 0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp - up and ramp - down sequences.

(5) For current pulse injection:

Pins stressed per JEDEC JESD78E (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

For overvoltage performance:

Supplies stressed per JEDEC JESD78E (Class II) and passed specified voltage injection.

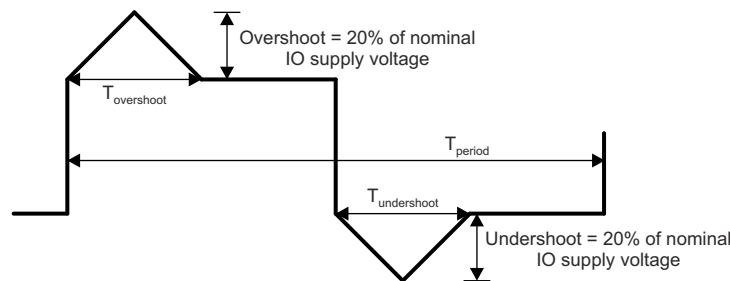
(6) For tape and reel the storage temperature range is [ - 10°C; +50°C] with a maximum relative humidity of 70%. TI recommends returning to ambient room temperature before usage.

(7) VDD is the voltage on the corresponding power-supply pin(s) for the IO.

(8) The VMON\_ER\_VSYS pin provides a way to monitor the system power supply. For more information, see [System Power Supply Monitor Design Guidelines using VMON/POK](#).

(9) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see the [USB VBUS Design Guidelines](#).

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The I2C0\_SCL, I2C0\_SDA, I2C1\_SCL, I2C1\_SDA, DDR\_FS\_RESETh, and NMIh are the only fail - safe IO terminals. All other IO terminals are not fail - safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in [Absolute Maximum Ratings](#).



A.  $T_{\text{overshoot}} + T_{\text{undershoot}} < 20\% \text{ of } T_{\text{period}}$

图 7-1. IO Transient Voltage Ranges

## 7.2 ESD Ratings

|                    |                         |                                                         |                        | VALUE | UNIT |
|--------------------|-------------------------|---------------------------------------------------------|------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> |                        | ±1000 | V    |
|                    |                         | Charged-device model (CDM), per AEC Q100-011            | All pins               | ±250  |      |
|                    |                         |                                                         | Corner pins (A1, AJ29) | ±750  |      |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Power-On-Hour (POH) Limits

| IP <sup>(1)</sup> (2) (3) | VOLTAGE DOMAIN | VOLTAGE (V) (MAX) | FREQUENCY (MHz) (MAX) | T <sub>j</sub> (°C)                      | POH    |
|---------------------------|----------------|-------------------|-----------------------|------------------------------------------|--------|
| All                       | 100%           | All               | All Supported OPPs    | Automotive -40°C to 125°C <sup>(4)</sup> | 20000  |
| All                       | 100%           | All               | All Supported OPPs    | Extended -40°C to 105°C                  | 100000 |
| All                       | 100%           | All               | All Supported OPPs    | Commercial 0°C to 90°C                   | 100000 |

- The information in the section below is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
- Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures
- POH is a functional of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH to achieve the same reliability performance. For assessment of alternate use cases, contact your local TI representative.
- Automotive profile is defined as 20000 power on hours with junction temperature as follows: 5%@-40°C, 65%@70°C, 20%@110°C, 10%@125°C.

## 7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| SUPPLY NAME       | DESCRIPTION                                                            |                 | MIN <sup>(1)</sup>                     | NOM                | MAX <sup>(1)</sup>                    | UNIT |
|-------------------|------------------------------------------------------------------------|-----------------|----------------------------------------|--------------------|---------------------------------------|------|
| VDD_CORE          | Boot/Active voltage for MAIN domain core supply                        |                 | 0.76 <sup>(1)</sup>                    | 0.8                | 0.84 <sup>(1)</sup>                   | V    |
| VDD_MCU           | Boot/Active voltage for MCUSS core supply                              |                 | 0.76 <sup>(1)</sup>                    | 0.8                | 0.89 <sup>(1)</sup>                   | V    |
| VDD_CPU           | Boot voltage for CPU core supply, applied at cold power up event       |                 | 0.76 <sup>(1)</sup>                    | 0.8                | 0.84 <sup>(1)</sup>                   | V    |
|                   | Active voltage for CPU core supply, after AVS mode enabled in software |                 | AVS <sup>(3)</sup> - 5% <sup>(1)</sup> | AVS <sup>(3)</sup> | AVS <sup>(3)</sup> +5% <sup>(1)</sup> | V    |
| VDD_CPU AVS Range | AVS valid voltage range for VDD_CPU                                    |                 | 0.6                                    |                    | 0.9                                   | V    |
| VDDAR_*(5)        | RAM supplis                                                            |                 | 0.81                                   | 0.85               | 0.89                                  | V    |
| VDDA_0P8_*(5)     | Analog supplies for 0.8V domains                                       |                 | 0.76                                   | 0.8                | 0.84                                  | V    |
| VDDA_1P8_*(5)     | Analog supplies for 1.8V PHY domains                                   |                 | 1.71                                   | 1.8                | 1.89                                  | V    |
| VDDA_3P3_USB(5)   | Analog supply for 3.3V USB domain                                      |                 | 3.14                                   | 3.3                | 3.46                                  | V    |
| VDDA_*(5)         | Analog supply for 1.8V PLL and other domains                           |                 | 1.71                                   | 1.8                | 1.89                                  | V    |
| VDDA_*            | Peak to Peak Noise for all VDDA inputs                                 |                 |                                        |                    | 25                                    | mV   |
| VDDS_DDR_*(5)     | DDR inteface power supply                                              |                 | 1.06                                   | 1.1                | 1.15                                  | V    |
| VDDS_MMC0         | MMC0 IO supply                                                         |                 | 1.71                                   | 1.8                | 1.89                                  | V    |
| VDDSHV*(5)        | Dual Voltage LVCMOS IO supplies                                        | 1.8-V operation | 1.71                                   | 1.8                | 1.89                                  | V    |
|                   |                                                                        | 3.3-V operation | 3.14                                   | 3.3                | 3.46                                  | V    |
| USB0_VBUS         | Voltage range for USB VBUS comparator input                            |                 | 0                                      | See <sup>(4)</sup> | 3.46                                  | V    |
| USB0_ID           | Voltage range for the USB ID input                                     |                 |                                        | See <sup>(2)</sup> |                                       | V    |
| VSS               | Ground                                                                 |                 |                                        | 0                  |                                       | V    |

over operating free-air temperature range (unless otherwise noted)

| SUPPLY NAME    | DESCRIPTION                          |            | MIN <sup>(1)</sup> | NOM | MAX <sup>(1)</sup> | UNIT |
|----------------|--------------------------------------|------------|--------------------|-----|--------------------|------|
| T <sub>J</sub> | Operating junction temperature range | Automotive | - 40               |     | 125                | °C   |
|                |                                      | Extended   | -40                |     | 105                | °C   |
|                |                                      | Commercial | 0                  |     | 90                 | °C   |

- (1) For all VDD\* supply inputs, the voltage at the device ball must never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, and so forth. This is required for all supply inputs, but special care should be given to the VDD\_CORE, VDD\_MCU, and VDD\_CPU domains which have higher transient current demand compared to other rails.
- (2) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSS with a resistance less than 10  $\Omega$  or greater than 100 k $\Omega$ . The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.
- (3) The AVS Voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the VTM\_DEVINFO\_VDn. For information about VTM\_DEVINFO\_VDn Registers address, please refer to Voltage and Thermal Manager section in the device TRM. The power supply should be adjustable over the ranges shown in the VDD\_CPU AVS Range entry.
- (4) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see [USB VBUS Design Guidelines](#).
- (5) **VDD\_\* includes:** VDD\_CORE, VDD\_CPU, VDD\_MCU, VDD\_MCU\_WAKE1, VDD\_WAKE0  
**VDDAR\_\* includes:** VDDAR\_CORE, VDDAR\_CPU, VDDAR\_MCU  
**VDDA\_0P8\_\* includes:** VDDA\_0P8\_CSIRX0\_1, VDDA\_0P8\_CSIRX2, VDDA\_0P8\_DLL\_MMC0, VDDA\_0P8\_DSITX, VDDA\_0P8\_DSITX\_C, VDDA\_0P8\_PLL\_DDR0, VDDA\_0P8\_PLL\_DDR1, VDDA\_0P8\_PLL\_DDR2, VDDA\_0P8\_PLL\_DDR3, VDDA\_0P8\_SERDES\_C0\_1, VDDA\_0P8\_SERDES\_C2, VDDA\_0P8\_SERDES\_C4, VDDA\_0P8\_SERDES0\_1, VDDA\_0P8\_SERDES2, VDDA\_0P8\_SERDES4, VDDA\_0P8\_UFS, VDDA\_0P8\_USB  
**VDDA\_1P8\_\* includes:** VDDA\_1P8\_CSIRX0\_1, VDDA\_1P8\_CSIRX2, VDDA\_1P8\_DSITX, VDDA\_1P8\_SERDES0\_1, VDDA\_1P8\_SERDES2, VDDA\_1P8\_SERDES2\_4, VDDA\_1P8\_SERDES4, VDDA\_1P8\_UFS, VDDA\_1P8\_USB  
**VDDA\_\* includes:** VDDA\_ADC0, VDDA\_ADC1, VDDA\_MCU\_PLLGRP0, VDDA\_MCU\_TEMP, VDDA\_OSC1, VDDA\_PLLGRP0, VDDA\_PLLGRP1, VDDA\_PLLGRP10, VDDA\_PLLGRP12, VDDA\_PLLGRP13, VDDA\_PLLGRP2, VDDA\_PLLGRP5, VDDA\_PLLGRP6, VDDA\_PLLGRP7, VDDA\_PLLGRP8, VDDA\_PLLGRP9, VDDA\_POR\_WKUP, VDDA\_TEMP0, VDDA\_TEMP1, VDDA\_TEMP2, VDDA\_TEMP3, VDDA\_TEMP4, VDDA\_WKUP  
**VDDS\_DDR\_\* includes:** VDDS\_DDR, VDDS\_DDR\_C0, VDDS\_DDR\_C1, VDDS\_DDR\_C2, VDDS\_DDR\_C3  
**VDDSHV\* includes:** VDDSHV0, VDDSHV0\_MCU, VDDSHV1\_MCU, VDDSHV2, VDDSHV2\_MCU, VDDSHV5

## 7.5 运行性能点

本节介绍了器件的运行条件。本节还包含处理器时钟和器件内核时钟的每个运行性能点 (OPP) 的说明。

表 7-1 描述了器件每个速度等级支持的最大频率。

**表 7-1. 速度等级最大频率**

| 器件         | 最大频率 (MHz) |        |          |           |     |        |      |                                     |      |                         |
|------------|------------|--------|----------|-----------|-----|--------|------|-------------------------------------|------|-------------------------|
|            | A72SS0     | C71SS0 | R5FSS0/1 | MCU_R5SS0 | GPU | CBASS0 | VPAC | VENCDEC                             | DMSC | LPDDR4                  |
| AM69Ax...T | 2000       | 1000   | 1000     | 1000      | 800 | 500    | 720  | 550 ( 960MP/s<br>或 480MP/s )<br>(2) | 333  | 4266MT/s <sup>(1)</sup> |

- (1) 最大 DDR 频率将根据系统中使用的特定存储器类型 ( 供应商 ) 以及根据 PCB 实现进行限制。TI 强烈建议所有设计的每个细节 ( 布线、间距、过孔/背钻、PCB 材料等 ) 都严格遵循 TI LPDDR4 EVM PCB 布局, 以便完全实现指定的时钟频率。有关详细信息, 请参阅 Jacinto 7 [LPDDR 电路板设计和布局布线指南](#)
- (2) 请参阅 [器件比较](#) 表以确定具体器件型号, 包括 1 个 VENCDEC 模块 (480MP/s) 或 2 个 VENCDEC 模块 (960MP/s)。

## 7.6 Electrical Characteristics

### 备注

The interfaces or signals described in 节 7.6.1 through 节 7.6.8 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

### 7.6.1 I2C, Open-Drain, Fail-Safe (I2C OD FS) Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER         |                                         | TEST CONDITIONS               | MIN                          | TYP                          | MAX | UNIT |
|-------------------|-----------------------------------------|-------------------------------|------------------------------|------------------------------|-----|------|
| <b>1.8-V MODE</b> |                                         |                               |                              |                              |     |      |
| V <sub>IL</sub>   | Input low-level threshold               |                               |                              | 0.3 × VDDSHV <sup>(1)</sup>  |     | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state  |                               |                              | 0.3 × VDDSHV <sup>(1)</sup>  |     | V    |
| V <sub>IH</sub>   | Input high-level threshold              |                               | 0.7 × VDDSHV <sup>(1)</sup>  |                              |     | V    |
| V <sub>IHSS</sub> | Input high-level threshold steady state |                               | 0.7 × VDDSHV <sup>(1)</sup>  |                              |     | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage                |                               | 0.1 × VDDSHV <sup>(1)</sup>  |                              |     | mV   |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 1.8 V or 0 V |                              |                              | ±10 | μA   |
| V <sub>OL</sub>   | Output low-level voltage                |                               |                              | 0.2 × VDDSHV <sup>(1)</sup>  |     | V    |
| I <sub>OL</sub>   | Low Level Output Current                | V <sub>OL(MAX)</sub>          | 6                            |                              |     | mA   |
| <b>3.3-V MODE</b> |                                         |                               |                              |                              |     |      |
| V <sub>IL</sub>   | Input low-level threshold               |                               |                              | 0.3 × VDDSHV <sup>(1)</sup>  |     | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state  |                               |                              | 0.25 × VDDSHV <sup>(1)</sup> |     | V    |
| V <sub>IH</sub>   | Input high-level threshold              |                               | 0.7 × VDDSHV <sup>(1)</sup>  |                              |     | V    |
| V <sub>IHSS</sub> | Input high-level threshold steady state |                               | 0.7 × VDDSHV <sup>(1)</sup>  |                              |     | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage                |                               | 0.05 × VDDSHV <sup>(1)</sup> |                              |     | mV   |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 3.3 V or 0 V |                              |                              | ±10 | μA   |
| V <sub>OL</sub>   | Output low-level voltage                |                               |                              | 0.4                          |     | V    |
| I <sub>OL</sub>   | Low Level Output Current                | V <sub>OL(MAX)</sub>          | 6                            |                              |     | mA   |

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see the [Pin Attributes](#), POWER column.

### 7.6.2 Fail-Safe Reset (FS Reset) Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER         |                                        | TEST CONDITIONS | MIN | TYP                         | MAX | UNIT |
|-------------------|----------------------------------------|-----------------|-----|-----------------------------|-----|------|
| V <sub>IL</sub>   | Input low-level threshold              |                 |     | 0.3 × VDDSHV <sup>(1)</sup> |     | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state |                 |     | 0.3 × VDDSHV <sup>(1)</sup> |     | V    |

Over recommended operating conditions (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS                         | MIN                           | TYP | MAX | UNIT |
|-------------------|-----------------------------------------|-------------------------------|-----|-----|------|
| V <sub>IH</sub>   | Input high-level threshold              | 0.7 × VDDSHV <sup>(1)</sup>   |     |     | V    |
| V <sub>IHSS</sub> | Input high-level threshold steady state | 0.7 × VDDSHV <sup>(1)</sup>   |     |     | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage                | 200                           |     |     | mV   |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 1.8 V or 0 V |     | ±10 | μA   |

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column.

### 7.6.3 HFOSC/LFOSC Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER                        | TEST CONDITIONS            | MIN                             | TYP                             | MAX | UNIT |
|----------------------------------|----------------------------|---------------------------------|---------------------------------|-----|------|
| <b>HIGH FREQUENCY OSCILLATOR</b> |                            |                                 |                                 |     |      |
| V <sub>IH</sub>                  | Input high-level threshold | 0.65 × VDDSHV <sup>(1)</sup>    |                                 |     | V    |
| V <sub>IL</sub>                  | Input low-level threshold  |                                 | 0.35 × VDDSHV <sup>(1)</sup>    |     | V    |
| V <sub>HYS</sub>                 | Input Hysteresis Voltage   |                                 | 49                              |     | mV   |
| <b>LOW FREQUENCY OSCILLATOR</b>  |                            |                                 |                                 |     |      |
| V <sub>IH</sub>                  | Input high-level threshold | 0.65 × VDDA_WKUP <sup>(1)</sup> |                                 |     | V    |
| V <sub>IL</sub>                  | Input low-level threshold  |                                 | 0.35 × VDDA_WKUP <sup>(1)</sup> |     | V    |
| V <sub>HYS</sub>                 | Input Hysteresis Voltage   | Active Mode                     | 85                              |     | mV   |
|                                  |                            | Bypass Mode                     | 324                             |     | mV   |

(1) VDDSHV stands for corresponding power supply. For WKUP\_OSC0, the corresponding power supply is VDDA\_WKUP. For OSC1\_XI, the corresponding power supply is VDDA\_OSC1.

### 7.6.4 eMMC PHY Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS                         | MIN                           | NOM | MAX                          | UNIT |
|-------------------|-----------------------------------------|-------------------------------|-----|------------------------------|------|
| V <sub>IL</sub>   | Input low-level threshold               |                               |     | 0.35 × VDDSHV <sup>(1)</sup> | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state  |                               |     | 0.20                         | V    |
| V <sub>IH</sub>   | Input high-level threshold              | 0.65 × VDDSHV <sup>(1)</sup>  |     |                              | V    |
| V <sub>IHSS</sub> | Input high-level threshold steady state | 1.4                           |     |                              | V    |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 1.8 V or 0 V |     | ±10                          | μA   |
| I <sub>OZ</sub>   | Tri-state Output Leakage Current        | V <sub>O</sub> = 1.8 V or 0 V |     | ±10                          | μA   |
| R <sub>PU</sub>   | Pull-up Resistor                        | 15                            | 20  | 25                           | kΩ   |
| R <sub>PD</sub>   | Pull-down Resistor                      | 15                            | 20  | 25                           | kΩ   |
| V <sub>OL</sub>   | Output low-level voltage                |                               |     | 0.30                         | V    |
| V <sub>OH</sub>   | Output high-level voltage               | VDDSHV - 0.30 <sup>(1)</sup>  |     |                              | V    |
| I <sub>OL</sub>   | Low Level Output Current                | V <sub>OL(MAX)</sub>          | 2   |                              | mA   |
| I <sub>OH</sub>   | High Level Output Current               | V <sub>OH(MAX)</sub>          | 2   |                              | mA   |



Over operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS | MIN   | NOM | MAX | UNIT |
|-----------------|-----------------|-------|-----|-----|------|
| SR <sub>I</sub> | Input Slew Rate | 5E +8 |     |     | V/s  |

- (1) VDDSHV stands for corresponding power supply (vddshv8). For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column..

### 7.6.5 SDIO Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER         |                                         | TEST CONDITIONS               | MIN                           | NOM | MAX | UNIT |
|-------------------|-----------------------------------------|-------------------------------|-------------------------------|-----|-----|------|
| 1.8-V MODE        |                                         |                               |                               |     |     |      |
| V <sub>IL</sub>   | Input low-level threshold               |                               | 0.58                          |     |     | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state  |                               | 0.58                          |     |     | V    |
| V <sub>IH</sub>   | Input high-level threshold              |                               | 1.27                          |     |     | V    |
| V <sub>IHSS</sub> | Input high-level threshold steady state |                               | 1.7                           |     |     | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage                |                               | 150                           |     |     | mV   |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 1.8 V or 0 V | ±10                           |     |     | μA   |
| R <sub>PU</sub>   | Pull-up Resistor                        |                               | 40                            | 50  | 60  | kΩ   |
| R <sub>PD</sub>   | Pull-down Resistor                      |                               | 40                            | 50  | 60  | kΩ   |
| V <sub>OL</sub>   | Output low-level voltage                |                               | 0.45                          |     |     | V    |
| V <sub>OH</sub>   | Output high-level voltage               |                               | VDDSHV-0.45 <sup>(1)</sup>    |     |     | V    |
| I <sub>OL</sub>   | Low Level Output Current                | V <sub>OL(MAX)</sub>          | 4                             |     |     | mA   |
| I <sub>OH</sub>   | High Level Output Current               | V <sub>OH(MAX)</sub>          | 4                             |     |     | mA   |
| 3.3-V Mode        |                                         |                               |                               |     |     |      |
| V <sub>IL</sub>   | Input low-level threshold               |                               | 0.25 × VDDSHV <sup>(1)</sup>  |     |     | V    |
| V <sub>ILSS</sub> | Input low-level threshold steady state  |                               | 0.15 × VDDSHV <sup>(1)</sup>  |     |     | V    |
| V <sub>IH</sub>   | Input high-level threshold              |                               | 0.625 × VDDSHV <sup>(1)</sup> |     |     | V    |
| V <sub>IHSS</sub> | Input high-level threshold steady state |                               | 0.625 × VDDSHV <sup>(1)</sup> |     |     | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage                |                               | 150                           |     |     | mV   |
| I <sub>IN</sub>   | Input Leakage Current                   | V <sub>I</sub> = 1.8 V or 0 V | ±10                           |     |     | μA   |
| R <sub>PU</sub>   | Pull-up Resistor                        |                               | 40                            | 50  | 60  | kΩ   |
| R <sub>PD</sub>   | Pull-down Resistor                      |                               | 40                            | 50  | 60  | kΩ   |
| V <sub>OL</sub>   | Output low-level voltage                |                               | 0.125 × VDDSHV <sup>(1)</sup> |     |     | V    |
| V <sub>OH</sub>   | Output high-level voltage               |                               | 0.75 × VDDSHV <sup>(1)</sup>  |     |     | V    |
| I <sub>OL</sub>   | Low Level Output Current                | V <sub>OL(MAX)</sub>          | 6                             |     |     | mA   |
| I <sub>OH</sub>   | High Level Output Current               | V <sub>OH(MAX)</sub>          | 10                            |     |     | mA   |

- (1) VDDSHV stands for corresponding power supply (vddshv8). For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column.

### 7.6.6 CSI2/DSI D-PHY Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER                         | MIN                        | NOM | MAX | UNIT |
|-----------------------------------|----------------------------|-----|-----|------|
| <b>Low-Power Receiver (LP-RX)</b> |                            |     |     |      |
| V <sub>IH</sub>                   | Input high-level threshold | 740 |     | mV   |

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                |                                         | MIN | NOM | MAX | UNIT |
|------------------------------------------|-----------------------------------------|-----|-----|-----|------|
| V <sub>IL</sub>                          | Input low-level threshold               |     |     | 550 | mV   |
| V <sub>HYS</sub>                         | Hysteresis                              | 25  |     |     | mV   |
| <b>Ultra-Low Power Receiver (ULP-RX)</b> |                                         |     |     |     |      |
| V <sub>ITH</sub>                         | Input high-level threshold              | 740 |     |     | mV   |
| V <sub>ITL-ULPM</sub>                    | Input low-level threshold               |     |     | 300 | mV   |
| V <sub>HYS</sub>                         | Hysteresis                              | 25  |     |     | mV   |
| <b>High Speed Receiver (HS-RX)</b>       |                                         |     |     |     |      |
| V <sub>IDTH</sub>                        | Differential input high-level threshold |     |     | 40  | mV   |
| V <sub>IDTL</sub>                        | Differential input low-level threshold  | -40 |     |     | mV   |
| V <sub>IDMAX</sub>                       | Maximum differential input voltage      |     |     | 270 | mV   |
| V <sub>ILHS</sub>                        | Single-ended input low-level threshold  | -40 |     |     | mV   |
| V <sub>IHHS</sub>                        | Single-ended input high-level threshold |     |     | 460 | mV   |
| V <sub>CMRXDC</sub>                      | Common-mode voltage                     | 70  |     | 330 | mV   |

### 7.6.7 ADC12B Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER                        |                                        | TEST CONDITIONS                                       | MIN                                                         | TYP         | MAX | UNIT |
|----------------------------------|----------------------------------------|-------------------------------------------------------|-------------------------------------------------------------|-------------|-----|------|
| Analog Input                     |                                        |                                                       |                                                             |             |     |      |
| V <sub>MCU_ADC0/1_AIN[7:0]</sub> | Full-scale Input Range                 |                                                       | VSS                                                         | VDDA_ADC0/1 |     | V    |
| DNL                              | Differential Non-Linearity             |                                                       | -1                                                          | 0.5         | 4   | LSB  |
| INL                              | Integral Non-Linearity                 |                                                       |                                                             | ±1          | ±4  | LSB  |
| LSB <sub>GAIN-ERROR</sub>        | Gain Error                             |                                                       |                                                             | ±2          |     | LSB  |
| LSB <sub>OFFSET-ERROR</sub>      | Offset Error                           |                                                       |                                                             | ±2          |     | LSB  |
| C <sub>IN</sub>                  | Input Sampling Capacitance             |                                                       |                                                             | 5.5         |     | pF   |
| SNR                              | Signal-to-Noise Ratio                  | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale |                                                             | 70          |     | dB   |
| THD                              | Total Harmonic Distortion              | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale |                                                             | 73          |     | dB   |
| SFDR                             | Spurious Free Dynamic Range            | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale |                                                             | 76          |     | dB   |
| SNR <sub>(PLUS)</sub>            | Signal-to-Noise Plus Distortion        | Input Signal: 200 kHz sine wave at -0.5 dB Full Scale |                                                             | 69          |     | dB   |
| R <sub>MCU_ADC0/1_AIN[0:7]</sub> | Input Impedance of MCU_ADC0/1_AIN[7:0] | f = input frequency                                   | $[1/((65.97 \times 10^{-12}) \times f_{\text{SMPL\_CLK}})]$ |             |     | Ω    |
| I <sub>IN</sub>                  | Input Leakage                          | MCU_ADC0/1_AIN[7:0] = VSS                             |                                                             |             | -10 | μA   |
|                                  |                                        | MCU_ADC0/1_AIN[7:0] = VDDA_ADC0/1                     |                                                             |             | 24  | μA   |
| Sampling Dynamics                |                                        |                                                       |                                                             |             |     |      |
| F <sub>SMPL_CLK</sub>            | SMPL_CLK Frequency                     |                                                       |                                                             | 60          |     | MHz  |

Over recommended operating conditions (unless otherwise noted)

| PARAMETER                                       |                                         | TEST CONDITIONS                       | MIN                              | TYP                              | MAX | UNIT                           |
|-------------------------------------------------|-----------------------------------------|---------------------------------------|----------------------------------|----------------------------------|-----|--------------------------------|
| $t_C$                                           | Conversion Time                         |                                       |                                  | 13                               |     | ADC0/1<br>SMPL_CLK<br>K Cycles |
| $t_{ACQ}$                                       | Acquisition time                        |                                       | 2                                |                                  | 257 | ADC0/1<br>SMPL_CLK<br>K Cycles |
| $T_R$                                           | Sampling Rate                           | ADC0/1 SMPL_CLK<br>= 60 MHz           |                                  | 4                                |     | MSPS                           |
| CCISO                                           | Channel to Channel Isolation            |                                       |                                  | 100                              |     | dB                             |
| <b>General Purpose Input Mode<sup>(1)</sup></b> |                                         |                                       |                                  |                                  |     |                                |
| $V_{IL}$                                        | Input low-level threshold               |                                       |                                  | $0.35 \times$<br>VDDA_ADC0/<br>1 |     | V                              |
| $V_{ILSS}$                                      | Input high-level threshold steady state |                                       |                                  | $0.35 \times$<br>VDDA_ADC0/<br>1 |     | V                              |
| $V_{IH}$                                        | Input high-level threshold              |                                       | $0.65 \times$<br>VDDA_ADC0/<br>1 |                                  |     | V                              |
| $V_{IHSS}$                                      | Input high-level threshold steady state |                                       | $0.65 \times$<br>VDDA_ADC0/<br>1 |                                  |     | V                              |
| $V_{HYS}$                                       | Input Hysteresis Voltage                |                                       | 200                              |                                  |     | mV                             |
| $I_{IN}$                                        | Input Leakage Current                   | $V_I = 1.8 \text{ V or } 0 \text{ V}$ |                                  |                                  | 6   | $\mu\text{A}$                  |

(1) MCU\_ADC0/1 can be configured to operate in General Purpose Input mode, where all MCU\_ADC0/1\_AIN[7:0] inputs are globally enabled to operate as digital inputs via the ADC0/1\_CTRL register (gpi\_mode\_en = 1).

### 7.6.8 LVCMOS Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER         |                                 | TEST CONDITIONS                       | MIN                     | TYP                     | MAX      | UNIT          |
|-------------------|---------------------------------|---------------------------------------|-------------------------|-------------------------|----------|---------------|
| <b>1.8-V MODE</b> |                                 |                                       |                         |                         |          |               |
| $V_{IL}$          | Input Low Voltage               |                                       |                         | $0.35 \times VDD^{(1)}$ |          | V             |
| $V_{ILSS}$        | Input Low Voltage Steady State  |                                       |                         | $0.3 \times VDD^{(1)}$  |          | V             |
| $V_{IH}$          | Input High Voltage              |                                       | $0.65 \times VDD^{(1)}$ |                         |          | V             |
| $V_{IHSS}$        | Input High Voltage Steady State |                                       | $0.85 \times VDD^{(1)}$ |                         |          | V             |
| $V_{HYS}$         | Input Hysteresis Voltage        |                                       | 150                     |                         |          | mV            |
| $I_{IN}$          | Input Leakage Current.          | $V_I = 1.8 \text{ V or } 0 \text{ V}$ |                         |                         | $\pm 10$ | $\mu\text{A}$ |
| $R_{PU}$          | Pull-up Resistor                |                                       | 15                      | 22                      | 30       | $k\Omega$     |
| $R_{PD}$          | Pull-down Resistor              |                                       | 15                      | 22                      | 30       | $k\Omega$     |
| $V_{OL}$          | Output Low Voltage              |                                       |                         |                         | 0.45     | V             |
| $V_{OH}$          | Output High Voltage             |                                       | $VDD^{(1)} - 0.45$      |                         |          | V             |
| $I_{OL}$          | Low Level Output Current        | $V_{OL(MAX)}$                         | 3                       |                         |          | mA            |
| $I_{OH}$          | High Level Output Current       | $V_{OH(MIN)}$                         | 3                       |                         |          | mA            |
| <b>3.3-V MODE</b> |                                 |                                       |                         |                         |          |               |
| $V_{IL}$          | Input Low Voltage               |                                       |                         |                         | 0.8      | V             |
| $V_{ILSS}$        | Input Low Voltage Steady State  |                                       |                         |                         | 0.6      | V             |
| $V_{IH}$          | Input High Voltage              |                                       | 2.0                     |                         |          | V             |
| $V_{IHSS}$        | Input High Voltage Steady State |                                       | 2.0                     |                         |          | V             |
| $V_{HYS}$         | Input Hysteresis Voltage        |                                       | 150                     |                         |          | mV            |

Over recommended operating conditions (unless otherwise noted)

| PARAMETER       |                           | TEST CONDITIONS               | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------|-------------------------------|-----|-----|-----|------|
| I <sub>IN</sub> | Input Leakage Current.    | V <sub>I</sub> = 3.3 V or 0 V |     |     | ±10 | μA   |
| R <sub>PU</sub> | Pull-up Resistor          |                               | 15  | 22  | 30  | kΩ   |
| R <sub>PD</sub> | Pull-down Resistor        |                               | 15  | 22  | 30  | kΩ   |
| V <sub>OL</sub> | Output Low Voltage        |                               |     |     | 0.4 | V    |
| V <sub>OH</sub> | Output High Voltage       |                               | 2.4 |     |     | V    |
| I <sub>OL</sub> | Low Level Output Current  | V <sub>OL(MAX)</sub>          | 5   |     |     | mA   |
| I <sub>OH</sub> | High Level Output Current | V <sub>OH(MIN)</sub>          | 6   |     |     | mA   |

- (1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see the *Pin Attributes*, POWER column.

### 7.6.9 USB2PHY Electrical Characteristics

#### 备注

USB0 and USB1 Electrical Characteristics are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

### 7.6.10 SerDes 2-L-PHY/4-L-PHY Electrical Characteristics

#### 备注

The PCIe interfaces are compliant with the electrical parameters specified in PCI Express® Base Specification Revision 4.0, September 27, 2017.

This Device imposes an additional limit on SERDES REFCLK when used in Input mode with internal termination enabled, as described by parameter V<sub>REFCLK\_TERM</sub> in 表 7-2, 4-L-PHY SERDES REFCLK Electrical Characteristics. Internal termination is enabled by default and must be disabled before applying a reference clock signal that exceeds the limits defined by V<sub>REFCLK\_TERM</sub>. External termination should always be enabled on the source side.

**表 7-2. 4-L-PHY SERDES REFCLK Electrical Characteristics**

Only applies when internal termination is enabled. Over recommended operating conditions (unless otherwise noted)

| PARAMETER                |                                                                                                | MIN | TYP | MAX  | UNIT |
|--------------------------|------------------------------------------------------------------------------------------------|-----|-----|------|------|
| V <sub>REFCLK_TERM</sub> | Single ended voltage threshold at the reference clock pin when internal termination is enabled |     |     | 400  | mV   |
| R <sub>TERM</sub>        | Internal termination                                                                           | 40  | 50  | 62.5 | Ω    |

#### 备注

The SerDes USB interfaces are compliant with the USB3.1 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the Universal Serial Bus 3.1 Specification, Revision 1.0, July 26, 2013.

#### 备注

The SGMII interfaces electrical characteristics are compliant with 1000BASE-KX per IEEE802.3 Clause 70.

## 备注

The SGMII 2.5G / XAUI interfaces electrical characteristics are compliant with IEEE802.3 Clause 47.

## 备注

The QSGMII interface electrical characteristics are compliant with QSGMII Specification revision 1.2.

## 备注

The UFS interface electrical characteristics are compliant with MIPI M-PHY Specification v3.1, February 17, 2014.

## 备注

The DP interface electrical characteristics are compliant with the VESA DisplayPort (DP) Standard v 1.4 February 23, 2016.

## 备注

The eDP interface electrical characteristics are compliant with the VESA Embedded DisplayPort (eDP) Standard v1.4b October 23, 2015.

### 7.6.13 DDR0 Electrical Characteristics

## 备注

The DDR interface is compatible with JESD209-4B standard compliant LPDDR4 SDRAM devices.

## 7.7 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for High-Security Devices.

### 7.7.1 Recommended Operating Conditions for OTP eFuse Programming

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION                                                                         | MIN                                                  | NOM | MAX  | UNIT |
|-----------|-------------------------------------------------------------------------------------|------------------------------------------------------|-----|------|------|
| VDD_CORE  | Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)       | See <a href="#">Recommended Operating Conditions</a> |     |      | V    |
| VDD_MCU   | Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)       | See <a href="#">Recommended Operating Conditions</a> |     |      | V    |
| VPP_CORE  | Supply voltage range for the eFuse ROM domain during normal operation               | N/A <sup>(2)</sup>                                   |     |      |      |
|           | Supply voltage range for the eFuse ROM domain during OTP programming <sup>(1)</sup> | 1.71                                                 | 1.8 | 1.89 | V    |
| VPP_MCU   | Supply voltage range for the eFuse ROM domain during normal operation               | N/A <sup>(2)</sup>                                   |     |      |      |
|           | Supply voltage range for the eFuse ROM domain during OTP programming <sup>(1)</sup> | 1.71                                                 | 1.8 | 1.89 | V    |

(1) Supply voltage range includes DC errors and peak-to-peak noise. TI power management solutions [TLV70018-Q1](#) from the TLV707x family meet the supply voltage range needed for VPP\_CORE and VPP\_MCU.

(2) N/A stands for Not Applicable.

### 7.7.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP\_CORE and VPP\_MCU power supplies must be disabled when not programming OTP registers.
- The VPP\_CORE and VPP\_MCU power supplies must be ramped up after the proper device power-up sequence (for more details, see *Power Supply Sequencing*).

### 7.7.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP\_CORE and VPP\_MCU terminals during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP\_CORE and VPP\_MCU terminals according to the specification in [节 7.7.1](#).
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP\_CORE and VPP\_MCU terminals.

### 7.7.4 Impact to Your Hardware Warranty

You recognize and accept at your own risk that your use of eFuse permanently alters the TI device. You acknowledge that eFuse can fail due to incorrect operating conditions or programming sequence. Such a failure may render the TI device inoperable and TI will be unable to confirm the TI device conformed to TI device specifications prior to the attempted eFuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY FOR ANY TI DEVICES THAT HAVE BEEN eFUSED.

## 7.8 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the  $T_J$  value identified in [Recommended Operating Conditions](#).

### 7.8.1 Thermal Resistance Characteristics for ALY Package

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

| NO. | PARAMETER         | DESCRIPTION             | ALY PACKAGE                           |                                  |
|-----|-------------------|-------------------------|---------------------------------------|----------------------------------|
|     |                   |                         | $^{\circ}\text{C}/\text{W}^{(1) (3)}$ | AIR FLOW<br>(m/s) <sup>(2)</sup> |
| T1  | $R_{\Theta_{JC}}$ | Junction-to-case        | 0.11                                  | N/A                              |
| T2  | $R_{\Theta_{JB}}$ | Junction-to-board       | 1.6                                   | N/A                              |
| T3  | $R_{\Theta_{JA}}$ | Junction-to-free air    | 8.3                                   | 0                                |
| T4  |                   | Junction-to-moving air  | 4.7                                   | 1                                |
| T5  |                   |                         | 3.9                                   | 2                                |
| T7  | $\Psi_{JT}$       | Junction-to-package top | 0.1                                   | 0                                |
| T8  |                   |                         | 0.1                                   | 1                                |
| T9  |                   |                         | 0.1                                   | 2                                |
| T11 | $\Psi_{JB}$       | Junction-to-board       | 1.3                                   | 0                                |
| T12 |                   |                         | 1.1                                   | 1                                |
| T13 |                   |                         | 1.0                                   | 2                                |

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the  $\Theta_{JC}$  [ $R_{\Theta_{JC}}$ ] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.

(3)  $^{\circ}\text{C}/\text{W}$  = degrees Celsius per watt.

## 7.9 Temperature Sensor Characteristics

This section summarizes the Voltage and Temperature Module (VTM) on die temperature sensor characteristics.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the  $T_J$  value identified in the [Recommended Operating Conditions](#).

**表 7-3. VTM Die Temperature sensor Characteristics**

| PARAMETER |                                 | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---------------------------------|-----------------|-----|-----|-----|------|
| $T_{acc}$ | VTM temperature sensor accuracy | - 40 to 110 °C  | - 5 |     | 5   | °C   |
|           |                                 | 110 to 125 °C   | - 2 |     | 2   | °C   |



## 7.10 Timing and Switching Characteristics

### 备注

The timings presented in this section are valid when the DRV\_STR (Drive Strength) control in the associated PADCONFIG registers are set to the default “0h - Nominal (recommended)” value.

### 7.10.1 Timing Parameters and Information

The timing parameter symbols used in [Timing and Switching Characteristics](#) are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in [表 7-4](#):

表 7-4. Timing Parameters Subscripts

| SYMBOL | PARAMETER                              |
|--------|----------------------------------------|
| c      | Cycle time (period)                    |
| d      | Delay time                             |
| dis    | Disable time                           |
| en     | Enable time                            |
| h      | Hold time                              |
| su     | Setup time                             |
| START  | Start bit                              |
| t      | Transition time                        |
| v      | Valid time                             |
| w      | Pulse duration (width)                 |
| X      | Unknown, changing, or don't care level |
| F      | Fall time                              |
| H      | High                                   |
| L      | Low                                    |
| R      | Rise time                              |
| V      | Valid                                  |
| IV     | Invalid                                |
| AE     | Active Edge                            |
| FE     | First Edge                             |
| LE     | Last Edge                              |
| Z      | High impedance                         |

## 7.10.2 Power Supply Sequencing

This section describes power supply sequencing required to ensure proper device operation. The device can be operated using either an isolated or combined MCU & Main power distribution network (PDN). Two different primary power sequences are recommended based upon isolated and combined MCU & Main PDNs. In addition, the device can be operated in either MCU Only or DDR Retention or GPIO Retention low power modes. Two different desired device power supply sequences for entry and exit of low power modes are shown.

The power supply names used in this section are specific to this device and align to names given in the Signal Descriptions section. Common power supply names may be used across different devices within the Jacinto 7™ processor family. These common supply names will have very similar if not identical functions across devices.

All power sequencing timing diagrams shown will use the following terminology:

- Primary = Essential power sequences of all voltage domains between off and full active states.
- $V_{OPR\ MIN}$  = Minimum operational voltage level that ensures functionality as specified in Recommended Operating Conditions
- Ramp-up = start of a voltage supply transition time from off condition to  $V_{opr\ min}$ .
- Ramp-down = start of a voltage supply transition time from  $V_{opr}$  to off condition
- Supply\_ “n” = multiple instances of similar power supplies (i.e.  $VDDSHVn = VDDSHV0, VDDSHV1, VDDSHV2 \dots VDDSHV6$ )
- Supply\_ “xxx” = multiple instances of similar power supplies used for different signal types (i.e.  $VDDA\_1P8\_xxx = VDDA\_1P8\_DSITX, VDDA\_1P8\_USB, VDDA\_0P8\_DSITX, VDDA\_0P8\_USB, \text{etc.}$ )
- Time stamps = “T#” markers with descriptions and approximate elapsed times for general reference. Specific timing transitions are dependent upon PDN design (see PDN User Guide for details).

### 7.10.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 100 mV/us, as shown in 图 7-2. For instance, a 1.8V supply should have a ramp time  $> 18\ \mu s$  to ensure the slew rate  $< 100\text{mV/us}$ .

图 7-2 describes the Power Supply Slew Rate Requirement in the device.

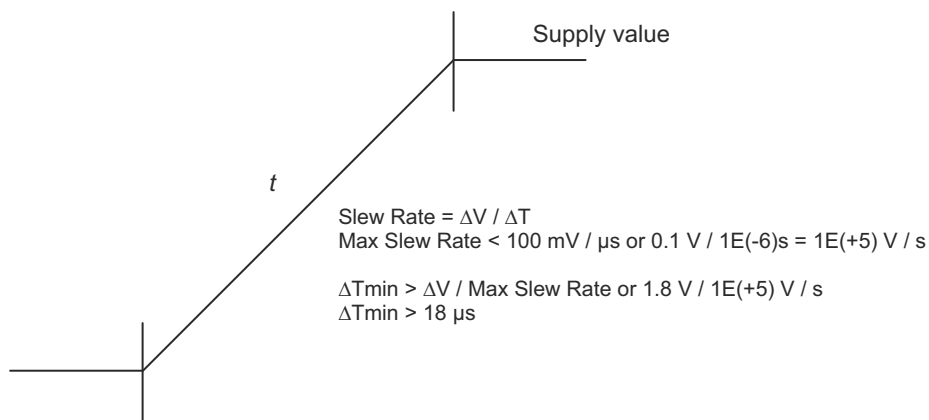
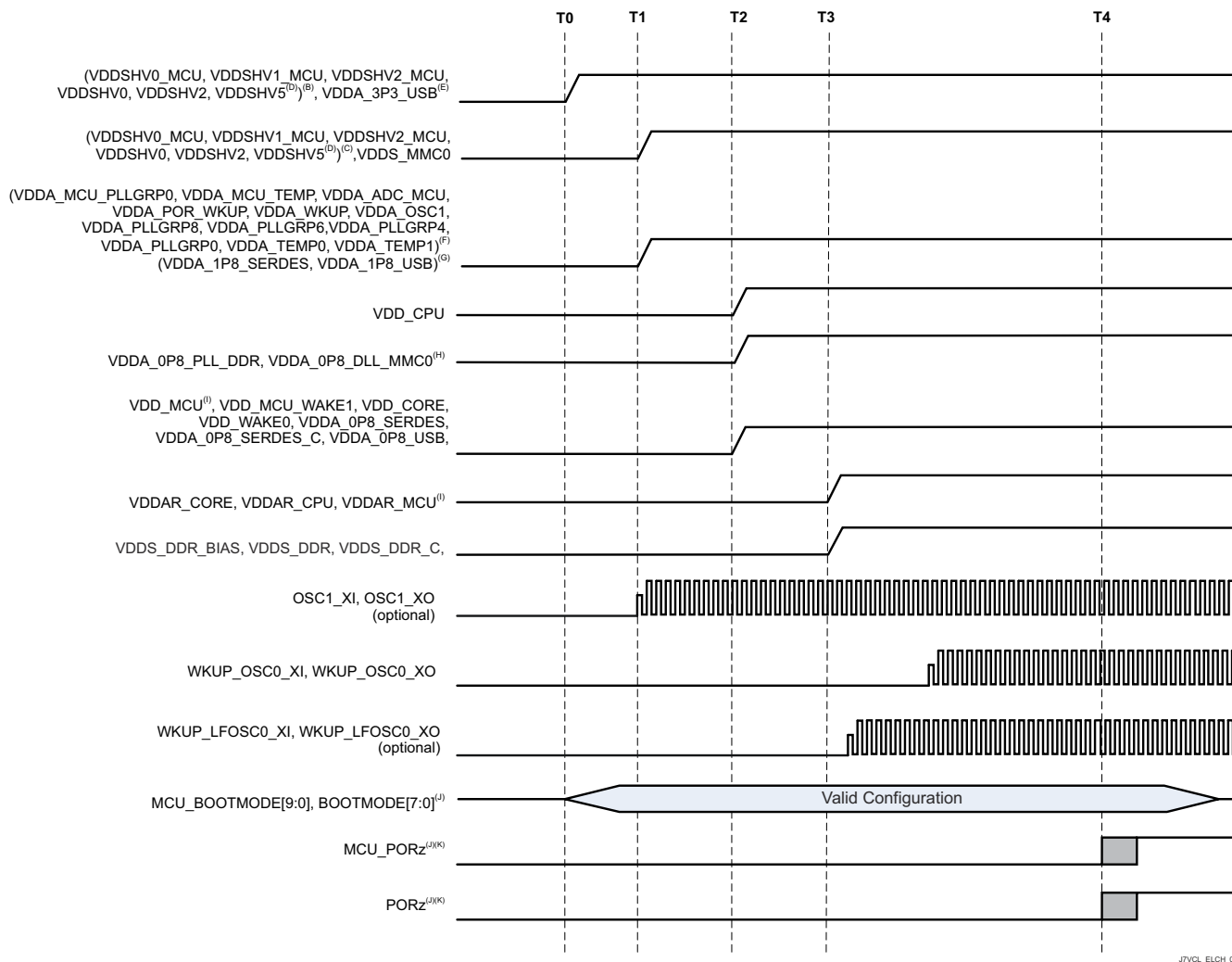


图 7-2. Power Supply Slew and Slew Rate

### 7.10.2.2 Combined MCU and Main Domains Power- Up Sequencing

节 7.10.2.2 describes the primary power-up sequencing when similar MCU and Main voltage domains are combined into common power rails. Combining MCU and Main voltage domains simplifies PDN design by reducing total number of power rails and sources while making MCU and Main processor sub-systems operational dependent on common power rails.



J7VCL\_ELCH\_01

#### A. Time stamp markers:

- T0 - 3.3V voltages start ramp-up to  $V_{OPR\ MIN}$ . (0 ms)
- T1 - 1.8-V voltages start ramp-up to  $V_{OPR\ MIN}$ . (2 ms)
- T2 - Low voltage core supplies start ramp-up to  $V_{OPR\ MIN}$ . (3 ms)
- T3 - Low voltage RAM array voltages start ramp-up to  $V_{OPR\ MIN}$ . (4 ms)
- T4 - OSC1 is stable and PORz/MCU\_PORz are de-asserted to release processor from reset. (13 ms)

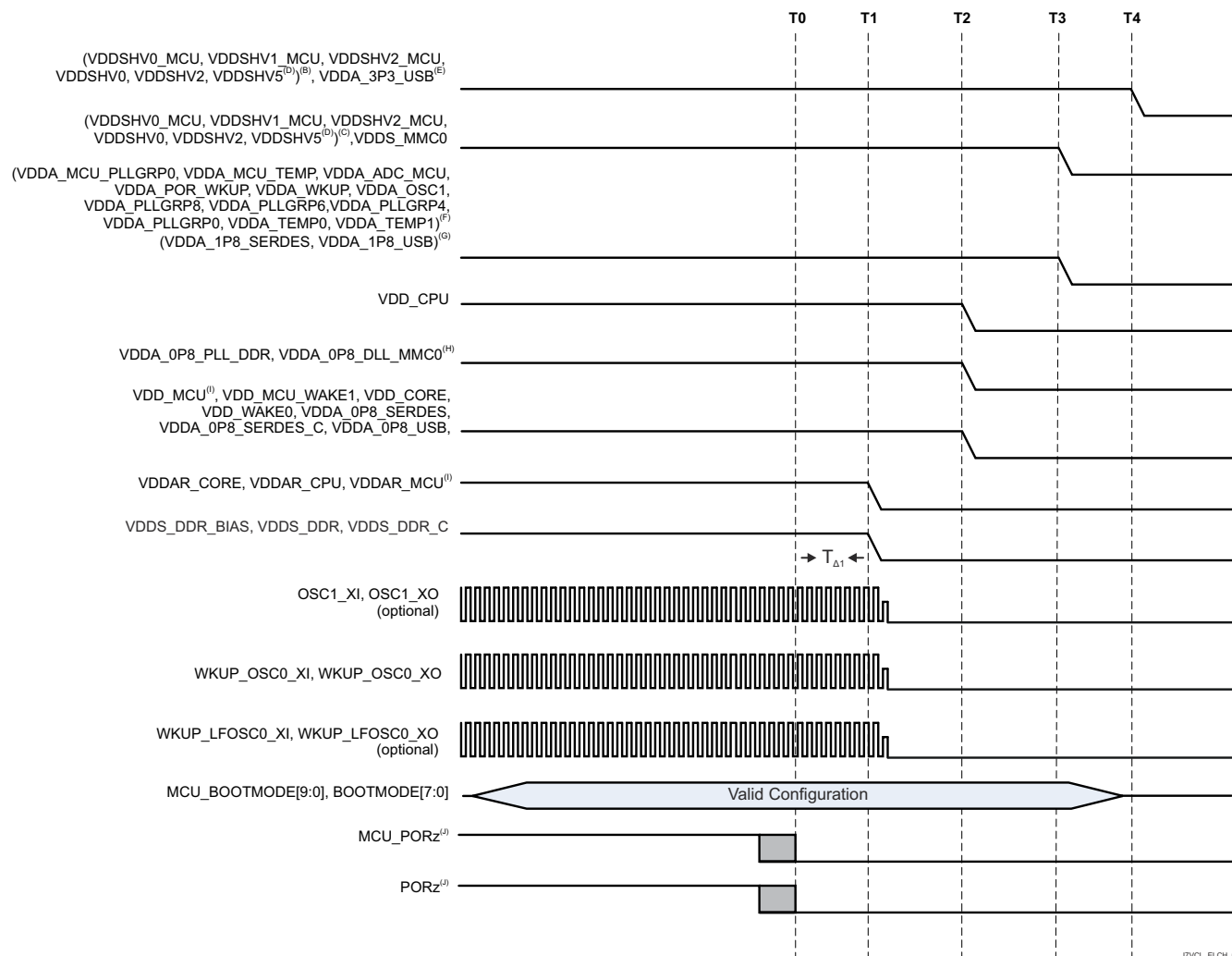
- B. Any MCU or Main dual voltage IO supplies (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces. A few supplies could have varying start times between T0 to T1 due to PDN designs using different power resources with varying turn-on & ramp-up time delays.
- C. Any MCU or Main dual voltage IO supplies (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces. When eMMC memories are used, Main 1.8-V supplies could have a ramp-up aligned to T3 due to PDN designs grouping supplies with VDD\_MMC0.
- D. VDDSHV5 supports MMC1 signaling for SD memory cards. If compliant high-speed SD card operation is needed, then an independent, dual voltage (3.3 V/1.8 V) power source and rail are required. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as

- shown. If SD card is not needed or standard data rates with fixed 3.3 V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then domain can be grouped with digital IO 1.8-V power rail.
- E. VDDA\_3P3\_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.
  - F. VDDA\_1P8\_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
  - G. VDDA\_1P8\_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
  - H. VDDA\_0P8\_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
  - I. VDD\_MCU is a digital voltage domain with a wide range enabling it to be grouped and ramped-up with either 0.8-V VDD\_CORE or 0.85-V RAM array (VDDAR\_xxx) domains.
  - J. Minimum set-up and hold times shown with respect to MCU\_PORz and PORz asserting high to latch MCU\_BOOTMODEn (referenced to MCU\_VDDSHV0) and BOOTMODEn (reference to VDDSHV2) settings into registers during power up sequence.
  - K. Minimum elapsed time from crystal oscillator circuitry being energized (VDDA\_OSC1 at T1) until stable clock frequency is reached depends upon on crystal oscillator, capacitor parameters and PCB parasitic values. A conservative 10 ms elapsed time defined by (T4 - T1) time stamps is shown. This could be reduced depending upon customer's clock circuit (that is, crystal oscillator or clock generator) and PCB designs.

**图 7-3. Combined MCU and Main Domains, Primary Power-Up Sequence**

### 7.10.2.3 Combined MCU and Main Domains Power- Down Sequencing

图 7-4 describes the device power-down sequencing.



#### A. Time stamp markers:

- T0 - MCU\_PORz & PORz assert low to put all processor resources in safe state. (0 ms)
- T1 - Main DDR, SRAM Core, and SRAM CPU power supplies start ramp-down. (0.5 ms)
- T2 - Low voltage core supplies start supply ramp-down. (2.5 ms)
- T3 - 1.8-V voltages start supply ramp-down. (3.0 ms)
- T4 - 3.3V voltages start supply ramp-down. (3.5 ms)

- B. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3 V to support 3.3-V digital interfaces.
- C. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces.
- D. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3 V/1.8 V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed 3.3-V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then domain can be grouped with digital IO 1.8-V power rail.
- E. VDDA\_3P3\_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.
- F. VDDA\_1P8\_<clk/pll/ana> are 1.8V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency

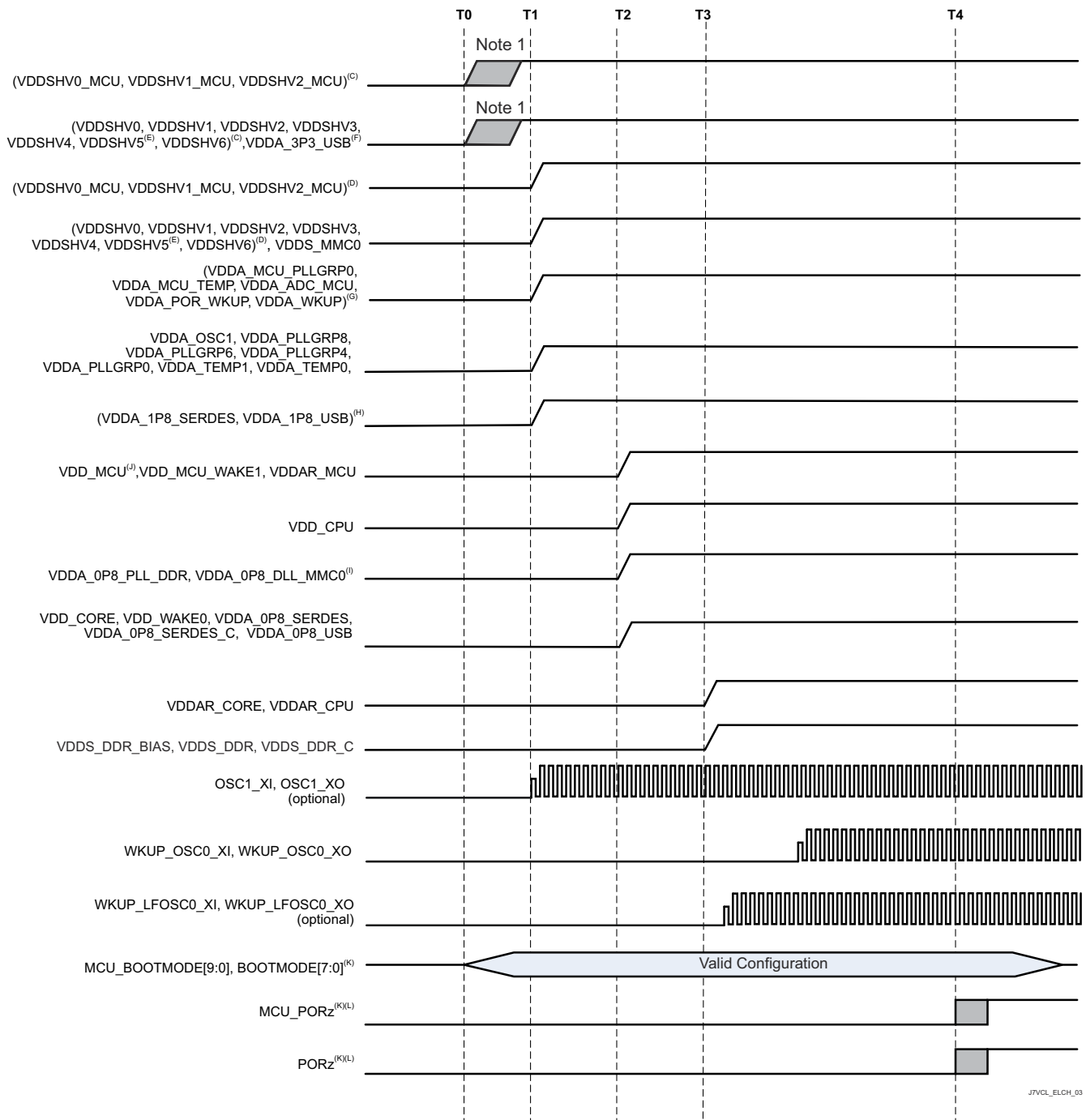
switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required .

- G. VDDA\_1P8\_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
- H. VDDA\_0P8\_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- I. VDD\_MCU is a digital voltage domain with a wide range enabling it to be grouped and ramped-up with either 0.8-V VDD\_CORE or 0.85-V RAM array (VDDAR\_xxx) domains.
- J. MCU\_PORz and PORz must be asserted low for  $T_{\Delta 1} = 200 \text{ us MIN}$  to ensure SoC resources enter into safe state before any voltage begins to ramp down.

**图 7-4. Combined MCU and Main Domains, Primary Power-Down Sequence**

#### 7.10.2.4 Isolated MCU and Main Domains Power- Up Sequencing

Isolated MCU and Main voltage domains enable an SoC's MCU and Main processor sub-systems to operate independently. There are 2 reasons an SoC's PDN design may need to support independent MCU and Main processor functionality. First is to provide flexibility to enable SoC low power modes that can significantly reduce SoC power dissipation when processor operations are not needed. Second is to enable robustness to gain freedom from interference (FFI) of a single fault impacting both MCU and Main processor sub-systems which is especially beneficial if using the SoC's MCU as the system safety monitoring processor. The number of additional PDN power rails needed is dependent upon number of different MCU IO signaling voltage levels. If only 1.8V IO signaling is used, then only 2 additional power rails could be required. If both 1.8 and 3.3V IO signaling is desired, then 4 additional power rails could be needed.



A. T1Time stamp markers:

- T0 - All 3.3-V voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (0 ms)
- T1 - All 1.8-V voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (2 ms)
- T2 - All core voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (3 ms)
- T3 - All RAM array voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (4 ms)
- T4 - OSC1 is stable and PORz/MCU\_PORz are de-asserted to release processor from reset. (13 ms)

- B. Any MCU or Main dual voltage IO supplies (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3 V to support 3.3-V digital interfaces. A few supplies could have varying start times between T0 to T1 due to PDN designs using different power resources with varying turn-on & ramp-up time delays.

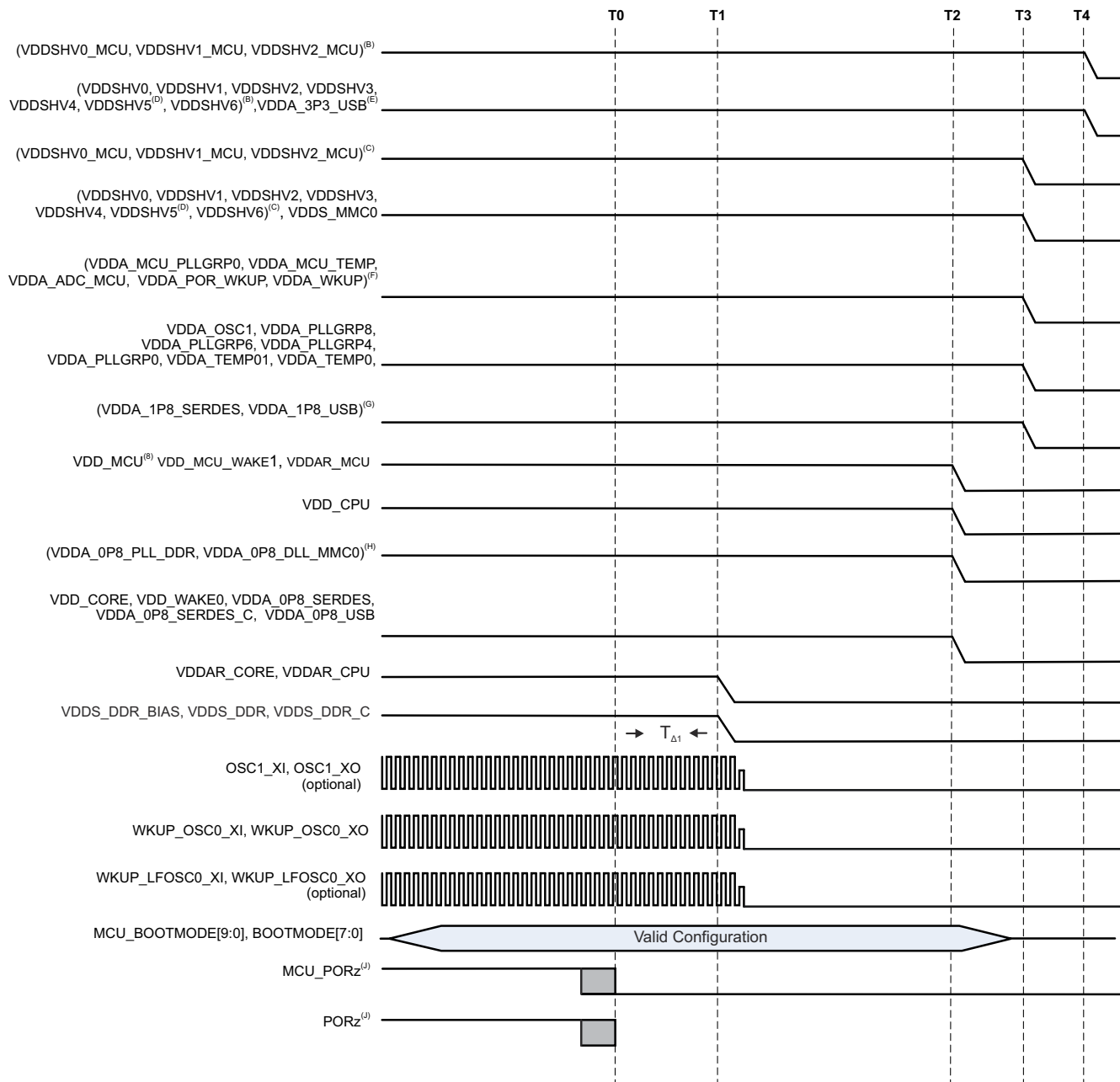


- C. Any MCU or Main dual voltage IO supplies (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces. When eMMC memories are used, Main 1.8-V supplies could have delayed start times that aligns to T3 due to PDN designs grouping supplies with VDD\_MMC0.
- D. VDDSHV5 supports MMC1 signaling for SD memory cards. If compliant UHS-I SD card operation is needed, then an independent, dual voltage (3.3 V/1.8 V) power source and rail are required. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If SD card is not needed or standard data rates with fixed 3.3-V operation is acceptable, then supply can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then supply can be grouped with digital IO 1.8-V power rail.
- E. VDDA\_3P3\_USB is 3.3-V analog supply used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-up to 3.3 V will be same as other 3.3-V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then supply can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.
- F. VDDA\_1P8\_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
- G. VDDA\_1P8\_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
- H. VDDA\_0P8\_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- I. VDD\_MCU is a digital voltage supply with a wide operational voltage range and power sequencing flexibility, enabling it to be grouped and ramped-up with either 0.8-V VDD\_CORE at time stamp T2 or 0.85-V RAM array domains (VDDAR\_xxx) at time stamp T3.
- J. Minimum set-up and hold times shown with respect to MCU\_PORz and PORz asserting high to latch MCU\_BOOTMODEn (referenced to MCU\_VDDSHV0) and BOOTMODEn (reference to VDDSHV2) settings into registers during power up sequence.
- K. Minimum elapsed time from crystal oscillator circuitry being energized (VDDA\_OSC1 at T1) until stable clock frequency is reached depends upon on crystal oscillator, capacitor parameters and PCB parasitic values. A conservative 10 ms elapsed time defined by (T4 - T1) time stamps is shown. This could be reduced depending upon customer's clock circuit (that is, crystal oscillator or clock generator) and PCB designs.

**图 7-5. Isolated MCU and Main Domains, Primary Power-Up Sequence**

### 7.10.2.5 Isolated MCU and Main Domains Power- Down Sequencing

图 7-6 describes the device power-down sequencing.



J7VCL\_ELCH\_04

#### A. Time stamp markers:

- T0 - MCU\_PORz and PORz assert low to put all processor resources in safe state. (0 ms)
- T1 - Main DDR, SRAM Core, and SRAM CPU power domains start ramp-down. (0.5 ms)
- T2 - All core voltages start supply ramp-down. (2.5 ms)
- T3 - All 1.8V voltages start supply ramp-down. (3.0 ms)
- T4 - All 3.3V voltages start supply ramp-down. (3.5 ms)

#### B. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3 V to support 3.3-V digital interfaces.

- C. Any MCU or Main dual voltage IO supplies (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces. When eMMC memories are used, Main 1.8-V supplies could have a ramp-down aligned to T1 due to PDN designs grouping supplies with VDD\_MMC0.
- D. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3 V/1.8 V) power rail is required for compliant, high-speed SD card operations. If compliant high-speed SD card operation is needed, then an independent, dual voltage (3.3 V/1.8 V) power source and rail are required. The start of ramp-down from 3.3 V/1.8 V will be same as other 3.3-V domains as shown. If SD card is not needed or standard data rates with fixed 3.3-V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then domain can be grouped with digital IO 1.8-V power rail.
- E. VDDA\_3P3\_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-down from 3.3 V will be same as other 3.3-V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.
- F. VDDA\_1P8\_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
- G. VDDA\_1P8\_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
- H. VDDA\_0P8\_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- I. VDD\_MCU is a digital voltage domain with a wide range enabling it to be grouped and ramped-up with either 0.8-V VDD\_CORE or 0.85V RAM array (VDDAR\_XXX) domains.
- J. MCU\_PORz and PORz must be asserted low for  $T_{\Delta 1} = 200 \text{ us MIN}$  to ensure SoC resources enter into safe state before any voltage begins to ramp down.

**图 7-6. Isolated MCU and Main Domains, Primary Power- Down Sequencing**

#### **7.10.2.6 Independent MCU and Main Domains, Entry and Exit of MCU Only Sequencing**

Entry into MCU Only state is accomplished by executing a power down sequence except for the 4 MCU domains that remain energized. Exit from MCU Only state is accomplished by executing a power up sequence with the 4 MCU domains remaining energized throughout the seque.

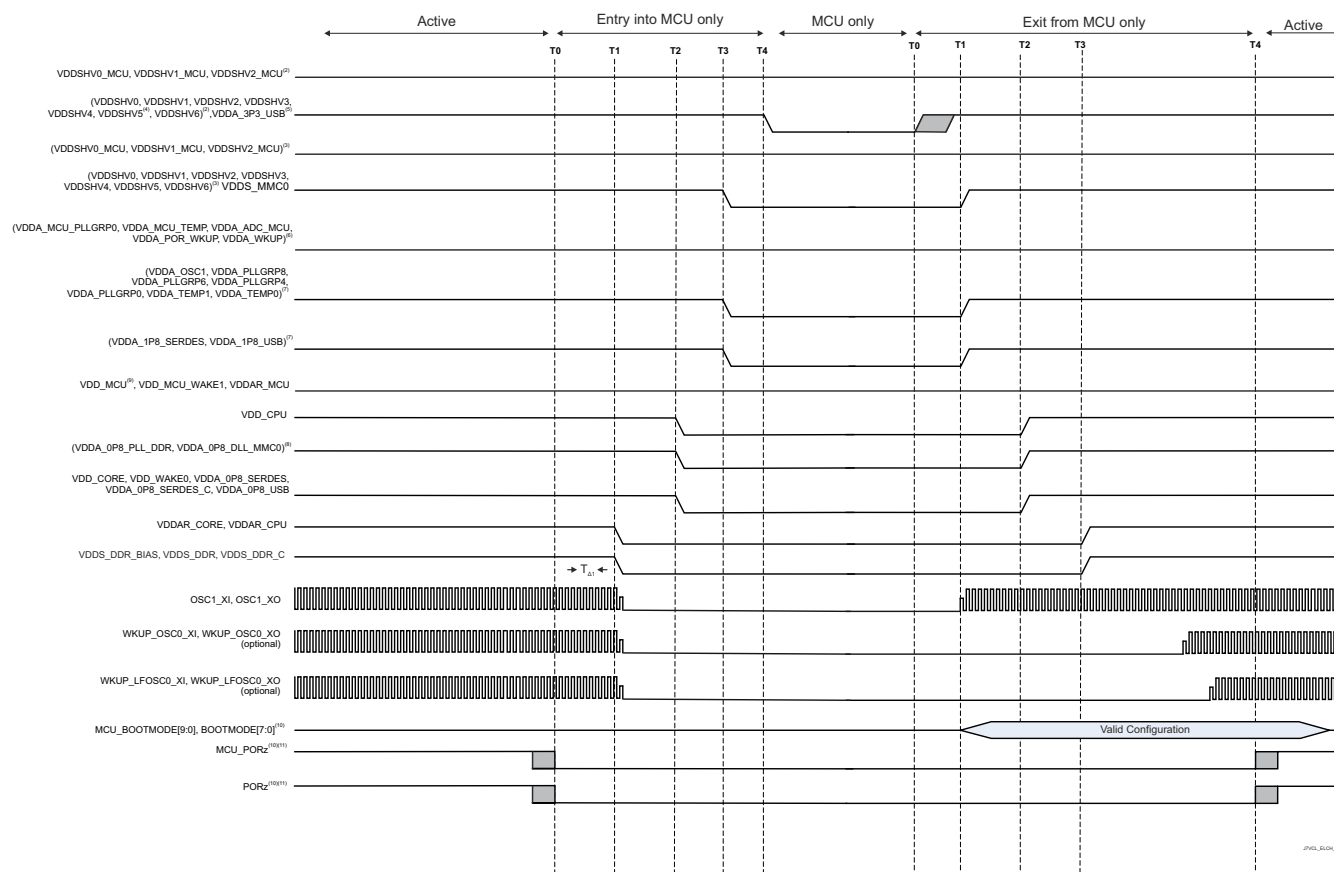


图 7-7. Independent MCU and Main Domains, Entry and Exit of MCU Only Sequencing

### 7.10.2.7 Independent MCU and Main Domains, Entry and Exit of DDR Retention State

Entry into DDR Retention state is accomplished by executing a power down sequence except for the 4 DDR domains that remain energized. Exit from DDR Retention state is accomplished by executing a power up sequence with the 3 DDR domains remaining energized throughout the sequence.

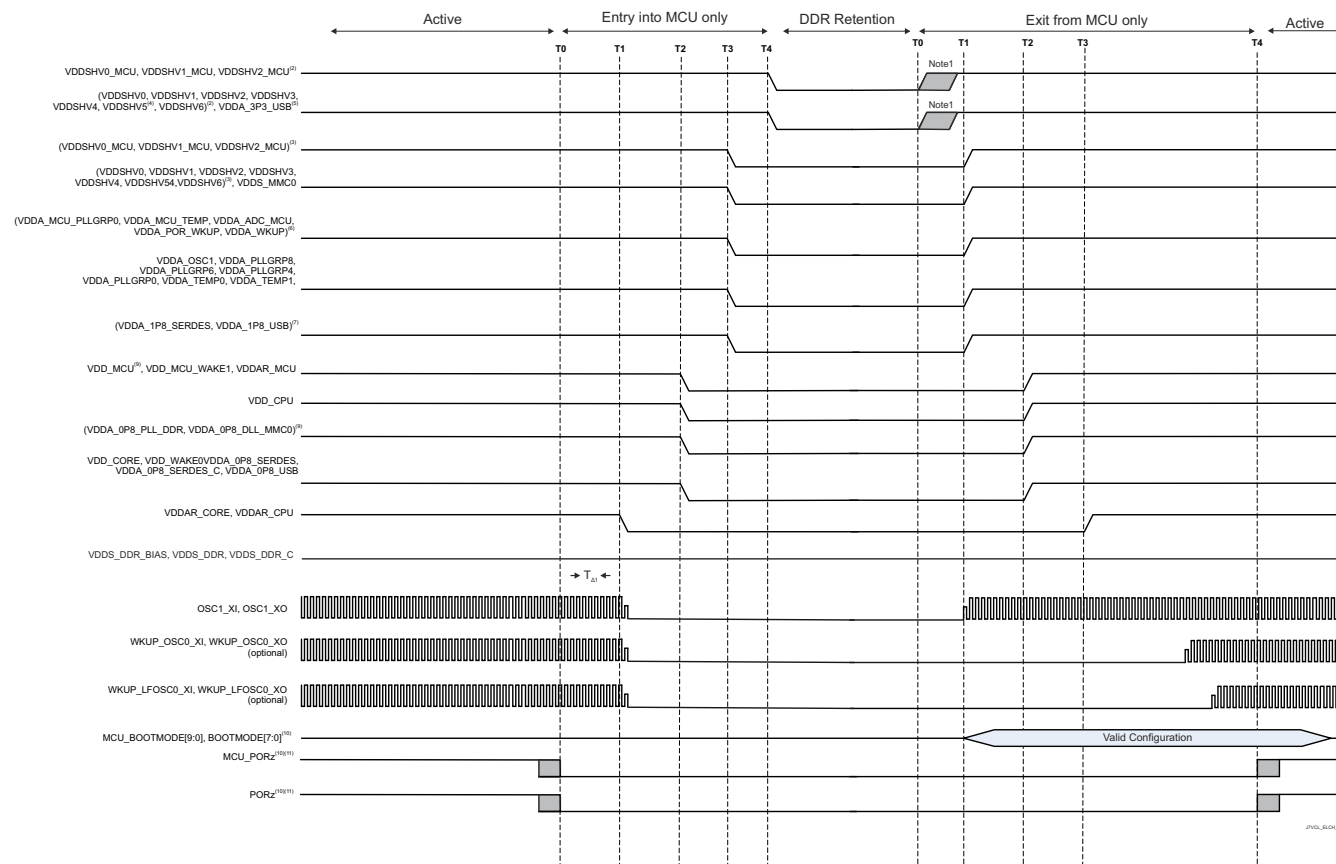


图 7-8. Independent MCU and Main Domains, Entry and Exit of DDR Retention State

### 7.10.2.8 Independent MCU and Main Domains, Entry and Exit of GPIO Retention Sequencing

Entry into GPIO Retention state is accomplished by executing a power down sequence except for the 2 or 4 wake domains that remain energized. Exit from GPIO Retention state is accomplished by executing a power up sequence with the 2 or 4 wake DDR domains remaining energized throughout the sequence.

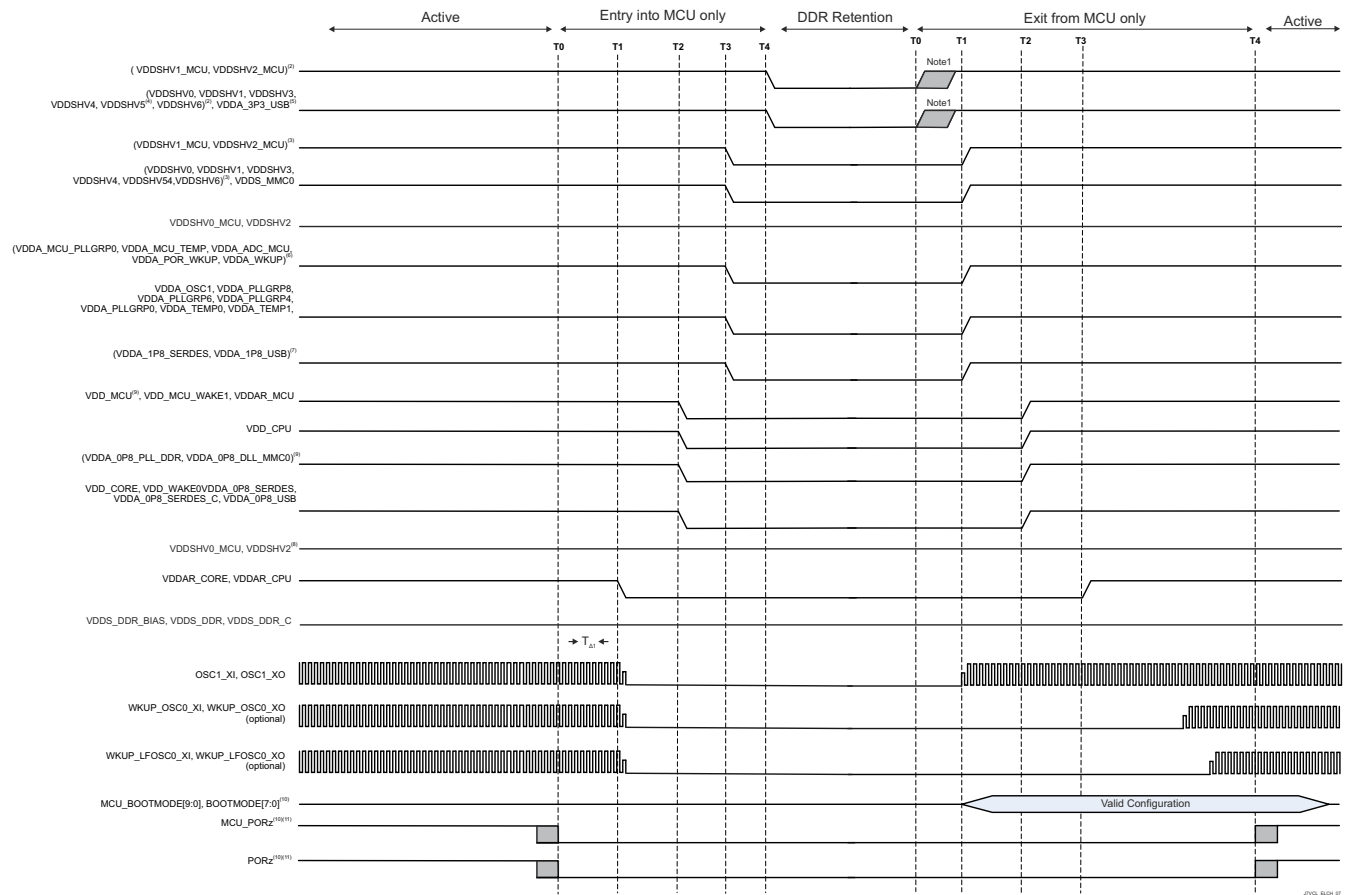


图 7-9. Independent MCU and Main Domains, Entry and Exit of GPIO Retention Sequencing

### 7.10.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

表 7-5. System Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.5 | 2   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 3   | 30  | pF   |

#### 7.10.3.1 Reset Timing

The tables and figures provided in this section define the timing requirements and switching characteristics for reset related signals.

表 7-6. MCU\_PORz Timing Requirements

see 图 7-10

| NO.  |                                                 |                                                                                                                                                              | MIN                     | TYP     | MAX | UNIT |
|------|-------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|---------|-----|------|
| RST1 |                                                 | Hold time, MCU_PORz active (low) at Power-up after all MCU DOMAIN supplies valid (using external crystal)                                                    | N + 1200 <sup>(2)</sup> | 9500000 |     | ns   |
| RST2 | t <sub>h</sub> (MCUD_SUPPLIES_VALID - MCU_PORz) | Hold time, MCU_PORz active (low) at Power-up after all MCU DOMAIN supplies <sup>(1)</sup> valid and external clock stable (using external LVCMOS oscillator) | 1200                    |         |     | ns   |
| RST3 | t <sub>w</sub> (MCU_PORzL)                      | Pulse Width minimum, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)                                         | 1200                    |         |     | ns   |

(1) For the definition of the MCU DOMAIN supplies, see the 节 7.10.2.2, *Combined MCU and Main Domains Poewr-Up Sequencing*.

(2) N = oscillator start-up time

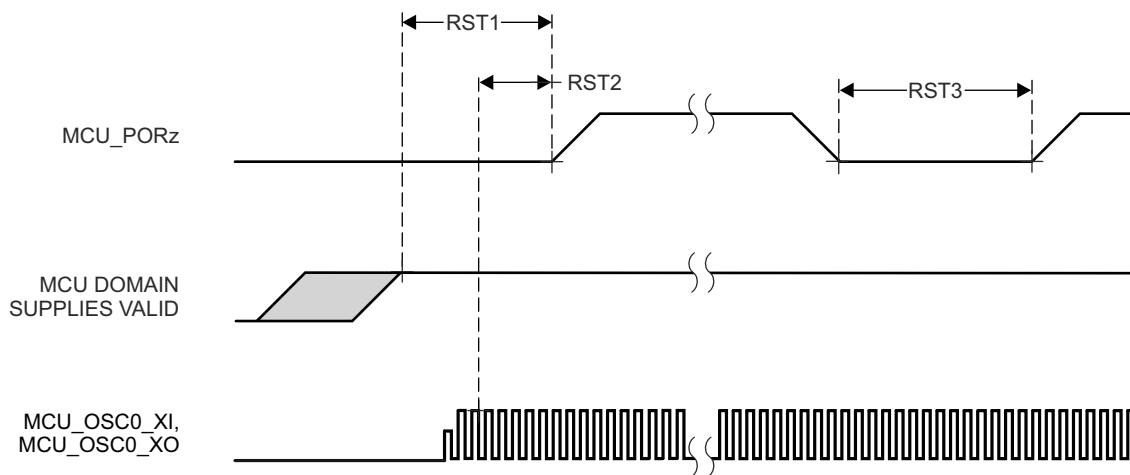


图 7-10. MCU\_PORz Timing Requirements

**表 7-7. PORz Timing Requirements**

see 图 7-11

| NO.  |                                       |                                                                                              | MIN  | MAX | UNIT |
|------|---------------------------------------|----------------------------------------------------------------------------------------------|------|-----|------|
| RST4 | $t_{h(MAIN\_SUPPLIES\_VALID - PORz)}$ | Hold time, PORz active (low) at Power-up after all MAIN DOMAIN supplies <sup>(1)</sup> valid | 1200 |     | ns   |
| RST5 | $t_{w(PORzL)}$                        | Pulse Width minimum, PORz low after Power-up                                                 | 1200 |     | ns   |

(1) For the definition of the MAIN DOMAIN supplies, see the 节 7.10.2.2, Combined MCU and Main Domains Poewr-Up Sequencing.

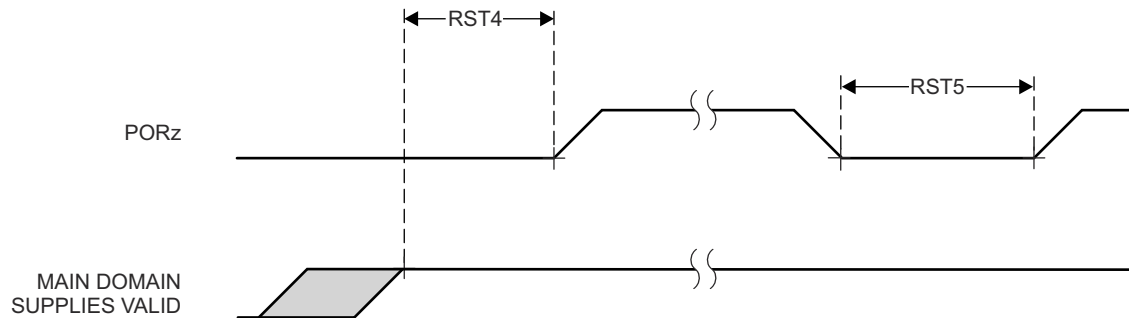


**图 7-11. PORz Timing Requirements**

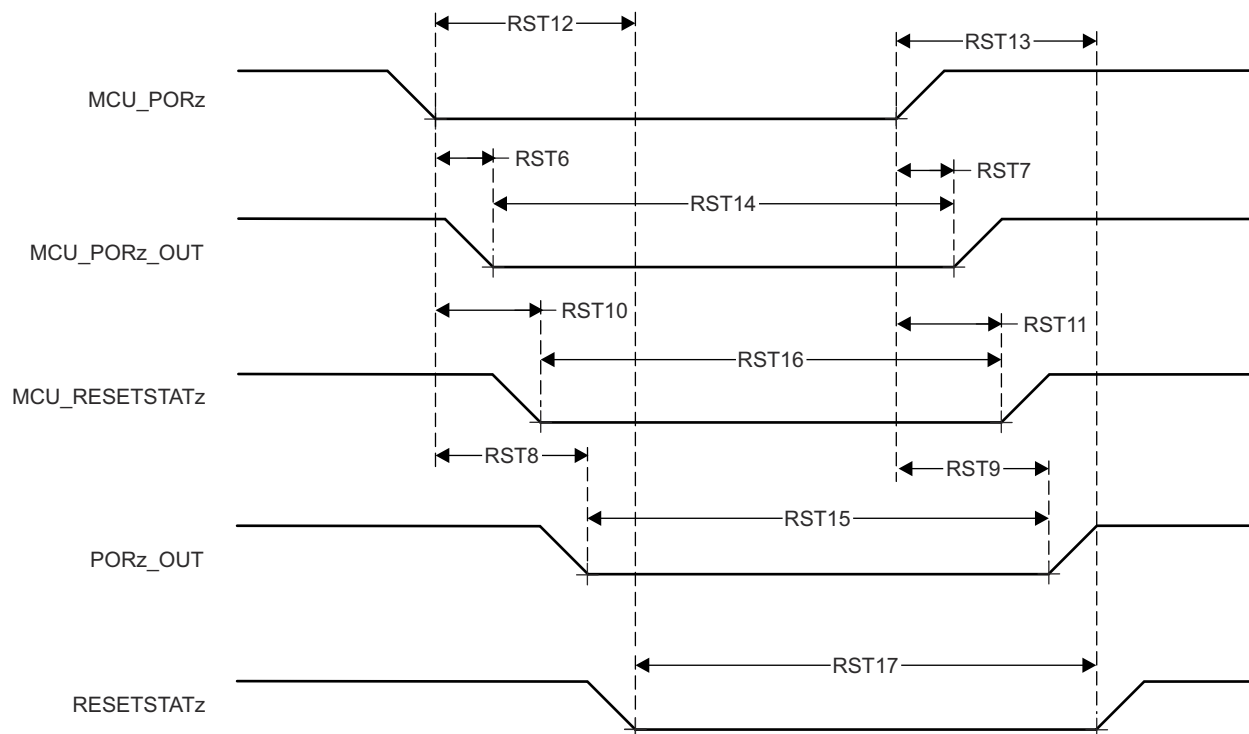
**表 7-8. MCU\_PORz initiates; MCU\_PORz\_OUT, PORz\_OUT, MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**

see 图 7-12

| NO.   | PARAMETER                          | MODE                                                                   | MIN                   | MAX                    | UNIT |
|-------|------------------------------------|------------------------------------------------------------------------|-----------------------|------------------------|------|
| RST6  | $t_d(MCU\_PORzL-MCU\_PORz\_OUTL)$  | Delay time, MCU_PORz active (low) to MCU_PORz_OUT active (low)         | 0                     |                        | ns   |
| RST7  | $t_d(MCU\_PORzH-MCU\_PORz\_OUTH)$  | Delay time, MCU_PORz inactive (high) to MCU_PORz_OUT inactive (high)   | 0                     |                        | ns   |
| RST8  | $t_d(MCU\_PORzL-PORz\_OUTL)$       | Delay time, MCU_PORz active (low) to PORz_OUT active (low)             | 0                     |                        | ns   |
| RST9  | $t_d(MCU\_PORzH-PORz\_OUTH)$       | Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high)       | 1500                  |                        | ns   |
| RST10 | $t_d(MCU\_PORzL-MCU\_RESETSTATzL)$ | Delay time, MCU_PORz active (low) to MCU_RESETSTATz active (low)       | 0                     |                        | ns   |
| RST11 | $t_d(MCU\_PORzH-MCU\_RESETSTATzH)$ | Delay time, MCU_PORz inactive (high) to MCU_RESETSTATz inactive (high) | POST bypass           | 12000*S <sup>(1)</sup> | ns   |
| RST12 | $t_d(MCU\_PORzL-RESETSTATzL)$      | Delay time, MCU_PORz active (low) to RESETSTATz active (low)           | 0                     |                        | ns   |
| RST13 | $t_d(MCU\_PORzH-RESETSTATzH)$      | Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)     |                       | 14500*S <sup>(1)</sup> | ns   |
| RST14 | $t_w(MCU\_PORz\_OUTL)$             | Pulse width minimum, MCU_PORz_OUT active (low)                         | 1200                  |                        | ns   |
| RST15 | $t_w(PORz\_OUTL)$                  | Pulse Width Minimum PORz_OUT low                                       | 2550                  |                        | ns   |
| RST16 | $t_w(MCU\_RESETSTATzL)$            | Pulse Width Minimum MCU_RESETSTATz low                                 | 3900*S <sup>(1)</sup> |                        | ns   |
| RST17 | $t_w(RESETSTATzL)$                 | Pulse Width Minimum RESETSTATz low                                     | 2650*S <sup>(1)</sup> |                        | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.





**7-12. MCU\_PORz initiates; MCU\_PORz\_OUT, PORz\_OUT, MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**

**表 7-9. PORz Initiates; PORz\_OUT and RESETSTATz Switching Characteristics**

see 图 7-13

| NO.   | PARAMETER                  |                                                            | MODE                                                | MIN                    | MAX | UNIT |
|-------|----------------------------|------------------------------------------------------------|-----------------------------------------------------|------------------------|-----|------|
| RST18 | $t_{d(PORzL-PORz\_OUTL)}$  | Delay time, PORz active (low) toPORz_OUT active (low)      | software control of POR_RST_ISO_DONE_Z              | $T^{(1)}$              |     |      |
|       |                            |                                                            | CTRLMMR_WKUP_POR_RST_CTRL[0].POR_RST_ISO_DONE_Z = 0 | 0                      |     | ns   |
| RST19 | $t_{d(PORzH-PORz\_OUTH)}$  | Delay time, PORz active (high) toPORz_OUT active (high)    |                                                     | 1300                   |     | ns   |
| RST20 | $t_{d(PORzL-RESETSTATzL)}$ | Delay time, PORz active (low) to RESETSTATz active (low)   |                                                     | $T^{(1)}$              |     |      |
|       |                            |                                                            | CTRLMMR_WKUP_POR_RST_CTRL[0].POR_RST_ISO_DONE_Z = 0 | 0                      |     | ns   |
| RST21 | $t_{d(PORzH-RESETSTATzH)}$ | Delay time, PORz active (high) to RESETSTATz active (high) |                                                     | 14500*S <sup>(2)</sup> |     | ns   |

(1) T = Reset Isolation Time (Software Dependent).

(2) S = MCU\_OSC0\_XI/XO clock period.

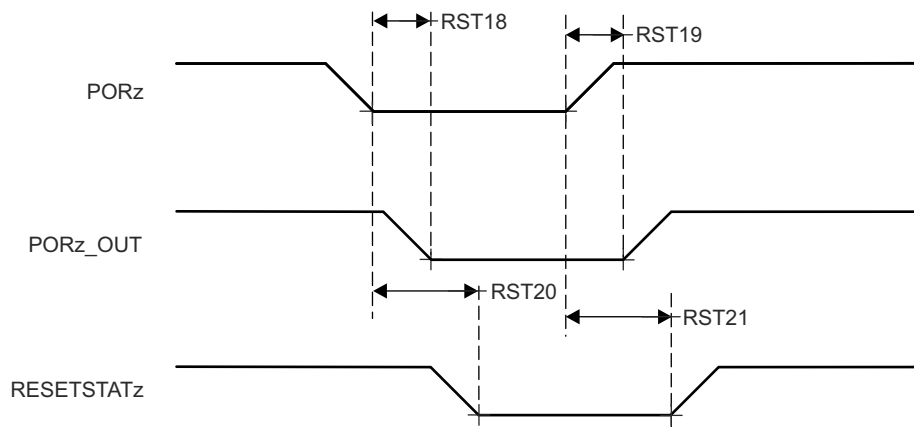


**图 7-13. PORz initiates; PORz\_OUT and RESETSTATz Switching Characteristics**

表 7-10. MCU\_RESETz Timing Requirements

see 图 7-14

| NO.   |                                      |                                              | MIN  | MAX | UNIT |
|-------|--------------------------------------|----------------------------------------------|------|-----|------|
| RST22 | $t_{w(MCU\_RESETzL)}$ <sup>(1)</sup> | Pulse Width minimum, MCU_RESETz active (low) | 1200 |     | ns   |

(1) Timing for MCU\_RESETz is valid only after all supplies are valid and MCU\_PORz has been asserted for the specified time.

表 7-11. MCU\_RESETz initiates; MCU\_RESETSTATz, and RESETSTATz Switching Characteristics

see 图 7-14

| NO.   |                                        | PARAMETER                                                                | MIN                   | MAX | UNIT |
|-------|----------------------------------------|--------------------------------------------------------------------------|-----------------------|-----|------|
| RST23 | $t_{d(MCU\_RESETzL-MCU\_RESETSTATzL)}$ | Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)       | 800                   |     | ns   |
| RST24 | $t_{d(MCU\_RESETzH-MCU\_RESETSTATzH)}$ | Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high) | 3900*S <sup>(1)</sup> |     | ns   |
| RST25 | $t_{d(MCU\_RESETzL-RESETSTATzL)}$      | Delay time, MCU_RESETz active (low) to RESETSTATz active (low)           | 800                   |     | ns   |
| RST26 | $t_{d(MCU\_RESETzH-RESETSTATzH)}$      | Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)     | 3900*S <sup>(1)</sup> |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.

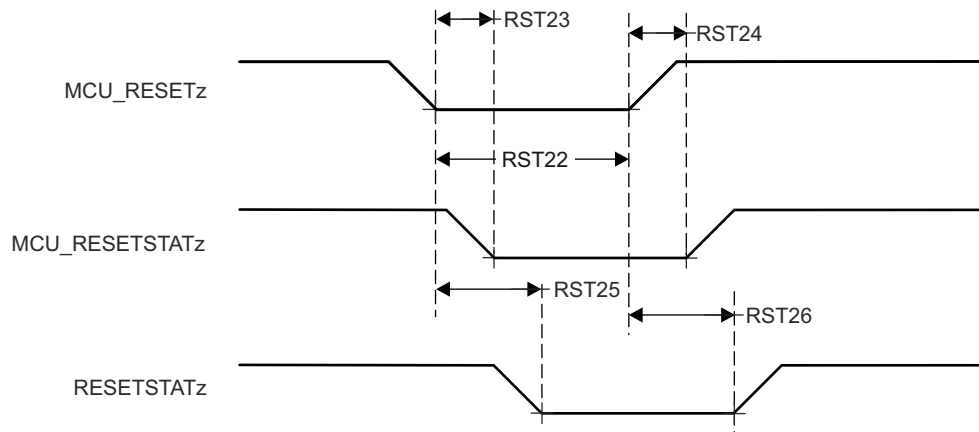


图 7-14. MCU\_RESETz initiates; MCU\_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics

表 7-12. RESET\_REQz Timing Requirements

see 图 7-15

| NO.   |                                    |                                              | MIN  | MAX | UNIT |
|-------|------------------------------------|----------------------------------------------|------|-----|------|
| RST27 | $t_{w(RES\_REQzL)}$ <sup>(1)</sup> | Pulse Width minimum, RESET_REQz active (low) | 1200 |     | ns   |

(1) Timing for RESET\_REQz is valid only after all supplies are valid and MCU\_PORz has been asserted for the specified time.

表 7-13. RESET\_REQz initiates; RESETSTATz Switching Characteristics

see 图 7-15

| NO.   | PARAMETER                       | MODE                                                                 | MIN                   | MAX | UNIT |
|-------|---------------------------------|----------------------------------------------------------------------|-----------------------|-----|------|
| RST28 | $t_{d(RES\_REQzL-RES\_STATzL)}$ | software control of SOC_WARMRST_ISO_DONE_Z                           | T <sup>(1)</sup>      |     |      |
|       |                                 | CTRLMMR_WKUP_MAIN_WARM_RST_CTRL[0].SOC_WARMRST_ISO_DONE_Z = 0        | 740                   |     | ns   |
| RST29 | $t_{d(RES\_REQzH-RES\_STATzH)}$ | Delay time, RESET_REQz inactive (high) to RESETSTATz inactive (high) | 2650*S <sup>(2)</sup> |     | ns   |

(1) T = Reset Isolation Time (Software Dependent).

(2) S = MCU\_OSC0\_XI/XO clock period.

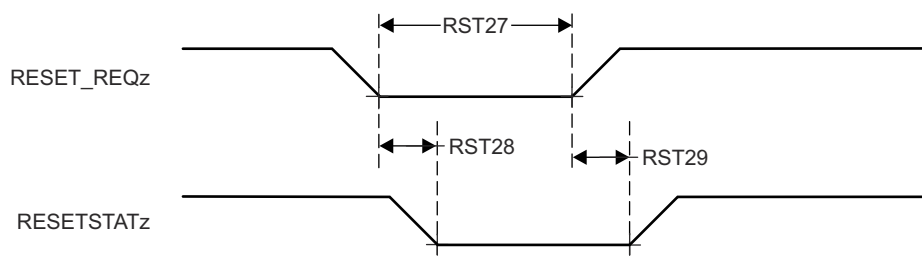


图 7-15. RESET\_REQz initiates; RESETSTATz Timing Requirements and Switching Characteristics

## 表 7-14. EMUx Timing Requirements

see 图 7-16

| NO.   |                          |                                                      | MIN               | MAX | UNIT |
|-------|--------------------------|------------------------------------------------------|-------------------|-----|------|
| RST30 | $t_{su}(EMUx-MCU\_PORz)$ | Setup time, EMU[1:0] before MCU_PORz inactive (high) | $3 \cdot S^{(1)}$ |     | ns   |
| RST31 | $t_h(MCU\_PORz - EMUx)$  | Hold time, EMU[1:0] after MCU_PORz inactive (high)   | 10                |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.

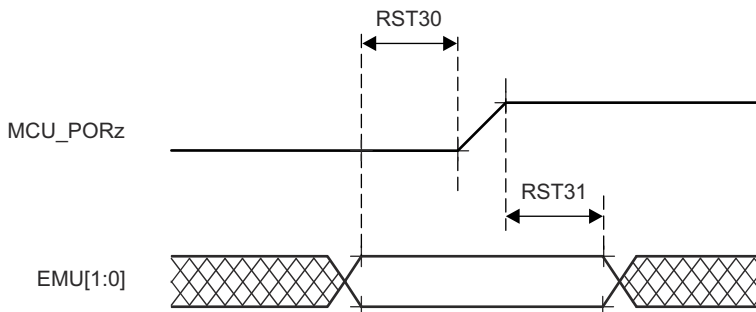


图 7-16. EMUx Timing Requirements

## 表 7-15. MCU\_BOOTMODE Timing Requirements

see 图 7-17

| NO.   |                                        |                                                          | MIN               | MAX | UNIT |
|-------|----------------------------------------|----------------------------------------------------------|-------------------|-----|------|
| RST32 | $t_{su}(MCU\_BOOTMODE-MCU\_PORz\_OUT)$ | Setup time, MCU_BOOTMODE[09:00] before MCU_PORz_OUT high | $3 \cdot S^{(1)}$ |     | ns   |
| RST33 | $t_h(MCU\_PORz\_OUT - MCU\_BOOTMODE)$  | Hold time, MCU_BOOTMODE[09:00] after MCU_PORz_OUT high   | 0                 |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.

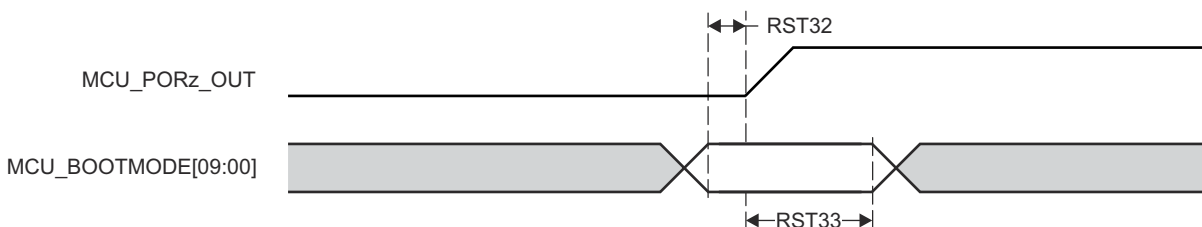


图 7-17. MCU\_BOOTMODE Timing Requirements

表 7-16. BOOTMODE Timing Requirements

see 图 7-18

| NO.   |                                     |                                                | MIN               | MAX | UNIT |
|-------|-------------------------------------|------------------------------------------------|-------------------|-----|------|
| RST34 | $t_{su}(\text{BOOTMODE-PORz\_OUT})$ | Setup time, BOOTMODE[7:0] before PORz_OUT high | $3 \cdot S^{(1)}$ |     | ns   |
| RST35 | $t_h(\text{PORz\_OUT - BOOTMODE})$  | Hold time, BOOTMODE[7:0] after PORz_OUT high   | 0                 |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.

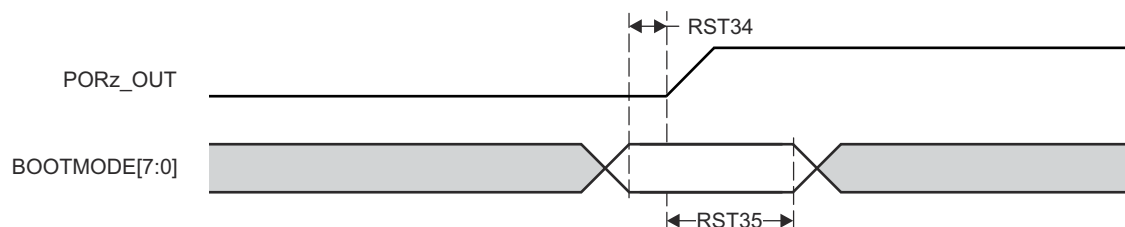


图 7-18. BOOTMODE Timing Requirements

### 7.10.3.2 Safety Signal Timing

Tables and figures provided in this section define switching characteristics for MCU\_SAFETY\_ERRORn and SOC\_SAFETY\_ERRORn.

表 7-17. MCU\_SAFETY\_ERRORn Switching Characteristics

see 图 7-19

| NO.   | PARAMETER                                                                                                  | MIN                   | MAX | UNIT |
|-------|------------------------------------------------------------------------------------------------------------|-----------------------|-----|------|
| SFTY1 | $t_{w(MCU\_SAFETY\_ERRORn)}$<br>Pulse width minimum, MCU_SAFETY_ERRORn active (PWM mode disabled)          | $P \cdot R^{(1) (2)}$ |     | ns   |
| SFTY2 | $t_{d (ERROR\_CONDITION-MCU\_SAFETY\_ERRORnL)}$<br>Delay time, ERROR CONDITION to MCU_SAFETY_ERRORn active | $50 \cdot P^{(1)}$    |     | ns   |

(1) P = ESM functional clock (MCU\_SYSCCLK0 /6).

(2) R = Error Pin Counter Pre-Load Register count value.

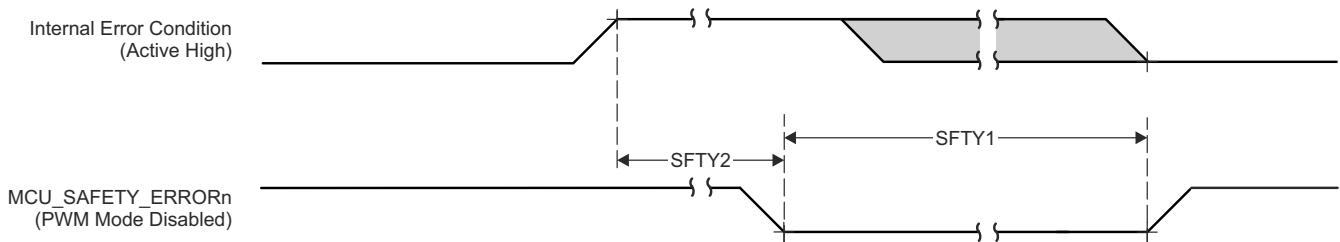


图 7-19. MCU\_SAFETY\_ERRORn Switching Characteristics

表 7-18. SOC\_SAFETY\_ERRORn Switching Characteristics

see 图 7-20

| NO.   | PARAMETER                                                                                                  | MIN                   | MAX | UNIT |
|-------|------------------------------------------------------------------------------------------------------------|-----------------------|-----|------|
| SFTY3 | $t_{w(SOC\_SAFETY\_ERRORn)}$<br>Pulse width minimum, SOC_SAFETY_ERRORn active (PWM mode disabled)          | $P \cdot R^{(1) (2)}$ |     | ns   |
| SFTY4 | $t_{d (ERROR\_CONDITION-SOC\_SAFETY\_ERRORnL)}$<br>Delay time, ERROR CONDITION to SOC_SAFETY_ERRORn active | $50 \cdot P^{(1)}$    |     | ns   |

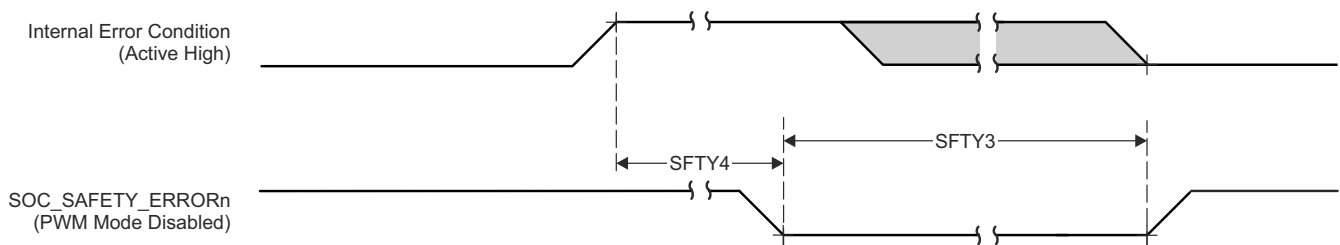


图 7-20. SOC\_SAFETY\_ERRORn Switching Characteristics

### 7.10.3.3 Clock Timing

Tables and figures provided in this section define timing requirements and switching characteristics for clock signals.

**表 7-19. Clock Timng Requiements**

see 图 7-21

| NO.  |                        |                                          | MIN            | MAX            | UNIT |
|------|------------------------|------------------------------------------|----------------|----------------|------|
| CLK1 | $t_{c(EXT\_REFCLK1)}$  | Cycle time minimum, EXT_REFCLK1          | 10             |                | ns   |
| CLK2 | $t_{w(EXT\_REFCLK1H)}$ | Pulse Duration minimum, EXT_REFCLK1 high | $E*0.45^{(1)}$ | $E*0.55^{(1)}$ | ns   |
| CLK3 | $t_{w(EXT\_REFCLK1L)}$ | Pulse Duration minimum, EXT_REFCLK1 low  | $E*0.45^{(1)}$ | $E*0.55^{(1)}$ | ns   |

(1) E = EXT\_REFCLK1 cycle time.

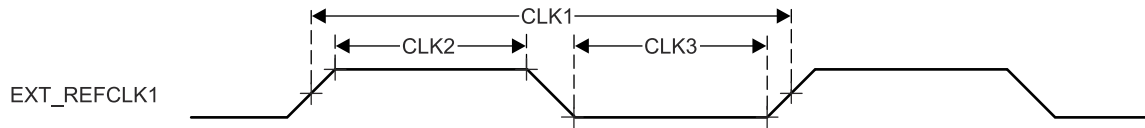


**图 7-21. Clock Timing Requirements**

**表 7-20. Clock Switching Characteristics**

see 图 7-22

| NO.   |                      | PARAMETER                               | MIN           | MAX           | UNIT |
|-------|----------------------|-----------------------------------------|---------------|---------------|------|
| CLK4  | $t_{c(SYSCLKOUT0)}$  | Cycle time minimum, SYSCLKOUT0          | 8             |               | ns   |
| CLK5  | $t_{w(SYSCLKOUT0H)}$ | Pulse Duration minimum, SYSCLKOUT0 high | $A*0.4^{(1)}$ | $A*0.6^{(1)}$ | ns   |
| CLK6  | $t_{w(SYSCLKOUT0L)}$ | Pulse Duration minimum, SYSCLKOUT0 low  | $A*0.4^{(1)}$ | $A*0.6^{(1)}$ | ns   |
| CLK7  | $t_{c(OBSCLK0)}$     | Cycle time minimum, OBSCLK0             | 5             |               | ns   |
| CLK8  | $t_{w(OBSCLK0H)}$    | Pulse Duration minimum, OBSCLK0 high    | $B*0.4^{(2)}$ | $B*0.6^{(2)}$ | ns   |
| CLK9  | $t_{w(OBSCLK0L)}$    | Pulse Duration minimum, OBSCLK0 low     | $B*0.4^{(2)}$ | $B*0.6^{(2)}$ | ns   |
| CLK10 | $t_{c(CLKOUT0)}$     | Cycle time minimum, CLKOUT0             | 20            |               | ns   |
| CLK11 | $t_{w(CLKOUT0H)}$    | Pulse Duration minimum, CLKOUT0 high    | $C*0.4^{(3)}$ | $C*0.6^{(3)}$ | ns   |
| CLK12 | $t_{w(CLKOUT0L)}$    | Pulse Duration minimum, CLKOUT0 low     | $C*0.4^{(3)}$ | $C*0.6^{(3)}$ | ns   |

(1) A = SYSCLKOUT0 cycle time.

(2) B = OBSCLK0 cycle time.

(3) C = CLKOUT0 cycle time.

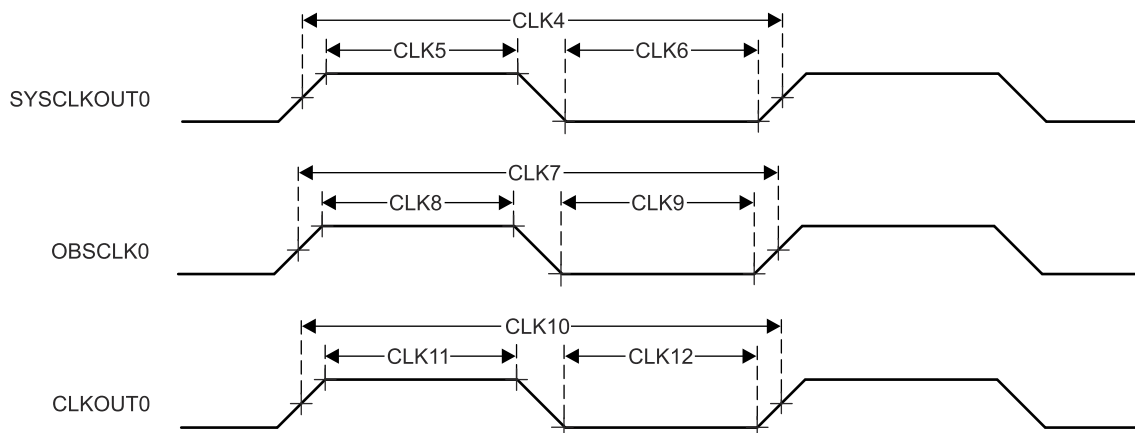


**图 7-22. Clock Switching Characteristics**



## 7.10.4 Clock Specifications

### 7.10.4.1 Input and Output Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- High frequency oscillators inputs
  - OSC1\_XO/OSC1\_XI — external main crystal interface pins connected to internal oscillator which sources reference clock. Provides reference clock to PLLs within MCU domain and MAIN domain. This high-frequency oscillator is used to provide audio clock frequencies to MCASPs.
  - WKUP\_OSC0\_XO/WKUP\_OSC0\_XI — external main crystal interface pins connected to internal oscillator which sources reference clock. Provides reference clock to PLLs within WKUP and MAIN domain.
- Low frequency digital input
  - WKUP\_LF\_CLKIN - Low Frequency 32k digital clock input, optionally sourced from an external PMIC or other clock source. This SoC does not support a LFOSC crystal input.
- General purpose clock inputs
  - MCU\_EXT\_REFCLK0 - optional external System clock input (MCU domain).
  - EXT\_REFCLK1 — optional external System clock input (MAIN domain).
- Peripheral clocks - refer to the Signal Descriptions for peripheral specific clocks

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

#### 7.10.4.1.1 WKUP\_OSC0 Internal Oscillator Clock Source

图 7-23 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the WKUP\_OSC0\_XI and WKUP\_OSC0\_XO pins.

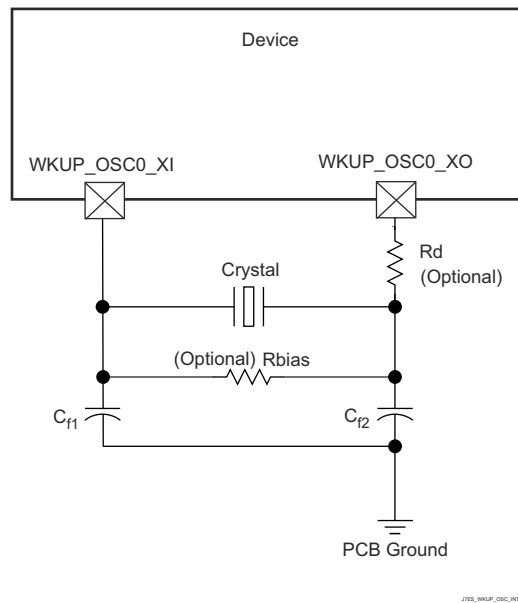


图 7-23. WKUP\_OSC0 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. 表 7-21 summarizes the required electrical constraints.

表 7-21. WKUP\_OSC0 Crystal Electrical Characteristics

| PARAMETER                                              | MIN                      | TYP | MAX | UNIT |
|--------------------------------------------------------|--------------------------|-----|-----|------|
| F <sub>xtal</sub> Crystal Parallel Resonance Frequency | 19.2, 20, 24, 25, 26, 27 |     |     | MHz  |

**表 7-21. WKUP\_OSC0 Crystal Electrical Characteristics (continued)**

| PARAMETER             |                                                     |                                             | MIN                                              | TYP | MAX  | UNIT |
|-----------------------|-----------------------------------------------------|---------------------------------------------|--------------------------------------------------|-----|------|------|
| F <sub>xtal</sub>     | Crystal Frequency Stability and Tolerance           | Ethernet RGMII and RMII not used            |                                                  |     | ±100 | ppm  |
|                       |                                                     | Ethernet RGMII and RMII using derived clock |                                                  |     | ±50  |      |
| C <sub>L1+PCBXI</sub> | Capacitance of C <sub>L1</sub> + C <sub>PCBXI</sub> |                                             | 12                                               |     | 24   | pF   |
| C <sub>L2+PCBXO</sub> | Capacitance of C <sub>L2</sub> + C <sub>PCBXO</sub> |                                             | 12                                               |     | 24   | pF   |
| C <sub>L</sub>        | Crystal Load Capacitance                            |                                             | 6                                                |     | 12   | pF   |
| C <sub>shunt</sub>    | Crystal Circuit Shunt Capacitance                   | ESR <sub>xtal</sub> = 30 Ω                  | 19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz |     | 7    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 40 Ω                  | 19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz |     | 5    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 50 Ω                  | 19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz |     | 5    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 60 Ω                  | 19.2 MHz, 20 MHz, 24 MHz                         |     | 5    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 80 Ω                  | 19.2 MHz, 20 MHz                                 |     | 5    | pF   |
|                       |                                                     |                                             | 25 MHz                                           |     | 3    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 100 Ω                 | 19.2 MHz, 20 MHz                                 |     | 3    | pF   |
| ESR <sub>xtal</sub>   | Crystal Effective Series Resistance                 |                                             |                                                  |     | 100  | Ω    |

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

表 7-22 details the switching characteristics of the oscillator and the requirements of the input clock.

**表 7-22. WKUP\_OSC0 Switching Characteristics - Crystal Mode**

| PARAMETER         |                             | MIN | TYP                | MAX  | UNIT |
|-------------------|-----------------------------|-----|--------------------|------|------|
| C <sub>XI</sub>   | XI Capacitance              |     |                    | 1.55 | pF   |
| C <sub>XO</sub>   | XO Capacitance              |     |                    | 1.35 | pF   |
| C <sub>XIXO</sub> | XI to XO Mutual Capacitance |     |                    | 0.9  | fF   |
| t <sub>s</sub>    | Maximum Start-up Time       |     | 9.5 <sup>(1)</sup> |      | ms   |

- (1) TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.

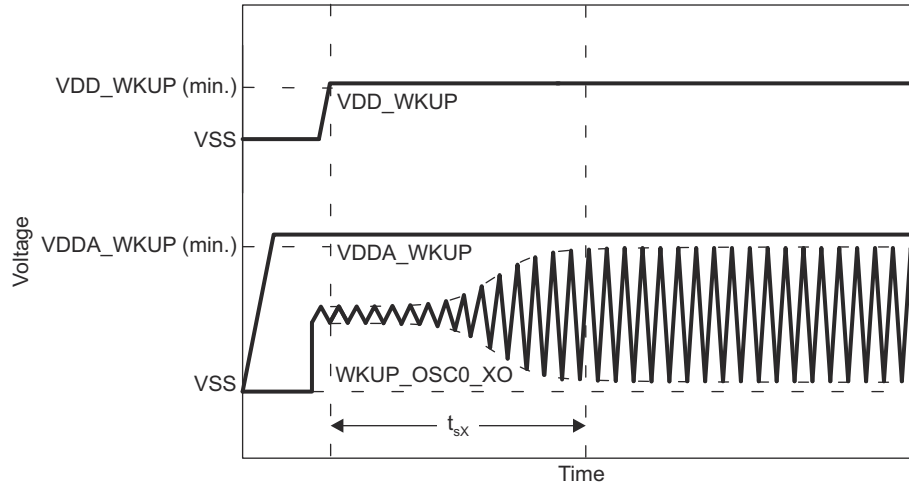


图 7-24. WKUP\_OSC0 Start-up Time

#### 7.10.4.1.1.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load,  $C_L$ , of this circuit is a combination of discrete capacitors  $C_{L1}$ ,  $C_{L2}$ , and several parasitic contributions. PCB signal traces which connect crystal circuit components to WKUP\_OSC0\_XI and WKUP\_OSC0\_XO have parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where the PCB designer should be able to extract parasitic capacitance for each signal trace. The WKUP\_OSC0 circuits and device package have combined parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where these parasitic capacitance values are defined in 表 7-22.

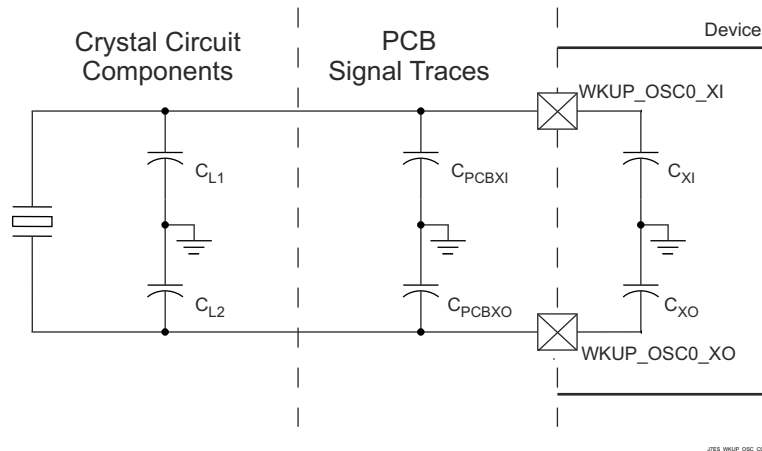


图 7-25. Load Capacitance

Load capacitors,  $C_{L1}$  and  $C_{L2}$  in 图 7-23, should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of  $C_{L1}$  and  $C_{L2}$ , multiply the capacitive load value  $C_L$  by 2. Using this result, subtract the combined values of  $C_{PCBXI} + C_{XI}$  to determine the value of  $C_{L1}$  and the combined values of  $C_{PCBXO} + C_{XO}$  to determine the value of  $C_{L2}$ . For example, if  $C_L = 10$  pF,  $C_{PCBXI} = 2.9$  pF,  $C_{XI} = 0.5$  pF,  $C_{PCBXO} = 3.7$  pF,  $C_{XO} = 0.5$  pF, the value of  $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10 \text{ pF}) - 2.9 \text{ pF} - 0.5 \text{ pF}] = 16.6 \text{ pF}$  and  $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10 \text{ pF}) - 3.7 \text{ pF} - 0.5 \text{ pF}] = 15.8 \text{ pF}$

#### 7.10.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for WKUP\_OSC0 operating conditions defined in 表 7-21. Shunt capacitance,  $C_{shunt}$ , of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to WKUP\_OSC0 have mutual parasitic capacitance to each other,  $C_{PCBXIXO}$ , where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance,  $C_{XIXO}$ , where this mutual parasitic capacitance value is defined in 表 7-22.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

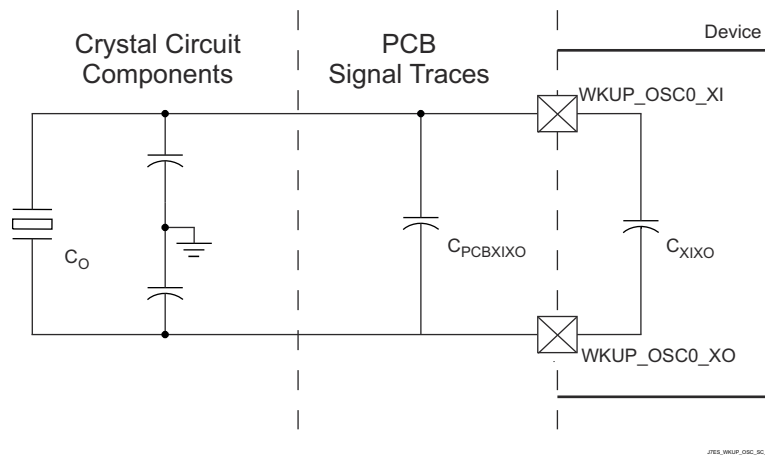


图 7-26. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied.  $C_O$  in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30  $\Omega$ ,  $C_{PCBXIXO}$  = 0.04 pF,  $C_{XIXO}$  = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

#### 7.10.4.1.2 WKUP\_OSC0 LVC MOS Digital Clock Source

图 7-27 shows the recommended oscillator connections when WKUP\_OSC0\_XI is connected to a 1.8-V LVC MOS square-wave digital clock source.

#### 备注

A DC steady-state condition is not allowed on WKUP\_OSC0\_XI when the oscillator is powered up. This is not allowed because WKUP\_OSC0\_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down WKUP\_OSC0 any time WKUP\_OSC0\_XI is not toggling between logic states.

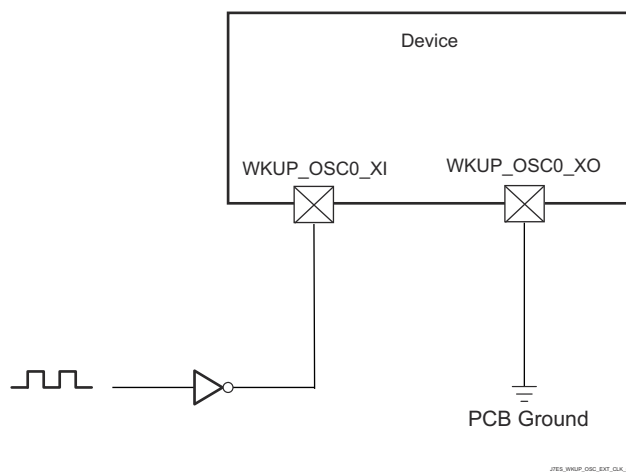


图 7-27. 1.8-V LVC MOS-Compatible Clock Input

#### 7.10.4.1.3 Auxiliary OSC1 Internal Oscillator Clock Source

图 7-28 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the OSC1\_XI and OSC1\_XO pins.

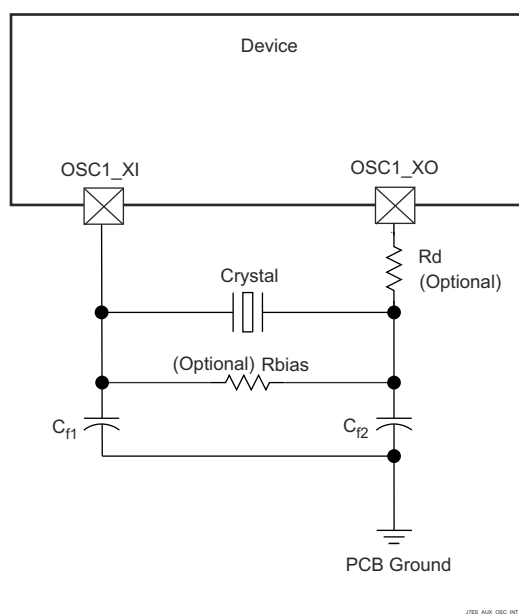


图 7-28. OSC1 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. 表 7-23 summarizes the required electrical constraints.

**表 7-23. OSC1 Crystal Electrical Characteristics**

| PARAMETER             |                                                     |                             |                                                  | MIN  | TYP | MAX  | UNIT |
|-----------------------|-----------------------------------------------------|-----------------------------|--------------------------------------------------|------|-----|------|------|
| F <sub>xtal</sub>     | Crystal Parallel Resonance Frequency                |                             |                                                  | 19.2 |     | 27   | MHz  |
| F <sub>xtal</sub>     | Crystal Frequency Stability and Tolerance           |                             | Ethernet RGMII and RMII not used                 |      |     | ±100 | ppm  |
|                       |                                                     |                             | Ethernet RGMII and RMII using derived clock      |      |     | ±50  |      |
| C <sub>L1+PCBXI</sub> | Capacitance of C <sub>L1</sub> + C <sub>PCBXI</sub> |                             |                                                  | 12   |     | 24   | pF   |
| C <sub>L2+PCBXO</sub> | Capacitance of C <sub>L2</sub> + C <sub>PCBXO</sub> |                             |                                                  | 12   |     | 24   | pF   |
| C <sub>L</sub>        | Crystal Load Capacitance                            |                             |                                                  | 6    |     | 12   | pF   |
| C <sub>shunt</sub>    | Crystal Circuit Shunt Capacitance                   | ESR <sub>xtal</sub> = 30 Ω  | 19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz |      |     | 7    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 40 Ω  | 19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz |      |     | 5    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 50 Ω  | 19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz |      |     | 5    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 60 Ω  | 19.2 MHz, 20 MHz, 24 MHz                         |      |     | 5    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 80 Ω  | 19.2 MHz, 20 MHz                                 |      |     | 5    | pF   |
|                       |                                                     |                             | 25 MHz                                           |      |     | 3    | pF   |
|                       |                                                     | ESR <sub>xtal</sub> = 100 Ω | 19.2 MHz, 20 MHz                                 |      |     | 3    | pF   |
| ESR <sub>xtal</sub>   | Crystal Effective Series Resistance                 |                             |                                                  |      |     | 100  | Ω    |

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

表 7-24 details the switching characteristics of the oscillator and the requirements of the input clock.

**表 7-24. OSC1 Switching Characteristics - Crystal Mode**

| PARAMETER         |                             | MIN | TYP                | MAX  | UNIT |
|-------------------|-----------------------------|-----|--------------------|------|------|
| C <sub>XI</sub>   | XI Capacitance              |     |                    | 1.55 | pF   |
| C <sub>XO</sub>   | XO Capacitance              |     |                    | 1.35 | pF   |
| C <sub>XIXO</sub> | XI to XO Mutual Capacitance |     |                    | 0.9  | fF   |
| t <sub>s</sub>    | Maximum Start-up Time       |     | 9.5 <sup>(1)</sup> |      | ms   |

- (1) TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.

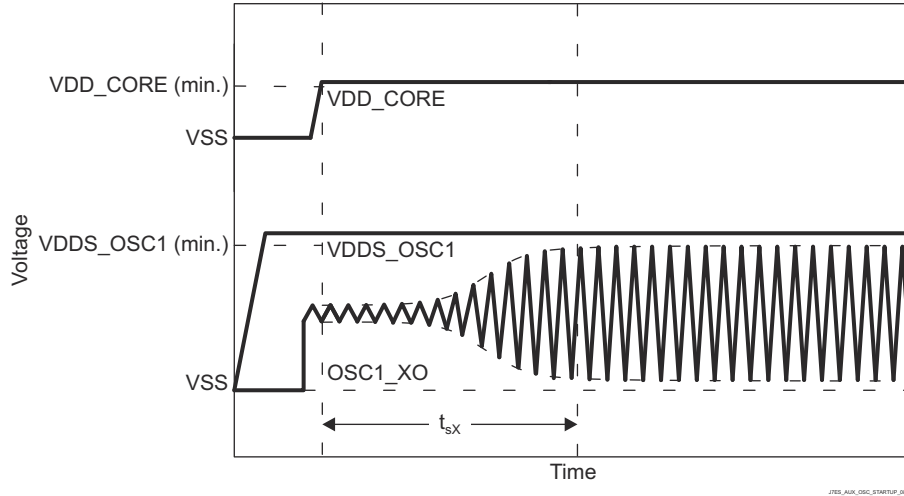


图 7-29. OSC1 Start-up Time

#### 7.10.4.1.3.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load,  $C_L$ , of this circuit is a combination of discrete capacitors  $C_{L1}$ ,  $C_{L2}$ , and several parasitic contributions. PCB signal traces which connect crystal circuit components to OSC1\_XI and OSC1\_XO have parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where the PCB designer should be able to extract parasitic capacitance for each signal trace. The OSC1 circuits and device package have combined parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where these parasitic capacitance values are defined in 表 7-24.

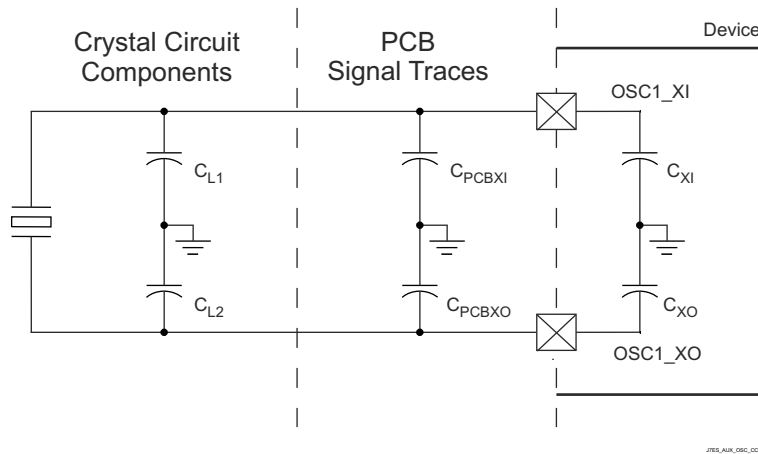


图 7-30. Load Capacitance

Load capacitors,  $C_{L1}$  and  $C_{L2}$  in 图 7-28, should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of  $C_{L1}$  and  $C_{L2}$ , multiply the capacitive load value  $C_L$  by 2. Using this result, subtract the combined values of  $C_{PCBXI} + C_{XI}$  to determine the value of  $C_{L1}$  and the combined values of  $C_{PCBXO} + C_{XO}$  to determine the value of  $C_{L2}$ . For example, if  $C_L = 10$  pF,  $C_{PCBXI} = 2.9$  pF,  $C_{XI} = 0.5$  pF,  $C_{PCBXO} = 3.7$  pF,  $C_{XO} = 0.5$  pF, the value of  $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10 \text{ pF}) - 2.9 \text{ pF} - 0.5 \text{ pF}] = 16.6 \text{ pF}$  and  $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10 \text{ pF}) - 3.7 \text{ pF} - 0.5 \text{ pF}] = 15.8 \text{ pF}$

#### 7.10.4.1.3.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for OSC1 operating conditions defined in 表 7-23. Shunt capacitance,  $C_{shunt}$ , of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to OSC1 have mutual parasitic capacitance to each other,  $C_{PCBXIXO}$ , where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance,  $C_{XIXO}$ , where this mutual parasitic capacitance value is defined in 表 7-24.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

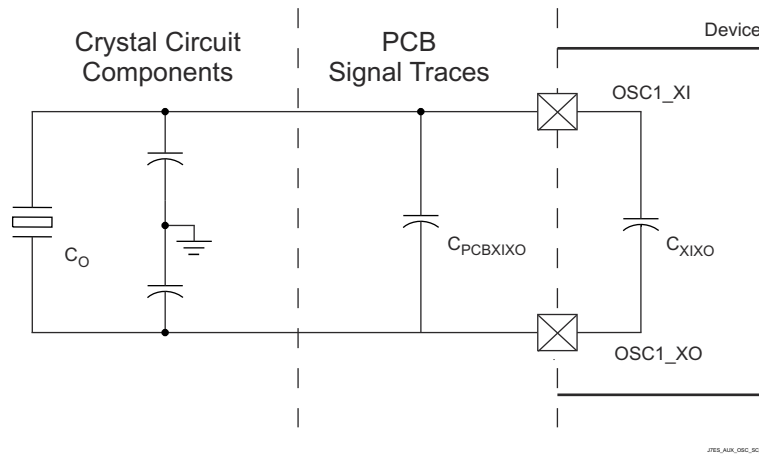


图 7-31. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied.  $C_O$  in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30  $\Omega$ ,  $C_{PCBXIXO}$  = 0.04 pF,  $C_{XIXO}$  = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

#### 7.10.4.1.4 Auxiliary OSC1 LVCMOS Digital Clock Source

图 7-32 shows the recommended oscillator connections when OSC1 is connected to a 1.8-V LVCMOS square-wave digital clock source.

#### 备注

A DC steady-state condition is not allowed on OSC1\_XI when the oscillator is powered up. This is not allowed because OSC1\_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down OSC1 any time OSC1\_XI is not toggling between logic states.



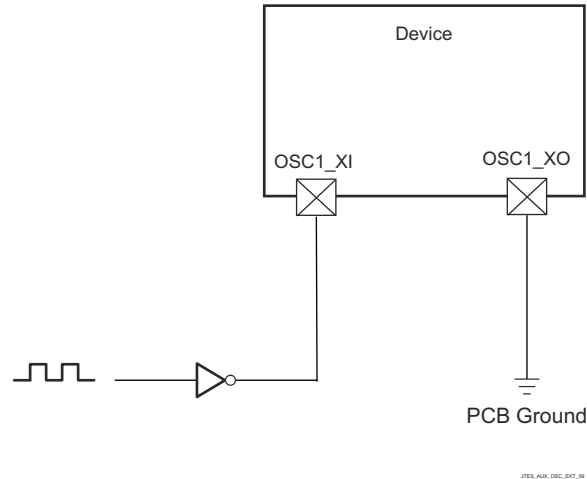


图 7-32. 1.8-V LVC MOS-Compatible Clock Input

#### 7.10.4.1.5 Auxiliary OSC1 Not Used

图 7-33 shows the recommended oscillator connections when OSC1 is not used. OSC1\_XI must be connected to VSS through an external pull resistor ( $R_{pd}$ ) to ensure this input is held to a valid low level when unused since the internal pull-down resistor is disabled by default.

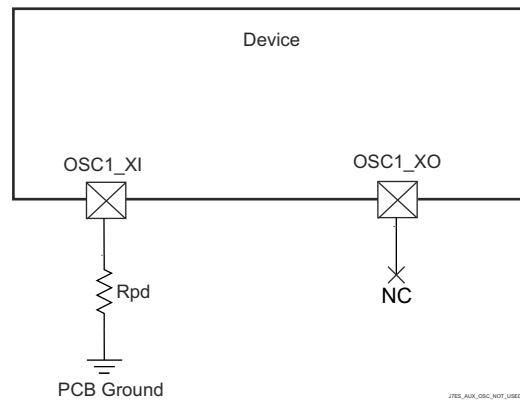


图 7-33. OSC1 Not Used

#### 7.10.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU\_CLKOUT0**
  - Reference clock output for Ethernet PHYs (50 MHz or 25 MHz)
- **MCU\_SYSCCLKOUT0**
  - MCU\_SYSCCLK0 is divided by 4 and then sent out of the device as a LVC MOS clock signal (MCU\_SYSCCLKOUT0). This signal can be used to test if the main chip clock is functioning or not. This signal should not be used as a clock source for external devices on a board.
- **MCU\_OBSCLK0**
  - On the clock output MCU\_OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug. This signal should not be used as a clock source for external devices on a board.
- **SYSCCLKOUT0**
  - SYSCCLK0 is divided by 4 and then sent out of the device as a LVC MOS clock signal (SYSCCLKOUT0). This signal can be used to test if the main chip clock is functioning or not. This signal should not be used as a clock source for external devices on a board.

- **CLKOUT**
  - Reference clock output for Ethernet PHYs (50 MHz)
- **OBSCCLK[1:0]**
  - On the clock output OBSCCLK0/1, oscillators and PLLs clocks can be observed for tests and debug.

### 7.10.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuitries (PLLs) by internal regulators that derive power from the off-chip power-supply.

There are total of three PLLs in the device in WKUP and MCU domains:

- MCU\_PLL0 (MCU R5FSS PLL) with WKUP\_PLLCTRL0
- MCU\_PLL1 (MCU PERIPHERAL PLL)
- MCU\_PLL2 (MCU CPSW PLL)

There are total of twenty PLLs in the device in MAIN domain:

- PLL0 (MAIN PLL) with PLLCTRL0
- PLL1 (PER0 PLL)
- PLL2 (PER1 PLL)
- PLL3 (CPSW9G PLL)
- PLL4 (AUDIO0 PLL)
- PLL5 (VIDEO PLL)
- PLL6 (GPU PLL)
- PLL7 (C7x PLL)
- PLL8 (ARM0 PLL)
- PLL12 (DDR PLL)
- PLL13 (C66 PLL)
- PLL14 (R5F PLL)
- PLL15 (AUDIO1 PLL)
- PLL16 (DSS PLL0)
- PLL17 (DSS PLL1)
- PLL18 (DSS PLL2)
- PLL19 (DSS PLL3)
- PLL23 (DSS PLL7)
- PLL24 (MLB PLL)
- PLL25 (VISION PLL)

#### 备注

For more information, see:

- *Device Configuration / Clocking / PLLs* section in the device TRM.
- *Peripherals / Display Subsystem Overview* section in the device TRM.

#### 备注

The input reference clock (OSC1\_XI/OSC1\_XO) is specified and the lock time is ensured by the PLL controller, as documented in the *Device Configuration* chapter in the device TRM.

### 7.10.4.4 Module and Peripheral Clocks Frequencies

节 7.10.5, *Peripherals* section documents the maximum frequency associated with the peripheral clocks of the device.

For more details on the clocking structure of each module, reference *Device Configurations* chapter in the device TRM.

## 7.10.5 Peripherals

### 7.10.5.1 ATL

The device contains ATL module that can be used for asynchronous sample rate conversion of audio. The ATL calculates the error between two time bases, such as audio syncs, and optionally generates an averaged clock using cycle stealing via software.

#### 备注

For more information about ATL, see *Audio Tracking Logic (ATL)* section in *Peripherals* chapter in the device TRM.

表 7-25 represents ATL timing conditions.

表 7-25. ATL Timing Conditions

| PARAMETER         |                         | MODE                   | MIN | MAX | UNIT |
|-------------------|-------------------------|------------------------|-----|-----|------|
| INPUT CONDITIONS  |                         |                        |     |     |      |
| SR <sub>I</sub>   | Input slew rate         | External reference CLK | 0.5 | 5   | V/ns |
| OUTPUT CONDITIONS |                         |                        |     |     |      |
| C <sub>L</sub>    | Output load capacitance | Internal reference CLK | 1   | 10  | pF   |

节 7.10.5.1.1, 节 7.10.5.1.2, 节 7.10.5.1.3, and 节 7.10.5.1.4 present timing requirements and switching characteristics for ATL.

#### 7.10.5.1.1 ATL\_PCLK Timing Requirements

| NO. | PARAMETER             | MODE                          | MIN                    | MAX                         | UNIT |
|-----|-----------------------|-------------------------------|------------------------|-----------------------------|------|
| D1  | t <sub>c(pclk)</sub>  | Cycle time, ATL_PCLK          | External reference CLK | 5                           | ns   |
| D2  | t <sub>w(pclkL)</sub> | Pulse Duration, ATL_PCLK low  | External reference CLK | $0.45 \times M^{(1)} + 2.5$ | ns   |
| D3  | t <sub>w(pclkH)</sub> | Pulse Duration, ATL_PCLK high | External reference CLK | $0.45 \times M^{(1)} + 2.5$ | ns   |

(1) M = ATL\_CLK[x] period

#### 7.10.5.1.2 ATL\_AWS[x] Timing Requirements

| NO. | PARAMETER            | MODE                                           | MIN                    | MAX                         | UNIT |
|-----|----------------------|------------------------------------------------|------------------------|-----------------------------|------|
| D4  | t <sub>c(aws)</sub>  | Cycle Time, ATL_AWS[x] <sup>(3)</sup>          | External reference CLK | $2 \times M^{(1)}$          | ns   |
| D5  | t <sub>w(awsL)</sub> | Pulse Duration, ATL_AWS[x] <sup>(3)</sup> low  | External reference CLK | $0.45 \times A^{(2)} + 2.5$ | ns   |
| D6  | t <sub>w(awsH)</sub> | Pulse Duration, ATL_AWS[x] <sup>(3)</sup> high | External reference CLK | $0.45 \times A^{(2)} + 2.5$ | ns   |

(1) M = ATL\_CLK[x] period

(2) A = ATL\_AWS[x] period

(3) x = 0 to 3

#### 7.10.5.1.3 ATL\_BWS[x] Timing Requirements

| NO. | PARAMETER            | MODE                                          | MIN                      | MAX                         | UNIT |
|-----|----------------------|-----------------------------------------------|--------------------------|-----------------------------|------|
| D7  | t <sub>c(bws)</sub>  | Cycle Time, ATL_BWS[x] <sup>(3)</sup>         | External reference clock | $2 \times M^{(1)}$          | ns   |
| D8  | t <sub>w(bwsL)</sub> | Pulse Duration, ATL_BWS[x] low <sup>(3)</sup> | External reference clock | $0.45 \times B^{(2)} + 2.5$ | ns   |

| NO. |               |                                                | MODE                     | MIN                         | MAX | UNIT |
|-----|---------------|------------------------------------------------|--------------------------|-----------------------------|-----|------|
| D9  | $t_{w(bwsH)}$ | Pulse Duration, ATL_BWS[x] high <sup>(3)</sup> | External reference clock | $0.45 \times B^{(2)} + 2.5$ |     | ns   |

- (1) M = ATL\_CLK[x] period
- (2) B = ATL\_BWS[x] period
- (3) x = 0 to 3

7.10.5.1.4 ATCLK[x] Switching Characteristics

| NO. | PARAMETER       |                                              | MODE                   | MIN                                   | MAX | UNIT |
|-----|-----------------|----------------------------------------------|------------------------|---------------------------------------|-----|------|
| D10 | $t_{c(atclk)}$  | Cycle time, ATCLK[x] <sup>(3)</sup>          | Internal reference CLK | 20                                    |     | ns   |
| D11 | $t_{w(atclkL)}$ | Pulse Duration, ATCLK[x] low <sup>(3)</sup>  | Internal reference CLK | $0.45 \times P^{(2)} - M^{(1)} - 0.3$ |     | ns   |
| D12 | $t_{w(atclkH)}$ | Pulse Duration, ATCLK[x] high <sup>(3)</sup> | Internal reference CLK | $0.45 \times P^{(2)} - M^{(1)} - 0.3$ |     | ns   |

- (1) M = ATL\_CLK[x] period
- (2) P = ATCLK[x] period
- (3) x = 0 to 3

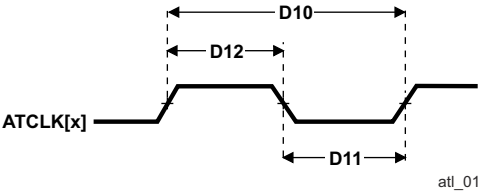


图 7-34. ATCLK[x] Timing

### 7.10.5.2 CPSW2G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

#### 7.10.5.2.1 CPSW2G MDIO Interface Timings

表 7-26 represents CPSW2G timing conditions.

表 7-26. CPSW2G MDIO Timing Conditions

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| $SR_I$                   | Input signal slew rate  | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| $C_L$                    | Output load capacitance | 10  | 470 | pF   |

表 7-27, 表 7-28, and 图 7-35 present timing requirements for MDIO.

表 7-27. CPSW2G MDIO Timing Requirements

| NO.   |                      |                                                        | MIN | MAX | UNIT |
|-------|----------------------|--------------------------------------------------------|-----|-----|------|
| MDIO1 | $t_{su(mdioV-mdcH)}$ | Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high | 90  |     | ns   |
| MDIO2 | $t_{h(mdcH-mdioV)}$  | Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high   | 0   |     | ns   |

表 7-28. CPSW2G MDIO Switching Characteristics

| NO.   | PARAMETER                  |                                                   | MIN   | MAX | UNIT |
|-------|----------------------------|---------------------------------------------------|-------|-----|------|
| MDIO3 | t <sub>c(mdc)</sub>        | Cycle time, MDIO[x]_MDC                           | 400   |     | ns   |
| MDIO4 | t <sub>w(mdcH)</sub>       | Pulse Duration, MDIO[x]_MDC high                  | 160   |     | ns   |
| MDIO5 | t <sub>w(mdcL)</sub>       | Pulse Duration, MDIO[x]_MDC low                   | 160   |     | ns   |
| MDIO7 | t <sub>d(mdcL-mdioV)</sub> | Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid | - 150 | 150 | ns   |

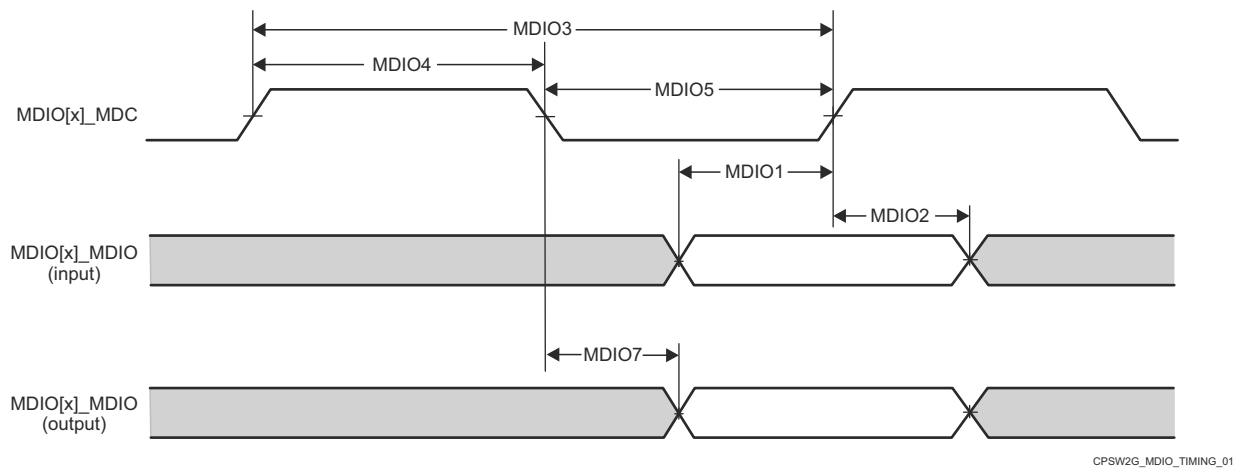


图 7-35. CPSW2G MDIO Timing Requirements and Switching Characteristics

备注

x = 0 in MCU domain

### 7.10.5.2.2 CPSW2G RMII Timings

表 7-29, 节 7.10.5.2.2.1, 节 7.10.5.2.2.2, 和 节 7.10.5.2.2.3 present timing conditions, requirements, and switching characteristics for CPSW2G RMII.

表 7-29. CPSW2G RMII Timing Conditions

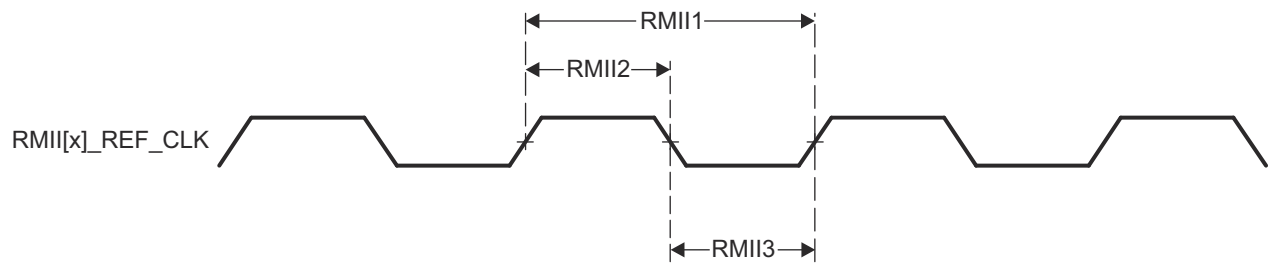
| PARAMETER         |                         |                            | MIN   | MAX  | UNIT |
|-------------------|-------------------------|----------------------------|-------|------|------|
| INPUT CONDITIONS  |                         |                            |       |      |      |
| SR <sub>I</sub>   | Input signal slew rate  | VDD <sup>(1)</sup> = 1.8 V | 0.108 | 0.54 | V/ns |
|                   |                         | VDD <sup>(1)</sup> = 3.3 V | 0.4   | 1.2  | V/ns |
| OUTPUT CONDITIONS |                         |                            |       |      |      |
| C <sub>L</sub>    | Output load capacitance |                            | 3     | 25   | pF   |

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the [Pin Attributes](#)

#### 7.10.5.2.2.1 CPSW2G RMII[x]\_REF\_CLK Timing Requirements - RMII Mode

see 图 7-36

| NO.   |                          |                                      | MIN    | MAX | UNIT |
|-------|--------------------------|--------------------------------------|--------|-----|------|
| RMII1 | t <sub>c(ref_clk)</sub>  | Cycle time, RMII[x]_REF_CLK          | 19.999 | 20  | ns   |
| RMII2 | t <sub>w(ref_clkH)</sub> | Pulse Duration, RMII[x]_REF_CLK high | 7      | 13  | ns   |
| RMII3 | t <sub>w(ref_clkL)</sub> | Pulse Duration, RMII[x]_REF_CLK low  | 7      | 13  | ns   |



A. x = 1 in MCU domain.

图 7-36. CPSW2G RMII[x]\_REFCLK Timing Requirements - RMII Mode

#### 7.10.5.2.2.2 CPSW2G RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, and RMII[x]\_RX\_ER Timing Requirements - RMII Mode

| NO.   |                                   |                                                                       | MIN | MAX | UNIT |
|-------|-----------------------------------|-----------------------------------------------------------------------|-----|-----|------|
| RMII4 | t <sub>su(rxdV-ref_clkH)</sub>    | Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK rising edge | 4   |     | ns   |
|       | t <sub>su(crs_dvV-ref_clkH)</sub> | Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK rising edge   | 4   |     | ns   |
|       | t <sub>su(rx_erV-ref_clkH)</sub>  | Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK rising edge    | 4   |     | ns   |
| RMII5 | t <sub>h(ref_clkH-rxdV)</sub>     | Hold time, RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK rising edge   | 2   |     | ns   |
|       | t <sub>h(ref_clkH-crs_dvV)</sub>  | Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK rising edge     | 2   |     | ns   |
|       | t <sub>h(ref_clkH-rx_erV)</sub>   | Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK rising edge      | 2   |     | ns   |

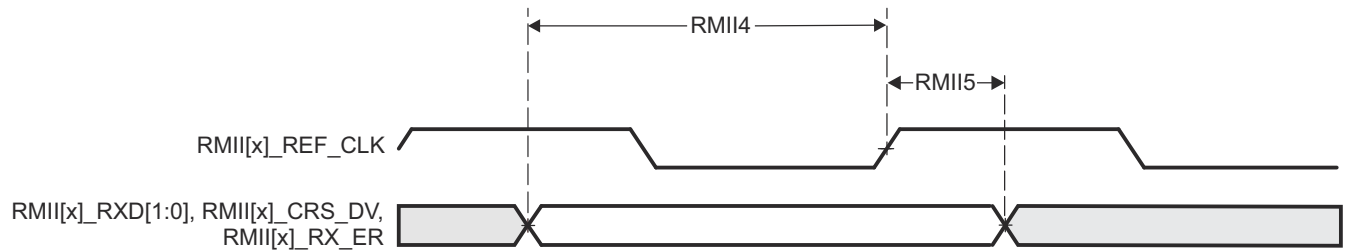


图 7-37. CPSW2G RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, RMII[x]\_RX\_ER Timing Requirements - RMII Mode

节 7.10.5.2.2.3, and 图 7-38 present switching characteristics for CPSW2G RMII Transmit.

#### 7.10.5.2.2.3 CPSW2G RMII[x]\_TXD[1:0], and RMII[x]\_TX\_EN Switching Characteristics - RMII Mode

see 图 7-38

| NO.   | PARAMETER                                                                                        | MIN | MAX | UNIT |
|-------|--------------------------------------------------------------------------------------------------|-----|-----|------|
| RMII6 | $t_{d(\text{ref\_clkH-txdV})}$ Delay time, RMII[x]_REF_CLK rising edge to RMII[x]_TXD[1:0] valid | 2   | 10  | ns   |
|       | $t_{d(\text{ref\_clkH-tx\_enV})}$ Delay time, RMII[x]_REF_CLK rising edge to RMII[x]_TX_EN valid | 2   | 10  | ns   |

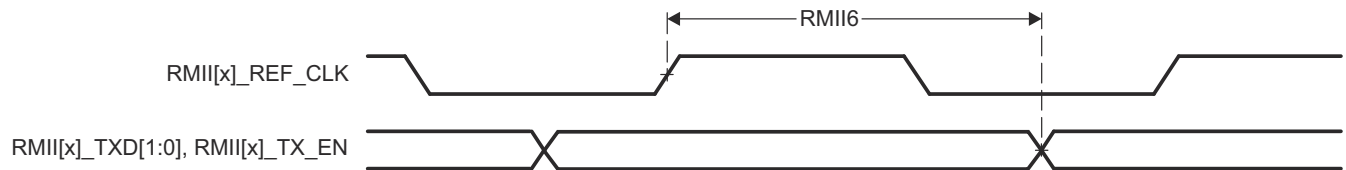


图 7-38. RMII[x]\_TXD[1:0], and RMII[x]\_TX\_EN Switching Characteristics - RMII Mode

#### 7.10.5.2.3 CPSW2G RGMII Timings

节 7.10.5.2.3.1, 节 7.10.5.2.3.2, and 图 7-40 present timing requirements for receive RGMII operation.

For more information, see *Gigabit Ethernet MAC (MCU\_CPSW0)* section in *Peripherals* chapter in the device TRM.

表 7-30. CPSW2G RGMII Timing Conditions

| PARAMETER                             |                                              |                                                       | MIN  | MAX | UNIT |
|---------------------------------------|----------------------------------------------|-------------------------------------------------------|------|-----|------|
| INPUT CONDITIONS                      |                                              |                                                       |      |     |      |
| SR <sub>I</sub>                       | Input slew rate                              | VDD <sup>(1)</sup> = 1.8 V                            | 1.44 | 5   | V/ns |
|                                       |                                              | VDD <sup>(1)</sup> = 3.3 V                            | 2.64 | 5   | V/ns |
| OUTPUT CONDITIONS                     |                                              |                                                       |      |     |      |
| C <sub>L</sub>                        | Output load capacitance                      |                                                       | 2    | 20  | pF   |
| PCB CONNECTIVITY REQUIREMENTS         |                                              |                                                       |      |     |      |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | RGMII[x]_RXC,<br>RGMII[x]_RD[3:0],<br>RGMII[x]_RX_CTL |      | 50  | ps   |
|                                       |                                              | RGMII[x]_TXC,<br>RGMII[x]_TD[3:0],<br>RGMII[x]_TX_CTL |      | 50  | ps   |

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the [Pin Attributes](#).



### 7.10.5.2.3.1 RGMII[x]\_RXC Timing Requirements - RGMII Mode

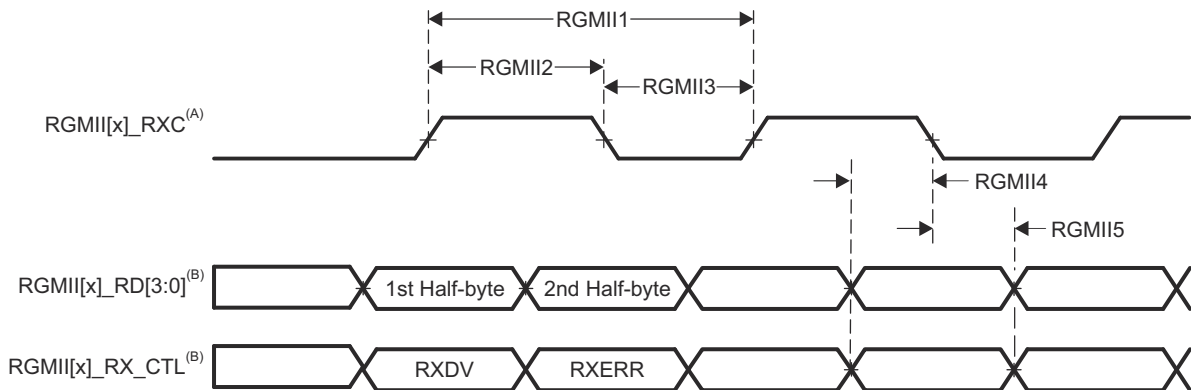
see 图 7-39

| NO.    |               |                                   | MODE     | MIN | MAX | UNIT |
|--------|---------------|-----------------------------------|----------|-----|-----|------|
| RGMII1 | $t_{c(rxc)}$  | Cycle time, RGMII[x]_RXC          | 10Mbps   | 360 | 440 | ns   |
|        |               |                                   | 100Mbps  | 36  | 44  | ns   |
|        |               |                                   | 1000Mbps | 7.2 | 8.8 | ns   |
| RGMII2 | $t_{w(rxcH)}$ | Pulse duration, RGMII[x]_RXC high | 10Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000Mbps | 3.6 | 4.4 | ns   |
| RGMII3 | $t_{w(rxcL)}$ | Pulse duration, RGMII[x]_RXC low  | 10Mbps   | 160 | 240 | ns   |
|        |               |                                   | 100Mbps  | 16  | 24  | ns   |
|        |               |                                   | 1000Mbps | 3.6 | 4.4 | ns   |

### 7.10.5.2.3.2 CPSW2G Timing Requirements for RGMII[x]\_RD[3:0], and RGMII[x]\_RCTL - RGMII Mode

see 图 7-39

| NO.    |                         |                                                                   | MODE     | MIN | MAX | UNIT |
|--------|-------------------------|-------------------------------------------------------------------|----------|-----|-----|------|
| RGMII4 | $t_{su(rdV-rxcV)}$      | Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC transition | 10Mbps   | 1   |     | ns   |
|        |                         |                                                                   | 100Mbps  | 1   |     | ns   |
|        |                         |                                                                   | 1000Mbps | 1   |     | ns   |
|        | $t_{su(rx\_ctlV-rxcV)}$ | Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC transition  | 10Mbps   | 1   |     | ns   |
|        |                         |                                                                   | 100Mbps  | 1   |     | ns   |
|        |                         |                                                                   | 1000Mbps | 1   |     | ns   |
| RGMII5 | $t_{h(rxcV-rdV)}$       | Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC transition   | 10Mbps   | 1   |     | ns   |
|        |                         |                                                                   | 100Mbps  | 1   |     | ns   |
|        |                         |                                                                   | 1000Mbps | 1   |     | ns   |
|        | $t_{h(rxcV-rx\_ctlV)}$  | Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC transition    | 10Mbps   | 1   |     | ns   |
|        |                         |                                                                   | 100Mbps  | 1   |     | ns   |
|        |                         |                                                                   | 1000Mbps | 1   |     | ns   |



- A. RGMII\_RXC must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. RGMII\_RXD[3:0] carries data bits 3-0 on the rising edge of RGMII\_RXC and data bits 7-4 on the falling edge of RGMII\_RXC. Similarly, RGMII\_RXCTL carries RXDV on rising edge of RGMII\_RXC and RXERR on falling edge of RGMII\_RXC.

图 7-39. CPSW2G Receive Interface Timing, RGMII Operation

节 7.10.5.2.3.3, 节 7.10.5.2.3.4 present switching characteristics for transmit - RGMII for 10 Mbps, 100 Mbps, and 1000 Mbps.

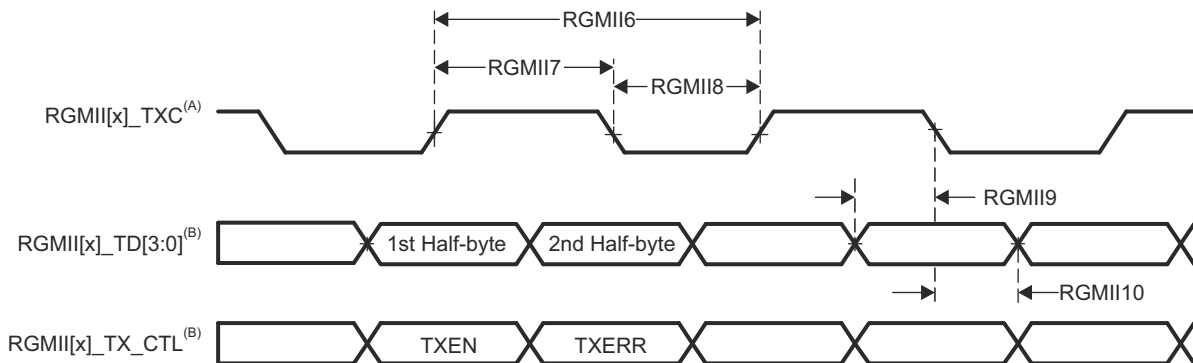
#### 7.10.5.2.3.3 CPSW2G RGMII[x]\_TXC Switching Characteristics - RGMII Mode

| NO.    | PARAMETER    |                                   | MODE     | MIN | MAX | UNIT |
|--------|--------------|-----------------------------------|----------|-----|-----|------|
| RGMII6 | $t_{c(tc)}$  | Cycle time, RGMII[x]_TXC          | 10Mbps   | 360 | 440 | ns   |
|        |              |                                   | 100Mbps  | 36  | 44  | ns   |
|        |              |                                   | 1000Mbps | 7.2 | 8.8 | ns   |
| RGMII7 | $t_{w(tcH)}$ | Pulse duration, RGMII[x]_TXC high | 10Mbps   | 160 | 240 | ns   |
|        |              |                                   | 100Mbps  | 16  | 24  | ns   |
|        |              |                                   | 1000Mbps | 3.6 | 4.4 | ns   |
| RGMII8 | $t_{w(tcL)}$ | Pulse duration, RGMII[x]_TXC low  | 10Mbps   | 160 | 240 | ns   |
|        |              |                                   | 100Mbps  | 16  | 24  | ns   |
|        |              |                                   | 1000Mbps | 3.6 | 4.4 | ns   |

#### 7.10.5.2.3.4 RGMII[x]\_TD[3:0], and RGMII[x]\_TX\_CTL Switching Characteristics - RGMII Mode

see 图 7-40

| NO.     | PARAMETER               |                                                                        | MODE     | MIN | MAX | UNIT |
|---------|-------------------------|------------------------------------------------------------------------|----------|-----|-----|------|
| RGMII9  | $t_{osu(tdV-txcV)}$     | Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC transition   | 10Mbps   | 1.2 |     | ns   |
|         |                         |                                                                        | 100Mbps  | 1.2 |     | ns   |
|         |                         |                                                                        | 1000Mbps | 1.2 |     | ns   |
|         | $t_{osu(tx_ctlV-txcV)}$ | Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC transition    | 10Mbps   | 1.2 |     | ns   |
|         |                         |                                                                        | 100Mbps  | 1.2 |     | ns   |
| RGMII10 | $t_{oh(tdV-txcV)}$      | Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC transition | 10Mbps   | 1.2 |     | ns   |
|         |                         |                                                                        | 100Mbps  | 1.2 |     | ns   |
|         |                         |                                                                        | 1000Mbps | 1.2 |     | ns   |
|         | $t_{oh(tx_ctlV-txcV)}$  | Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC transition  | 10Mbps   | 1.2 |     | ns   |
|         |                         |                                                                        | 100Mbps  | 1.2 |     | ns   |



- A. TXC is delayed internally before being driven to the RGMII[x]\_TXC pin. This internal delay is always enabled.
- B. Data and control information is received using both edges of the clocks. RGMII\_TD[3:0] carries data bits 3-0 on the rising edge of RGMII\_TXC and data bits 7-4 on the falling edge of RGMII\_TXC. Similarly, RGMII\_TX\_CTL carries TXDV on rising edge of RGMII\_TXC and RTXERR on falling edge of RGMII\_TXC.

图 7-40. CPSW2G Transmit Interface Timing RGMII Mode

### 7.10.5.3 CSI-2

#### 备注

For more information, see the Camera Streaming Interface Receiver (CSI\_RX\_IF) chapter in the device TRM.

The CSI\_RX\_IF deals with the processing of the pixel data coming from an external image sensor and data from memory. It is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture.

The CSI\_RX\_IF has a primary serial interface (CSI-2 port) compliant with the MIPI D-PHY RX specification v1.2 and the MIPI CSI-2 specification v1.3, with 4 differential data lanes plus 1 differential clock lane in synchronous mode, double data rate. Refer to the specification for timing details.

- 2.5 Gbps (1.25 GHz) for each lane.

### 7.10.5.4 DDRSS

For more details about features and additional description information on the device LPDDR4 Memory Interfaces, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

The device has dedicated interface to LPDDR4. It supports JEDEC JESD209-4B standard compliant LPDDR4 SDRAM devices with the following features:

- 32-bit data path to external SDRAM memory
- Memory device capacity: Up to 8GB address space available over two chip selects (4GB per rank)
- No support for byte mode LPDDR4 memories, or memories with more than 17 row address bits

表 7-31 和 图 7-41 呈现 switching characteristics for DDRSS.

表 7-31. Switching Characteristics for DDRSS

| NO. | PARAMETER                                                    | DDR TYPE | MIN    | MAX   | UNIT |
|-----|--------------------------------------------------------------|----------|--------|-------|------|
| 1   | $t_{C(DDR\_CKP/DDR\_CKN)}$ Cycle time, DDR0_CKP and DDR0_CKN | LPDDR4   | 0.4681 | 3.003 | ns   |

- Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. TI strongly recommends all designs to follow the TI LPDDR4 EVM PCB layout exactly in every detail (routing, spacing, vias/backdrill, PCB material, etc.) in order to achieve the full specified clock frequency. Refer to the Jacinto 7 DDR Board Design and Layout Guidelines for details.

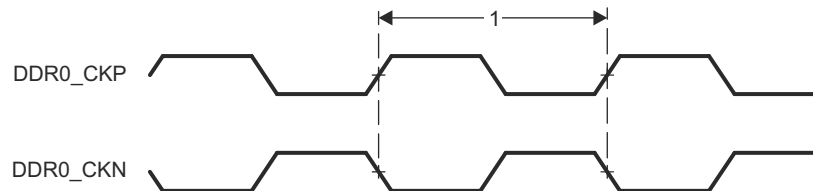


图 7-41. DDRSS Memory Interface Clock Timing

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

### 7.10.5.5 DSS

For more details about features and additional description information on the device Display Subsystem - Video Output Ports, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

表 7-32 代表 DPI timing conditions.

表 7-32. DPI Timing Conditions

| PARAMETER        | MIN | MAX | UNIT |
|------------------|-----|-----|------|
| INPUT CONDITIONS |     |     |      |

**表 7-32. DPI Timing Conditions (continued)**

| PARAMETER                             |                                              | MIN  | MAX  | UNIT |
|---------------------------------------|----------------------------------------------|------|------|------|
| SR <sub>I</sub>                       | Input slew rate                              | 1.44 | 26.4 | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |      |      |      |
| C <sub>L</sub>                        | Output load capacitance                      | 1.5  | 5    | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |      |      |      |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |      | 100  | ps   |

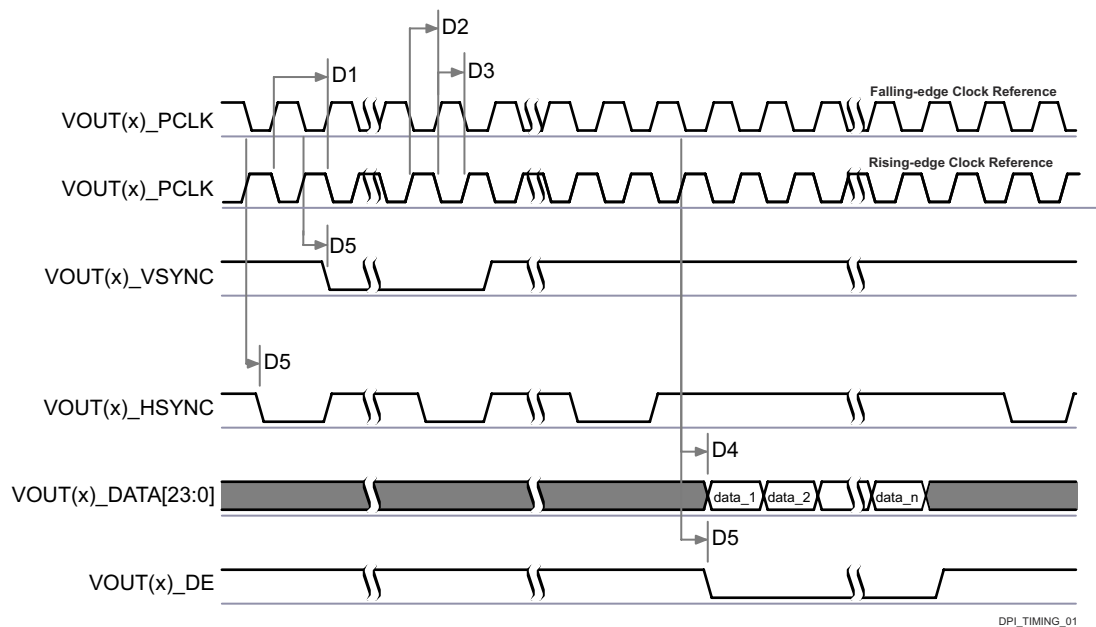
表 7-33, 表 7-34, 图 7-42 和 图 7-43 assume testing over the recommended operating conditions and electrical characteristic conditions.

**表 7-33. DPI Video Output Switching Characteristics**

| NO.(2) | PARAMETER                    |                                                                                                              | MIN                    | MAX  | UNIT |
|--------|------------------------------|--------------------------------------------------------------------------------------------------------------|------------------------|------|------|
| D1     | t <sub>c</sub> (pclk)        | Cycle time, VOUT(x)_PCLK                                                                                     | 6.06                   |      | ns   |
| D2     | t <sub>w</sub> (pclkL)       | Pulse duration, VOUT(x)_PCLK low                                                                             | 0.475×P <sup>(1)</sup> |      | ns   |
| D3     | t <sub>w</sub> (pclkH)       | Pulse duration, VOUT(x)_PCLK high                                                                            | 0.475×P <sup>(1)</sup> |      | ns   |
| D4     | t <sub>d</sub> (pclkV-dataV) | Delay time, VOUT(x)_PCLK transition to VOUT(x)_DATA[23:0] transition                                         | -0.68                  | 1.78 | ns   |
| D5     | t <sub>d</sub> (pclkV-ctrlL) | Delay time, VOUT(x)_PCLK transition to control signals VOUT(x)_VSYNC, VOUT(x)_HSYNC, VOUT(x)_DE falling edge | -0.68                  | 1.78 | ns   |

(1) P = output VOUT(x)\_PCLK period in ns.

(2) x in VOUT(x) = 1 or 2



- A. The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.
- B. The polarity and the pulse width of VOUT(x)\_HSYNC and VOUT(x)\_VSYNC are programmable, refer to *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.
- C. The VOUT(x)\_PCLK frequency can be configured, refer to *Display Subsystem* section in *Peripherals* chapter in the device TRM.
- D. x in VOUT(x) = 1 or 2.

**图 7-42. DPI Video Output**

表 7-34. DPI External Pixel Clock Timing Requirements

| NO. (2) |                          |                                        | MIN                   | MAX | UNIT |
|---------|--------------------------|----------------------------------------|-----------------------|-----|------|
| D6      | $t_{c(\text{extpclk})}$  | Cycle time, VOUT(x)_EXTPCLKIN          | 6.06                  |     | ns   |
| D7      | $t_{w(\text{extpclk}L)}$ | Pulse duration, VOUT(x)_EXTPCLKIN low  | $0.45 \times P^{(1)}$ |     | ns   |
| D8      | $t_{w(\text{extpclk}H)}$ | Pulse duration, VOUT(x)_EXTPCLKIN high | $0.45 \times P^{(1)}$ |     | ns   |

(1) P = output VOUT(x)\_PCLK period in ns.

(2) x in VOUT(x) = 1 or 2

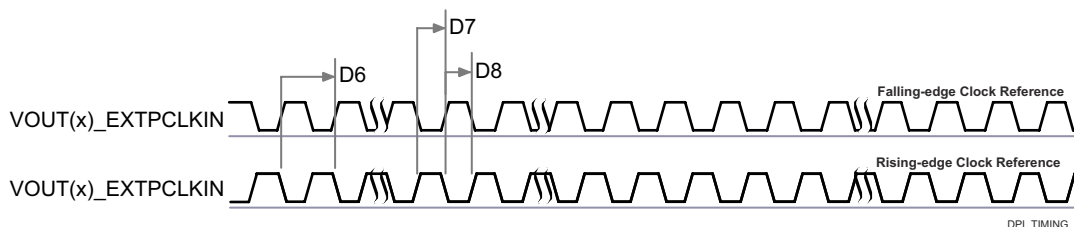


图 7-43. DPI External Pixel Clock Input

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.6 eCAP

The supported features by the device ECAP are:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt capabilities on any of the four capture events
- Input capture signal pre-scaling (from 1 to 16)
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or difference mode time-stamp capture)

表 7-35 represents ECAP timing conditions.

表 7-35. ECAP Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

节 7.10.5.6.1 和 节 7.10.5.6.2 present timing and switching characteristics for eCAP (see 图 7-44 和 图 7-45).

#### 7.10.5.6.1 Timing Requirements for eCAP

| NO.  | PARAMETER    | DESCRIPTION                        | MIN            | MAX | UNIT |
|------|--------------|------------------------------------|----------------|-----|------|
| CAP1 | $t_{w(cap)}$ | Pulse duration, CAP (asynchronous) | $2 + 2P^{(1)}$ |     | ns   |

(1) P = sysclk

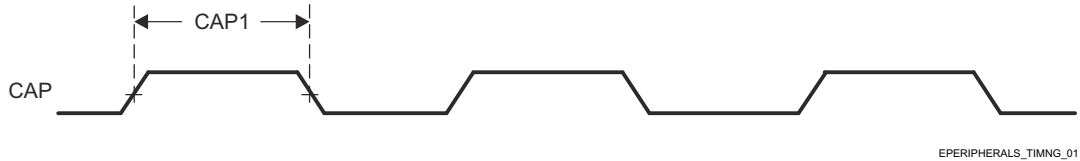


图 7-44. eCAP Input Timings

#### 7.10.5.6.2 Switching Characteristics for eCAP

| NO.  | PARAMETER     | DESCRIPTION          | MIN             | MAX | UNIT |
|------|---------------|----------------------|-----------------|-----|------|
| CAP2 | $t_{w(apwm)}$ | Pulse duration, APWM | $-2 + 2P^{(1)}$ |     | ns   |

(1) P = sysclk

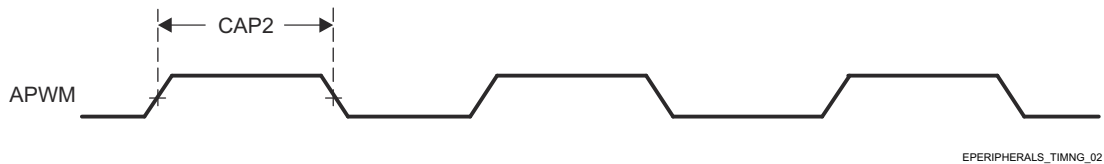


图 7-45. eCAP Output Timings

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.7 EPWM

The supported features by the device EPWM are:

- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs which can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals during fault conditions
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both latched and un-latched fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

表 7-36 represents EPWM timing conditions.

表 7-36. EPWM Timing Conditions

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>i</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

节 7.10.5.7.2, 节 7.10.5.7.1 and present timing and switching characteristics for eHRPWM (see 图 7-47, 图 7-48, 图 7-49, and 图 7-46).

### 7.10.5.7.1 Timing Requirements for eHRPWM

| NO.  | PARAMETER      | DESCRIPTION                       | MIN            | MAX | UNIT |
|------|----------------|-----------------------------------|----------------|-----|------|
| PWM6 | $t_{w(synci)}$ | Pulse duration, EHRPWM_SYNCI      | $2 + 2P^{(1)}$ |     | ns   |
| PWM7 | $t_{w(tz)}$    | Pulse duration, EHRPWM_TZn_IN low | $2 + 3P^{(1)}$ |     | ns   |

(1) P = sysclk

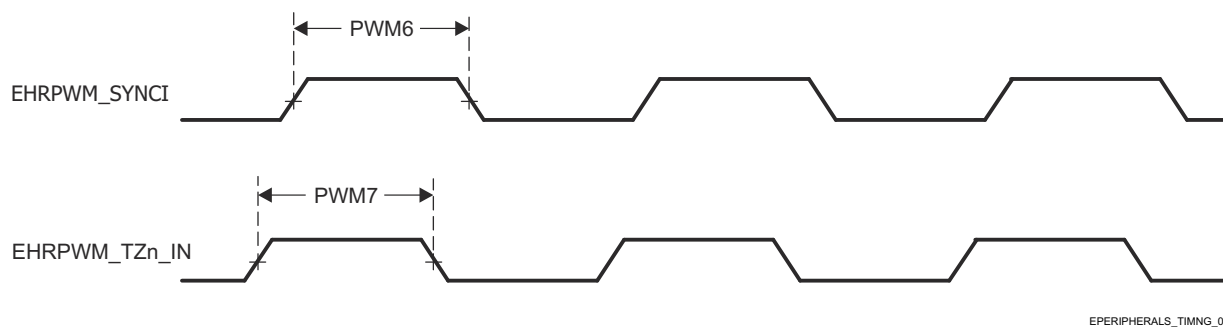


图 7-46. ePWM\_SYNCI and ePWM\_TZn\_IN Output Timings

For more information, see *Camera Subsystem* section in *Peripherals* chapter in the device TRM.

### 7.10.5.7.2 Switching Characteristics for eHRPWM

| NO.  | PARAMETER         | DESCRIPTION                                                | MIN         | MAX | UNIT |
|------|-------------------|------------------------------------------------------------|-------------|-----|------|
| PWM1 | $t_{w(pwm)}$      | Pulse duration, EHRPWM_A/B, high or low                    | $P-3^{(1)}$ |     | ns   |
| PWM2 | $t_{w(syncout)}$  | Pulse duration, EHRPWM_SYNCO                               | $P-3^{(1)}$ |     | ns   |
| PWM3 | $t_{d(tzL-pwmV)}$ | Delay time, EHRPWM_TZn_IN falling edge to EHRPWM_A/B valid |             | 11  | ns   |
| PWM4 | $t_{d(tzL-pwmZ)}$ | Delay time, EHRPWM_TZn_IN falling edge to EHRPWM_A/B Hi-Z  |             | 11  | ns   |

| NO.  | PARAMETER    | DESCRIPTION                    | MIN                | MAX | UNIT |
|------|--------------|--------------------------------|--------------------|-----|------|
| PWM5 | $t_{w(soc)}$ | Pulse duration, EHRPWM_SOC/A/B | P-3 <sup>(1)</sup> |     | ns   |

(1) P = sysclk

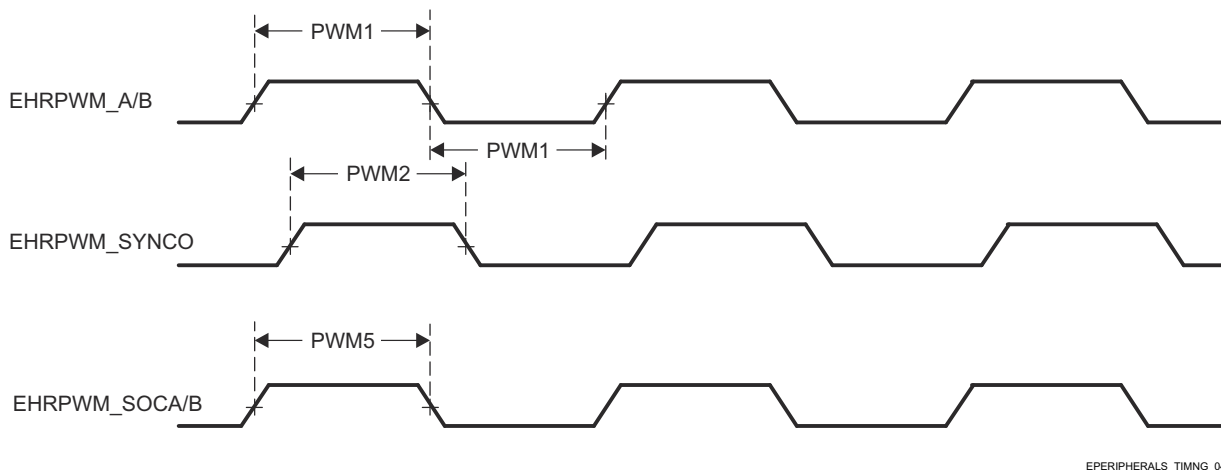


图 7-47. EPWM\_A/B\_out, ePWM\_SYNCO, and ePWM\_SOC/A/B Input Timings

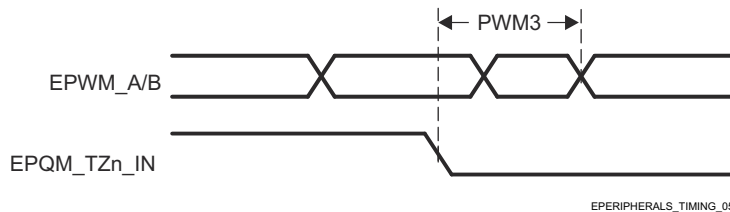


图 7-48. EPWM\_A/B and ePWM\_TZn\_IN Forced High/Low Input Timings

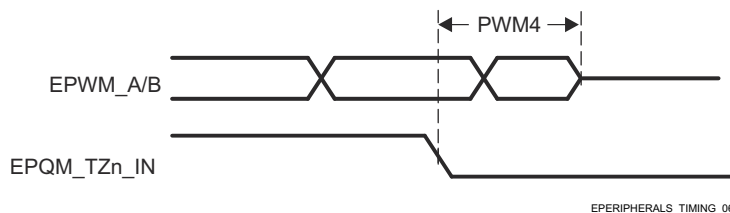


图 7-49. EPWM\_A/B and ePWM\_TZn\_IN Hi - Z Input Timings

### 7.10.5.8 eQEP

The supported features by the device eQEP are:

- Input Synchronization
- Three Stage/Six Stage Digital Noise Filter
- Quadrature Decoder Unit
- Position Counter and Control unit for position measurement
- Quadrature Edge Capture unit for low speed measurement
- Unit Time base for speed/frequency measurement
- Watchdog Timer for detecting stalls

表 7-37 represents EQEP timing conditions.



表 7-37. EQEP Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 1   | 4   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 2   | 7   | pF   |

节 7.10.5.8.1 和 节 7.10.5.8.2 present timing requirements and switching characteristics for eQEP (see 图 7-50).

#### 7.10.5.8.1 Timing Requirements for eQEP

| NO.  |                |                            | MIN            | MAX | UNIT |
|------|----------------|----------------------------|----------------|-----|------|
| QEP1 | $t_{w(qep)}$   | Pulse duration, QEP_A/B    | $2 + 2P^{(1)}$ |     | ns   |
| QEP2 | $t_{w(qepiH)}$ | Pulse duration, QEP_I high | $2 + 2P^{(1)}$ |     | ns   |
| QEP3 | $t_{w(qepiL)}$ | Pulse duration, QEP_I low  | $2 + 2P^{(1)}$ |     | ns   |
| QEP4 | $t_{w(qepsH)}$ | Pulse duration, QEP_S high | $2 + 2P^{(1)}$ |     | ns   |
| QEP5 | $t_{w(qepsL)}$ | Pulse duration, QEP_S low  | $2 + 2P^{(1)}$ |     | ns   |

(1) P = sysclk

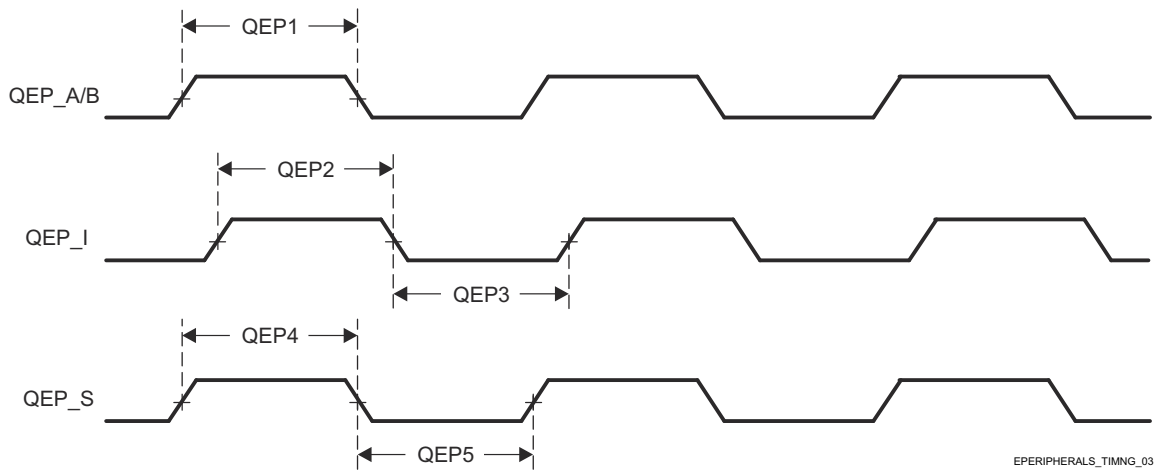


图 7-50. eQEP Input Timings

#### 7.10.5.8.2 Switching Characteristics for eQEP

| NO.  | PARAMETER         |                                                 | MIN | MAX | UNIT |
|------|-------------------|-------------------------------------------------|-----|-----|------|
| QEP6 | $t_{d(QEP-CNTR)}$ | Delay time, external clock to counter increment |     | 24  | ns   |

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.9 GPIO

The device has ten instances of GPIO modules. The GPIO modules are integrated in three groups.

- Group one: WKUP\_GPIO0 and WKUP\_GPIO1
- Group two: GPIO0, GPIO2, GPIO4, and GPIO6
- Group three: GPIO1, GPIO3, GPIO5, and GPIO7

Within each group, exactly one module is selected to control the corresponding I/O pins and pin interrupts.

The GPIO pins are grouped into banks (16 pins per bank), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 432 (3 instances × (9 banks × 16 pins)) pins. Since WKUP\_GPIOu\_[84:143] (u = 0, 1), GPIO\_n\_[128:143] (n = 0, 2, 4, 6), and GPIO\_m\_[36:143] (m = 1, 3, 5, 7) are reserved in this device, general purpose interface supports up to 248 I/O pins.

For more details about features and additional description information on the device General-Purpose Interface, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

#### 备注

The general-purpose input/output i (i = 0 to 1) is also referred to as GPIOi.

表 7-38, 节 7.10.5.9.1, and 节 7.10.5.9.2 present timing conditions, requirements, and switching characteristics for GPIO.

表 7-38. GPIO Timing Conditions

| PARAMETER         |                         | BUFFER TYPE | MIN | MAX | UNIT |
|-------------------|-------------------------|-------------|-----|-----|------|
| INPUT CONDITIONS  |                         |             |     |     |      |
| SR <sub>i</sub>   | Input slew rate         | LVC MOS     | 0.2 | 6.6 | V/ns |
|                   |                         | I2C OD FS   | 0.2 | 0.8 | V/ns |
| OUTPUT CONDITIONS |                         |             |     |     |      |
| C <sub>L</sub>    | Output load capacitance | LVC MOS     | 3   | 10  | pF   |
|                   |                         | I2C OD FS   | 3   | 100 | pF   |

#### 7.10.5.9.1 GPIO Timing Requirements

| NO.   | PARAMETER                |                       | BUFFER TYPE | MIN                     | MAX | UNIT |
|-------|--------------------------|-----------------------|-------------|-------------------------|-----|------|
| GPIO1 | t <sub>w</sub> (gpio_in) | Pulse width, GPIO_n_x | 1.8 V       | 2P + 2.6 <sup>(1)</sup> |     | ns   |
|       |                          |                       | 3.3 V       | 2P + 3.4 <sup>(1)</sup> |     | ns   |

(1) P = functional clock period in ns.

#### 7.10.5.9.2 GPIO Switching Characteristics

| NO.   | PARAMETER                 |                                 | BUFFER TYPE    | MIN                           | MAX | UNIT |
|-------|---------------------------|---------------------------------|----------------|-------------------------------|-----|------|
| GPIO3 | t <sub>w</sub> (GPIO_OUT) | Minimum Output Pulse Width      | LVC MOS        | - 3.6 + 0.975P <sup>(1)</sup> |     | ns   |
| GPIO4 | t <sub>w</sub> (GPIO_OUT) | Minimum Output Pulse Width Low  | I2C Open Drain | 160                           |     | ns   |
| GPIO5 | t <sub>w</sub> (GPIO_OUT) | Minimum Output Pulse Width High | I2C Open Drain | 60                            |     | ns   |

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.10 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

表 7-39 represents GPMC timing conditions.

#### 备注

The IO timings provided in this section are applicable for all combinations of signals for GPMC0. However, the timings are only valid for GPMC0 if signals within a single IOSET are used. The IOSETs are defined in the [GPMC0\\_IOSET](#), *GPMC0\_IOSET* table.

表 7-39. GPMC Timing Conditions

| PARAMETER                             | DESCRIPTION                            | MIN                      | MAX | UNIT |    |
|---------------------------------------|----------------------------------------|--------------------------|-----|------|----|
| Input Conditions                      |                                        |                          |     |      |    |
| SR <sub>I</sub>                       | Input slew rate                        | 1.65                     | 4   | V/ns |    |
| Output Conditions                     |                                        |                          |     |      |    |
| C <sub>L</sub>                        | Output load capacitance                | 5                        | 20  | pF   |    |
| PCB Connectivity Requirements         |                                        |                          |     |      |    |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace        | 133 MHz Synchronous Mode | 140 | 360  | ps |
|                                       |                                        | All other modes          | 140 | 720  |    |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation mismatch across all traces |                          |     | 200  | ps |

## 7.10.5.10.1 GPMC and NOR Flash — Synchronous Mode

节 7.10.5.10.1.1 和 节 7.10.5.10.1.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 图 7-51 through 图 7-55).

## 7.10.5.10.1.1 GPMC and NOR Flash Timing Requirements — Synchronous Mode

| NO. | PARAMETER                    | DESCRIPTION <sup>(2)</sup>                                                                 | MODE <sup>(3)</sup>                                            | MIN                    | MAX | MIN                    | MAX | UNIT |
|-----|------------------------------|--------------------------------------------------------------------------------------------|----------------------------------------------------------------|------------------------|-----|------------------------|-----|------|
|     |                              |                                                                                            |                                                                | 100 MHz <sup>(4)</sup> |     | 133 MHz <sup>(4)</sup> |     |      |
| F12 | t <sub>su</sub> (dV-clkH)    | Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high               | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.81                   |     | 1.11                   |     | ns   |
|     |                              |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.06                   |     |                        | ns  |      |
| F13 | t <sub>h</sub> (clkH-dV)     | Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high                 | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.78                   |     | 2.28                   |     | ns   |
|     |                              |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.78                   |     |                        | ns  |      |
| F21 | t <sub>su</sub> (waitV-clkH) | Setup time, input wait GPMC_WAIT[j] valid before output clock GPMC_CLK high <sup>(1)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.81                   |     | 1.11                   |     | ns   |
|     |                              |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.06                   |     |                        | ns  |      |
| F22 | t <sub>h</sub> (clkH-waitV)  | Hold time, input wait GPMC_WAIT[j] valid after output clock GPMC_CLK high <sup>(1)</sup>   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.78                   |     | 2.28                   |     | ns   |
|     |                              |                                                                                            | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.78                   |     |                        | ns  |      |

(1) In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

(2) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.

(3) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency / (2 to 4)
- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = PER1\_PLL\_CLKOUT / 3 = 300 / 3 = 100 MHz

- For TIMEPARAGRANULARITY\_X1:
  - GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESTIME, PAGEBURSTACCESTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

(4) For 100 MHz:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = MAIN\_PLL2\_HSDIV1\_CLKOUT / 3

For 133 MHz:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = MAIN\_PLL0\_HSDIV3\_CLKOUT

#### 7.10.5.10.1.2 GPMC and NOR Flash Switching Characteristics – Synchronous Mode

| NO. <sup>(2)</sup> | PARAMETER                     | DESCRIPTION                                                                                                                                                                  | MODE <sup>(19)</sup>                                                          | MIN                              | MAX                     | MIN                              | MAX                     | UNI<br>T |
|--------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|----------------------------------|-------------------------|----------------------------------|-------------------------|----------|
|                    |                               |                                                                                                                                                                              |                                                                               | 100 MHz <sup>(20)</sup>          |                         | 133 MHz <sup>(20)</sup>          |                         |          |
| F0                 | tc(clk)                       | Period, output clock GPMC_CLK <sup>(18)</sup>                                                                                                                                | div_by_1_mode;<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                  | 10                               |                         | 7.52                             |                         | ns       |
| F1                 | t <sub>w</sub> (clkH)         | Typical pulse duration, output clock GPMC_CLK high                                                                                                                           | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | 0.475*P<br><sup>(15)</sup> - 0.3 |                         | 0.475*P<br><sup>(15)</sup> - 0.3 |                         | ns       |
| F1                 | t <sub>w</sub> (clkL)         | Typical pulse duration, output clock GPMC_CLK low                                                                                                                            | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | 0.475*P<br><sup>(15)</sup> - 0.3 |                         | 0.475*P<br><sup>(15)</sup> - 0.3 |                         | ns       |
| F2                 | t <sub>d</sub> (clkH-csnV)    | Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] transition <sup>(14)</sup>                                                                   | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | F <sup>(6)</sup> - 2.2           | F+3.75                  | F <sup>(6)</sup> - 2.2           | F <sup>(6)</sup> + 3.75 | ns       |
| F3                 | t <sub>d</sub> (clkH-CSn[i]V) | Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] invalid <sup>(14)</sup>                                                                      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | E <sup>(5)</sup> - 2.2           | E <sup>(5)</sup> + 3.75 | E <sup>(5)</sup> - 2.2           | E <sup>(5)</sup> + 3.75 | ns       |
| F4                 | t <sub>d</sub> (aV-clk)       | Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge                                                                                            | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | B <sup>(2)</sup> -2.3            | B <sup>(2)</sup> +4.5   | B <sup>(2)</sup> -2.3            | B <sup>(2)</sup> +4.5   | ns       |
| F5                 | t <sub>d</sub> (clkH-aV)      | Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid                                                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | - 2.3                            | 4.5                     | - 2.3                            | 4.5                     | ns       |
| F6                 | t <sub>d</sub> (be[x]nV-clk)  | Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge                    | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | B <sup>(2)</sup> -2.3            | B <sup>(2)</sup> +1.9   | B <sup>(2)</sup> -2.3            | B <sup>(2)</sup> +1.9   | ns       |
| F7                 | t <sub>d</sub> (clkH-be[x]nV) | Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid <sup>(11)</sup> | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | D <sup>(4)</sup> -2.3            | D <sup>(4)</sup> +1.9   | D <sup>(4)</sup> -2.3            | D <sup>(4)</sup> +1.9   | ns       |
| F7                 | t <sub>d</sub> (clkL-be[x]nV) | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid <sup>(12)</sup>                                                                                        | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | D <sup>(4)</sup> -2.3            | D <sup>(4)</sup> +1.9   | D <sup>(4)</sup> -2.3            | D <sup>(4)</sup> +1.9   | ns       |

| NO. <sup>(2)</sup> | PARAMETER                     | DESCRIPTION                                                                                                                                 | MODE <sup>(19)</sup>                                                          | MIN                     | MAX                    | MIN                     | MAX                    | UNIT |
|--------------------|-------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-------------------------|------------------------|-------------------------|------------------------|------|
|                    |                               |                                                                                                                                             |                                                                               | 100 MHz <sup>(20)</sup> |                        | 133 MHz <sup>(20)</sup> |                        |      |
| F7                 | $t_{d(\text{clkL-be}[x]nIV)}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid <sup>(13)</sup>                                                       | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +1.9  | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +1.9  | ns   |
| F8                 | $t_{d(\text{clkH-advn})}$     | Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition                     | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | G <sup>(7)</sup> -2.3   | G <sup>(7)</sup> +4.5  | G <sup>(7)</sup> -2.3   | G <sup>(7)</sup> +4.5  | ns   |
| F9                 | $t_{d(\text{clkH-advnIV})}$   | Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid                        | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay  | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +4.5  | D <sup>(4)</sup> -2.3   | D <sup>(4)</sup> +4.5  | ns   |
| F10                | $t_{d(\text{clkH-oen})}$      | Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition                                                      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | H <sup>(8)</sup> -2.3   | H <sup>(8)</sup> +3.5  | H <sup>(8)</sup> -2.3   | H <sup>(8)</sup> +3.5  | ns   |
| F11                | $t_{d(\text{clkH-oenIV})}$    | Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid                                                         | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | E <sup>(8)</sup> -2.3   | E <sup>(8)</sup> +3.5  | E <sup>(8)</sup> -2.3   | E <sup>(8)</sup> +3.5  | ns   |
| F14                | $t_{d(\text{clkH-wen})}$      | Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition                                                    | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1<br>no extra_delay | I <sup>(9)</sup> -2.3   | I <sup>(9)</sup> +4.5  | I <sup>(9)</sup> -2.3   | I <sup>(9)</sup> +4.5  | ns   |
| F15                | $t_{d(\text{clkH-do})}$       | Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition <sup>(11)</sup>                                       | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | ns   |
| F15                | $t_{d(\text{clkL-do})}$       | Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition <sup>(12)</sup>                                                      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | ns   |
| F15                | $t_{d(\text{clkL-do})}$       | Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition <sup>(13)</sup>                                                      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +2.7 | ns   |
| F17                | $t_{d(\text{clkH-be}[x]n)}$   | Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition <sup>(11)</sup> | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | ns   |
| F17                | $t_{d(\text{clkL-be}[x]n)}$   | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(12)</sup>                                                    | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | ns   |
| F17                | $t_{d(\text{clkL-be}[x]n)}$   | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(13)</sup>                                                    | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                   | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | J <sup>(10)</sup> -2.3  | J <sup>(10)</sup> +1.9 | ns   |
| F18                | $t_{w(\text{csnV})}$          | Pulse duration, output chip select GPMC_CSn[i] low <sup>(14)</sup>                                                                          | Read                                                                          | A <sup>(1)</sup>        |                        | A <sup>(1)</sup>        |                        | ns   |
|                    |                               |                                                                                                                                             | Write                                                                         | A <sup>(1)</sup>        |                        | A <sup>(1)</sup>        |                        | ns   |
| F19                | $t_{w(\text{be}[x]nV)}$       | Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low                     | Read                                                                          | C <sup>(3)</sup>        |                        | C <sup>(3)</sup>        |                        | ns   |
|                    |                               |                                                                                                                                             | Write                                                                         | C <sup>(3)</sup>        |                        | C <sup>(3)</sup>        |                        | ns   |

| NO.(2) | PARAMETER      | DESCRIPTION                                                                     | MODE(19) | MIN         | MAX | MIN         | MAX | UNIT |
|--------|----------------|---------------------------------------------------------------------------------|----------|-------------|-----|-------------|-----|------|
|        |                |                                                                                 |          | 100 MHz(20) |     | 133 MHz(20) |     |      |
| F20    | $t_{w(advnV)}$ | Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low | Read     | K(16)       |     | K(16)       |     | ns   |
|        |                |                                                                                 | Write    | K(16)       |     | K(16)       |     | ns   |

- (1) For single read:  $A = (CSRdOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$   
 For burst read:  $A = (CSRdOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$   
 For burst write:  $A = (CSWrOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$   
 With n being the page burst access number.

- (2)  $B = ClkActivationTime \times GPMC\_FCLK^{(17)}$

- (3) For single read:  $C = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$   
 For burst read:  $C = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$   
 For burst write:  $C = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$   
 With n being the page burst access number.

- (4) For single read:  $D = (RdCycleTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$   
 For burst read:  $D = (RdCycleTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$   
 For burst write:  $D = (WrCycleTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$

- (5) For single read:  $E = (CSRdOffTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$   
 For burst read:  $E = (CSRdOffTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$   
 For burst write:  $E = (CSWrOffTime - AccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(17)}$

- (6) For csn falling edge (CS activated):

- Case GPMCFCLKDIVIDER = 0:  
 $F = 0.5 \times CSEExtraDelay \times GPMC\_FCLK^{(17)}$
- Case GPMCFCLKDIVIDER = 1:  
 $F = 0.5 \times CSEExtraDelay \times GPMC\_FCLK^{(17)}$  if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)  
 $F = (1 + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:  
 $F = 0.5 \times CSEExtraDelay \times GPMC\_FCLK^{(17)}$  if ((CSOnTime - ClkActivationTime) is a multiple of 3)  
 $F = (1 + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK^{(17)}$  if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)  
 $F = (2 + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK^{(17)}$  if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

- (7) For ADV falling edge (ADV activated):

- Case GPMCFCLKDIVIDER = 0:  
 $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK^{(17)}$
- Case GPMCFCLKDIVIDER = 1:  
 $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK^{(17)}$  if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)  
 $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:  
 $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK^{(17)}$  if ((ADVOnTime - ClkActivationTime) is a multiple of 3)  
 $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK^{(17)}$  if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)  
 $G = (2 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK^{(17)}$  if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- Case GPMCFCLKDIVIDER = 0:  
 $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK^{(17)}$
- Case GPMCFCLKDIVIDER = 1:  
 $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK^{(17)}$  if (ClkActivationTime and ADVrOffTime are odd) or (ClkActivationTime and ADVrOffTime are even)  
 $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:  
 $G = 0.5 \times ADVExtraDelay \times GPMC\_FCLK^{(17)}$  if ((ADVrOffTime - ClkActivationTime) is a multiple of 3)  
 $G = (1 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK^{(17)}$  if ((ADVrOffTime - ClkActivationTime - 1) is a multiple of 3)  
 $G = (2 + 0.5 \times ADVExtraDelay) \times GPMC\_FCLK^{(17)}$  if ((ADVrOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GPMCFCLKDIVIDER = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GPMCFCLKDIVIDER = 0:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $H = (2 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $H = 0.5 \times \text{OEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - $H = (1 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $H = (2 + 0.5 \times \text{OEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) For WE falling edge (WE activated):

- Case GPMCFCLKDIVIDER = 0:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - $I = (1 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $I = (2 + 0.5 \times \text{WEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

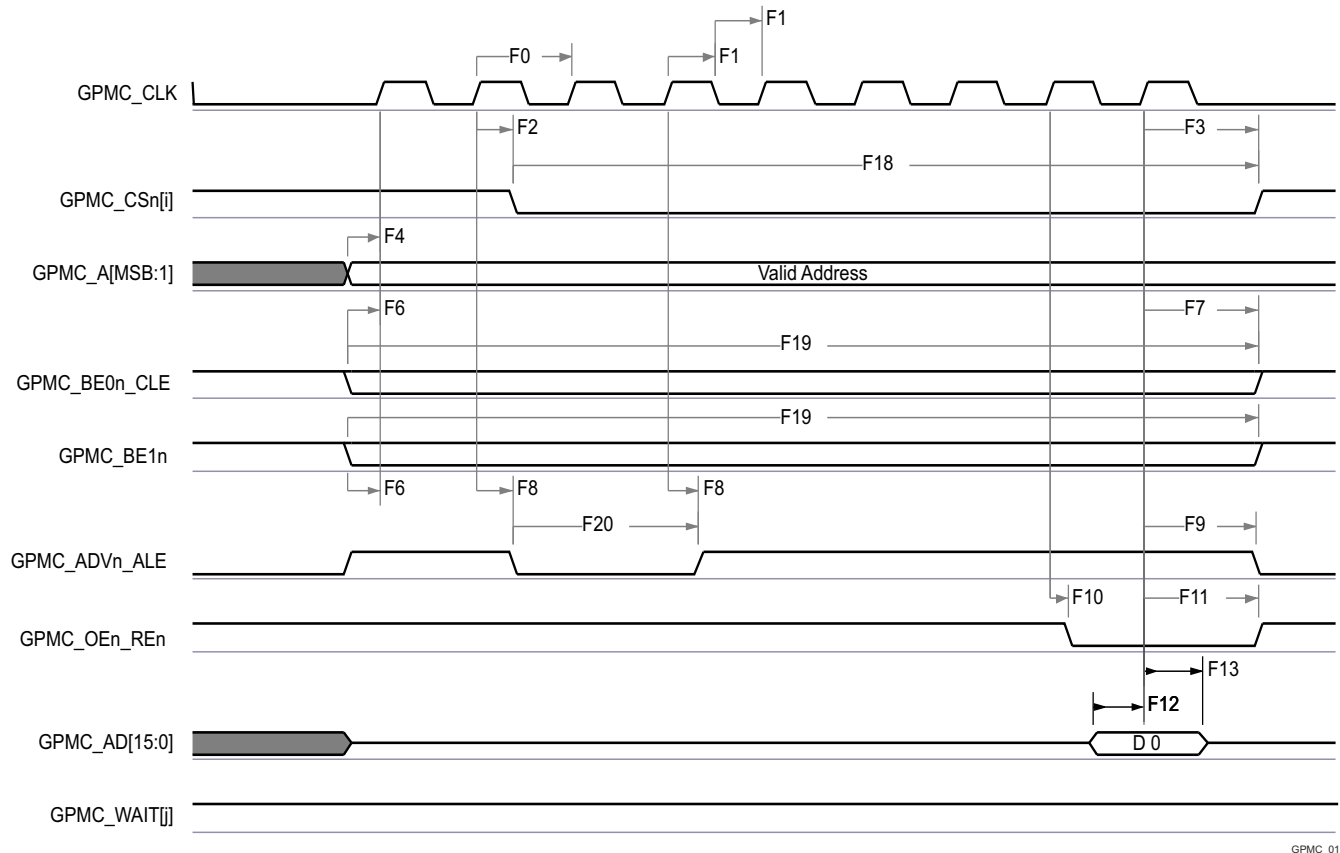
For WE rising edge (WE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $I = 0.5 \times \text{WEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)



- $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case  $\text{GPMCFCLKDIVIDER} = 2$ :
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{WEOffTime} - \text{ClkActivationTime})$  is a multiple of 3)
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)
  - $I = (2 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)
- (10)  $J = \text{GPMC\_FCLK}^{(17)}$
- (11) First transfer only for CLK DIV 1 mode.
- (12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.
- (13) Half cycle of  $\text{GPMC\_CLKOUT}$ ; for all data for modes other than CLK DIV 1 mode.  $\text{GPMC\_CLKOUT}$  divide down from  $\text{GPMC\_FCLK}$ .
- (14) In  $\text{GPMC\_CSn}[i]$ ,  $i$  is equal to 0, 1, 2, or 3. In  $\text{GPMC\_WAIT}[j]$ ,  $j$  is equal to 0, 1, 2, or 3.
- (15)  $P = \text{GPMC\_CLK}$  period in ns
- (16) For read:  $K = (\text{ADVrOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
For write:  $K = (\text{ADVWrOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$
- (17)  $\text{GPMC\_FCLK}$  is general-purpose memory controller internal functional clock period in ns.
- (18) Related to the  $\text{GPMC\_CLK}$  output clock maximum and minimum frequencies programmable in the GPMC module by setting the  $\text{GPMC\_CONFIG1\_i}$  configuration register bit field  $\text{GPMCFCLKDIVIDER}$ .
- (19) For  $\text{div\_by\_1\_mode}$ :
  - $\text{GPMC\_CONFIG1\_i}$  register:  $\text{GPMCFCLKDIVIDER} = 0h$ :
    - $\text{GPMC\_CLK}$  frequency =  $\text{GPMC\_FCLK}$  frequency
  - $\text{CTRLMMR\_GPMC\_CLKSEL}[1-0] \text{ CLK\_SEL} = 01 = \text{PER1\_PLL\_CLKOUT} / 3 = 300 / 3 = 100 \text{ MHz}$
  - $\text{GPMC\_CONFIG1\_i}$  Register:  $\text{TIMEPARAGRANULARITY} = 0h = x1$  latencies (affecting  $\text{RD}/\text{WRCYCLETIME}$ ,  $\text{RD}/\text{WRACCESSTIME}$ ,  $\text{PAGEBURSTACCESSTIME}$ ,  $\text{CSONTIME}$ ,  $\text{CSRd}/\text{WROFFTIME}$ ,  $\text{ADVONTIME}$ ,  $\text{ADVrd}/\text{WROFFTIME}$ ,  $\text{OEONTIME}$ ,  $\text{OEOFFTIME}$ ,  $\text{WEONTIME}$ ,  $\text{WEOFFTIME}$ ,  $\text{CYCLE2CYCLEDELAY}$ ,  $\text{BUSTURNAROUND}$ ,  $\text{TIMEOUTSTARTVALUE}$ ,  $\text{WRDATAONADMUXBUS}$ )
- For no extra\_delay:
  - $\text{GPMC\_CONFIG2\_i}$  Register:  $\text{CSEXTRADELAY} = 0h = \text{CSn}$  Timing control signal is not delayed
  - $\text{GPMC\_CONFIG4\_i}$  Register:  $\text{WEEEXTRADELAY} = 0h = n\text{WE}$  timing control signal is not delayed
  - $\text{GPMC\_CONFIG4\_i}$  Register:  $\text{OEEXTRADELAY} = 0h = n\text{OE}$  timing control signal is not delayed
  - $\text{GPMC\_CONFIG3\_i}$  Register:  $\text{ADVEXTRADELAY} = 0h = n\text{ADV}$  timing control signal is not delayed
- (20) For 100 MHz:
  - $\text{CTRLMMR\_GPMC\_CLKSEL}[1-0] \text{ CLK\_SEL} = 01 = \text{MAIN\_PLL2\_HSDIV1\_CLKOUT} / 3$
- For 133 MHz:
  - $\text{CTRLMMR\_GPMC\_CLKSEL}[1-0] \text{ CLK\_SEL} = 00 = \text{MAIN\_PLL0\_HSDIV3\_CLKOUT}$

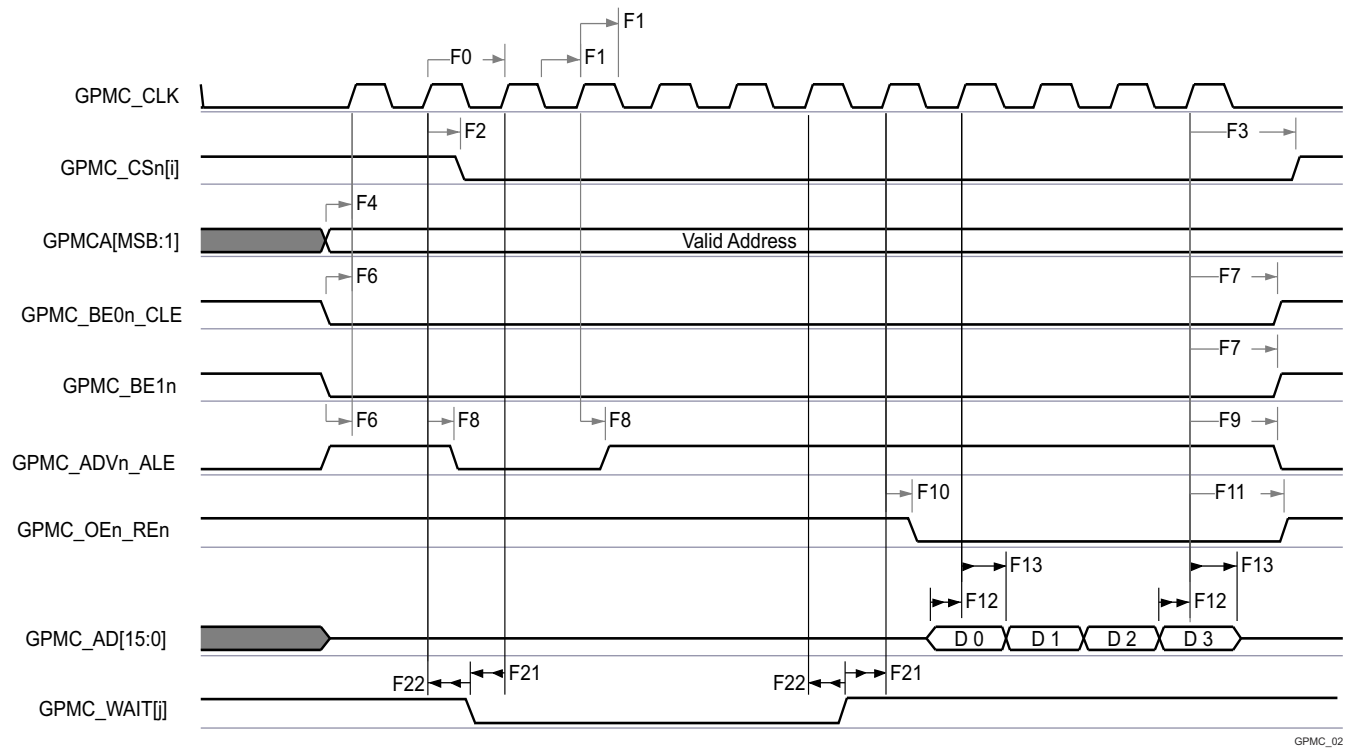




GPMC\_01

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.  
 B. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

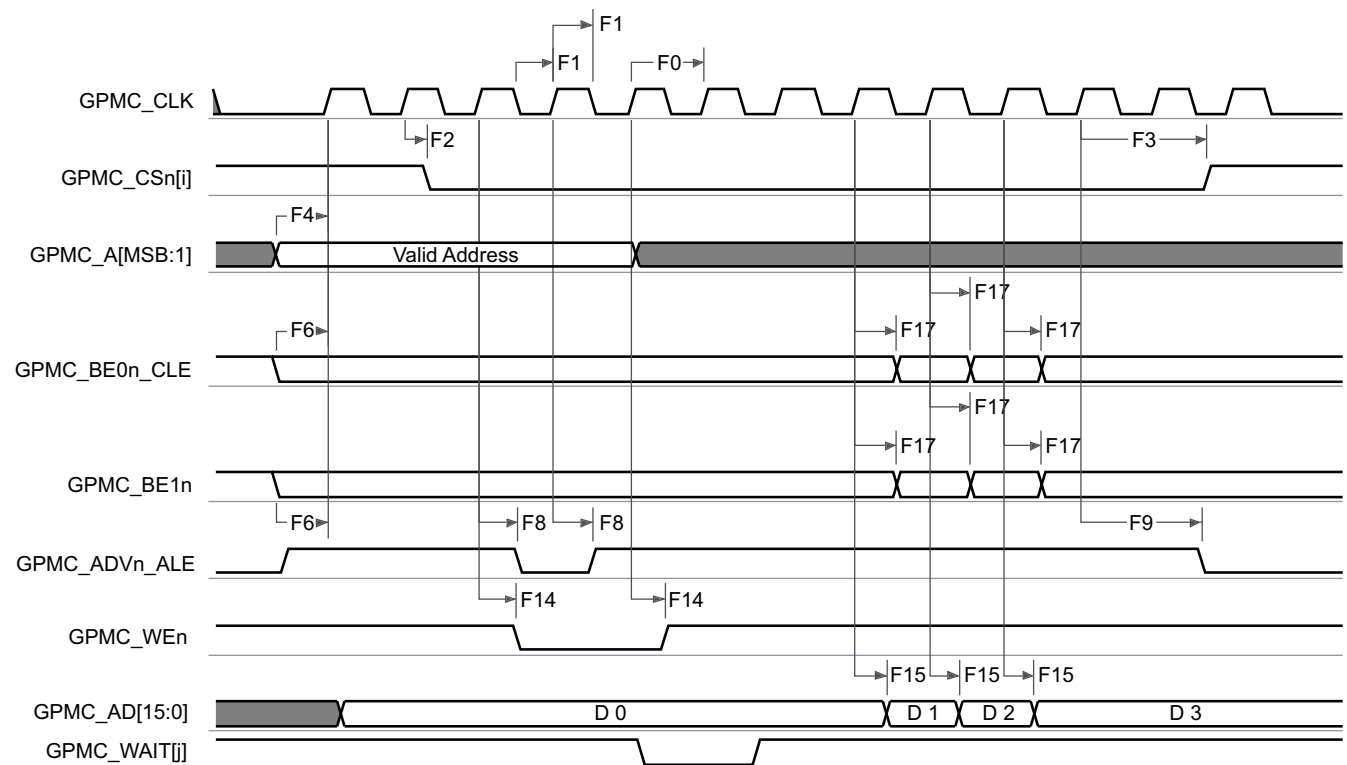
**图 7-51. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)**



GPMC\_02

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.  
B. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

**图 7-52. GPMC and NOR Flash — Synchronous Burst Read — 4x16 - bit (GPMCFCLKDIVIDER = 0)**

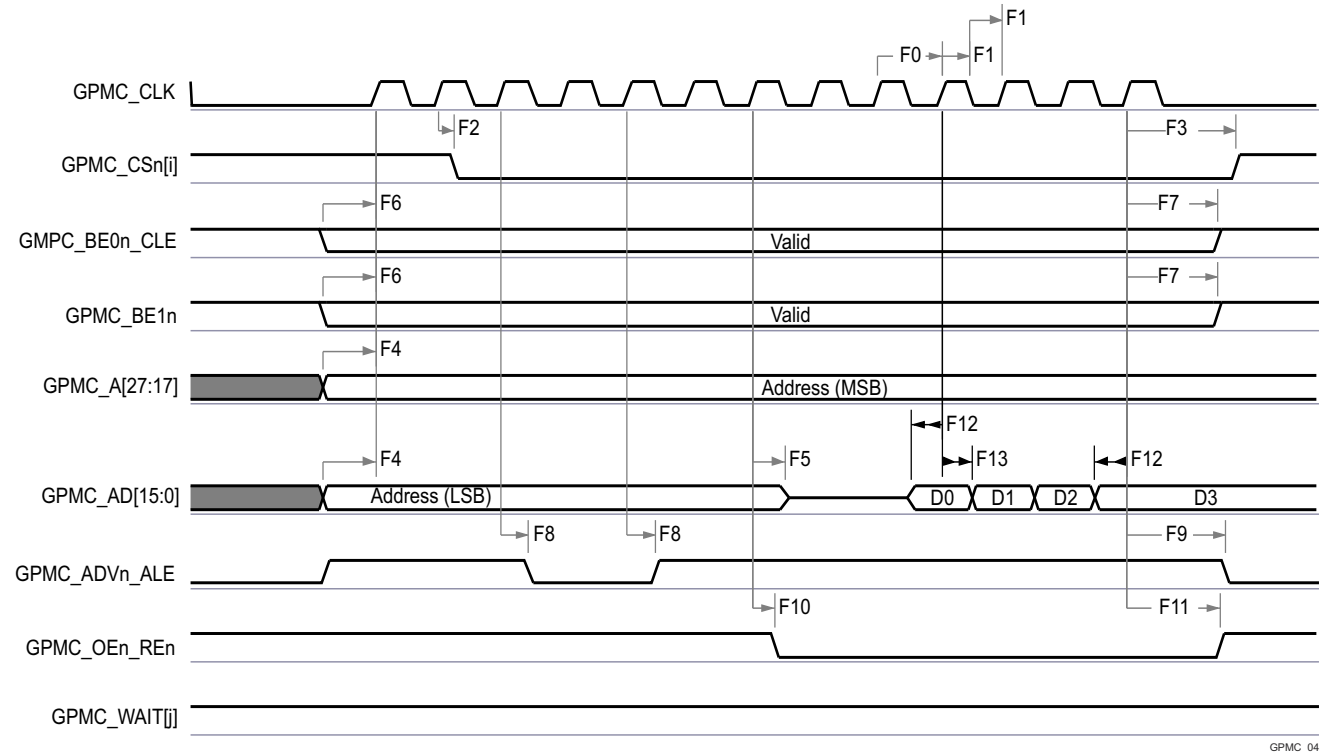


GPMC\_03

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

图 7-53. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)

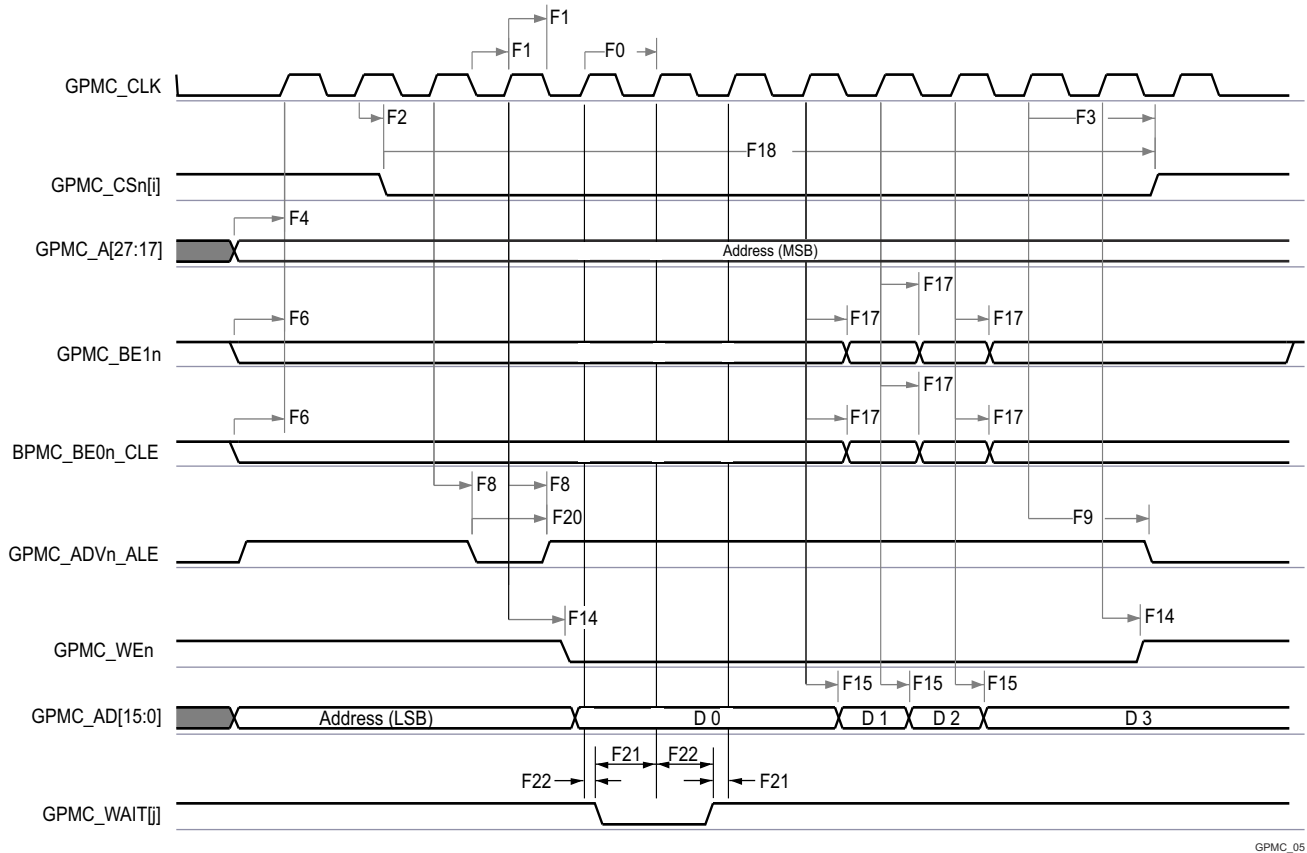


GPMC\_04

A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

图 7-54. GPMC and Multiplexed NOR Flash — Synchronous Burst Read



GPMC\_05

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.  
B. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

**图 7-55. GPMC and Multiplexed NOR Flash — Synchronous Burst Write**

#### 7.10.5.10.2 GPMC and NOR Flash — Asynchronous Mode

节 7.10.5.10.2.1 和 节 7.10.5.10.2.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 图 7-56 through 图 7-61).

##### 7.10.5.10.2.1 GPMC and NOR Flash Timing Requirements - Asynchronous Mode

| NO.                 |                      |                                       | MODE <sup>(7)</sup>                                             | MIN | MAX              | UNIT |
|---------------------|----------------------|---------------------------------------|-----------------------------------------------------------------|-----|------------------|------|
| FA5 <sup>(1)</sup>  | $t_{acc(d)}$         | Data access time                      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X<br>1 |     | H <sup>(5)</sup> | ns   |
| FA20 <sup>(2)</sup> | $t_{acc1-pgmode(d)}$ | Page mode successive data access time | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X<br>1 |     | P <sup>(4)</sup> | ns   |
| FA21 <sup>(3)</sup> | $t_{acc2-pgmode(d)}$ | Page mode first data access time      | div_by_1_mode<br>; GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X<br>1 |     | H <sup>(5)</sup> | ns   |

- (1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.  
(2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.

- (3) The FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.
- (4)  $P = \text{PageBurstAccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(6)}$
- (5)  $H = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(6)}$
- (6) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (7) For div\_by\_1\_mode:
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
    - GPMC\_CLK frequency = GPMC\_FCLK frequency
  - CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHS DIV\_CLKOUT3 = 2000/15 = 133.33 MHz
  - GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

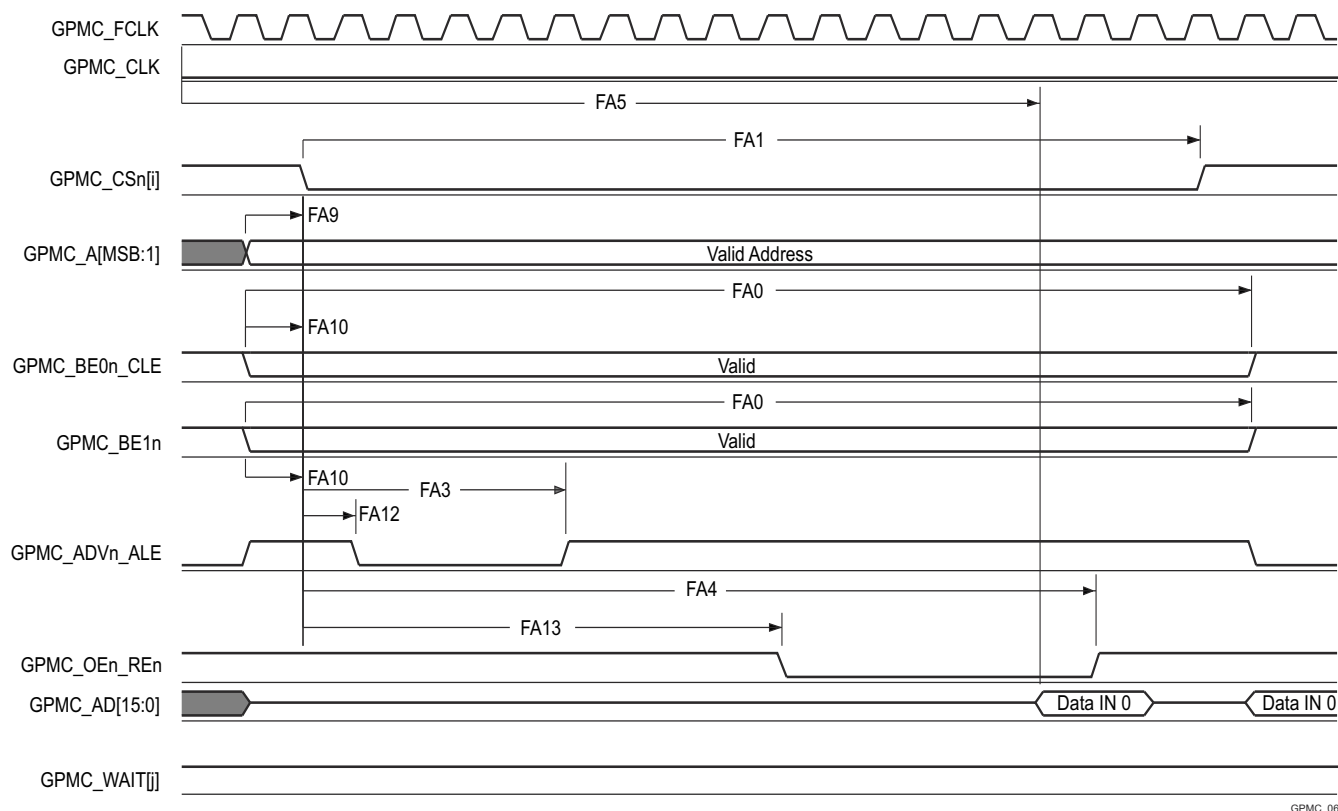
#### 7.10.5.10.2.2 GPMC and NOR Flash Switching Characteristics - Asynchronous Mode

| NO.  | PARAMETER                           | DESCRIPTION                                                                                                                                                                                     | MODE <sup>(15)</sup>                                       | MIN                                             | MAX                      | UNIT |
|------|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------|--------------------------|------|
|      |                                     |                                                                                                                                                                                                 |                                                            | 133 MHz <sup>(16)</sup>                         |                          |      |
| FA0  | $t_{w(\text{be}[x]nV)}$             | Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time                                                                  | Read                                                       | N <sup>(12)</sup>                               |                          | ns   |
|      |                                     |                                                                                                                                                                                                 | Write                                                      | N <sup>(12)</sup>                               |                          |      |
| FA1  | $t_{w(\text{csn}V)}$                | Pulse duration, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> low                                                                                                            | Read                                                       | A <sup>(1)</sup>                                |                          | ns   |
|      |                                     |                                                                                                                                                                                                 | Write                                                      | A <sup>(1)</sup>                                |                          |      |
| FA3  | $t_{d(\text{csn}V\text{-advn}IV)}$  | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADV <i>n</i> _ALE invalid                              | Read                                                       | B <sup>(2)</sup> - 2.55                         | B <sup>(2)</sup> + 2.65  | ns   |
|      |                                     |                                                                                                                                                                                                 | Write                                                      | B <sup>(2)</sup> - 2.55                         | B <sup>(2)</sup> + 2.65  |      |
| FA4  | $t_{d(\text{csn}V\text{-oen}IV)}$   | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output enable GPMC_OEn_RE <i>n</i> invalid (Single read)                                                  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | C <sup>(3)</sup> - 2.55 C <sup>(3)</sup> + 2.65 |                          | ns   |
| FA9  | $t_{d(aV\text{-csn}V)}$             | Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid                                                                         | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J <sup>(9)</sup> - 2.55 J <sup>(9)</sup> + 2.65 |                          | ns   |
| FA10 | $t_{d(\text{be}[x]nV\text{-csn}V)}$ | Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J <sup>(9)</sup> - 2.55 J <sup>(9)</sup> + 2.65 |                          | ns   |
| FA12 | $t_{d(\text{csn}V\text{-advn}V)}$   | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADV <i>n</i> _ALE valid                                | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | K <sup>(10)</sup> - 2.55                        | K <sup>(10)</sup> + 2.65 | ns   |
| FA13 | $t_{d(\text{csn}V\text{-oen}V)}$    | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output enable GPMC_OEn_RE <i>n</i> valid                                                                  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | L <sup>(11)</sup> - 2.55                        | L <sup>(11)</sup> + 2.65 | ns   |
| FA16 | $t_{w(aI}V)$                        | Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses                                                                                                 | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | G <sup>(7)</sup>                                |                          | ns   |
| FA18 | $t_{d(\text{csn}V\text{-oen}IV)}$   | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output enable GPMC_OEn_RE <i>n</i> invalid (Burst read)                                                   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | I <sup>(8)</sup> - 2.55 I <sup>(8)</sup> + 2.65 |                          | ns   |

| NO.  | PARAMETER                  | DESCRIPTION                                                                                                                | MODE <sup>(15)</sup>                                       | MIN                                             | MAX | UNIT |
|------|----------------------------|----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------|-----|------|
|      |                            |                                                                                                                            |                                                            | 133 MHz <sup>(16)</sup>                         |     |      |
| FA20 | t <sub>w(aV)</sub>         | Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses                                             | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | D <sup>(4)</sup>                                |     | ns   |
| FA25 | t <sub>d(csnV-wenV)</sub>  | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output write enable GPMC_WEn valid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | E <sup>(5)</sup> - 2.55 E <sup>(5)</sup> + 2.65 |     | ns   |
| FA27 | t <sub>d(csnV-wenIV)</sub> | Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid to output write enable GPMC_WEn invalid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | F <sup>(6)</sup> - 2.55 F <sup>(6)</sup> + 2.65 |     | ns   |
| FA28 | t <sub>d(wenV-dV)</sub>    | Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 2.65                                            |     | ns   |
| FA29 | t <sub>d(dV-csnV)</sub>    | Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(13)</sup> valid      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | J <sup>(9)</sup> - 2.55 J <sup>(9)</sup> + 2.65 |     | ns   |
| FA37 | t <sub>d(oenV-aIV)</sub>   | Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end                                     | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 2.65                                            |     | ns   |

- (1) For single read:  $A = (CSRdOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For single write:  $A = (CSWrOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst read:  $A = (CSRdOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst write:  $A = (CSWrOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
with n being the page burst access number
- (2) For reading:  $B = ((ADVrdOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
For writing:  $B = ((ADVwrOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (3)  $C = ((OEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (4)  $D = PageBurstAccessTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$
- (5)  $E = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (6)  $F = ((WEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (7)  $G = Cycle2CycleDelay \times GPMC\_FCLK^{(14)}$
- (8)  $I = ((OEOffTime + (n - 1) \times PageBurstAccessTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (9)  $J = (CSOnTime \times (TimeParaGranularity + 1) + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK^{(14)}$
- (10)  $K = ((ADVOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (11)  $L = ((OEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (12) For single read:  $N = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For single write:  $N = WrCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst read:  $N = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst write:  $N = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$
- (13) In GPMC\_CS*n*[*j*], i is equal to 0, 1, 2 or 3.
- (14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (15) For div\_by\_1\_mode:
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
- GPMC\_CLK frequency = GPMC\_FCLK frequency
  - CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHSIDV\_CLKOUT3 = 2000/15 = 133.33 MHz
  - GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRd/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOffTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)
- (16) For 133 MHz:

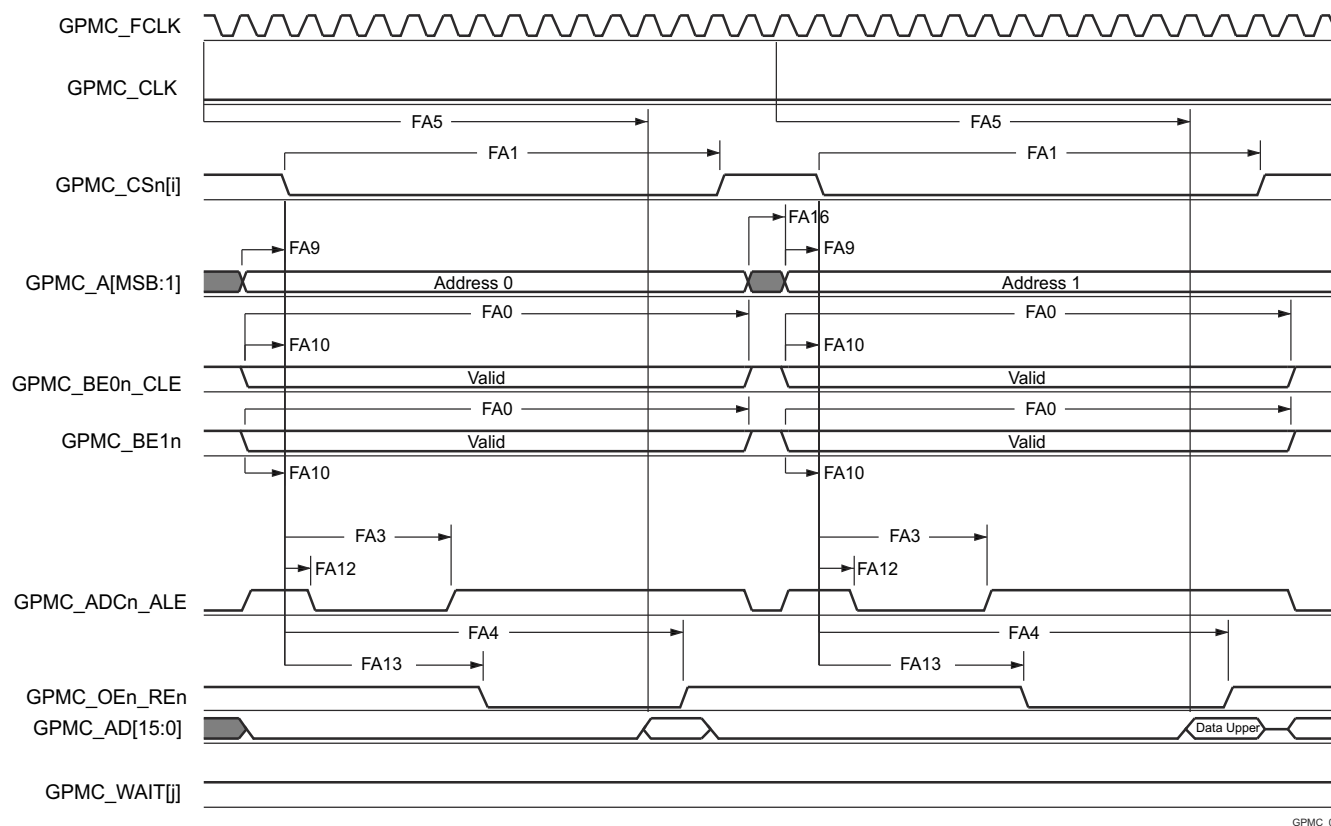
- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = MAIN\_PLL0\_HSDIV3\_CLKOUT



GPMC\_06

- In GPMC\_CS[n], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

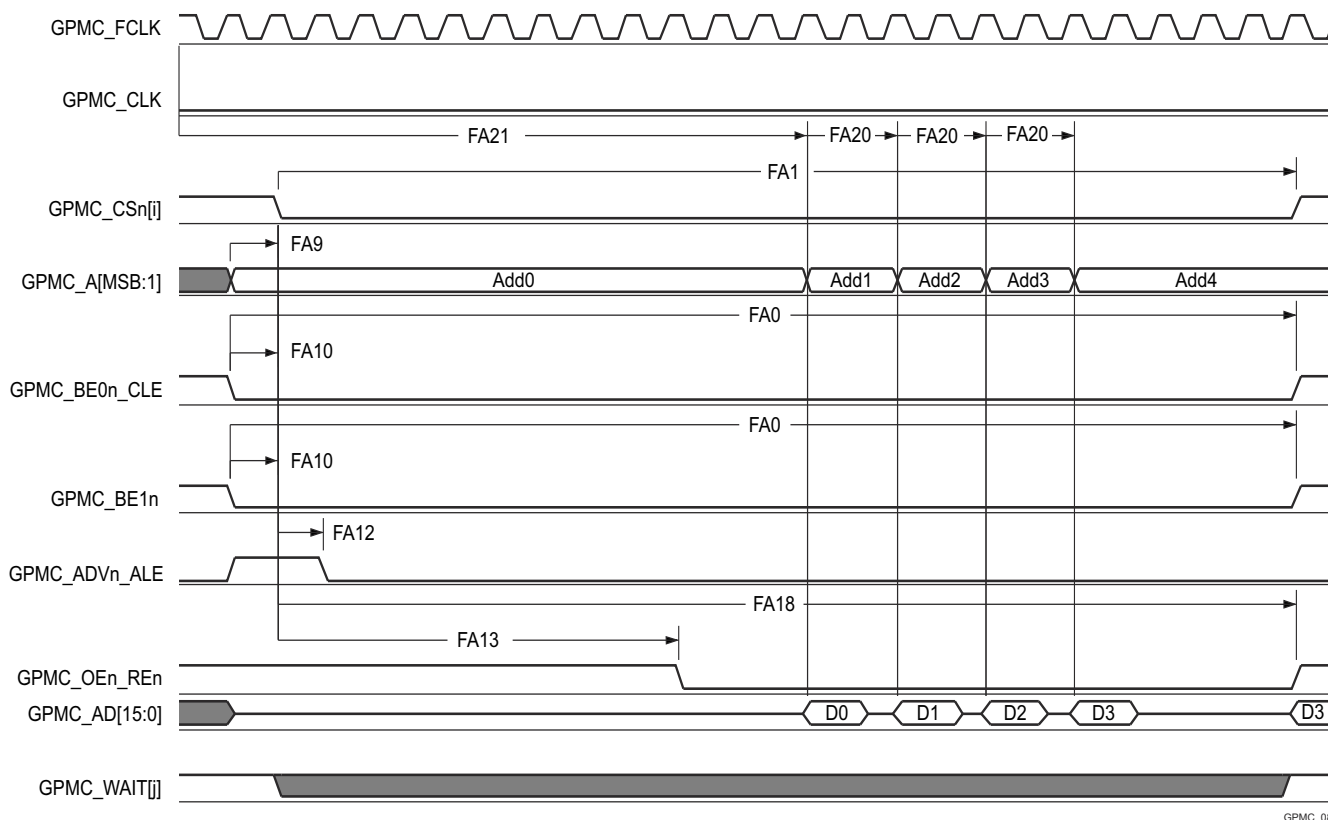
**图 7-56. GPMC and NOR Flash — Asynchronous Read — Single Word**



- A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**图 7-57. GPMC and NOR Flash — Asynchronous Read — 32 - Bit**

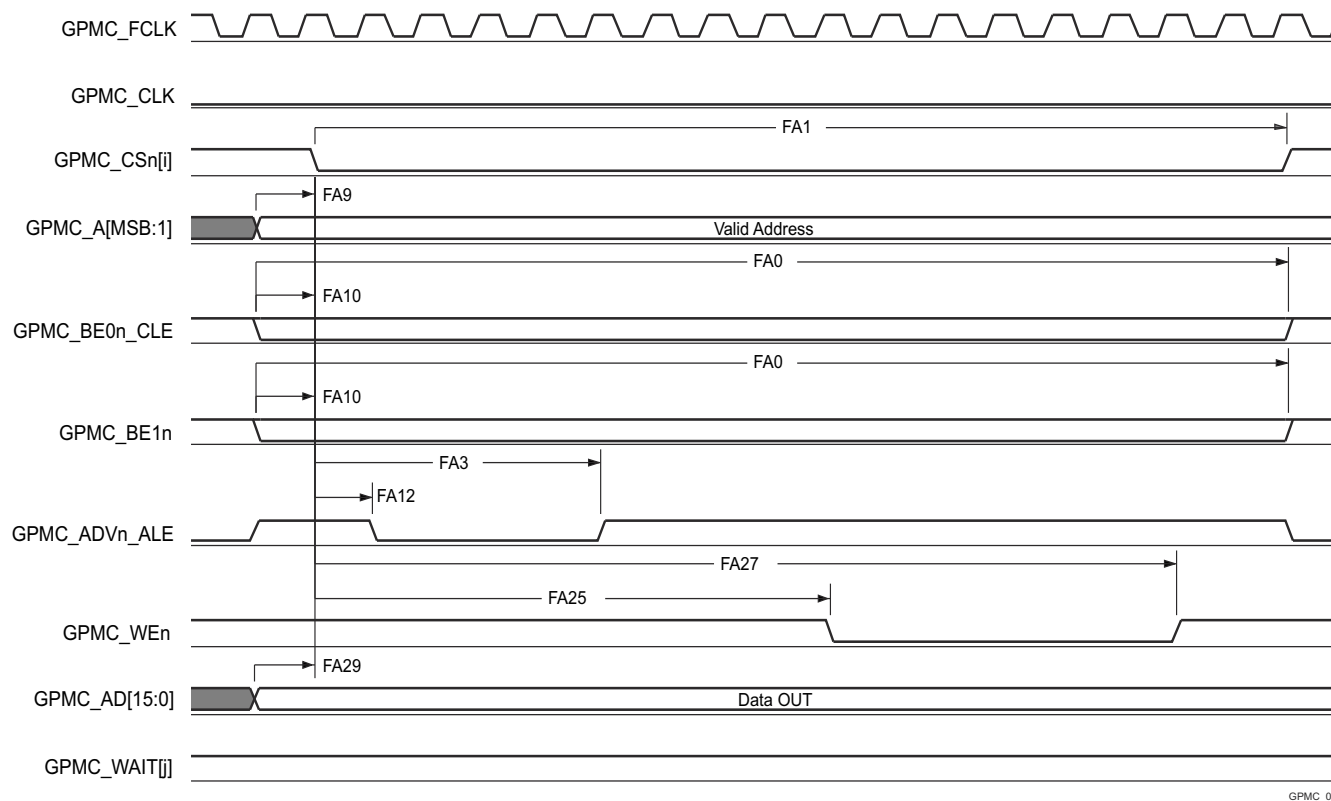




GPMC\_08

- A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.
- B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
- C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
- D. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

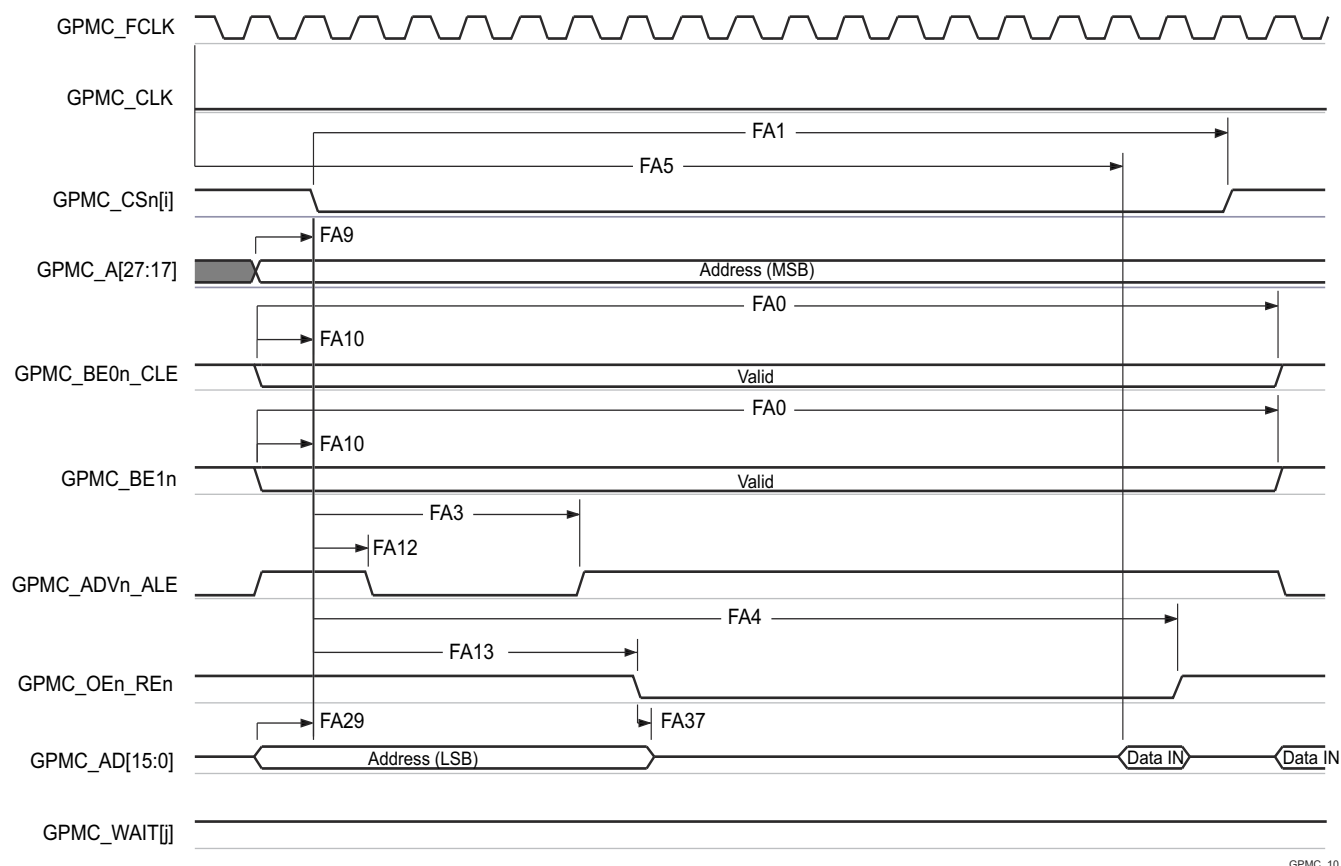
**图 7-58. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16 - Bit**



GPMC\_09

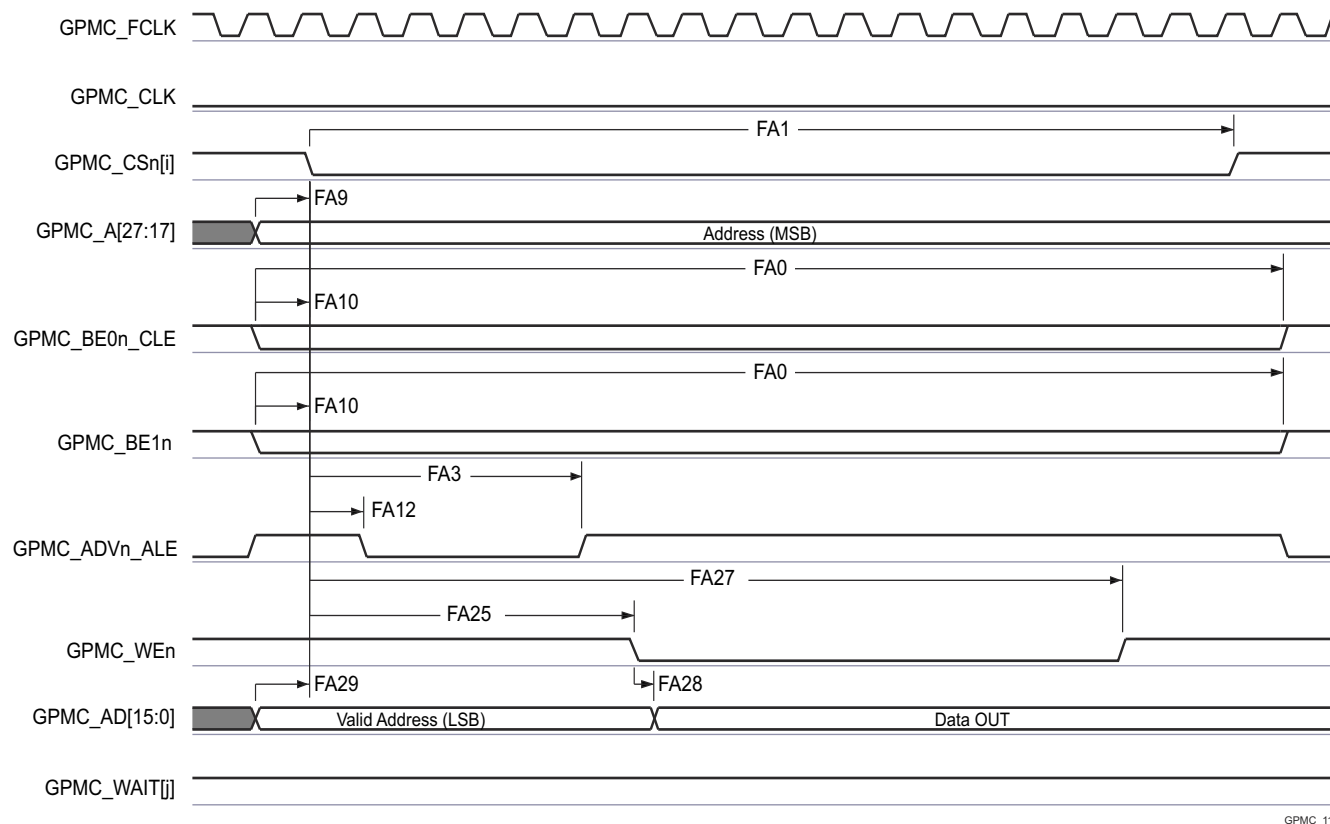
A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

**图 7-59. GPMC and NOR Flash — Asynchronous Write — Single Word**



- In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**图 7-60. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word**



GPMC\_11

A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

图 7-61. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word

### 7.10.5.10.3 GPMC and NAND Flash — Asynchronous Mode

节 7.10.5.10.3.1 和 节 7.10.5.10.3.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 图 7-62 through 图 7-65).

#### 7.10.5.10.3.1 GPMC and NAND Flash Timing Requirements - Asynchronous Mode

| NO.                  |                     | MODE <sup>(4)</sup>                                  | MIN                                                        | MAX | UNIT                |
|----------------------|---------------------|------------------------------------------------------|------------------------------------------------------------|-----|---------------------|
|                      |                     |                                                      | 133 MHz <sup>(5)</sup>                                     |     |                     |
| GNF12 <sup>(1)</sup> | t <sub>acc(d)</sub> | Access time, input data GPMC_AD[15:0] <sup>(3)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |     | J <sup>(2)</sup> ns |

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2)  $J = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(3)}$

(3) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

(4) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
- GPMC\_CLK frequency = GPMC\_FCLK frequency
- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHSIDIV\_CLKOUT3 = 2000/15 = 133.33 MHz
- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

(5) For 133 MHz:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = MAIN\_PLL0\_HSDIV3\_CLKOUT

#### 7.10.5.10.3.2 GPMC and NAND Flash Switching Characteristics - Asynchronous Mode

| NO.  | PARAMETER                   |                                                                                                                             | MODE <sup>(15)</sup>                                       | MIN                     | MAX                     | UNIT |
|------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|-------------------------|-------------------------|------|
|      |                             |                                                                                                                             |                                                            | 133 MHz <sup>(16)</sup> |                         |      |
| GNF0 | t <sub>w(wenV)</sub>        | Pulse duration, output write enable GPMC_WEn valid                                                                          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | A <sup>(1)</sup>        |                         | ns   |
| GNF1 | t <sub>d(csnV-wenV)</sub>   | Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output write enable GPMC_WEn valid                       | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | B <sup>(2)</sup> - 2.55 | B <sup>(2)</sup> + 2.65 | ns   |
| GNF2 | t <sub>w(cleH-wenV)</sub>   | Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | C <sup>(3)</sup> - 2.55 | C <sup>(3)</sup> + 2.65 | ns   |
| GNF3 | t <sub>w(wenV-dV)</sub>     | Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid                                           | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | D <sup>(4)</sup> - 2.55 | D <sup>(4)</sup> + 2.65 | ns   |
| GNF4 | t <sub>w(wenIV-dIV)</sub>   | Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid                                       | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | E <sup>(5)</sup> - 2.55 | E <sup>(5)</sup> + 2.65 | ns   |
| GNF5 | t <sub>w(wenIV-cleIV)</sub> | Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | F <sup>(6)</sup> - 2.55 | F <sup>(6)</sup> + 2.65 | ns   |

| NO.   | PARAMETER                     |                                                                                                                         | MODE <sup>(15)</sup>                                       | MIN                      | MAX                      | UNIT |
|-------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|--------------------------|--------------------------|------|
|       |                               |                                                                                                                         |                                                            | 133 MHz <sup>(16)</sup>  |                          |      |
| GNF6  | t <sub>w(wenIV-CSn[i]V)</sub> | Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CSn[i] <sup>(13)</sup> invalid              | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | G <sup>(7)</sup> - 2.55  | G <sup>(7)</sup> + 2.65  | ns   |
| GNF7  | t <sub>w(aleH-wenV)</sub>     | Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | C <sup>(3)</sup> - 2.55  | C <sup>(3)</sup> + 2.65  | ns   |
| GNF8  | t <sub>w(wenIV-aleIV)</sub>   | Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | F <sup>(6)</sup> - 2.55  | F <sup>(6)</sup> + 2.65  | ns   |
| GNF9  | t <sub>c(wen)</sub>           | Cycle time, write                                                                                                       | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | H <sup>(8)</sup>         |                          | ns   |
| GNF10 | t <sub>d(csnV-oenV)</sub>     | Delay time, output chip select GPMC_CSn[i] <sup>(13)</sup> valid to output enable GPMC_OEn_REn valid                    | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | I <sup>(9)</sup> - 2.55  | I <sup>(9)</sup> + 2.65  | ns   |
| GNF13 | t <sub>w(oenV)</sub>          | Pulse duration, output enable GPMC_OEn_REn valid                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | K <sup>(10)</sup>        |                          | ns   |
| GNF14 | t <sub>c(oen)</sub>           | Cycle time, read                                                                                                        | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | L <sup>(11)</sup>        |                          | ns   |
| GNF15 | t <sub>w(oenIV-CSn[i]V)</sub> | Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CSn[i] <sup>(13)</sup> invalid                | div_by_1_mode;                                             | M <sup>(12)</sup> - 2.55 | M <sup>(12)</sup> + 2.65 | ns   |

- (1)  $A = (WEOffTime - WEOntime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
(2)  $B = ((WEOntime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(3)  $C = ((WEOntime - ADVOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - ADVExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(4)  $D = (WEOntime \times (TimeParaGranularity + 1) + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK^{(14)}$   
(5)  $E = ((WrCycleTime - WEOffTime) \times (TimeParaGranularity + 1) - 0.5 \times WEEExtraDelay) \times GPMC\_FCLK^{(14)}$   
(6)  $F = ((ADVWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - WEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(7)  $G = ((CSWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - WEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(8)  $H = WrCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
(9)  $I = ((OEOntime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(10)  $K = (OEOffTime - OEOntime) \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
(11)  $L = RdCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
(12)  $M = ((CSRdOffTime - OEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - OEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(13) In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3.  
(14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.  
(15) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
- GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHS

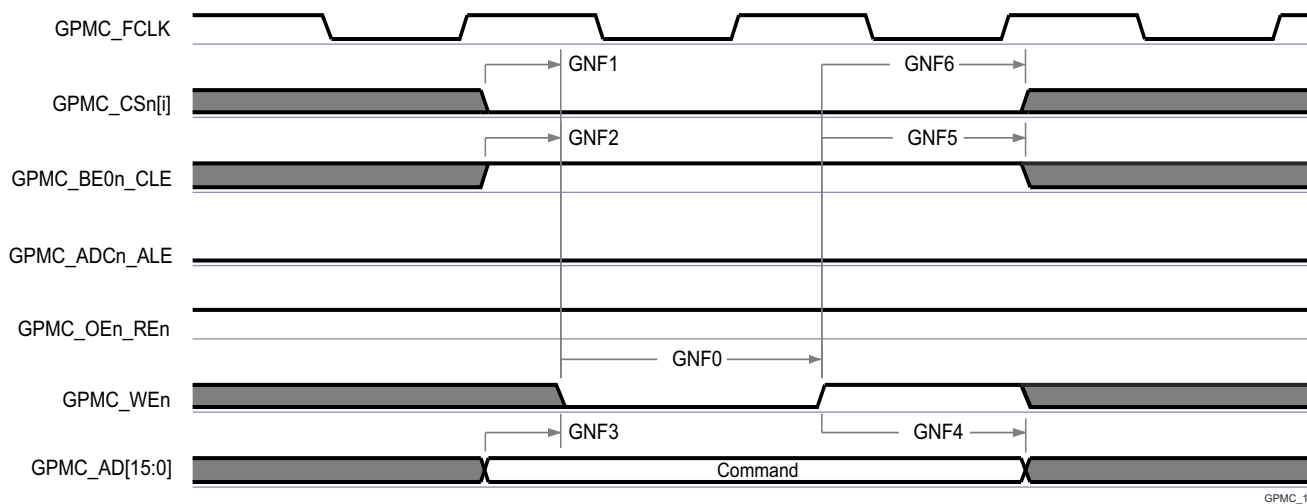
\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRd/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEOntime, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

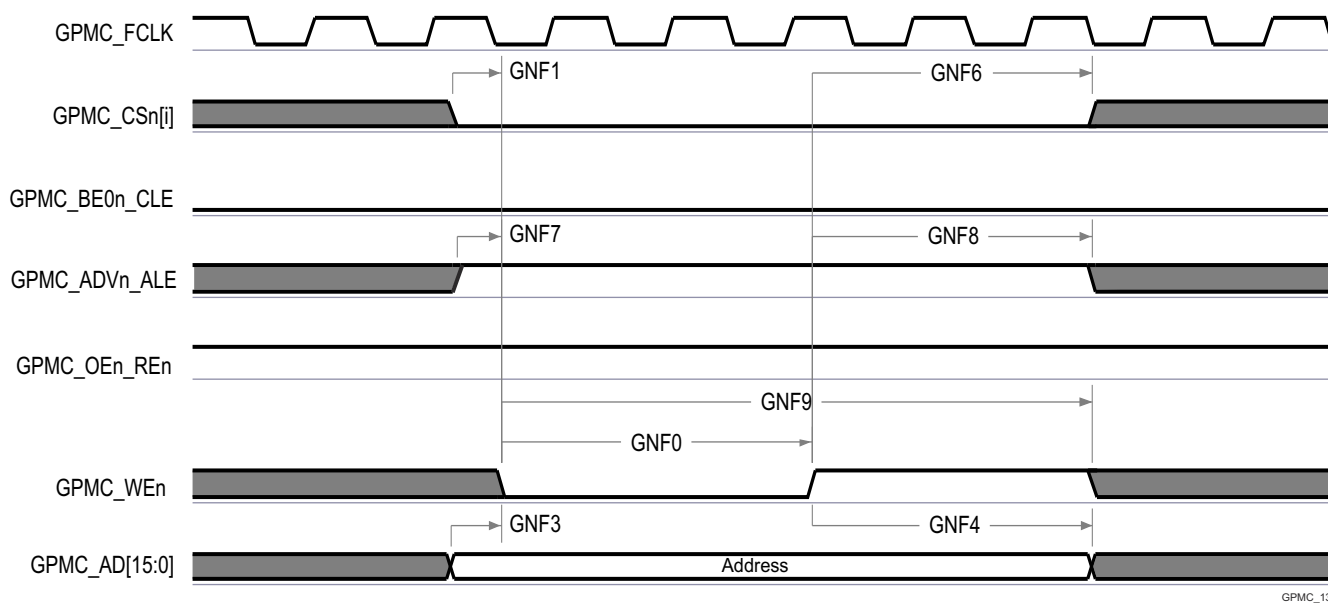
- (16) For 133 MHz:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = MAIN\_PLL0\_HSDIV3\_CLKOUT



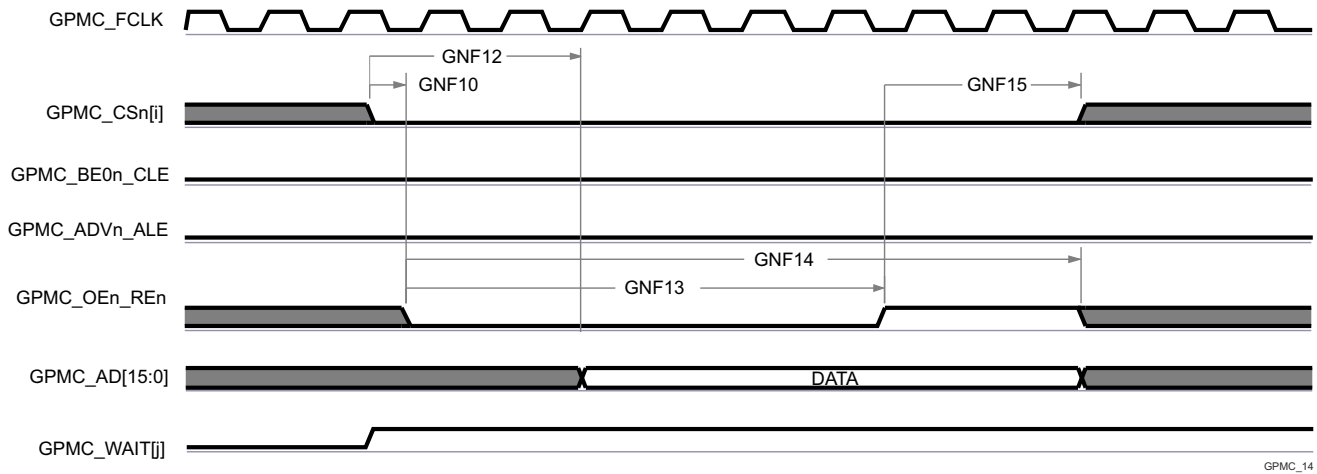
A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

图 7-62. GPMC and NAND Flash — Command Latch Cycle



A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

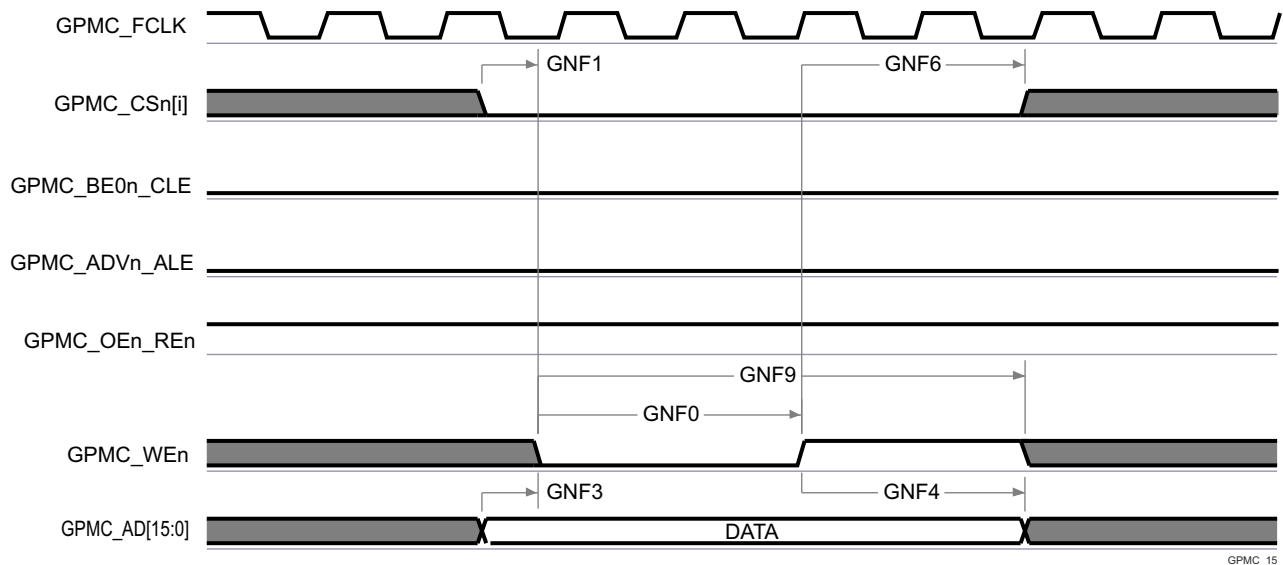
图 7-63. GPMC and NAND Flash — Address Latch Cycle



GPMC\_14

- A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- B. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.
- C. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0, 1, 2, or 3.

图 7-64. GPMC and NAND Flash — Data Read Cycle



GPMC\_15

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

图 7-65. GPMC and NAND Flash — Data Write Cycle

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.10.4 GPMC0 IOSET

表 7-40 present the specific groupings of signals (IOSET) for use with GPMC0.

表 7-40. GPMC0 IOSET

| Signals     | IOSET1         |     | IOSET2     |     |
|-------------|----------------|-----|------------|-----|
|             | BALL NAME      | MUX | BALL NAME  | MUX |
| GPMC0_WAIT2 | MDIO0_MDC      | 8   | MDIO0_MDC  | 8   |
| GPMC0_BE1n  | PRG1_PRU0_GPO0 | 8   | RGMII6_RD1 | 8   |



表 7-40. GPMC0 IOSET (continued)

| Signals        | IOSET1          |     | IOSET2          |     |
|----------------|-----------------|-----|-----------------|-----|
|                | BALL NAME       | MUX | BALL NAME       | MUX |
| GPMC0_WAIT0    | PRG1_PRU0_GPO1  | 8   | PRG1_PRU0_GPO1  | 8   |
| GPMC0_WAIT1    | PRG1_PRU0_GPO2  | 8   | PRG1_PRU0_GPO2  | 8   |
| GPMC0_DIR      | PRG1_PRU0_GPO3  | 8   | PRG1_PRU0_GPO3  | 8   |
| GPMC0_CSn2     | PRG1_PRU0_GPO4  | 8   | PRG1_PRU0_GPO4  | 8   |
| GPMC0_WEn      | PRG1_PRU0_GPO5  | 8   | PRG1_PRU0_GPO5  | 8   |
| GPMC0_CSn3     | PRG1_PRU0_GPO6  | 8   | PRG1_PRU0_GPO6  | 8   |
| GPMC0_OEn_REn  | PRG1_PRU0_GPO8  | 8   | PRG1_PRU0_GPO8  | 8   |
| GPMC0_ADVn_ALE | PRG1_PRU0_GPO9  | 8   | PRG1_PRU0_GPO9  | 8   |
| GPMC0_BE0n_CLE | PRG1_PRU0_GPO10 | 8   | PRG1_PRU0_GPO10 | 8   |
| GPMC0_WPn      | PRG1_PRU1_GPO5  | 8   | PRG1_PRU1_GPO5  | 8   |
| GPMC0_CSn1     | PRG1_PRU1_GPO8  | 8   | PRG1_PRU1_GPO8  | 8   |
| GPMC0_CSn0     | PRG1_PRU1_GPO9  | 8   | PRG1_PRU1_GPO9  | 8   |
| GPMC0_CLKOUT   | PRG1_PRU1_GPO10 | 8   | PRG1_PRU1_GPO10 | 8   |
| GPMC0_AD0      | PRG0_PRU0_GPO5  | 8   | PRG0_PRU0_GPO5  | 8   |
| GPMC0_AD1      | PRG0_PRU0_GPO7  | 8   | PRG0_PRU0_GPO7  | 8   |
| GPMC0_AD2      | PRG0_PRU0_GPO8  | 8   | PRG0_PRU0_GPO8  | 8   |
| GPMC0_AD3      | PRG0_PRU0_GPO9  | 8   | PRG0_PRU0_GPO9  | 8   |
| GPMC0_AD4      | PRG0_PRU0_GPO10 | 8   | PRG0_PRU0_GPO10 | 8   |
| GPMC0_AD5      | PRG0_PRU0_GPO17 | 8   | PRG0_PRU0_GPO17 | 8   |
| GPMC0_AD6      | PRG0_PRU0_GPO18 | 8   | PRG0_PRU0_GPO18 | 8   |
| GPMC0_AD7      | PRG0_PRU0_GPO19 | 8   | PRG0_PRU0_GPO19 | 8   |
| GPMC0_AD8      | PRG0_PRU1_GPO5  | 8   | PRG0_PRU1_GPO5  | 8   |
| GPMC0_AD9      | PRG0_PRU1_GPO7  | 8   | PRG0_PRU1_GPO7  | 8   |
| GPMC0_AD10     | PRG0_PRU1_GPO8  | 8   | PRG0_PRU1_GPO8  | 8   |
| GPMC0_AD11     | PRG0_PRU1_GPO9  | 8   | PRG0_PRU1_GPO9  | 8   |
| GPMC0_AD12     | PRG0_PRU1_GPO10 | 8   | PRG0_PRU1_GPO10 | 8   |
| GPMC0_AD13     | PRG0_PRU1_GPO17 | 8   | PRG0_PRU1_GPO17 | 8   |
| GPMC0_AD14     | PRG0_PRU1_GPO18 | 8   | PRG0_PRU1_GPO18 | 8   |
| GPMC0_AD15     | PRG0_PRU1_GPO19 | 8   | PRG0_PRU1_GPO19 | 8   |
| GPMC0_A0       | PRG0_MDIO0_MDC  | 8   | PRG0_MDIO0_MDC  | 8   |
| GPMC0_A1       | RGMII5_TX_CTL   | 8   | RGMII5_TX_CTL   | 8   |
| GPMC0_A2       | RGMII5_RX_CTL   | 8   | RGMII5_RX_CTL   | 8   |
| GPMC0_A3       | RGMII5_TD3      | 8   | RGMII5_TD3      | 8   |
| GPMC0_A4       | RGMII5_TD2      | 8   | RGMII5_TD2      | 8   |
| GPMC0_A5       | RGMII5_TD1      | 8   | RGMII5_TD1      | 8   |
| GPMC0_A6       | RGMII5_TD0      | 8   | RGMII5_TD0      | 8   |
| GPMC0_A7       | RGMII5_TXC      | 8   | RGMII5_TXC      | 8   |
| GPMC0_A8       | RGMII5_RXC      | 8   | RGMII5_RXC      | 8   |
| GPMC0_A9       | RGMII5_RD3      | 8   | RGMII5_RD3      | 8   |
| GPMC0_A10      | RGMII5_RD2      | 8   | RGMII5_RD2      | 8   |
| GPMC0_A11      | RGMII5_RD1      | 8   | RGMII5_RD1      | 8   |
| GPMC0_A12      | RGMII5_RD0      | 8   | RGMII5_RD0      | 8   |
| GPMC0_A13      | RGMII6_TX_CTL   | 8   | RGMII6_TX_CTL   | 8   |
| GPMC0_A14      | RGMII6_RX_CTL   | 8   | RGMII6_RX_CTL   | 8   |

表 7-40. GPMC0 IOSET (continued)

| Signals     | IOSET1          |     | IOSET2          |     |
|-------------|-----------------|-----|-----------------|-----|
|             | BALL NAME       | MUX | BALL NAME       | MUX |
| GPMC0_A15   | RGMII6_TD3      | 8   | RGMII6_TD3      | 8   |
| GPMC0_A16   | RGMII6_TD2      | 8   | RGMII6_TD2      | 8   |
| GPMC0_A17   | RGMII6_TD1      | 8   | RGMII6_TD1      | 8   |
| GPMC0_A18   | RGMII6_TD0      | 8   | RGMII6_TD0      | 8   |
| GPMC0_A19   | RGMII6_TXC      | 8   | RGMII6_TXC      | 8   |
| GPMC0_A20   | RGMII6_RXC      | 8   | RGMII6_RXC      | 8   |
| GPMC0_A21   | RGMII6_RD3      | 8   | RGMII6_RD3      | 8   |
| GPMC0_A22   | RGMII6_RD2      | 8   | RGMII6_RD2      | 8   |
| GPMC0_A23   | PRG0_PRU1_GPO2  | 8   | PRG0_PRU1_GPO2  | 8   |
| GPMC0_A24   | PRG0_PRU1_GPO4  | 8   | PRG0_PRU1_GPO4  | 8   |
| GPMC0_A25   | PRG0_PRU1_GPO6  | 8   | PRG0_PRU1_GPO6  | 8   |
| GPMC0_A26   | PRG0_PRU1_GPO11 | 8   | PRG0_PRU1_GPO11 | 8   |
| GPMC0_A27   | PRG0_MDIO0_MDIO | 8   | PRG0_MDIO0_MDIO | 8   |
| GPMC0_WAIT3 | MDIO0_MDIO      | 8   | MDIO0_MDIO      | 8   |

#### 7.10.5.11 HyperBus

For more details about features and additional description information on the device HyperBus, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

节 7.10.5.11, 节 7.10.5.11.2, and 节 7.10.5.11.3 assume testing over the recommended operating conditions and electrical characteristic conditions (see 图 7-66, 图 7-67, and 图 7-68).

表 7-41 represents HyperBus timing conditions.

表 7-41. HyperBus Timing Conditions

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 2   | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance |     |     |      |

#### 7.10.5.11.1 Timing Requirements for HyperBus

| NO. | PARAMETER                    | DESCRIPTION                               | MIN    | MAX | UNIT |
|-----|------------------------------|-------------------------------------------|--------|-----|------|
| D1  | t <sub>w</sub> (RESETn)      | Pulse width, RESETn                       | 200    |     | ns   |
| D2  | t <sub>w</sub> (csL)         | Pulse width, Chip Select                  | 1000   |     | ns   |
| D3  | t <sub>d</sub> (RESETnH-csL) | Delay time, RESETn inactive to CSn active | 200.34 |     | ns   |
| D4  | t <sub>d</sub> (csL-RWDSL)   | Delay time, CSn active to RWDS falling    | 115    |     | ns   |

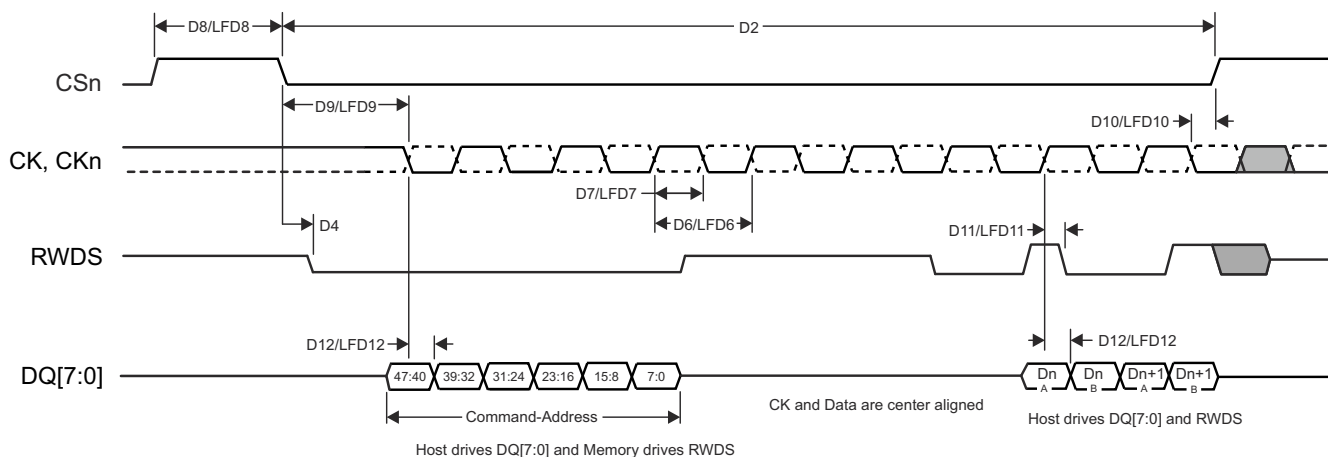
#### 7.10.5.11.2 HyperBus 166 MHz Switching Characteristics

| NO. | PARAMETER                     | DESCRIPTION                                                    | MIN   | MAX   | UNIT |
|-----|-------------------------------|----------------------------------------------------------------|-------|-------|------|
| D5  | t <sub>skn</sub> (rwdsX-dV)   | Input skew, RWDS transitioning to D0:D7 valid                  | -0.46 | 0.46  | ns   |
| D6  | t <sub>c</sub> (clk/clKn)     | CLK period, CLK/CLKn                                           | 6     |       | ns   |
| D7  | t <sub>w</sub> (clk/clKn)     | Pulse width, CLK/CLKn                                          | 2.7   |       | ns   |
| D8  | t <sub>w</sub> (csIV)         | Pulse width, CS0 invalid between operations                    | 6     |       | ns   |
| D9  | t <sub>d</sub> (clkH-csL)     | Delay time, CS0 active to CLK rising/ CLKn falling             |       | -3.34 | ns   |
| D10 | t <sub>d</sub> (clkL[LE]-csH) | Delay time, last falling CLK/ rising CLKn edge to CS0 inactive | 0.41  |       | ns   |

| NO. | PARAMETER                           | DESCRIPTION                                  | MIN  | MAX  | UNIT |
|-----|-------------------------------------|----------------------------------------------|------|------|------|
| D11 | $t_{d(\text{clkX-rwdsV})}$          | Delay time, CLK transition to RWDS valid     | 1.01 | 2.08 | ns   |
| D12 | $t_{d(\text{clkX-d}[0:7]\text{V})}$ | Delay time, CLK transitioning to D0:D7 valid | 0.84 | 2.17 | ns   |

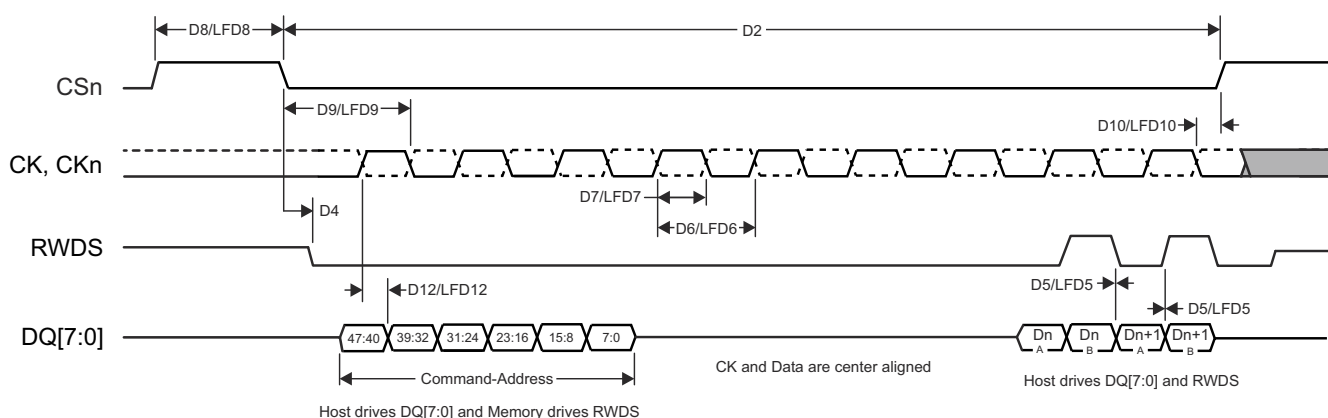
### 7.10.5.11.3 HyperBus 100 MHz Switching Characteristics

| NO.   | PARAMETER                           | DESCRIPTION                                       | MIN   | MAX   | UNIT |
|-------|-------------------------------------|---------------------------------------------------|-------|-------|------|
| LFD5  | $t_{\text{skn}(\text{rwdsX-dV})}$   | Input skew, RWDS transitioning to D0:D7 valid     | -0.81 | 0.81  | ns   |
| LFD6  | $t_{c(\text{clk})}$                 | CLK period, CLK                                   | 10    |       | ns   |
| LFD7  | $t_{w(\text{clk})}$                 | Pulse width, CLK                                  | 4.75  |       | ns   |
| LFD8  | $t_{w(\text{csIV})}$                | Pulse width, CS0 invalid between operations       | 10    |       | ns   |
| LFD9  | $t_{d(\text{clkH-csL})}$            | Delay time, CS0 active to CLK rising              |       | -3.51 | ns   |
| LFD10 | $t_{d(\text{clkL}[LE]\text{-csH})}$ | Delay time, last falling CLK edge to CS0 inactive | 0.51  |       | ns   |
| LFD11 | $t_{d(\text{clkX-rwdsV})}$          | Delay time, CLK transition to RWDS valid          | 1.51  | 3.49  | ns   |
| LFD12 | $t_{d(\text{clkX-d}[0:7]\text{V})}$ | Delay time, CLK transitioning to D0:D7 valid      | 1.34  | 3.66  | ns   |



HYPERBUS\_TIMING\_01

图 7-66. HyperBus Timing Diagrams - Transmitter Mode



HYPERBUS\_TIMING\_02

图 7-67. HyperBus Timing Diagrams - Receiver Mode

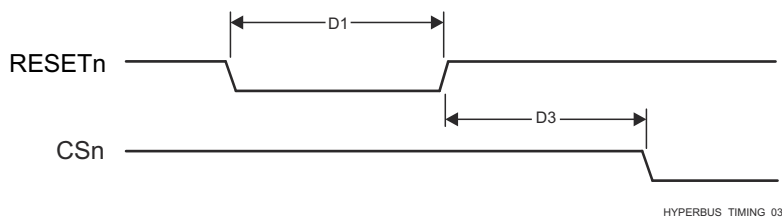


图 7-68. HyperBus Timing Diagrams - Reset

For more information, see *HyperBus Interface* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.12 I2C

The device contains **several** multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I2C-bus™ specification version 2.1. However, the device **IO Buffers** are not fully compliant to the I2C electrical specification. **Some I2C instances use the LVCMOS Buffer Type, while other instances use the I2S OD FS Buffer type. See the Pin Attributes table to determine the IO Buffer Type used for each I2C instance on this device.** The I2C speeds supported and exceptions are described per **IO Buffer Type** below:

- I2C instances that use the LVCMOS buffer type
  - Speeds:
    - Standard-mode (up to 100 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Fast-mode (up to 400 Kbits/s)
      - 1.8 V
      - 3.3 V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage  $V_{IH}$  of  $(V_{DD_{max}} + 0.5 V)$ , which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the [Absolute Maximum Ratings](#) section of this data sheet.
- I2C instances that use the I2C OD FS buffer type
  - Speeds:
    - Standard-mode (up to 100 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Fast-mode (up to 400 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Hs-mode (up to 3.4 Mbit/s)
      - 1.8 V
  - Exceptions:
    - The IOs associated with these ports were not design to support Hs-mode while operating at 3.3 V. So Hs-mode is limited to 1.8-V operation.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.8 V/ns (or 8E+7 V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C

specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.8 V/ns.

- The I2C specification defines a maximum input voltage  $V_{IH}$  of  $(V_{DD_{max}} + 0.5 \text{ V})$ , which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the [Absolute Maximum Ratings](#) section of this data sheet.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within [节 6.3](#) and *Detailed Description*.

#### 7.10.5.13 I3C

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding sections within [Signal Descriptions](#), *Signal Descriptions* and *Detailed Description*.

表 7-42, 表 7-43, 图 7-69, 表 7-44, and 图 7-70 assume testing over the recommended operating conditions and electrical characteristic conditions.

**表 7-42. I3C Open Drain Timing Conditions**

| PARAMETER                |                         | MIN    | MAX | UNIT |
|--------------------------|-------------------------|--------|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |        |     |      |
| $SR_I$                   | Input slew rate         | 0.2276 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |        |     |      |
| $C_L$                    | Output load capacitance |        | 50  | pF   |

**表 7-43. I3C Open Drain Timing Parameters**

| NO. | PARAMETER        | DESCRIPTION                                                            | MODE               | MIN                                   | MAX      | UNIT |
|-----|------------------|------------------------------------------------------------------------|--------------------|---------------------------------------|----------|------|
| D1  | $t_{LOW\_OD}$    | Low Period of SCL Clock                                                | Controller         | 200                                   |          | ns   |
|     | $t_{DIG\_OD\_L}$ |                                                                        |                    | $t_{LOW\_OD\_MIN} + t_{FDA\_OD\_MIN}$ |          | ns   |
| D2  | $t_{HIGH}$       | High Period of SCL Clock                                               | Controller         |                                       | 41       | ns   |
|     | $t_{DIG\_H}$     |                                                                        |                    | $t_{HIGH} + t_{CF}$                   |          | ns   |
| D3  | $t_{FDA\_OD}$    | Fall Time of SDA Signal                                                | Controller, Target | $t_{CF}$                              | 12       | ns   |
| D4  | $t_{SU\_OD}$     | SDA Data Setup Time During Open Drain Mode                             | Controller, Target | 3                                     |          | ns   |
| D5  | $t_{CAS}$        | Clock After START (S) Condition                                        | Controller, ENTAS0 | 38.4                                  | 1000     | ns   |
|     |                  |                                                                        | Controller, ENTAS1 | 38.4                                  | 100000   | ns   |
|     |                  |                                                                        | Controller, ENTAS2 | 38.4                                  | 2000000  | ns   |
|     |                  |                                                                        | Controller, ENTAS3 | 38.4                                  | 50000000 | ns   |
| D6  | $t_{CBP}$        | Clock Before STOP (P) Condition                                        | Controller         | $t_{CAS\_MIN} / 2$                    |          | ns   |
| D7  | $t_{MMOVERLAP}$  | Current Controller to Secondary Controller Overlap time during handoff | Controller         | $t_{DIG\_OD\_L\_min}$                 |          | ns   |
| D8  | $t_{AVAL}$       | Bus Available Condition                                                | Controller         | 1000                                  |          | ns   |
| D9  | $t_{IDLE}$       | Bus Idle Condition                                                     | Controller         | 1000000                               |          | ns   |
| D10 | $t_{MMLOCK}$     | Time Interval Where New Controller Not Driving SDA Low                 | Controller         | $t_{AVAL\_min}$                       |          | ns   |

1. This is approximately equal to  $t_{LOW\_min} + t_{DS\_OD\_min} + t_{rDA\_OD\_typ} + t_{SU\_OD\_min}$ .

- The Controller may use a shorter Low period if the Controller knows that this is safe, when SDA is already above  $V_{IH}$ .
- Based on  $t_{SPIKE}$ , rise and fall times, and interconnect.
- This maximum High period may be exceeded when the signals can be safely seen by Legacy I2C Devices, and/or in consideration of the interconnect (for example: a short Bus).
- On a Legacy Bus where I2C Devices need to see Start, the  $t_{CAS}$  Min value is further constrained.
- Targets that do not support the optional ENTASx CCCs shall use the  $t_{CAS}$  Max value shown for ENTAS3.
- On a Mixed Bus with Fm Legacy I2C Devices,  $t_{AVAIL}$  is 300ns shorter than the Fm Bus Free Condition time ( $t_{BUF}$ ).

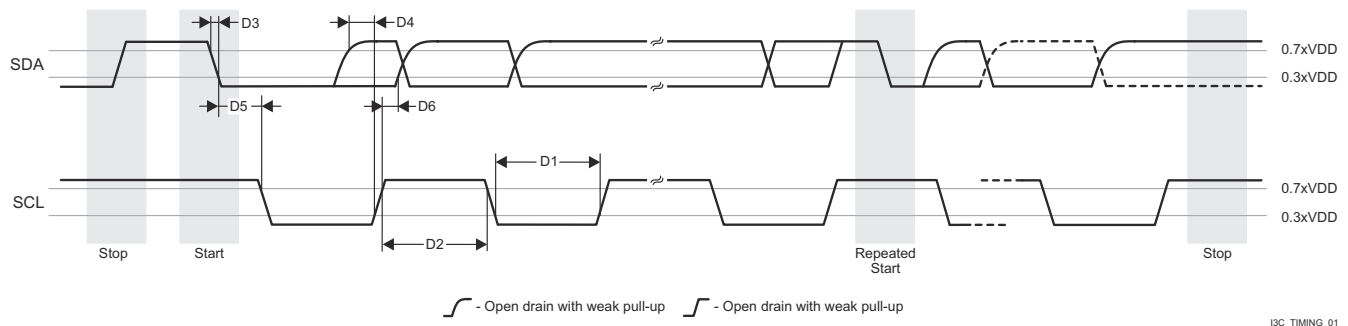


图 7-69. I3C Open Drain Timing

表 7-44. I3C Push-Pull Timing Parameters for SDR and HDR-DDR Modes

| NO. | PARAMETER           | DESCRIPTION                                                           | MODE               | MIN                              | MAX    | UNIT |
|-----|---------------------|-----------------------------------------------------------------------|--------------------|----------------------------------|--------|------|
| D1  | $f_{SCL}$           | SCL Clock Period                                                      | Controller         | 80                               | 100000 | ns   |
| D2  | $t_{LOW}$           | SCL Clock Low Period                                                  | Controller         | 24                               |        | ns   |
|     | $t_{DIG\_L}$        |                                                                       |                    | 32                               |        | ns   |
| D3  | $t_{HIGH\_MIXED}$   | SCL Clock High Period of Mixed Bus (Mixed Bus Topology Not Supported) | Controller         | 24                               |        | ns   |
|     | $t_{DIG\_H\_MIXED}$ |                                                                       |                    | 32                               | 45     | ns   |
| D4  | $t_{HIGH}$          | SCL Clock High Period                                                 | Controller         | 24                               |        | ns   |
|     | $t_{DIG\_H}$        |                                                                       |                    | 32                               |        | ns   |
| D5  | $t_{SCO}$           | Clock in to Data Out for Target                                       | Target             | 12                               |        | ns   |
| D6  | $t_{CR}$            | SCL Clock Rise Time                                                   | Controller         | $150 \times 1 / f_{SCL}$         | 60     | ns   |
| D7  | $t_{CF}$            | SCL Clock Fall Time                                                   | Controller         | $150 \times 1 / f_{SCL}$         | 60     | ns   |
| D8  | $t_{HD\_PP}$        | SDA Signal Data Hold in Push Pull Mode                                | Controller         | $t_{CR} + 3$<br>and $t_{CF} + 3$ |        | ns   |
|     |                     |                                                                       | Target             | 0                                |        | ns   |
| D9  | $t_{SU\_PP}$        | SDA Signal Data Setup In Push-Pull Mode                               | Controller, Target | 3                                |        | ns   |
| D10 | $t_{CASr}$          | Clock After Repeated START (Sr)                                       | Controller         | $t_{CAS}$ MIN                    |        | ns   |
| D11 | $t_{CBSr}$          | Clock Before Repeated START (Sr)                                      | Controller         | $t_{CAS}$ MIN / 2                |        | ns   |

- $f_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$
- $t_{DIG\_L}$  and  $t_{DIG\_H}$  are the clock Low and High periods as seen at the receiver end of the I3C Bus using  $V_{IL}$  and  $V_{IH}$ .
- When communicating with an I3C Device on a mixed Bus, the  $t_{DIG\_H\_MIXED}$  period must be constrained to make sure that I2C Devices do not interpret I3C signaling as valid I2C signaling.
- As both edges are used, the hold time needs to be satisfied for the respective edges;  $t_{CF} + 3$  for falling edge clocks, and  $t_{CR} + 3$  for rising edge clocks.

## 5. Clock Frequency Minimum 0.01 MHz, Maximum 12.5 MHz

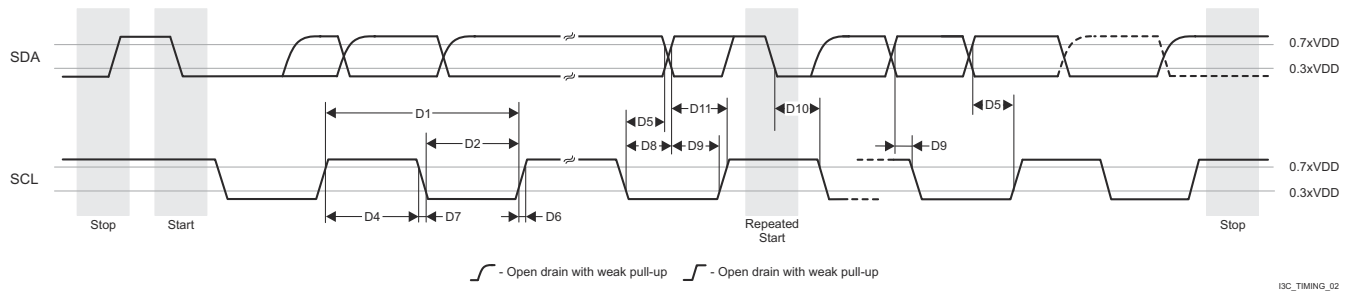


图 7-70. I3C Push-Pull Timing (SDR and HDR-DDR Modes)

### 7.10.5.14 MCAN

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

#### 备注

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

表 7-45. MCAN Timing Conditions

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 2   | 15  | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 5   | 20  | pF   |

表 7-46. MCAN Switching Characteristics

| NO.   | PARAMETER                |                                                                    | MIN | MAX | UNIT |
|-------|--------------------------|--------------------------------------------------------------------|-----|-----|------|
| MCAN1 | t <sub>d</sub> (MCAN_TX) | Delay time, transmit shift register to MCANn_TX pin <sup>(1)</sup> |     | 10  | ns   |
| MCAN2 | t <sub>d</sub> (MCAN_RX) | Delay time, MCANn_RX pin to receive shift register <sup>(1)</sup>  |     | 10  | ns   |

(1) n is [0:13] in MCANn\_\* or [0:1] in MCU\_MCANn\_\*

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

### 7.10.5.15 MCASP

For more details about features and additional description information on the device Multichannel Audio Serial Port, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

表 7-48 和 图 7-71 present timing requirements for MCASP0 to MCASP11.

表 7-47 represents MCASP timing conditions.

**表 7-47. MCASP Timing Conditions**

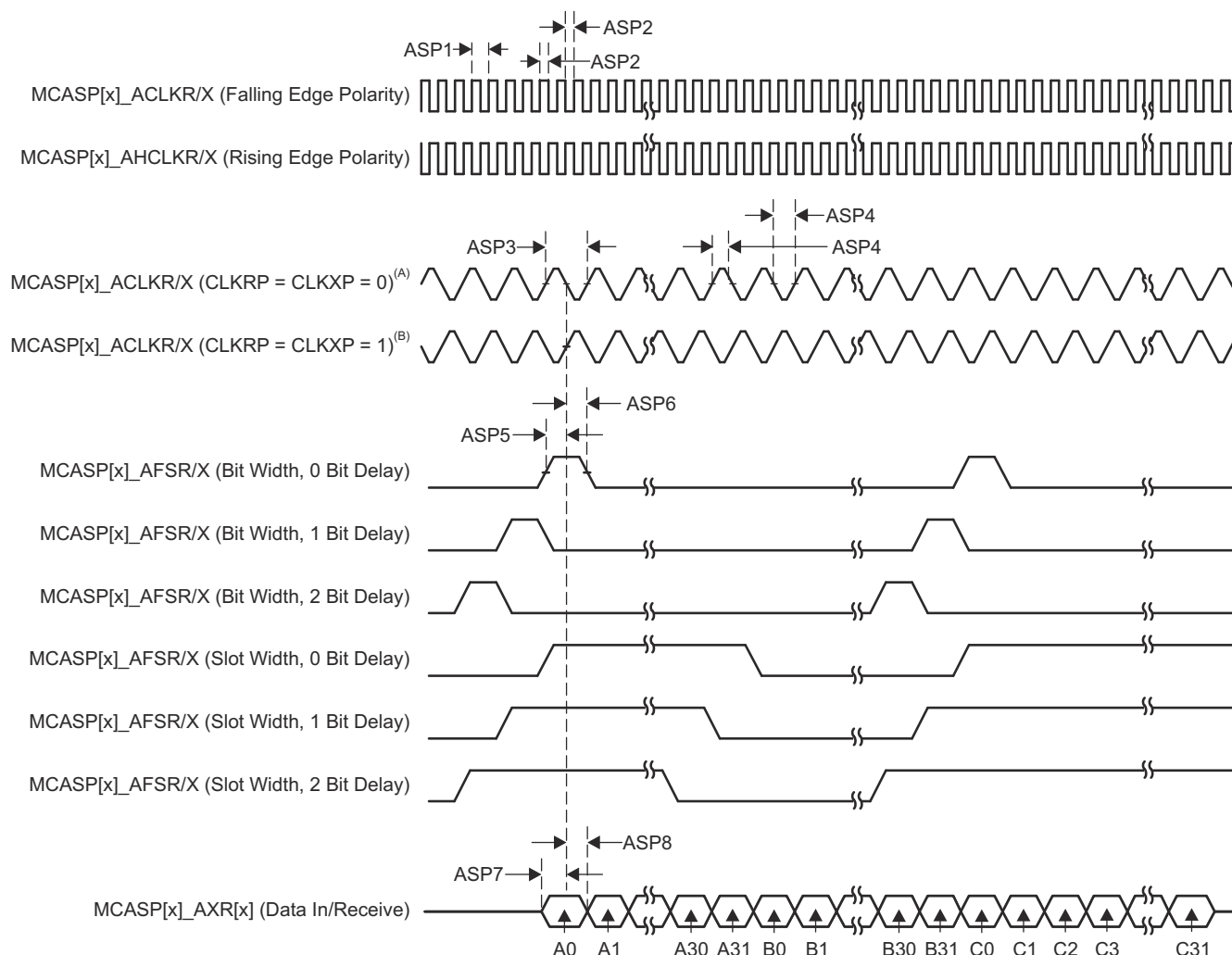
| PARAMETER                             |                                              | MIN | MAX  | UNIT |
|---------------------------------------|----------------------------------------------|-----|------|------|
| <b>INPUT CONDITIONS</b>               |                                              |     |      |      |
| SR <sub>I</sub>                       | Input slew rate                              | 0.7 | 5    | V/ns |
| <b>OUTPUT CONDITIONS</b>              |                                              |     |      |      |
| C <sub>L</sub>                        | Output load capacitance                      | 1   | 10   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |     |      |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | 100 | 1100 | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |     | 100  | ps   |

**表 7-48. MCASP Timing Requirements**

| NO.  |                                |                                                                 | MODE <sup>(1)</sup> | MIN                        | MAX | UNIT |
|------|--------------------------------|-----------------------------------------------------------------|---------------------|----------------------------|-----|------|
| ASP1 | t <sub>c</sub> (AHCLKRX)       | Cycle time, MCASP[x]_AHCLKR/X                                   |                     | 15.26                      |     | ns   |
| ASP2 | t <sub>w</sub> (AHCLKRX)       | Pulse duration, MCASP[x]_AHCLKR/X high or low                   |                     | 0.5P <sup>(2)</sup> - 1.53 |     | ns   |
| ASP3 | t <sub>c</sub> (ACLKRX)        | Cycle time, MCASP[x]_ACLKR/X                                    |                     | 15.26                      |     | ns   |
| ASP4 | t <sub>w</sub> (ACLKRX)        | Pulse duration, MCASP[x]_ACLKR/X high or low                    |                     | 0.5R <sup>(3)</sup> - 1.53 |     | ns   |
| ASP5 | t <sub>su</sub> (AFSRX-ACLKRX) | Setup time, MCASP[x]_AFSR/X input valid before MCASP[x]_ACLKR/X | ACLKR/X int         | 12.3                       |     | ns   |
|      |                                |                                                                 | ACLKR/X ext in/out  | 4                          |     |      |
| ASP6 | t <sub>h</sub> (ACLKRX-AFSRX)  | Hold time, MCASP[x]_AFSR/X input valid after MCASP[x]_ACLKR/X   | ACLKR/X int         | - 1                        |     | ns   |
|      |                                |                                                                 | ACLKR/X ext in/out  | 1.6                        |     |      |
| ASP7 | t <sub>su</sub> (AXR-ACLKRX)   | Setup time, MCASP[x]_AXR input valid before MCASP[x]_ACLKR/X    | ACLKR/X int         | 12.3                       |     | ns   |
|      |                                |                                                                 | ACLKR/X ext in/out  | 4                          |     |      |
| ASP8 | t <sub>h</sub> (ACLKRX-AXR)    | Hold time, MCASP[x]_AXR input valid after MCASP[x]_ACLKR/X      | ACLKR/X int         | -1                         |     | ns   |
|      |                                |                                                                 | ACLKR/X ext in/out  | 1.6                        |     |      |

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
- (2) P = AHCLKR/X period in ns.
- (3) R = ACLKR/X period in ns.





- A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).
- B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

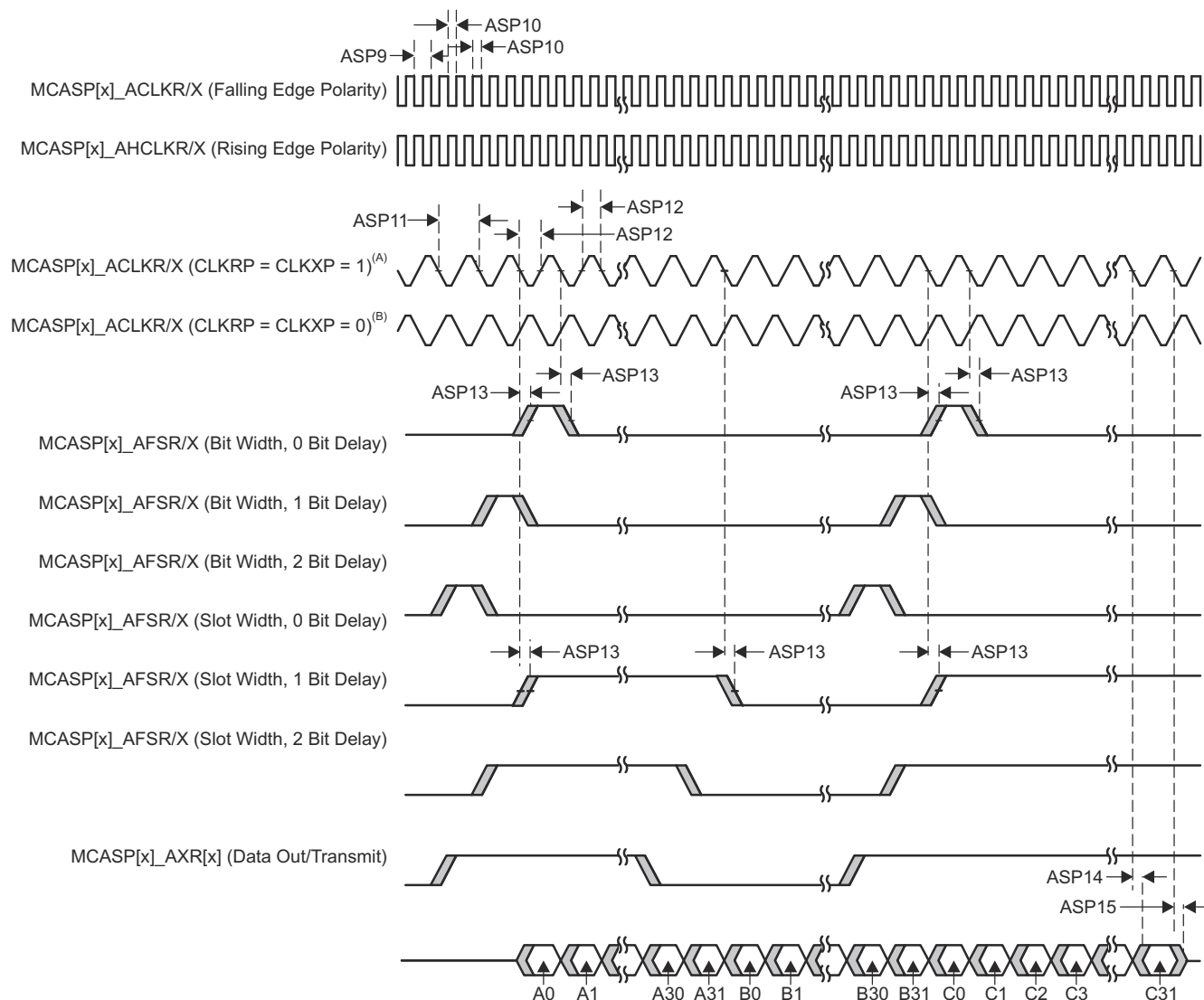
**图 7-71. MCASP Input Timing**

表 7-49 和 图 7-72 present switching characteristics over recommended operating conditions for MCASP0 to MCASP11.

**表 7-49. MCASP Switching Characteristics**

| NO.   | PARAMETER             | DESCRIPTION                                                                      | MODE <sup>(1)</sup> | MIN                     | MAX   | UNIT |
|-------|-----------------------|----------------------------------------------------------------------------------|---------------------|-------------------------|-------|------|
| ASP9  | $t_{c(AHCLKRX)}$      | Cycle time, MCASP[x]_AHCLKR/X                                                    |                     | 20                      |       | ns   |
| ASP10 | $t_{w(AHCLKRX)}$      | Pulse duration, MCASP[x]_AHCLKR/X high or low                                    |                     | 0.5P <sup>(2)</sup> - 2 |       | ns   |
| ASP11 | $t_{c(ACLKRX)}$       | Cycle time, MCASP[x]_ACLKR/X                                                     |                     | 20                      |       | ns   |
| ASP12 | $t_{w(ACLKRX)}$       | Pulse duration, MCASP[x]_ACLKR/X high or low                                     |                     | 0.5R <sup>(3)</sup> - 2 |       | ns   |
| ASP13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, MCASP[x]_ACLKR/X transmit edge to MCASP[x]_AFSR/X output valid       | ACLKR/X int         | 0                       | 7.25  | ns   |
|       |                       |                                                                                  | ACLKR/X ext in/out  | - 15.28                 | 12.84 |      |
| ASP14 | $t_{d(ACLKX-AXR)}$    | Delay time, MCASP[x]_ACLKX transmit edge to MCASP[x]_AXR output valid            | ACLKR/X int         | 0                       | 7.25  | ns   |
|       |                       |                                                                                  | ACLKR/X ext in/out  | - 15.28                 | 12.84 |      |
| ASP15 | $t_{dis(ACLKX-AXR)}$  | Disable time, MCASP[x]_ACLKX transmit edge to MCASP[x]_AXR output high impedance | ACLKR/X int         | 0                       | 7.25  | ns   |
|       |                       |                                                                                  | ACLKR/X ext in/out  | - 14.9                  | 14    |      |

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
- (2) P = AHCLKR/X period in ns.
- (3) R = ACLKR/X period in ns.



- A. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).
- B. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

图 7-72. MCASP Output Timing

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

### 7.10.5.16 MCSPI

For more details about features and additional description information on the device Serial Port Interface, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

表 7-50 represents MCSPI timing conditions.

#### 备注

The IO timings provided in this section are applicable for all combinations of signals for MCU\_SPI0 and MCU\_SPI1. However, the timings are only valid for MCU\_SPI0 and MCU\_SPI1 if signals within a single IOSET are used. The IOSETs are defined in the 表 7-55 and 表 7-56 tables.

表 7-50. MCSPI Timing Conditions

| PARAMETER                |                         |           | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |           |     |     |      |
| SR <sub>I</sub>          | Input slew rate         |           | 2   | 8.5 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |           |     |     |      |
| C <sub>L</sub>           | Output load capacitance | CLK       | 6   | 24  | pF   |
|                          |                         | D[x], CSi | 6   | 12  | pF   |

#### 7.10.5.16.1 MCSPI — Controller Mode

表 7-51, 图 7-73, 表 7-52, and 图 7-74 present timing requirements and switching characteristics for MCSPI - Controller Mode.

表 7-51. MCSPI Timing Requirements - Controller Mode

see 图 7-73

| NO. |                               |                                                       | MIN | MAX | UNIT |
|-----|-------------------------------|-------------------------------------------------------|-----|-----|------|
| SM4 | t <sub>su(misoV-spickV)</sub> | Setup time, SPI_D[x] valid before SPI_CLK active edge | 2.9 |     | ns   |
| SM5 | t <sub>h(spickV-misoV)</sub>  | Hold time, SPI_D[x] valid after SPI_CLK active edge   | 2   |     | ns   |

表 7-52. MCSPI Switching Characteristics - Controller Mode

see 图 7-74

| NO. | PARAMETER                    |                                                        | MODE                   | MIN                     | MAX | UNIT |
|-----|------------------------------|--------------------------------------------------------|------------------------|-------------------------|-----|------|
| SM1 | t <sub>c(spick)</sub>        | Cycle time, SPI_CLK                                    |                        | 20.8                    |     | ns   |
| SM2 | t <sub>w(spickL)</sub>       | Pulse duration, SPI_CLK low                            |                        | 0.5P - 1 <sup>(1)</sup> |     | ns   |
| SM3 | t <sub>w(spickH)</sub>       | Pulse duration, SPI_CLK high                           |                        | 0.5P - 1 <sup>(1)</sup> |     | ns   |
| SM6 | t <sub>d(spickV-simoV)</sub> | Delay time, SPI_CLK active edge to SPI_D[x] transition |                        | - 2                     | 2   | ns   |
| SM7 | t <sub>d(csV-simoV)</sub>    | Delay time, SPI_CSi active edge to SPI_D[x] transition |                        | 5                       |     | ns   |
| SM8 | t <sub>d(csV-spick)</sub>    | Delay time, SPI_CSi active to SPI_CLK first edge       | PHA = 0 <sup>(2)</sup> | B - 4 <sup>(3)</sup>    |     | ns   |
|     |                              |                                                        | PHA = 1 <sup>(2)</sup> | A - 4 <sup>(4)</sup>    |     | ns   |
| SM9 | t <sub>d(spickV-csV)</sub>   | Delay time, SPI_CLK last edge to SPI_CSi inactive      | PHA = 0 <sup>(2)</sup> | A - 4 <sup>(4)</sup>    |     | ns   |
|     |                              |                                                        | PHA = 1 <sup>(2)</sup> | B - 4 <sup>(3)</sup>    |     | ns   |

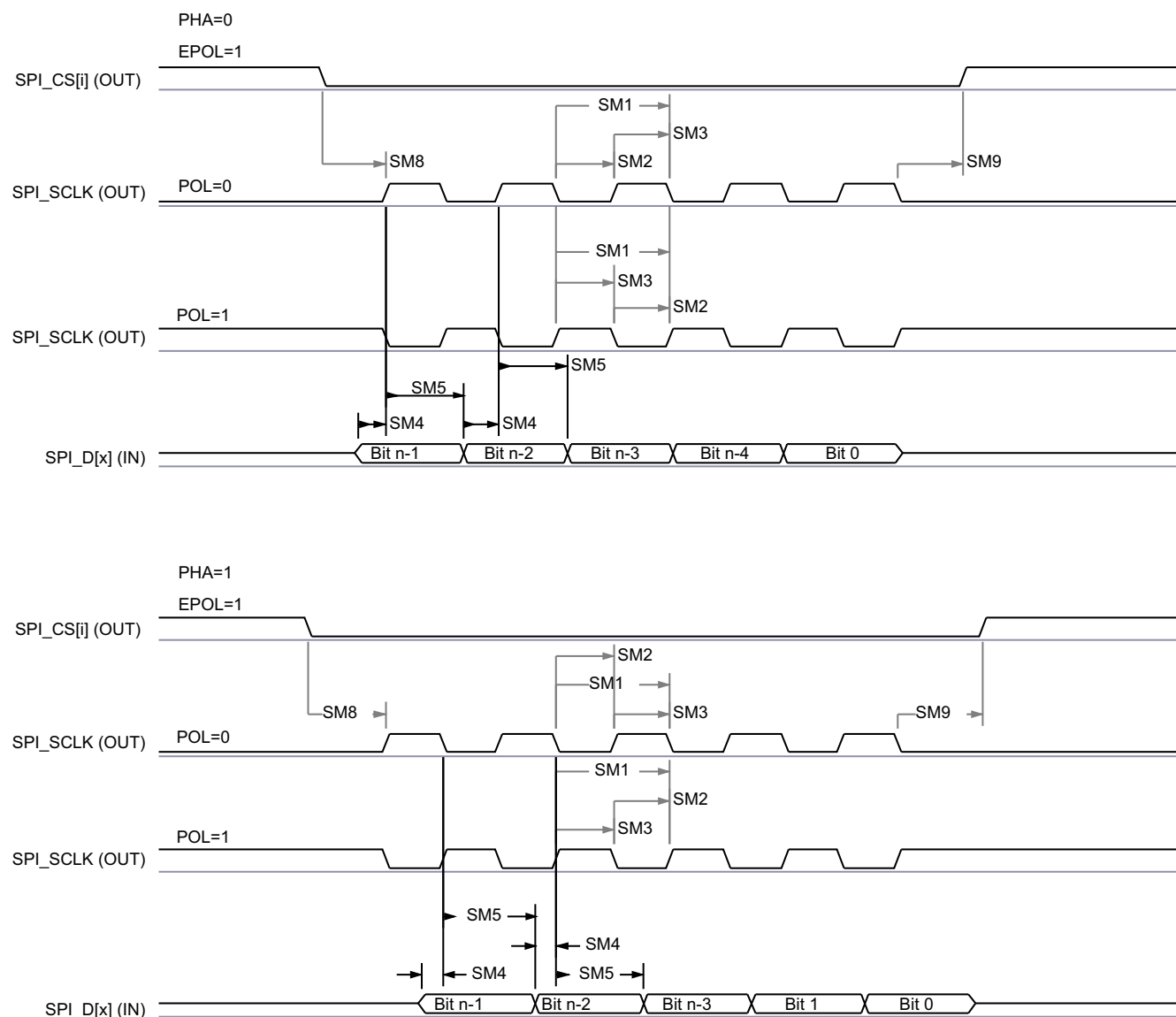
(1) P = SPI\_CLK period in ns

(2) SPI\_CLK phase is programmable with the PHA bit of the MCSPI\_CHCONF\_0/1/2/3 register

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- (3)  $B = (TCS + .5) * TSPICKREF$ , where TCSns a bit field of the MCSPI\_CHCONF\_0/1/2/3 register and Fratio = Even  $\geq 2$ .
- (4) When  $P = 20.8 \text{ ns}$ ,  $A = (TCS + 1) * TSPICKREF$ , where TCSns a bit field of the MCSPI\_CHCONF\_0/1/2/3 register.  
When  $P > 20.8 \text{ ns}$ ,  $A = (TCS + 0.5) * Fratio * TSPICKREF$ , where TCSns a bit field of the MCSPI\_CHCONF\_0/1/2/3 register.



SPRSP08\_TIMING\_McSPI\_02

图 7-73. SPI Controller Mode Receive Timing

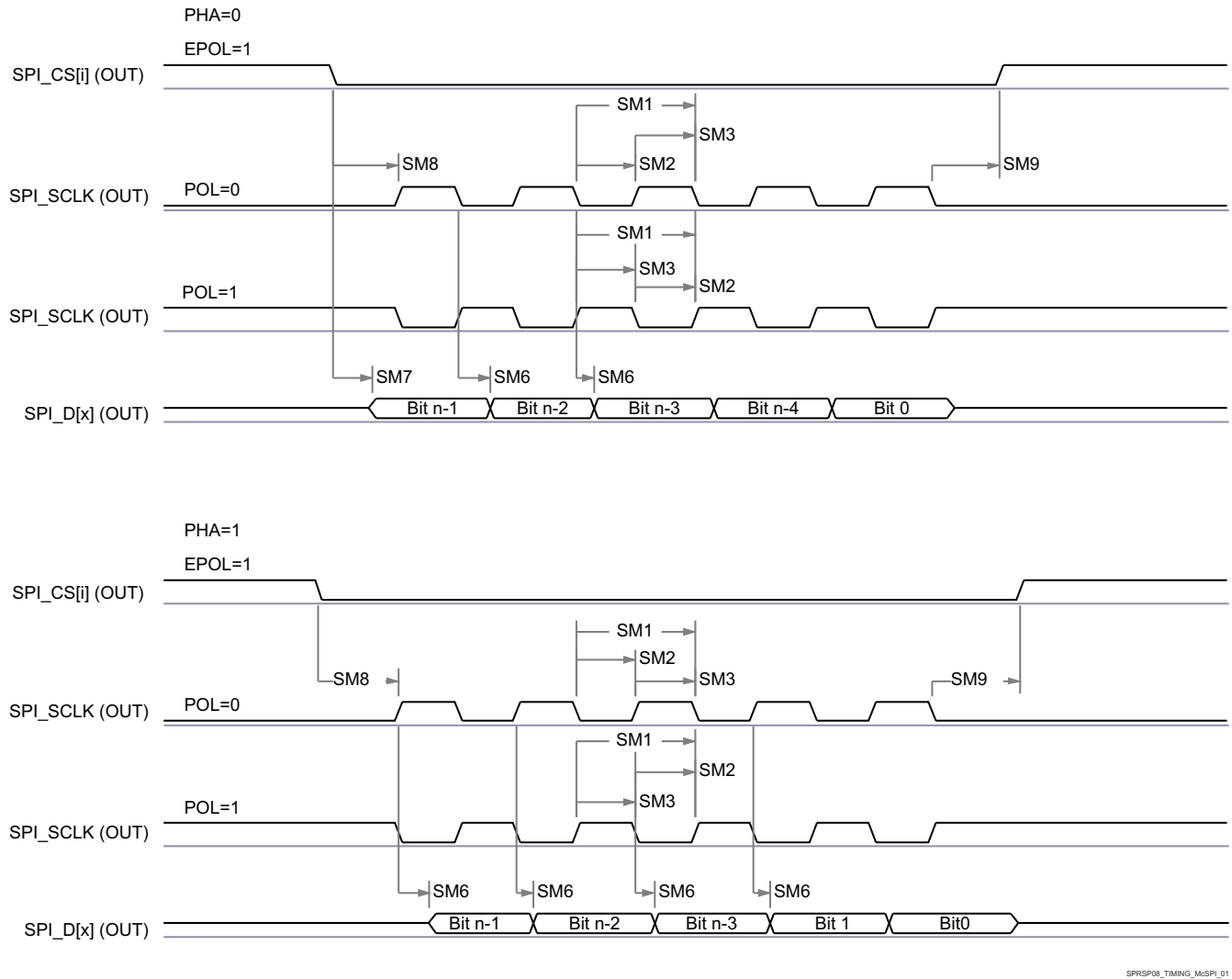


图 7-74. MCSPI Controller Mode Transmit Timing

#### 7.10.5.16.2 MCSPI — Peripheral Mode

表 7-53, 表 7-54, 图 7-75, and 图 7-76 present timing requirements and switching characteristics for MCSPI – Peripheral Mode.

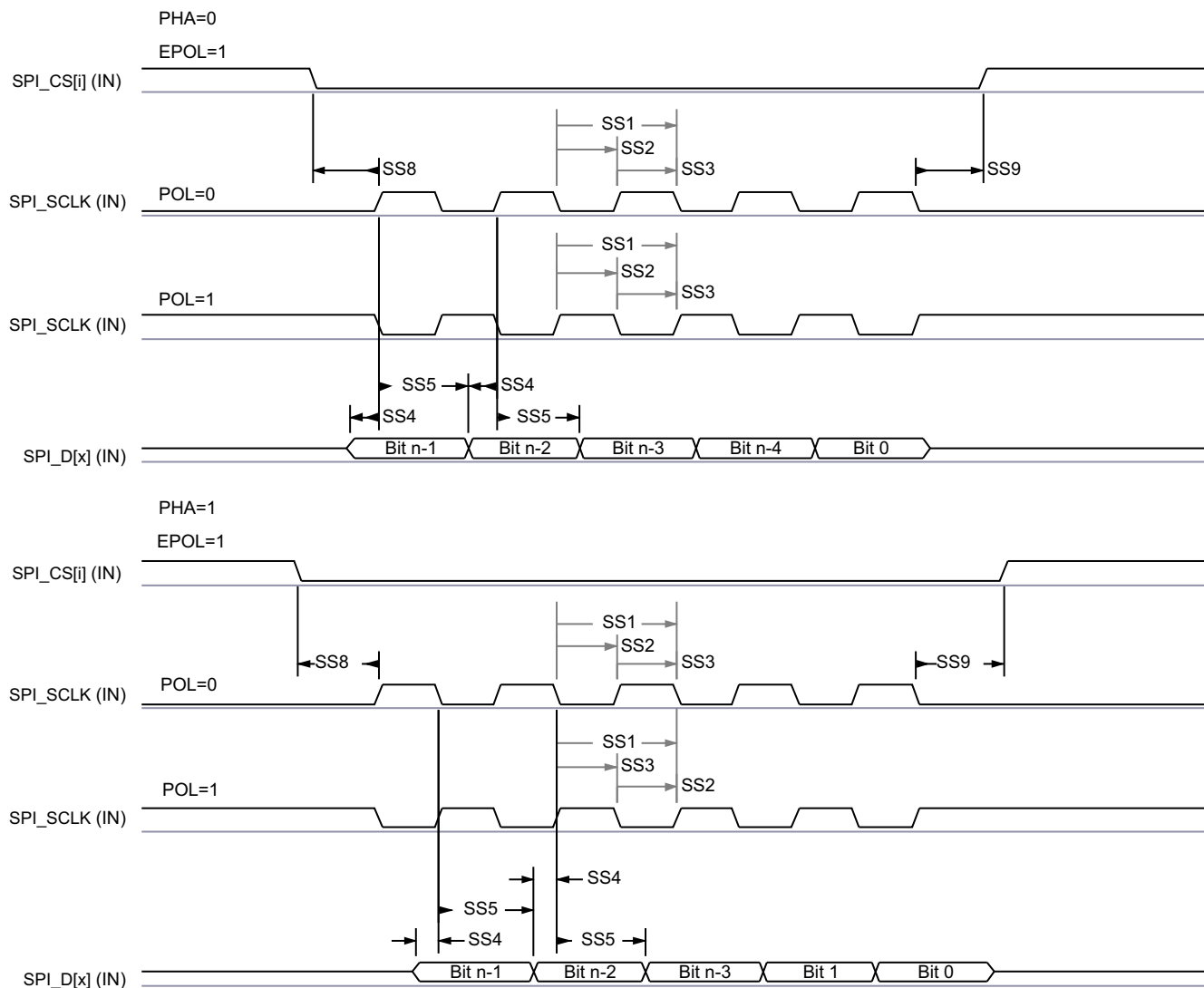
表 7-53. MCSPI Timing Requirements - Peripheral Mode

| NO. | PARAMETER               | DESCRIPTION                                           | MODE | MIN                  | MAX | UNIT |
|-----|-------------------------|-------------------------------------------------------|------|----------------------|-----|------|
| SS1 | $t_{c(spiclk)}$         | Cycle time, SPI_CLK                                   |      | 20.8                 |     | ns   |
| SS2 | $t_{w(spiclkL)}$        | Pulse duration, SPI_CLK low                           |      | 0.45P <sup>(1)</sup> |     | ns   |
| SS3 | $t_{w(spiclkH)}$        | Pulse duration, SPI_CLK high                          |      | 0.45P <sup>(1)</sup> |     | ns   |
| SS4 | $t_{su(simoV-spiclkV)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge |      | 5                    |     | ns   |
| SS5 | $t_{h(spiclkV-simoV)}$  | Hold time, SPI_D[x] valid after SPI_CLK active edge   |      | 5                    |     | ns   |
| SS8 | $t_{su(csV-spiclkV)}$   | Setup time, SPI_CSi valid before SPI_CLK first edge   |      | 5                    |     | ns   |
| SS9 | $t_{h(spiclkV-csV)}$    | Hold time, SPI_CSi valid after SPI_CLK last edge      |      | 5                    |     | ns   |

表 7-54. MCSPI Switching Characteristics - Peripheral Mode

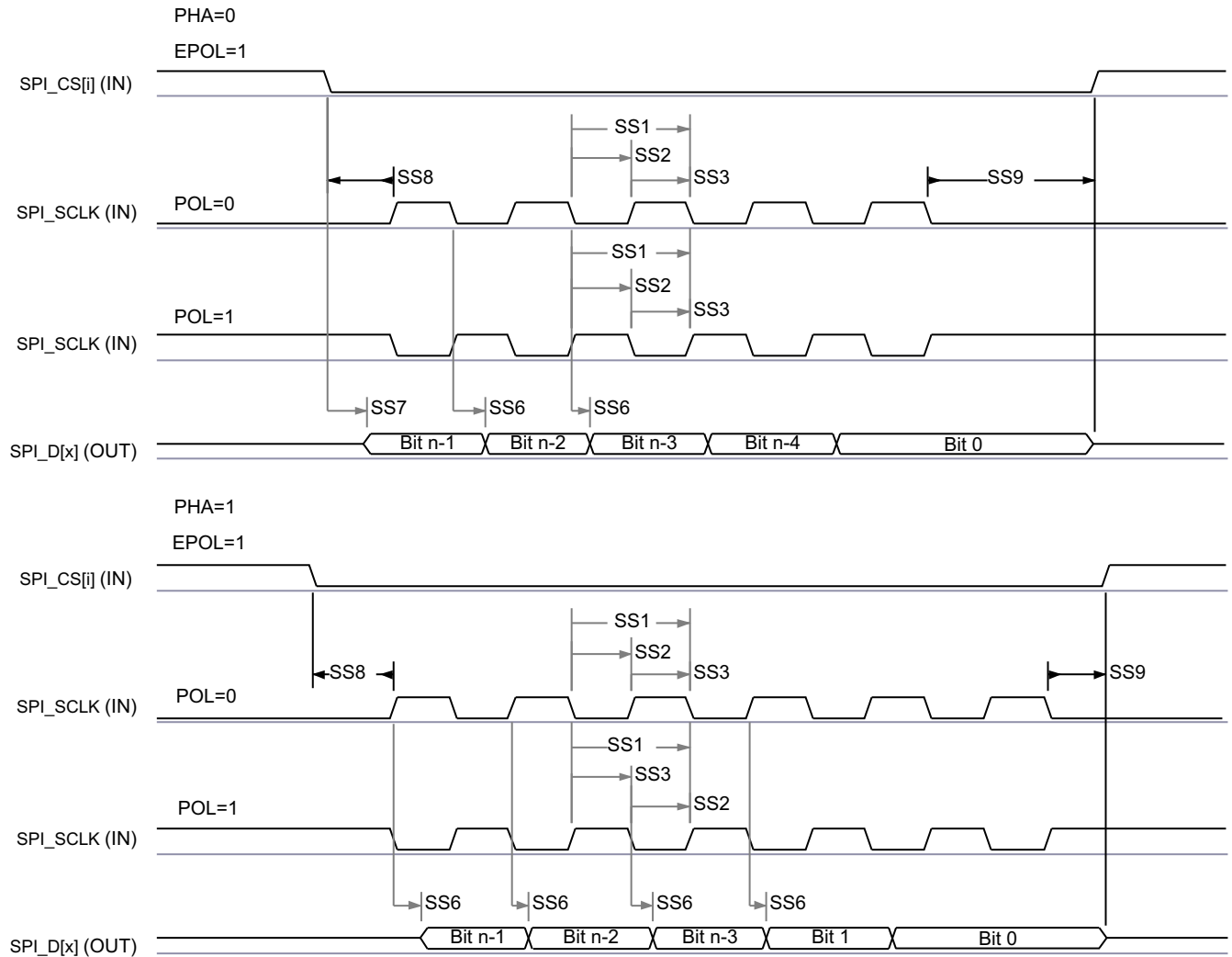
| NO. | PARAMETER             | DESCRIPTION                                            | MIN   | MAX   | UNIT |
|-----|-----------------------|--------------------------------------------------------|-------|-------|------|
| SS6 | $t_{d(spiclV-somIV)}$ | Delay time, SPI_CLK active edge to SPI_D[x] transition | 2     | 17.12 | ns   |
| SS7 | $t_{sk(csV-somIV)}$   | Delay time, SPI_CSi active edge to SPI_D[x] transition | 20.95 |       | ns   |

(1) P = SPI\_CLK period in ns.



SPRSP08\_TIMING\_McSPI\_04

图 7-75. SPI Peripheral Mode Receive Timing



SPRSP08\_TIMING\_McSPI\_03

图 7-76. MCSPI Peripheral Mode Transmit Timing

表 7-55 和 表 7-56 present the specific groupings of signals (IOSET) for use with MCU\_SPI0 and MCU\_SPI1.

表 7-55. MCU\_SPI0 IOSETs

| Signals      | IOSET1         |     | IOSET2        |     |
|--------------|----------------|-----|---------------|-----|
|              | BALL NAME      | MUX | BALL NAME     | MUX |
| MCU_SPI0_CLK | MCU_SPI0_CLK   | 0   | MCU_SPI0_CLK  | 0   |
| MCU_SPI0_D0  | MCU_SPI0_D0    | 0   | MCU_SPI0_D0   | 0   |
| MCU_SPI0_D1  | MCU_SPI0_D1    | 0   | MCU_SPI0_D1   | 0   |
| MCU_SPI0_CS0 | MCU_SPI0_CS0   | 0   | MCU_SPI0_CS0  | 0   |
| MCU_SPI0_CS1 | MCU_OSP11_D3   | 5   | WKUP_GPIO0_12 | 1   |
| MCU_SPI0_CS2 | MCU_OSP11_CSn1 | 5   | WKUP_GPIO0_14 | 1   |



表 7-56. MCU\_SPI1 IOSET

| Signals      | IOSET1       |     | IOSET2        |     |
|--------------|--------------|-----|---------------|-----|
|              | BALL NAME    | MUX | BALL NAME     | MUX |
| MCU_SPI1_CLK | MCU_SPI1_CLK | 0   | MCU_SPI1_CLK  | 0   |
| MCU_SPI1_D0  | MCU_SPI1_D0  | 0   | MCU_SPI1_D0   | 0   |
| MCU_SPI1_D1  | MCU_SPI1_D1  | 0   | MCU_SPI1_D1   | 0   |
| MCU_SPI1_CS0 | MCU_SPI1_CS0 | 0   | MCU_SPI1_CS0  | 0   |
| MCU_SPI1_CS1 | MCU_OSPI1_D1 | 5   | WKUP_GPIO0_13 | 1   |
| MCU_SPI1_CS2 | MCU_OSPI1_D2 | 5   | WKUP_GPIO0_15 | 1   |

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.17 MMCSD

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the corresponding MMC0, MMC1, and MMC2 sections within

[Signal Descriptions](#) and *Detailed Description*.

#### 备注

Some operating modes require software configuration of the MMC DLL delay settings, as shown in [表 7-57](#) 和 [表 7-67](#).

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.17.1 MMC0 - eMMC Interface

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and it supports the following eMMC applications:

- Legacy speed
- High speed SDR
- High speed DDR
- High Speed HS200
- High Speed HS400

[表 7-57](#) presents the required DLL software configuration settings for MMC0 timing modes.

表 7-57. MMC0 DLL Delay Mapping for All Timing Modes

| REGISTER NAME        |                                         | MMCS0_SS_PHY_CTRL_4_REG |                           |                          |                          |                         | MMCS0_SS_PHY_CTRL_5_REG       |                      |                             |
|----------------------|-----------------------------------------|-------------------------|---------------------------|--------------------------|--------------------------|-------------------------|-------------------------------|----------------------|-----------------------------|
| BIT FIELD            |                                         | [31:24]                 | [20]                      | [15:12]                  | [8]                      | [4:0]                   | [17:16]                       | [10:8]               | [2:0]                       |
| BIT FIELD NAME       |                                         | STRBSEL                 | OTAPDLYENA                | OTAPDLYSEL               | ITAPDLYENA               | ITAPDLYSEL              | SELDLYTXCLK<br>SELDLYRXCLK    | FRQSEL               | CLKBUFSEL                   |
| MODE                 | DESCRIPTION                             | STROBE<br>DELAY         | OUTPUT<br>DELAY<br>ENABLE | OUTPUT<br>DELAY<br>VALUE | INPUT<br>DELAY<br>ENABLE | INPUT<br>DELAY<br>VALUE | DLL/<br>DELAY CHAIN<br>SELECT | DLL REF<br>FREQUENCY | DELAY<br>BUFFER<br>DURATION |
| Legacy<br>SDR        | 8-bit PHY<br>operating 1.8 V,<br>25 MHz | 0x0                     | 0x0                       | NA                       | 0x1                      | 0x10                    | 0x1                           | 0x0                  | 0x7                         |
| High<br>Speed<br>SDR | 8-bit PHY<br>operating 1.8 V,<br>50 MHz | 0x0                     | 0x0                       | NA                       | 0x1                      | 0xA                     | 0x1                           | 0x0                  | 0x7                         |

**表 7-57. MMC0 DLL Delay Mapping for All Timing Modes (continued)**

| REGISTER NAME        |                                          | MMCS0_SS_PHY_CTRL_4_REG |                           |                          |                          |                         | MMCS0_SS_PHY_CTRL_5_REG       |                      |                             |
|----------------------|------------------------------------------|-------------------------|---------------------------|--------------------------|--------------------------|-------------------------|-------------------------------|----------------------|-----------------------------|
| BIT FIELD            |                                          | [31:24]                 | [20]                      | [15:12]                  | [8]                      | [4:0]                   | [17:16]                       | [10:8]               | [2:0]                       |
| BIT FIELD NAME       |                                          | STRBSEL                 | OTAPDLYENA                | OTAPDLYSEL               | ITAPDLYENA               | ITAPDLYSEL              | SELDLYTXCLK<br>SELDLYRXCLK    | FRQSEL               | CLKBUFSEL                   |
| MODE                 | DESCRIPTION                              | STROBE<br>DELAY         | OUTPUT<br>DELAY<br>ENABLE | OUTPUT<br>DELAY<br>VALUE | INPUT<br>DELAY<br>ENABLE | INPUT<br>DELAY<br>VALUE | DLL/<br>DELAY CHAIN<br>SELECT | DLL REF<br>FREQUENCY | DELAY<br>BUFFER<br>DURATION |
| High<br>Speed<br>DDR | 8-bit PHY<br>operating 1.8 V,<br>50 MHz  | 0x0                     | 0x1                       | 0x6                      | 0x1                      | Tuning                  | 0x0                           | 0x4                  | 0x7                         |
| HS200                | 8-bit PHY<br>operating 1.8 V,<br>200 MHz | 0x0                     | 0x1                       | 0x8                      | 0x1                      | Tuning                  | 0x0                           | 0x0                  | 0x7                         |
| HS400                | 8-bit PHY<br>operating 1.8 V,<br>200 MHz | 0x66                    | 0x1                       | 0x5                      | 0x1                      | Tuning                  | 0x0                           | 0x0                  | 0x7                         |

表 7-58 presents timing conditions for MMC0.

**表 7-58. MMC0 Timing Conditions**

| PARAMETER                             |                                              |                                            | MIN  | MAX  | UNIT |
|---------------------------------------|----------------------------------------------|--------------------------------------------|------|------|------|
| INPUT CONDITIONS                      |                                              |                                            |      |      |      |
| SR <sub>i</sub>                       | Input slew rate                              | Legacy SDR                                 | 0.14 | 1.44 | V/ns |
|                                       |                                              | High Speed SDR                             | 0.3  | 0.90 | V/ns |
|                                       |                                              | High Speed DDR (CMD)                       | 0.3  | 0.90 | V/ns |
|                                       |                                              | High Speed DDR (DAT[7:0])                  | 0.45 | 0.90 | V/ns |
| OUTPUT CONDITIONS                     |                                              |                                            |      |      |      |
| C <sub>L</sub>                        | Output load capacitance                      | HS200, HS400                               | 1    | 6    | pF   |
|                                       |                                              | All other modes                            | 1    | 12   | pF   |
| PCB CONNECTIVITY REQUIREMENTS         |                                              |                                            |      |      |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | All modes                                  | 134  | 756  | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | Legacy SDR, High Speed SDR, High Speed DDR |      | 100  | ps   |
|                                       |                                              | HS200, HS400                               |      | 8    | ps   |

### 7.10.5.17.1.1 Legacy SDR Mode

表 7-59, 图 7-77, 表 7-60, and 图 7-78 present timing requirements and switching characteristics for MMC0 - Legacy SDR Mode.

**表 7-59. MMC0 Timing Requirements - Legacy SDR Mode**

see 图 7-77

| NO.   |                     |                                                             | MIN | MAX | UNIT |
|-------|---------------------|-------------------------------------------------------------|-----|-----|------|
| LSDR1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge      | 2.5 |     | ns   |
| LSDR2 | $t_{h(clkH-cmdV)}$  | Hold time, MMC0_CMD valid after MMC0_CLK rising edge        | 6.5 |     | ns   |
| LSDR3 | $t_{su(dV-clkH)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge | 2.5 |     | ns   |
| LSDR4 | $t_{h(clkH-dV)}$    | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge   | 6.5 |     | ns   |

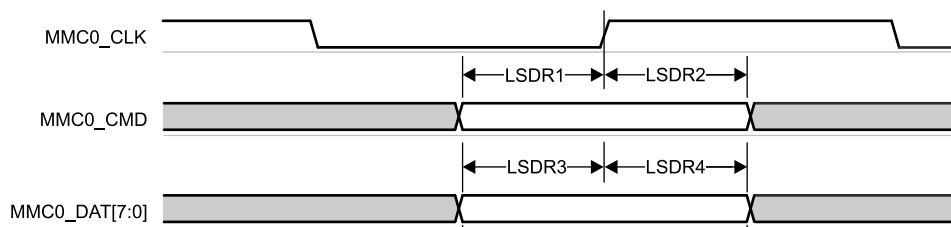


**图 7-77. MMC0 - Legacy SDR - Receive Mode**

**表 7-60. MMC0 Switching Characteristics - Legacy SDR Mode**

see 图 7-78

| NO.   |                    | PARAMETER                                                     | MIN   | MAX | UNIT |
|-------|--------------------|---------------------------------------------------------------|-------|-----|------|
|       | $f_{op(clk)}$      | Operating frequency, MMC0_CLK                                 |       | 25  | MHz  |
| LSDR5 | $t_{c(clk)}$       | Cycle time, MMC0_CLK                                          | 40    |     | ns   |
| LSDR6 | $t_{w(clkH)}$      | Pulse duration, MMC0_CLK high                                 | 18.7  |     | ns   |
| LSDR7 | $t_{w(clkL)}$      | Pulse duration, MMC0_CLK low                                  | 18.7  |     | ns   |
| LSDR8 | $t_{d(clkL-cmdV)}$ | Delay time, MMC0_CLK falling edge to MMC0_CMD transition      | - 3.2 | 3.8 | ns   |
| LSDR9 | $t_{d(clkL-dV)}$   | Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition | - 3.2 | 3.8 | ns   |

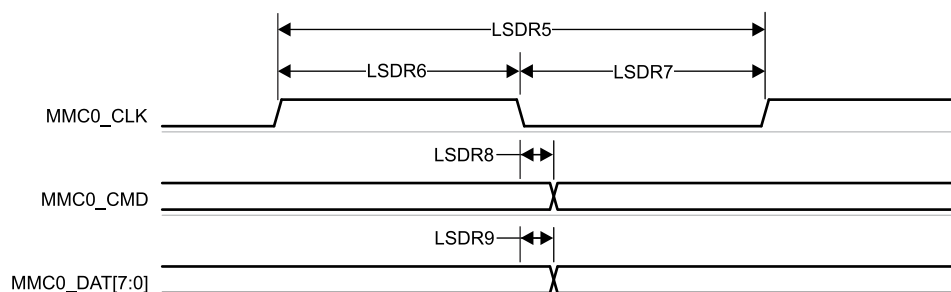


**图 7-78. MMC0 - Legacy SDR - Transmit Mode**

#### 7.10.5.17.1.2 High Speed SDR Mode

表 7-61, 图 7-79, 表 7-62, and 图 7-80 present timing requirements and switching characteristics for MMC0 - High Speed SDR Mode.

**表 7-61. MMC0 Timing Requirements - High Speed SDR Mode**

see 图 7-79

| NO.    |                     |                                                             | MIN  | MAX | UNIT |
|--------|---------------------|-------------------------------------------------------------|------|-----|------|
| HSSDR1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge      | 2.99 |     | ns   |
| HSSDR2 | $t_{h(clkH-cmdV)}$  | Hold time, MMC0_CMD valid after MMC0_CLK rising edge        | 2.67 |     | ns   |
| HSSDR3 | $t_{su(dV-clkH)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge | 2.99 |     | ns   |
| HSSDR4 | $t_{h(clkH-dV)}$    | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge   | 2.67 |     | ns   |

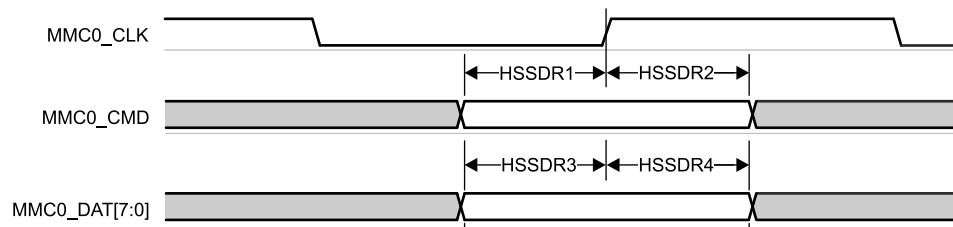


**图 7-79. MMC0 - High Speed SDR Mode - Receive Mode**

**表 7-62. MMC0 Switching Characteristics - High Speed SDR Mode**

see 图 7-80

| NO.    |                    | PARAMETER                                                     | MIN   | MAX | UNIT |
|--------|--------------------|---------------------------------------------------------------|-------|-----|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC0_CLK                                 |       | 50  | MHz  |
| HSSDR5 | $t_{c(clk)}$       | Cycle time, MMC0_CLK                                          | 20    |     | ns   |
| HSSDR6 | $t_{w(clkH)}$      | Pulse duration, MMC0_CLK high                                 | 9.2   |     | ns   |
| HSSDR7 | $t_{w(clkL)}$      | Pulse duration, MMC0_CLK low                                  | 9.2   |     | ns   |
| HSSDR8 | $t_{d(clkL-cmdV)}$ | Delay time, MMC0_CLK falling edge to MMC0_CMD transition      | - 3.2 | 3.8 | ns   |
| HSSDR9 | $t_{d(clkL-dV)}$   | Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition | - 3.2 | 3.8 | ns   |

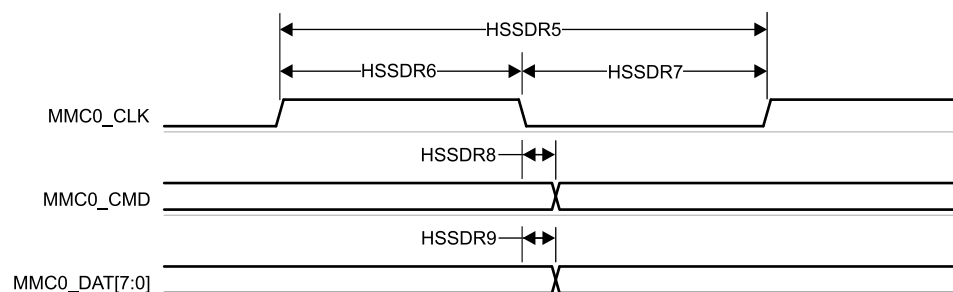


**图 7-80. MMC0 - High Speed SDR Mode - Transmit Mode**

### 7.10.5.17.1.3 High Speed DDR Mode

表 7-63, 图 7-81, 表 7-64, and 图 7-82 present timing requirements and switching characteristics for MMC0 - High Speed DDR Mode.

**表 7-63. MMC0 Timing Requirements - High Speed DDR Mode**

see 图 7-81

| NO.    |                     |                                                            | MIN  | MAX | UNIT |
|--------|---------------------|------------------------------------------------------------|------|-----|------|
| HSDDR1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge     | 3.79 |     | ns   |
| HSDDR2 | $t_{h(clkH-cmdV)}$  | Hold time, MMC0_CMD valid after MMC0_CLK rising edge       | 2.67 |     | ns   |
| HSDDR3 | $t_{su(dV-clkV)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK transition | 0.74 |     | ns   |
| HSDDR4 | $t_{h(clkV-dV)}$    | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK transition   | 1.67 |     | ns   |

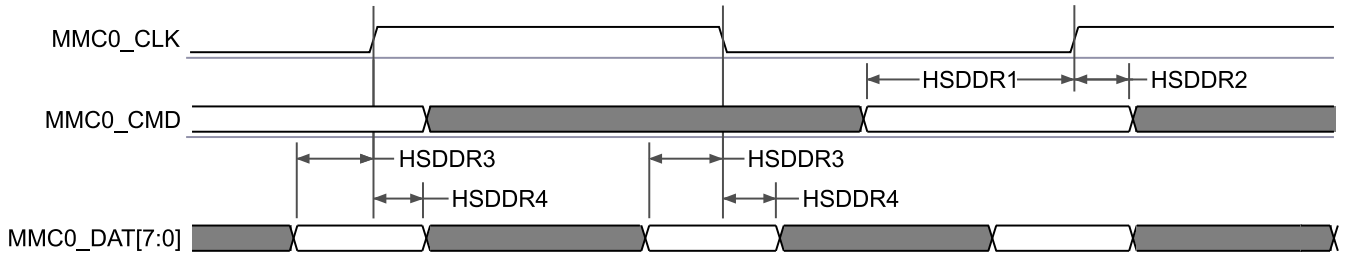


**图 7-81. MMC0 - High Speed DDR Mode - Receive Mode**

**表 7-64. MMC0 Switching Characteristics - High Speed DDR Mode**

see 图 7-82

| NO.    |                    | PARAMETER                                                   | MIN | MAX  | UNIT |
|--------|--------------------|-------------------------------------------------------------|-----|------|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC0_CLK                               |     | 50   | MHz  |
| HSDDR5 | $t_{c(clk)}$       | Cycle time, MMC0_CLK                                        | 20  |      | ns   |
| HSDDR6 | $t_{w(clkH)}$      | Pulse duration, MMC0_CLK high                               | 9.2 |      | ns   |
| HSDDR7 | $t_{w(clkL)}$      | Pulse duration, MMC0_CLK low                                | 9.2 |      | ns   |
| HSDDR8 | $t_{d(clkH-cmdV)}$ | Delay time, MMC0_CLK rising edge to MMC0_CMD transition     | 3.4 | 9.8  | ns   |
| HSDDR9 | $t_{d(clkV-dV)}$   | Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition | 2.9 | 6.85 | ns   |

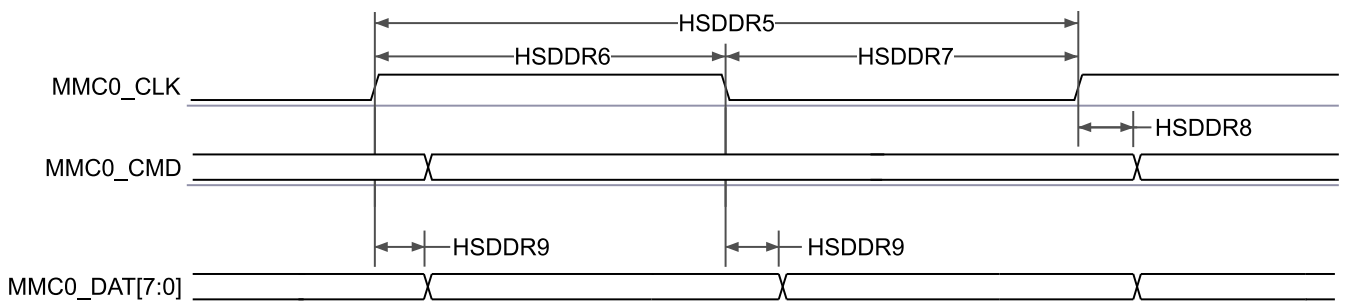


**图 7-82. MMC0 - High Speed DDR Mode - Transmit Mode**

#### 7.10.5.17.1.4 HS200 Mode

表 7-65 和 图 7-83 present switching characteristics for MMC0 - HS200 Mode.

**表 7-65. MMC0 Switching Characteristics - HS200 Mode**

see 图 7-83

| NO.    | PARAMETER          | MIN  | MAX  | UNIT |
|--------|--------------------|------|------|------|
|        | $f_{op}(clk)$      |      | 200  | MHz  |
| HS2005 | $t_{c}(clk)$       | 5    |      | ns   |
| HS2006 | $t_{w}(clkH)$      | 2.08 |      | ns   |
| HS2007 | $t_{w}(clkL)$      | 2.08 |      | ns   |
| HS2008 | $t_{d}(clkL-cmdV)$ | 0.99 | 3.16 | ns   |
| HS2009 | $t_{d}(clkL-dV)$   | 0.99 | 3.16 | ns   |

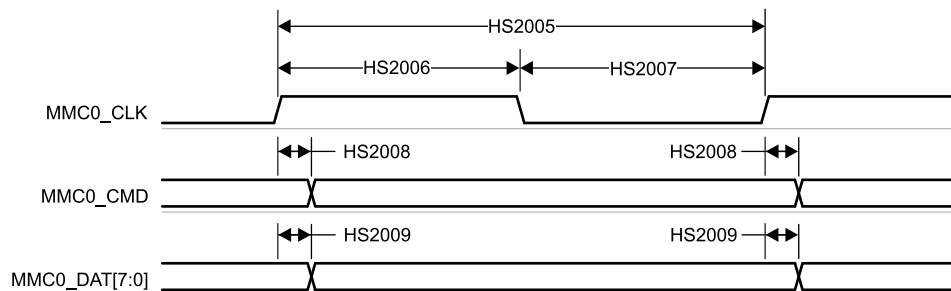


**图 7-83. MMC0 - HS200 Mode - Transmit Mode**

#### 7.10.5.17.1.5 HS400 Mode

表 7-66 和 图 7-84 present switching characteristics for MMC0 - HS400 Mode.

**表 7-66. MMC0 Switching Characteristics - HS400 Mode**

see 图 7-84

| NO.    | PARAMETER          | DESCRIPTION                                                   | MIN  | MAX  | UNIT |
|--------|--------------------|---------------------------------------------------------------|------|------|------|
|        | $f_{op}(clk)$      | Operating frequency, MMC0_CLK                                 |      | 200  | MHz  |
| HS4005 | $t_{c}(clk)$       | Cycle time, MMC0_CLK                                          | 5    |      | ns   |
| HS4006 | $t_{w}(clkH)$      | Pulse duration, MMC0_CLK high                                 | 2.08 |      | ns   |
| HS4007 | $t_{w}(clkL)$      | Pulse duration, MMC0_CLK low                                  | 2.08 |      | ns   |
| HS4008 | $t_{d}(clkH-cmdV)$ | Delay time, MMC0_CLK rising clock edge to MMC0_CMD transition | 0.99 | 3.28 | ns   |
| HS4009 | $t_{d}(clkV-dV)$   | Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition   | 0.59 | 1.84 | ns   |

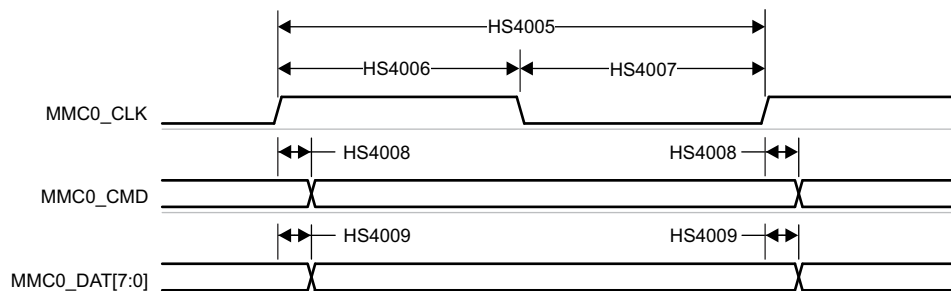


**图 7-84. eMMC in - HS400 Mode - Transmitter Mode**

### 7.10.5.17.2 MMC1/2 - SD/SDIO Interface

MMC1 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and they support the following SD Card applications:

- Default speed
- High speed
- UHS - I SDR12
- UHS - I SDR25
- UHS - I SDR50
- UHS - I SDR104
- UHS - I DDR50

表 7-67 presents the required DLL software configuration settings for MMC1 timing modes.

表 7-67. MMC1 DLL Delay Mapping for All Timing Modes

| REGISTER NAME  |                                    | MMCSD12_SS_PHY_CTRL_4_REG |             |                    |                   | MMCSD12_SS_PHY_CTRL_5_REG |
|----------------|------------------------------------|---------------------------|-------------|--------------------|-------------------|---------------------------|
| BIT FIELD      |                                    | [20]                      | [15:12]     | [8]                | [4:0]             | [2:0]                     |
| BIT FIELD NAME |                                    | OTAPDLYENA                | OTAPDLYSEL  | ITAPDLYENA         | ITAPDLYSEL        | CLKBUFSEL                 |
| MODE           | DESCRIPTION                        | DELAY ENABLE              | DELAY VALUE | INPUT DELAY ENABLE | INPUT DELAY VALUE | DELAY BUFFER DURATION     |
| Default Speed  | 4-bit PHY operating 3.3 V, 25 MHz  | 0x0                       | 0x0         | 0x0                | 0x0               | 0x7                       |
| High Speed     | 4-bit PHY operating 3.3 V, 50 MHz  | 0x0                       | 0x0         | 0x0                | 0x0               | 0x7                       |
| UHS-I SDR12    | 4-bit PHY operating 1.8 V, 25 MHz  | 0x1                       | 0xF         | 0x0                | 0x0               | 0x7                       |
| UHS-I SDR25    | 4-bit PHY operating 1.8 V, 50 MHz  | 0x1                       | 0xF         | 0x0                | 0x0               | 0x7                       |
| UHS-I SDR50    | 4-bit PHY operating 1.8 V, 100 MHz | 0x1                       | 0xC         | 0x1                | Tuning            | 0x7                       |
| UHS-I DR50     | 4-bit PHY operating 1.8 V, 50 MHz  | 0x1                       | 0xC         | 0x1                | 0x2               | 0x7                       |
| UHS-I SDR104   | 4-bit PHY operating 1.8 V, 200 MHz | 0x1                       | 0x5         | 0x1                | Tuning            | 0x7                       |

表 7-68 presents timing conditions for MMC1.

表 7-68. MMC1 Timing Conditions

| PARAMETER                             |                                              |                              | MIN    | MAX  | UNIT |
|---------------------------------------|----------------------------------------------|------------------------------|--------|------|------|
| INPUT CONDITIONS                      |                                              |                              |        |      |      |
| SR <sub>i</sub>                       | Input slew rate                              | Default Speed, High Speed    | 0.69   | 2.06 | V/ns |
|                                       |                                              | UHS - I SDR12, UHS - I SDR25 | 0.34   | 1.34 | V/ns |
|                                       |                                              | USH-1 DDR50                  | 1.00   | 2.00 | V/ns |
| OUTPUT CONDITIONS                     |                                              |                              |        |      |      |
| C <sub>L</sub>                        | Output load capacitance                      | All modes                    | 1      | 10   | pF   |
| PCB CONNECTIVITY REQUIREMENTS         |                                              |                              |        |      |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | UHS - I DDR50                | 240.03 | 1134 | ps   |
|                                       |                                              | All other modes              | 126    | 1386 | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | UHS - I DDR50                |        | 20   | ps   |
|                                       |                                              | UHS - I SDR104               |        | 8    | ps   |
|                                       |                                              | All other modes              |        | 100  | ps   |

#### 7.10.5.17.2.1 Default Speed Mode

表 7-69, 图 7-85, 表 7-70, and 图 7-86 present timing requirements and switching characteristics for MMC1/2 - Default Speed Mode.

**表 7-69. MMC1/2 Timing Requirements - Default Speed Mode**

see 图 7-85

| NO. |                     |                                                                 | MIN  | MAX | UNIT |
|-----|---------------------|-----------------------------------------------------------------|------|-----|------|
| DS1 | $t_{su}(cmdV-clkH)$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 2.15 |     | ns   |
| DS2 | $t_h(clkH-cmdV)$    | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 4.56 |     | ns   |
| DS3 | $t_{su}(dV-clkH)$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 2.15 |     | ns   |
| DS4 | $t_h(clkH-dV)$      | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 4.56 |     | ns   |

A. x = 1, 2 for MMC1 and MMC2

B. x = 1, 2 for MMC1 and MMC2

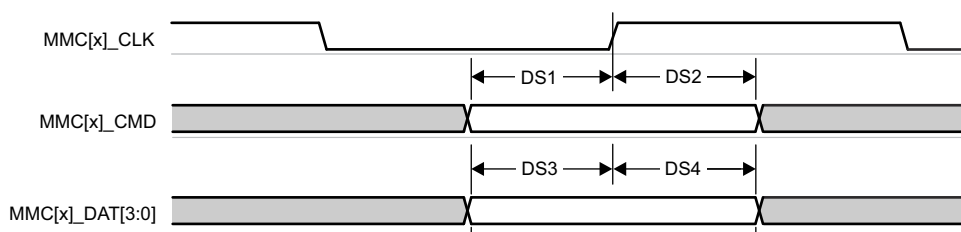


**图 7-85. MMC1/2 - Default Speed - Receive Mode**

**表 7-70. MMC1/2 Switching Characteristics - Default Speed Mode**

see 图 7-86

| NO. |                  | PARAMETER                                                         | MIN    | MAX  | UNIT |
|-----|------------------|-------------------------------------------------------------------|--------|------|------|
|     | $f_{op}(clk)$    | Operating frequency, MMC[x]_CLK                                   |        | 25   | MHz  |
| DS5 | $t_c(clk)$       | Cycle time, MMC[x]_CLK                                            | 40     |      | ns   |
| DS6 | $t_w(clkH)$      | Pulse duration, MMC[x]_CLK high                                   | 18.7   |      | ns   |
| DS7 | $t_w(clkL)$      | Pulse duration, MMC[x]_CLK low                                    | 18.7   |      | ns   |
| DS8 | $t_d(clkL-cmdV)$ | Delay time, MMC[x]_CLK falling edge to MMC[x]_CMD transition      | - 3.53 | 3.53 | ns   |
| DS9 | $t_d(clkL-dV)$   | Delay time, MMC[x]_CLK falling edge to MMC[x]_DAT[3:0] transition | - 3.53 | 3.53 | ns   |

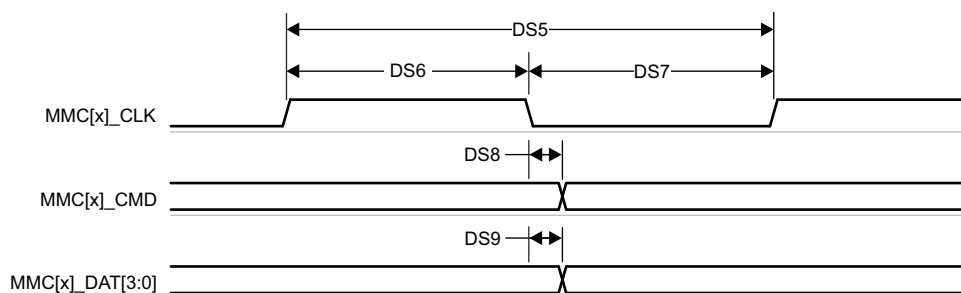


**图 7-86. MMC1/2 - Default Speed - Transmit Mode**



## 7.10.5.17.2.2 High Speed Mode

表 7-71, 图 7-87, 表 7-72, and 图 7-88 present timing requirements and switching characteristics for MMC1/2 - High Speed Mode.

表 7-71. MMC1/2 Timing Requirements - High Speed Mode

see 图 7-87

| NO. |                     |                                                                 | MIN  | MAX | UNIT |
|-----|---------------------|-----------------------------------------------------------------|------|-----|------|
| HS1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 2.15 |     | ns   |
| HS2 | $t_{h(clkH-cmdV)}$  | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 2.26 |     | ns   |
| HS3 | $t_{su(dV-clkH)}$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 2.15 |     | ns   |
| HS4 | $t_{h(clkH-dV)}$    | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 2.26 |     | ns   |

A. x = 1, 2 for MMC1 and MMC2

B. x = 1, 2 for MMC1 and MMC2

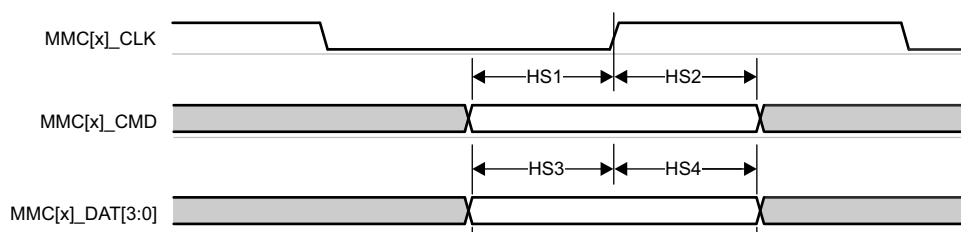


图 7-87. MMC1 /2 - High Speed - Receive Mode

表 7-72. MMC1/2 Switching Characteristics - High Speed Mode

see 图 7-88

| NO. |                    | PARAMETER                                                         | MIN    | MAX  | UNIT |
|-----|--------------------|-------------------------------------------------------------------|--------|------|------|
|     | $f_{op(clk)}$      | Operating frequency, MMC[x]_CLK                                   |        | 50   | MHz  |
| HS5 | $t_{c(clk)}$       | Cycle time, MMC[x]_CLK                                            | 20     |      | ns   |
| HS6 | $t_{w(clkH)}$      | Pulse duration, MMC[x]_CLK high                                   | 9.2    |      | ns   |
| HS7 | $t_{w(clkL)}$      | Pulse duration, MMC[x]_CLK low                                    | 9.2    |      | ns   |
| HS8 | $t_{d(clkL-cmdV)}$ | Delay time, MMC[x]_CLK falling edge to MMC[x]_CMD transition      | - 2.07 | 2.07 | ns   |
| HS9 | $t_{d(clkL-dV)}$   | Delay time, MMC[x]_CLK falling edge to MMC[x]_DAT[3:0] transition | - 2.07 | 2.07 | ns   |

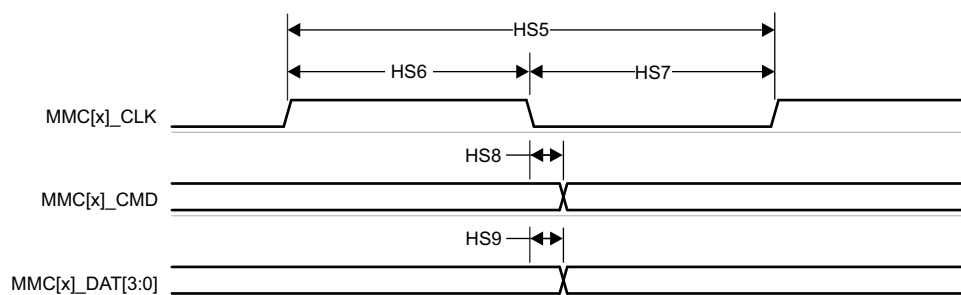


图 7-88. MMC1/2 - High Speed - Transmit Mode

#### 7.10.5.17.2.3 UHS -I SDR12 Mode

表 7-73, 图 7-89, 表 7-74, and 图 7-90 present timing requirements and switching characteristics for MMC1/2 - UHS-I SDR12 Mode.

**表 7-73. MMC1/2 Timing Requirements - UHS-I SDR12 Mode**

see 图 7-89

| NO.    |                     |                                                                 | MIN  | MAX | UNIT |
|--------|---------------------|-----------------------------------------------------------------|------|-----|------|
| SDR121 | $t_{su(cmdV-clkH)}$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 5.46 |     | ns   |
| SDR122 | $t_{h(clkH-cmdV)}$  | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 1.67 |     | ns   |
| SDR123 | $t_{su(dV-clkH)}$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 5.46 |     | ns   |
| SDR124 | $t_{h(clkH-dV)}$    | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 1.67 |     | ns   |

A. x = 1, 2 for MMC1 and MMC2

B. x = 1, 2 for MMC1 and MMC2

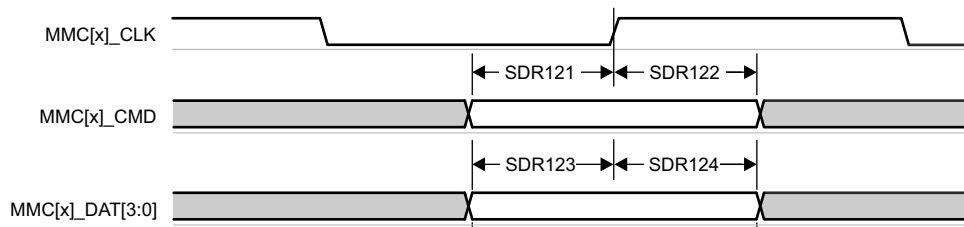


**图 7-89. MMC1/2 - UHS-I SDR12 - Receive Mode**

**表 7-74. MMC1/2 Switching Characteristics - UHS-I SDR12 Mode**

see 图 7-90

| NO.    |                    | PARAMETER                                                        | MIN  | MAX   | UNIT |
|--------|--------------------|------------------------------------------------------------------|------|-------|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC[x]_CLK                                  |      | 25    | MHz  |
| SDR125 | $t_{c(clk)}$       | Cycle time, MMC[x]_CLK                                           | 40   |       | ns   |
| SDR126 | $t_{w(clkH)}$      | Pulse duration, MMC[x]_CLK high                                  | 18.7 |       | ns   |
| SDR127 | $t_{w(clkL)}$      | Pulse duration, MMC[x]_CLK low                                   | 18.7 |       | ns   |
| SDR128 | $t_{d(clkH-cmdV)}$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 1.2  | 13.55 | ns   |
| SDR129 | $t_{d(clkH-dV)}$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 1.2  | 13.55 | ns   |

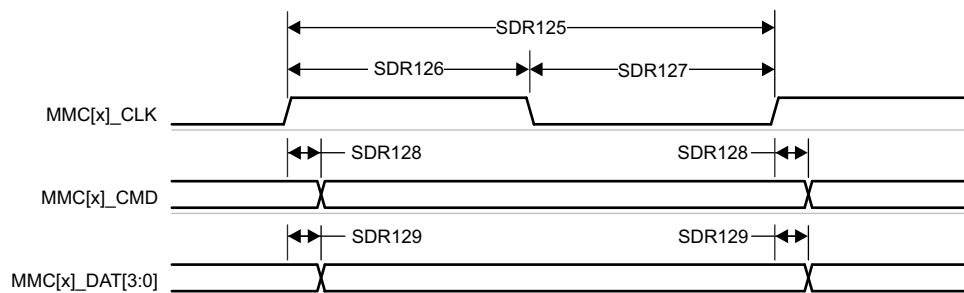


**图 7-90. MMC1/2 - UHS-I SDR12 - Transmit Mode**

## 7.10.5.17.2.4 UHS -I SDR25 Mode

表 7-75, 图 7-91, 表 7-76, and 图 7-92 present timing requirements and switching characteristics for MMC1/2 - UHS-I SDR25 Mode.

表 7-75. MMC1/2 Timing Requirements - UHS-I SDR25 Mode

see 图 7-91

| NO.    |                     |                                                                 | MIN  | MAX | UNIT |
|--------|---------------------|-----------------------------------------------------------------|------|-----|------|
| SDR251 | $t_{su(cmdV-clkH)}$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 2.1  |     | ns   |
| SDR252 | $t_{h(clkH-cmdV)}$  | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 1.67 |     | ns   |
| SDR253 | $t_{su(dV-clkH)}$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 2.1  |     | ns   |
| SDR254 | $t_{h(clkH-dV)}$    | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 1.67 |     | ns   |

A. x = 1, 2 for MMC1 and MMC2

B. x = 1, 2 for MMC1 and MMC2

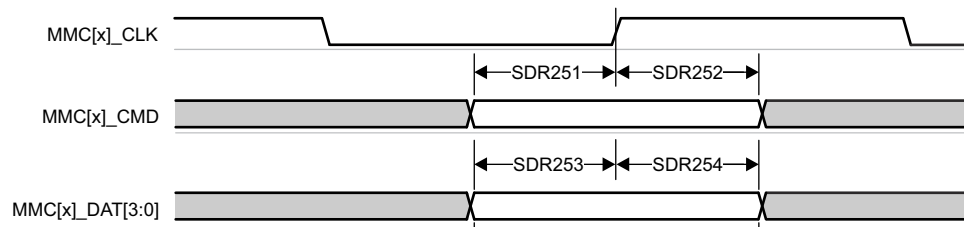


图 7-91. MMC1/2 - UHS-I SDR25 - Receive Mode

表 7-76. MMC1/2 Switching Characteristics - UHS-I SDR25 Mode

see 图 7-92

| NO.    |                    | PARAMETER                                                        | MIN | MAX  | UNIT |
|--------|--------------------|------------------------------------------------------------------|-----|------|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC[x]_CLK                                  |     | 50   | MHz  |
| SDR255 | $t_{c(clk)}$       | Cycle time, MMC[x]_CLK                                           | 20  |      | ns   |
| SDR256 | $t_{w(clkH)}$      | Pulse duration, MMC[x]_CLK high                                  | 9.2 |      | ns   |
| SDR257 | $t_{w(clkL)}$      | Pulse duration, MMC[x]_CLK low                                   | 9.2 |      | ns   |
| SDR258 | $t_{d(clkH-cmdV)}$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 2.4 | 9.37 | ns   |
| SDR259 | $t_{d(clkH-dV)}$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 2.4 | 9.37 | ns   |

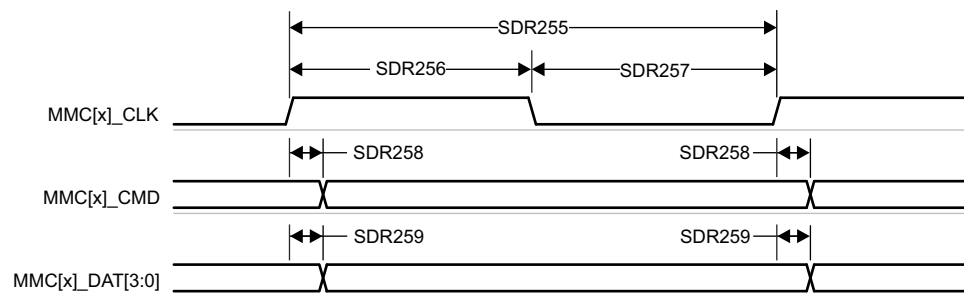


图 7-92. MMC1/2 - UHS-I SDR25 - Transmit Mode

#### 7.10.5.17.2.5 UHS -I SDR50 Mode

表 7-77, and 图 7-93 presents switching characteristics for MMC1/2 - UHS-I SDR50 Mode.

**表 7-77. MMC1/2 Switching Characteristics - UHS-I SDR50 Mode**

see 图 7-93

| NO.    | PARAMETER          |                                                                  | MIN  | MAX  | UNIT |
|--------|--------------------|------------------------------------------------------------------|------|------|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC[x]_CLK                                  |      | 100  | MHz  |
| SDR505 | $t_{c(clk)}$       | Cycle time, MMC[x]_CLK                                           | 10   |      | ns   |
| SDR506 | $t_{w(clkH)}$      | Pulse duration, MMC[x]_CLK high                                  | 4.45 |      | ns   |
| SDR507 | $t_{w(clkL)}$      | Pulse duration, MMC[x]_CLK low                                   | 4.45 |      | ns   |
| SDR508 | $t_{d(clkH-cmdV)}$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 1.2  | 6.35 | ns   |
| SDR509 | $t_{d(clkH-dV)}$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 1.2  | 6.35 | ns   |

A. x = 1, 2 for MMC1 and MMC2

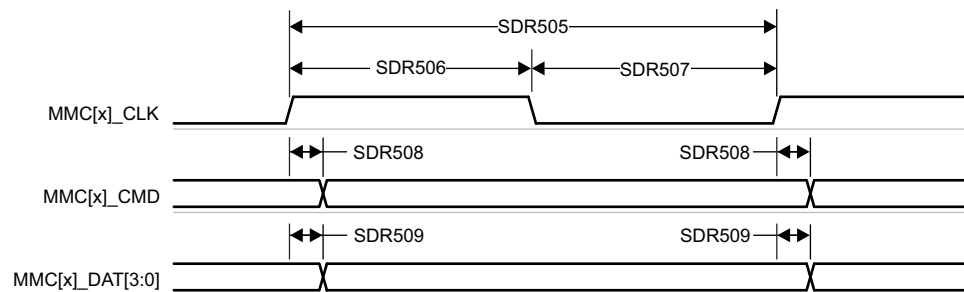


**图 7-93. MMC1/2 - UHS-I SDR50 - Transmit Mode**

### 7.10.5.17.2.6 UHS -I DDR50 Mode

表 7-78 和 图 7-94 呈现 switching characteristics for MMC1/2 - UHS-I DDR50 Mode.

**表 7-78. MMC1/2 Switching Characteristics - UHS-I DDR50 Mode**

see 图 7-94

| NO.    | PARAMETER          |                                                                 | MIN  | MAX  | UNIT |
|--------|--------------------|-----------------------------------------------------------------|------|------|------|
|        | $f_{op}(clk)$      | Operating frequency, MMC[x]_CLK                                 |      | 40   | MHz  |
| DDR505 | $t_{c}(clk)$       | Cycle time, MMC[x]_CLK                                          | 25   |      | ns   |
| DDR506 | $t_{w}(clkH)$      | Pulse duration, MMC[x]_CLK high                                 | 9.2  |      | ns   |
| DDR507 | $t_{w}(clkL)$      | Pulse duration, MMC[x]_CLK low                                  | 9.2  |      | ns   |
| DDR508 | $t_{d}(clkH-cmdV)$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition     | 1.12 | 3.46 | ns   |
| DDR509 | $t_{d}(clk-dV)$    | Delay time, MMC[x]_CLK transition to MMC[x]_DAT[3:0] transition | 1.12 | 6.12 | ns   |

A. x = 1, 2 for MMC1 and MMC2

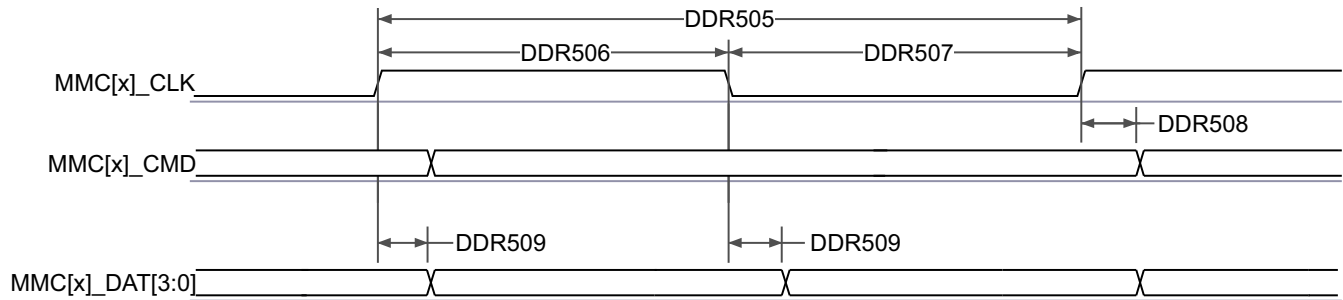


**图 7-94. MMC1/2 - UHS-I DDR50 - Transmit Mode**

#### 7.10.5.17.2.7 UHS -I SDR104 Mode

表 7-79, and 图 7-95 present switching characteristics for MMC1/2 - UHS-I SDR104 Mode.

表 7-79. MMC1/2 Switching Characteristics - UHS-I SDR104 Mode

see 图 7-95

| NO.     | PARAMETER          |                                                                  | MIN  | MAX  | UNIT |
|---------|--------------------|------------------------------------------------------------------|------|------|------|
|         | $f_{op}(clk)$      | Operating frequency, MMC[x]_CLK                                  |      | 200  | MHz  |
| SDR1045 | $t_{c}(clk)$       | Cycle time, MMC[x]_CLK                                           | 5    |      | ns   |
| SDR1046 | $t_{w}(clkH)$      | Pulse duration, MMC[x]_CLK high                                  | 2.12 |      | ns   |
| SDR1047 | $t_{w}(clkL)$      | Pulse duration, MMC[x]_CLK low                                   | 2.12 |      | ns   |
| SDR1048 | $t_{d}(clkH-cmdV)$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 1.07 | 3.21 | ns   |
| SDR1049 | $t_{d}(clkH-dV)$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 1.07 | 3.21 | ns   |

A. x = 1, 2 for MMC1 and MMC2

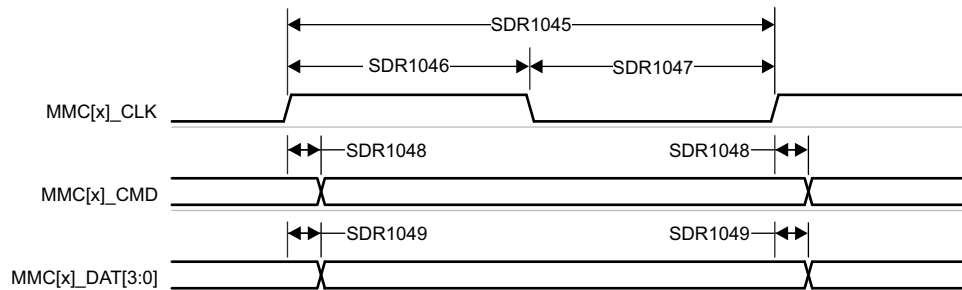


图 7-95. MMC1/2 - UHS-I SDR104 - Transmit Mode

#### 7.10.5.18 CPTS

表 7-80 represents CPTS timing conditions.

表 7-80. CPTS Timing Conditions

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| $SR_i$                   | Input slew rate         | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| $C_L$                    | Output load capacitance | 2   | 10  | pF   |

节 7.10.5.18.1, 节 7.10.5.18.2, 图 7-96, and 图 7-97 present timing requirements and switching characteristics of the CPTS interface.

#### 7.10.5.18.1 CPTS Timing Requirements

see 图 7-96

| NO. |                     |                                               | MIN                     | MAX | UNIT |
|-----|---------------------|-----------------------------------------------|-------------------------|-----|------|
| T1  | $t_{w}(HWnTSPUSH)$  | Pulse duration, HWnTSPUSH <sup>(2)</sup> high | 12P + 2 <sup>(1)</sup>  |     | ns   |
| T2  | $t_{w}(HWnTSPUSHL)$ | Pulse duration, HWnTSPUSH <sup>(2)</sup> low  | 12P + 2 <sup>(1)</sup>  |     | ns   |
| T3  | $t_{c}(RFT\_CLK)$   | Cycle time, RFT_CLK                           | 5                       | 8   | ns   |
| T4  | $t_{w}(RFT\_CLKH)$  | Pulse duration, RFT_CLK high                  | 0.45 * T <sup>(3)</sup> |     | ns   |
| T5  | $t_{w}(RFT\_CLKL)$  | Pulse duration, RFT_CLK low                   | 0.45 * T <sup>(3)</sup> |     | ns   |

(1) P = functional clock period in ns.

(2) In HWnTSPUSH, n = 1 to 2.

(3) T = RFT\_CLK period in ns.

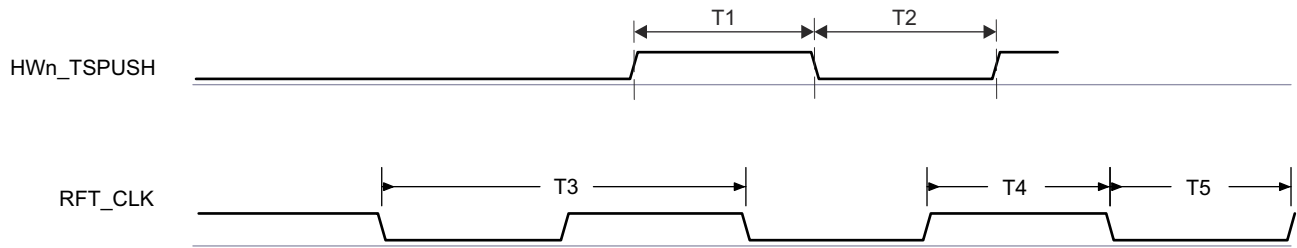


图 7-96. CPTS Timing Requirements

## 7.10.5.18.2 CPTS Switching Characteristics

see 图 7-97

| NO. | PARAMETER            |                                               | SOURCE  | MIN             | MAX | UNIT |
|-----|----------------------|-----------------------------------------------|---------|-----------------|-----|------|
| T6  | $t_{w(TS\_COMPH)}$   | Pulse duration, TS_COMP high                  |         | $36P - 2^{(1)}$ |     | ns   |
| T7  | $t_{w(TS\_COMPL)}$   | Pulse duration, TS_COMP low                   |         | $36P - 2^{(1)}$ |     | ns   |
| T8  | $t_{w(TS\_SYNCH)}$   | Pulse duration, TS_SYNC high                  |         | $36P - 2^{(1)}$ |     | ns   |
| T9  | $t_{w(TS\_SYNCL)}$   | Pulse duration, TS_SYNC low                   |         | $36P - 2^{(1)}$ |     | ns   |
| T10 | $t_{w(SYNCL\_OUTH)}$ | Pulse duration, SYNCn_OUT <sup>(2)</sup> high | TS_SYNC | $36P - 2^{(1)}$ |     | ns   |
|     |                      |                                               | TS_GENF | $5P - 2^{(1)}$  |     | ns   |
| T11 | $t_{w(SYNCL\_OUTL)}$ | Pulse duration, SYNCn_OUT <sup>(2)</sup> low  | TS_SYNC | $36P - 2^{(1)}$ |     | ns   |
|     |                      |                                               | TS_GENF | $5P - 2^{(1)}$  |     | ns   |

(1) P = functional clock period in ns.

(2) n = 0 to 3 in SYNCn\_OUT

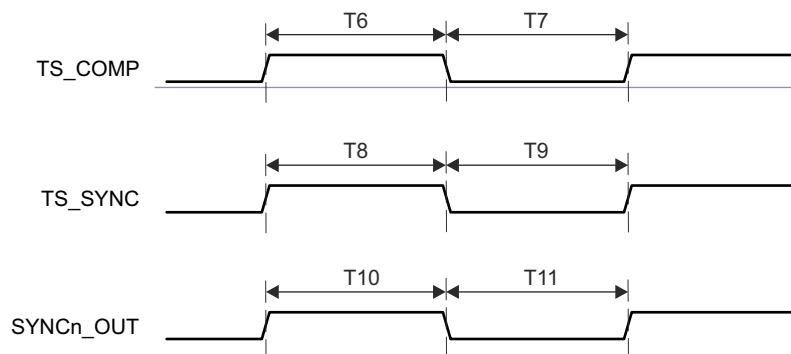


图 7-97. CPTS Switching Characteristics

For more information, see *Navigator Subsystem (NAVSS)* section in *Data Movement Architecture (DMA)* chapter in the device TRM.

## 7.10.5.19 OSPI

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

表 7-81 represents OSPI timing conditions.

表 7-81. OSPI Timing Conditions

| PARAMETER         |                 |                 | MIN | MAX | UNIT |
|-------------------|-----------------|-----------------|-----|-----|------|
| INPUT CONDITIONS  |                 |                 |     |     |      |
| SR <sub>I</sub>   | Input slew rate | 3.3 V           | 2   | 6   | V/ns |
|                   |                 | All other modes | 1   | 6   | V/ns |
| OUTPUT CONDITIONS |                 |                 |     |     |      |

**表 7-81. OSPI Timing Conditions (continued)**

| PARAMETER                             |                                                                                                     |                                          | MIN                   | MAX                   | UNIT |
|---------------------------------------|-----------------------------------------------------------------------------------------------------|------------------------------------------|-----------------------|-----------------------|------|
| C <sub>L</sub>                        | Output load capacitance                                                                             | All modes                                | 3                     | 10                    | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                                                                                     |                                          |                       |                       |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay<br>OSPI_CLK trace                                                                 | No Loopback;<br>Internal Pad<br>Loopback |                       | 450                   | ps   |
|                                       | Propagation delay<br>OSPI_LBCLKO trace                                                              | External Board<br>Loopback               | 2*L-30 <sup>(2)</sup> | 2*L+30 <sup>(2)</sup> | ps   |
|                                       | Propagation delay<br>OSPI_DQS trace                                                                 | DQS                                      | L-30 <sup>(2)</sup>   | L+30 <sup>(2)</sup>   | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch<br>OSPI_D[i:0] <sup>(1)</sup> , OSPI_CS <i>n</i><br>relative to OSPI_CLK | All modes                                |                       | 60                    | ps   |

- (1) i in D[i:0] = 0 to 7 for OSPI0; i in [i:0] = 3 for OSPI1  
(2) L = Propagation delay of OSPI\_CLK trace



### 7.10.5.19.1 OSPI0 PHY Mode

#### 7.10.5.19.1.1 OSPI With Data Training

##### 备注

I/O timing requirements and switching characteristics are not applicable when OSPI is used with data training. Follow the [OSPI and QSPI Board Design and Layout Guidelines](#) section to ensure proper operation.

#### 7.10.5.19.1.1.1 OSPI Switching Characteristics - Data Training

| PARAMETER    | DESCRIPTION     | MODE      | MIN | MAX | UNIT |
|--------------|-----------------|-----------|-----|-----|------|
| $t_{c(CLK)}$ | Cycle time, CLK | DDR, 1.8V | 6   |     | ns   |
|              |                 | DDR, 3.3V | 7.5 |     | ns   |
| $t_{c(CLK)}$ | Cycle time, CLK | SDR, 1.8V | 6   |     | ns   |
|              |                 | SDR, 3.3V | 7.5 |     | ns   |

#### 7.10.5.19.1.2 OSPI Without Data Training

##### 备注

The I/O Timings provided in this section are only applicable when data training is not implemented. Additionally, the I/O Timings are valid only for some OSPI usage modes when the corresponding DLL Delays are configured as described in [表 7-82](#) found in this section.

节 7.10.5.19.1.2.4, 节 7.10.5.19.1.2.2, 节 7.10.5.19.1.2, and 节 7.10.5.19.1.2 present switching characteristics for OSPI DDR and SDR Mode.

#### 7.10.5.19.1.2.1 OSPI Timing Requirements - SDR Mode

表 7-82. OSPI DLL Delay Mapping - SDR Timing Modes

| MODE      | OSPI_PHY_CONFIGURATION_REG BIT FIELD | DELAY VALUE |
|-----------|--------------------------------------|-------------|
| All modes | PHY_CONFIG_TX_DLL_DELAY_FLD          | 0x0         |
|           | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x0         |

表 7-83. OSPI Timing Requirements - SDR Mode

| NO. | PARAMETER         | DESCRIPTION                                                                  | MODE                          | MIN | MAX | UNIT |
|-----|-------------------|------------------------------------------------------------------------------|-------------------------------|-----|-----|------|
| O21 | $t_{su(D-LBCLK)}$ | Setup time, D[i:0] valid before active LBCLK input (DQS) edge <sup>(1)</sup> | 1.8V, External Board Loopback | 0.6 |     | ns   |
|     |                   |                                                                              | 3.3V, External Board Loopback | 0.9 |     | ns   |
| O22 | $t_h(LBCLK-D)$    | Hold time, D[i:0] valid after active LBCLK input (DQS) edge <sup>(1)</sup>   | 1.8V, External Board Loopback | 1.7 |     | ns   |
|     |                   |                                                                              | 3.3V, External Board Loopback | 2   |     | ns   |

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

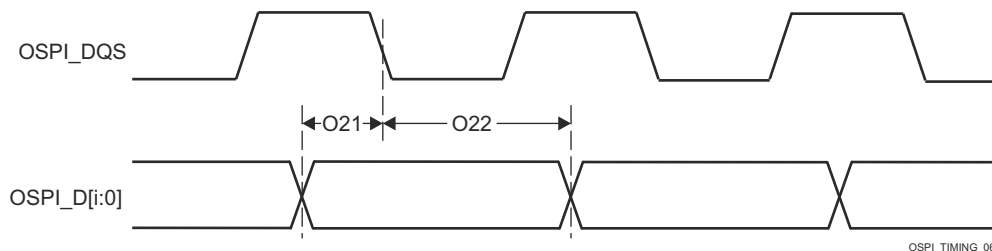


图 7-98. OSPI Timing Requirements - SDR, External Loopback Clock

#### 7.10.5.19.1.2.2 OSPI Switching Characteristics - SDR Mode

| NO. | PARAMETER        | DESCRIPTION                                                     | MODE | MIN                                                     | MAX                                                     | UNIT |
|-----|------------------|-----------------------------------------------------------------|------|---------------------------------------------------------|---------------------------------------------------------|------|
| O7  | $t_{c(CLK)}$     | Cycle time, CLK                                                 | 1.8V | 7                                                       |                                                         | ns   |
|     |                  |                                                                 | 3.3V | 7.5                                                     |                                                         | ns   |
| O8  | $t_{w(CLKL)}$    | Pulse duration, CLK low                                         |      | –<br>$0.3+0.475 \cdot P$<br>(2)                         |                                                         | ns   |
| O9  |                  | Pulse duration, CLK high                                        |      | –<br>$0.3+0.475 \cdot P$<br>(2)                         |                                                         | ns   |
| O10 | $t_{d(CSn-CLK)}$ | Delay time, CSn[3:0] active edge to CLK rising edge             | 1.8V | $0.475 \cdot P + 0.975 \cdot M \cdot R - 7$ (2) (3) (5) | $0.525 \cdot P + 1.025 \cdot M \cdot R + 1$ (2) (3) (5) | ns   |
|     |                  |                                                                 | 3.3V | $0.475 \cdot P + 0.975 \cdot M \cdot R - 7$ (2) (3) (5) | $0.525 \cdot P + 1.025 \cdot M \cdot R + 1$ (2) (3) (5) | ns   |
| O11 | $t_{d(CLK-CSn)}$ | Delay time, CLK rising edge to CSn inactive edge                | 1.8V | $0.475 \cdot P + 0.975 \cdot N \cdot R - 1$ (2) (4) (5) | $0.525 \cdot P + 1.025 \cdot N \cdot R + 1$ (2) (4) (5) | ns   |
|     |                  |                                                                 | 3.3V | $0.475 \cdot P + 0.975 \cdot N \cdot R - 1$ (2) (4) (5) | $0.525 \cdot P + 1.025 \cdot N \cdot R + 1$ (2) (4) (5) | ns   |
| O12 | $t_{d(CLK-D)}$   | Delay time, CLK active edge to D[i:0] transition <sup>(1)</sup> | 1.8V | – 1.16                                                  | 1.25                                                    | ns   |
|     |                  |                                                                 | 3.3V | – 1.33                                                  | 1.51                                                    | ns   |

- (1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1  
(2) P = CLK cycle time = SCLK period  
(3) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(4) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(5) R = refclk

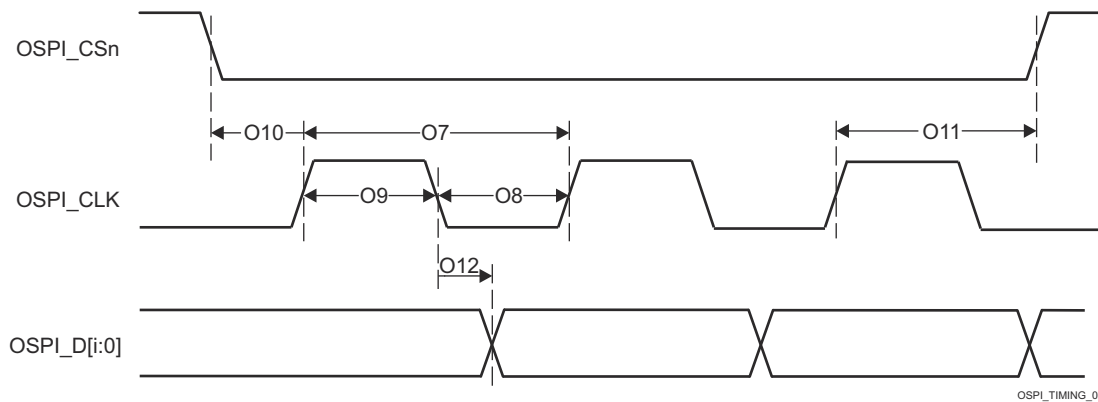


图 7-99. OSPI Switching Characteristics - SDR

节 7.10.5.19.1.2.3, 节 7.10.5.19.1.2.1, 节 7.10.5.19.1.2.2, 节 7.10.5.19.1.2.2, and 图 7-98 presents timing requirements for OSPI DDR and SDR Mode.

#### 7.10.5.19.1.2.3 OSPI Timing Requirements - DDR Mode

表 7-84. OSPI DLL Delay Mapping - DDR Timing Modes

| MODE     | OSPI_PHY_CONFIGURATION_REG<br>BIT FIELD | OSPI0       | OSPI1 |
|----------|-----------------------------------------|-------------|-------|
|          |                                         | DELAY VALUE |       |
| TRANSMIT |                                         |             |       |
| 1.8V     | PHY_CONFIG_TX_DLL_DELAY_FLD             | 0x54        | 0x54  |

表 7-84. OSPI DLL Delay Mapping - DDR Timing Modes (continued)

| MODE            | OSPI_PHY_CONFIGURATION_REG<br>BIT FIELD | OSPI0       | OSPI1 |
|-----------------|-----------------------------------------|-------------|-------|
|                 |                                         | DELAY VALUE |       |
| 3.3V            | PHY_CONFIG_TX_DLL_DELAY_FLD             | 0x55        | 0x5C  |
| <b>RECEIVE</b>  |                                         |             |       |
| 1.8V, DQS       | PHY_CONFIG_RX_DLL_DELAY_FLD             | 0x23        | 0x29  |
| 3.3V, DQS       | PHY_CONFIG_RX_DLL_DELAY_FLD             | 0x47        | 0x42  |
| All other modes | PHY_CONFIG_RX_DLL_DELAY_FLD             | 0x0         | 0x0   |

表 7-85. OSPI Timing Requirements - DDR Mode

| NO. | PARAMETER         | DESCRIPTION                                                            | MODE                          | MIN                 | MAX | UNIT |
|-----|-------------------|------------------------------------------------------------------------|-------------------------------|---------------------|-----|------|
| O15 | $t_{su}(D-LBCLK)$ | Setup time, D[i:0] valid before active LBCLK (DQS) edge <sup>(1)</sup> | 1.8V, External Board Loopback | 0.52                |     | ns   |
|     |                   |                                                                        | 3.3V, External Board Loopback | 1.97                |     | ns   |
| O16 | $t_h(LBCLK-D)$    | Hold time, D[i:0] valid after active LBCLK (DQS) edge <sup>(1)</sup>   | 1.8V, External Board Loopback | 1.24 <sup>(2)</sup> |     | ns   |
|     |                   |                                                                        | 3.3V, External Board Loopback | 1.44 <sup>(2)</sup> |     | ns   |
| O17 | $t_{su}(D-DQS)$   | Setup time, DQS edge to D[i:0] transition <sup>(1)</sup>               | 1.8V, DQS                     | - 0.46              |     | ns   |
|     |                   |                                                                        | 3.3V, DQS                     | - 0.66              |     | ns   |
| O18 | $t_h(DQS-D)$      | Hold time, DQS edge to D[i:0] transition <sup>(1)</sup>                | 1.8V, DQS                     | 3.59                |     | ns   |
|     |                   |                                                                        | 3.3V, DQS                     | 8.89                |     | ns   |

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

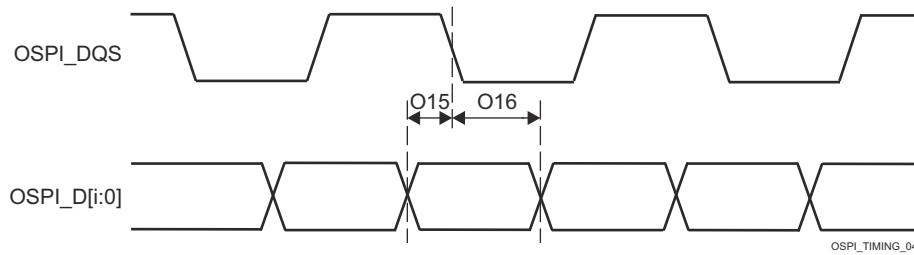
(2) This Hold time requirement is larger than the Hold time provided by a typical flash device. Therefore, the trace length between the SoC and flash device must be sufficiently long enough to ensure that the Hold time is met at the SoC. Refer to [OSPI and QSPI Board Design and Layout Guidelines](#) for more details.

图 7-100. OSPI Timing Requirements - DDR, External Loopback Clock and DQS

## 7.10.5.19.1.2.4 OSPI Switching Characteristics - DDR Mode

| NO. | PARAMETER      | DESCRIPTION                                    | MODE | MIN                                                  | MAX                                                  | UNIT |
|-----|----------------|------------------------------------------------|------|------------------------------------------------------|------------------------------------------------------|------|
| O1  | $t_c(CLK)$     | Cycle time, CLK                                | 1.8V | 19                                                   |                                                      | ns   |
|     |                |                                                | 3.3V | 19                                                   |                                                      | ns   |
| O2  | $t_w(CLKL)$    | Pulse duration, CLK low                        |      | 0.475 * P - 0.3 <sup>(2)</sup>                       |                                                      | ns   |
| O3  | $t_w(CLKH)$    | Pulse duration, CLK high                       |      | 0.475 * P - 0.3 <sup>(2)</sup>                       |                                                      | ns   |
| O4  | $t_d(CLK-CSn)$ | Delay time, CSn active edge to CLK rising edge | 1.8V | 0.475 * P + 0.975 * M * R - 7 <sup>(2) (3) (5)</sup> | 0.525 * P + 1.025 * M * R + 1 <sup>(2) (3) (5)</sup> | ns   |
|     |                |                                                | 3.3V | 0.475 * P + 0.975 * M * R - 7 <sup>(2) (3) (5)</sup> | 0.525 * P + 1.025 * M * R + 1 <sup>(2) (3) (5)</sup> | ns   |

| NO. | PARAMETER        | DESCRIPTION                                                     | MODE                                      | MIN                                           | MAX                                           | UNIT |
|-----|------------------|-----------------------------------------------------------------|-------------------------------------------|-----------------------------------------------|-----------------------------------------------|------|
| O5  | $t_{d(CLK-CSn)}$ | Delay time, CLK rising edge to CSn inactive edge                | 1.8V                                      | $0.475 * P + 0.975 * N * R - 7^{(2) (4) (5)}$ | $0.525 * P + 1.025 * N * R + 1^{(2) (4) (5)}$ | ns   |
|     |                  |                                                                 | 3.3V, OSPI0 DDR TX;<br>3.3V, OSPI1 DDR TX | $0.475 * P + 0.975 * N * R - 7^{(2) (4) (5)}$ | $0.525 * P + 1.025 * N * R + 1^{(2) (4) (5)}$ | ns   |
| O6  | $t_{d(CLK-D)}$   | Delay time, CLK active edge to D[i:0] transition <sup>(1)</sup> | 1.8V, OSPI0 DDR TX;<br>1.8V, OSPI1 DDR TX | - 7.71                                        | - 1.56                                        | ns   |
|     |                  |                                                                 | 3.3V, OSPI0 DDR TX;<br>3.3V, OSPI1 DDR TX | - 7.71                                        | - 1.56                                        | ns   |

- (1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1  
(2) P = CLK cycle time = SCLK period  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(4) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(5) R = refclk

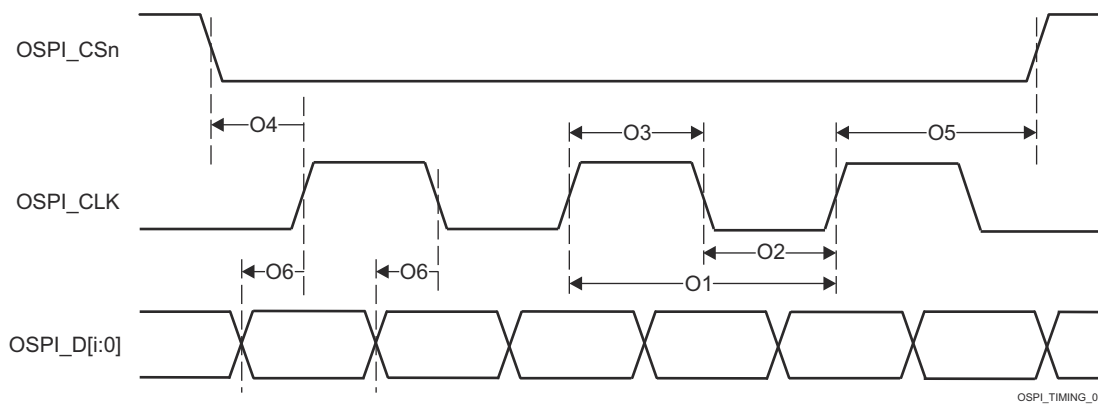


图 7-101. OSPI Switching Characteristics - DDR

### 7.10.5.19.2 OSPI0 Tap Mode

#### 7.10.5.19.2.1 OSPI0 Tap SDR Timing

表 7-86, 图 7-102, 表 7-87, and 图 7-103 present timing requirements and switching characteristics for OSPI0 Tap SDR Mode.

表 7-86. OSPI0/1 Timing Requirements - Tap SDR Mode

see 图 7-102

| NO. |                 |                                                                 | MODE        | MIN                              | MAX | UNIT |
|-----|-----------------|-----------------------------------------------------------------|-------------|----------------------------------|-----|------|
| O19 | $t_{su(D-CLK)}$ | Setup time, OSPI0/1_D[7:0] valid before active OSPI0/1_CLK edge | No Loopback | $(10.4 - (0.975T^{(1)}R^{(2)}))$ |     | ns   |
| O20 | $t_{h(CLK-D)}$  | Hold time, OSPI0/1_D[7:0] valid after active OSPI0/1_CLK edge   | No Loopback | $(-0.2 + (0.975T^{(1)}R^{(2)}))$ |     | ns   |

- (1) T = OSPI\_RD\_DATA\_CAPTURE\_REG[DELAY\_FLD]  
(2) R = refclk cycle time in ns

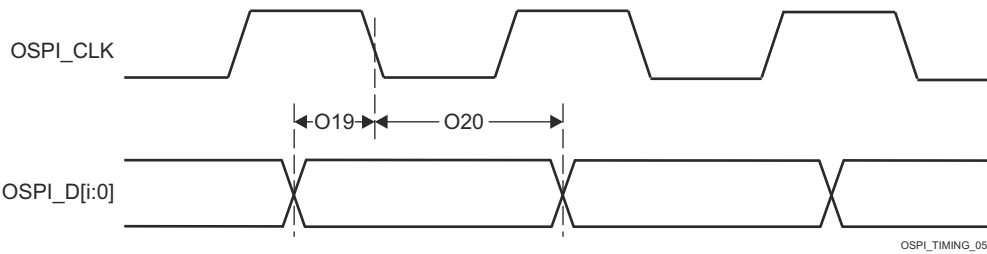


图 7-102. OSPI0/1 Timing Requirements - Tap SDR, No Loopback

**表 7-87. OSPI0/1 Switching Characteristics - Tap SDR Mode**

see 图 7-103

| NO. | PARAMETER        | MODE                                                                  | MIN                                            | MAX                                            | UNIT |
|-----|------------------|-----------------------------------------------------------------------|------------------------------------------------|------------------------------------------------|------|
| O7  | $t_{c(CLK)}$     | Cycle time, OSPI0/1_CLK                                               | 20                                             |                                                | ns   |
| O8  | $t_{w(CLKL)}$    | Pulse duration, OSPI0/1_CLK low                                       | $((0.475P^{(1)}) - 0.3)$                       |                                                | ns   |
| O9  | $t_{w(CLKH)}$    | Pulse duration, OSPI0/1_CLK high                                      | $((0.475P^{(1)}) - 0.3)$                       |                                                | ns   |
| O10 | $t_{d(CSn-CLK)}$ | Delay time, OSPI0/1_CSn[3:0] active edge to OSPI0/1_CLK rising edge   | $((0.475P^{(1)}) + (0.975M^{(2)}R^{(4)}) - 1)$ | $((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + 1)$ | ns   |
| O11 | $t_{d(CLK-CSn)}$ | Delay time, OSPI0/1_CLK rising edge to OSPI0/1_CSn[3:0] inactive edge | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)}) - 1)$ | $((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)}) + 1)$ | ns   |
| O12 | $t_{d(CLK-D)}$   | Delay time, OSPI0/1_CLK active edge to OSPI0/1_D[7:0] transition      | - 2                                            | 2                                              | ns   |

- (1) P = CLK cycle time = SCLK period in ns  
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) R = refclk cycle time in ns

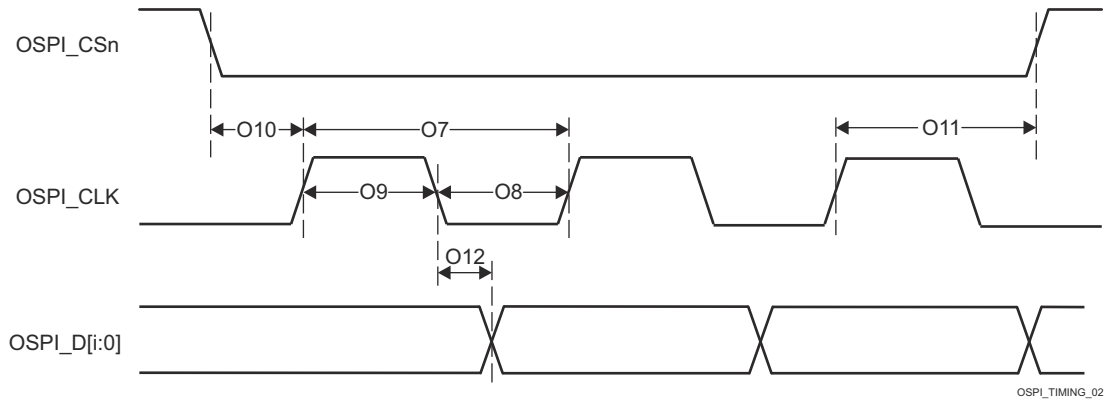


**图 7-103. OSPI0/1 Switching Characteristics - Tap SDR, No Loopback**

### 7.10.5.19.2.2 OSPI0 Tap DDR Timing

表 7-88, 图 7-104, 表 7-89, and 图 7-105 present timing requirements and switching characteristics for OSPI0 Tap DDR Mode.

**表 7-88. OSPI0/1 Timing Requirements - Tap DDR Mode**

see 图 7-104

| NO. |                 |                                                                 | MODE        | MIN                               | MAX | UNIT |
|-----|-----------------|-----------------------------------------------------------------|-------------|-----------------------------------|-----|------|
| O13 | $t_{su(D-CLK)}$ | Setup time, OSPI0/1_D[7:0] valid before active OSPI0/1_CLK edge | No Loopback | $(12.04 - (0.975T^{(1)}R^{(2)}))$ |     | ns   |
| O14 | $t_{h(CLK-D)}$  | Hold time, OSPI0/1_D[7:0] valid after active OSPI0/1_CLK edge   | No Loopback | $(1.84 + (0.975T^{(1)}R^{(2)}))$  |     | ns   |

(1) T = OSPI\_RD\_DATA\_CAPTURE\_REG[DELAY\_FLD]

(2) R = refclk cycle time in ns

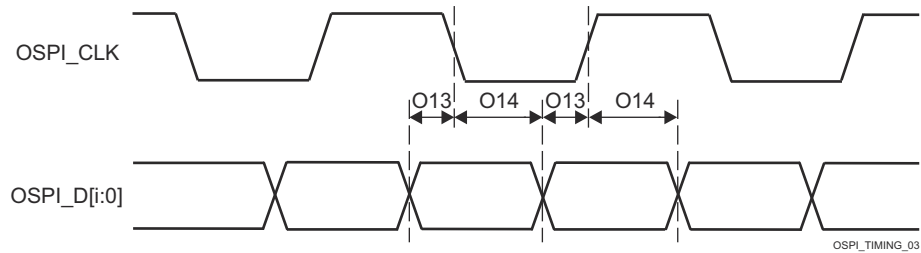


**图 7-104. OSPI0/1 Timing Requirements - Tap DDR, No Loopback**

**表 7-89. OSPI0/1 Switching Characteristics - Tap DDR Mode**

see 图 7-105

| NO. | PARAMETER                                                                              | MODE | MIN                                              | MAX                                            | UNIT |
|-----|----------------------------------------------------------------------------------------|------|--------------------------------------------------|------------------------------------------------|------|
| O1  | $t_{c(CLK)}$ Cycle time, OSPI0/1_CLK                                                   |      | 40                                               |                                                | ns   |
| O2  | $t_{w(CLKL)}$ Pulse duration, OSPI0/1_CLK low                                          |      | $((0.475P^{(1)}) - 0.3)$                         |                                                | ns   |
| O3  | $t_{w(CLKH)}$ Pulse duration, OSPI0/1_CLK high                                         |      | $((0.475P^{(1)}) - 0.3)$                         |                                                | ns   |
| O4  | $t_{d(CSn-CLK)}$ Delay time, OSPI0/1_CSn[3:0] active edge to OSPI0/1_CLK rising edge   |      | $((0.475P^{(1)}) + ((0.975M^{(2)}R^{(4)}) - 1))$ | $((0.525P^{(1)}) + (1.025M^{(2)}R^{(4)}) + 1)$ | ns   |
| O5  | $t_{d(CLK-CSn)}$ Delay time, OSPI0/1_CLK rising edge to OSPI0/1_CSn[3:0] inactive edge |      | $((0.475P^{(1)}) + (0.975N^{(3)}R^{(4)}) - 1)$   | $((0.525P^{(1)}) + (1.025N^{(3)}R^{(4)}) + 1)$ | ns   |
| O6  | $t_{d(CLK-D)}$ Delay time, OSPI0/1_CLK active edge to OSPI0/1_D[7:0] transition        |      | $(-17.94 + (0.975T^{(5)}R^{(4)}))$               | $(-1.56 + (1.025T^{(5)}R^{(4)}))$              | ns   |

- (1) P = CLK cycle time = SCLK period in ns  
(2) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]  
(3) N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]  
(4) R = refclk cycle time in ns  
(5) T = OSPI\_RD\_DATA\_CAPTURE\_REG[DDR\_READ\_DELAY\_FLD]

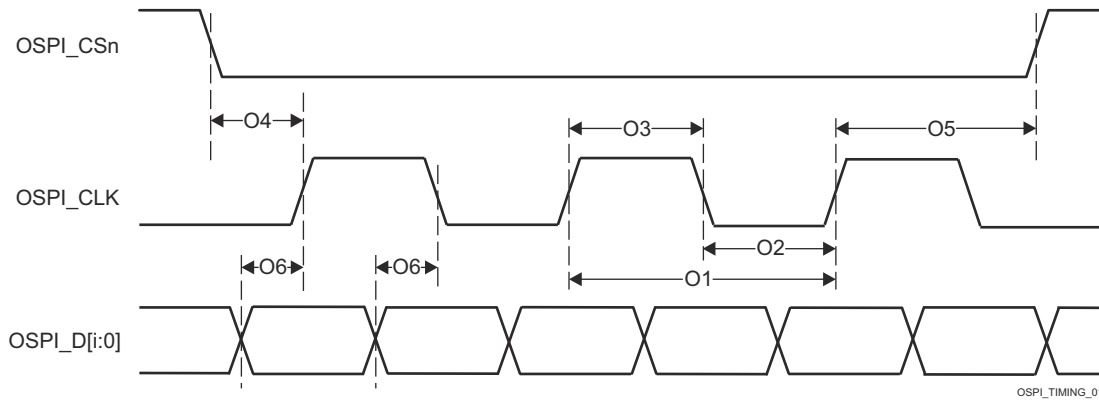


**图 7-105. OSPI0/1 Switching Characteristics - Tap DDR, No Loopback**

### 7.10.5.20 OLDI

#### 7.10.5.20.1 OLDI Switching Characteristics

| NO. | PARAMETER                                                                             | MODE   | MIN   | MAX   | UNIT |
|-----|---------------------------------------------------------------------------------------|--------|-------|-------|------|
| O1  | LVDS Low-to-High Transition Time max                                                  | IOSET1 | 0.18  | 0.5   | ns   |
| O2  | LVDS high-to-low Transition Time max                                                  | IOSET1 | 0.18  | 0.5   | ns   |
| O3  | Transmitter Output Bit Width min                                                      | IOSET1 | 1     | 1     | UI   |
| O4  | Transmitter Pulse Positions - Normalized                                              | IOSET1 | 0.25  | 0.75  | ns   |
| O5  | Variation in transmitter pulse position across Bit 7:0 pulse positions                | IOSET1 | -0.06 | 0.06  | ns   |
| O6  | TxOut Channel to Channel Skew                                                         | IOSET1 |       | 110   | ns   |
| O7  | Transmitter Jitter Cycle-to-Cycle                                                     | IOSET1 | 0.028 | 0.035 | ns   |
| O8  | Input Total Jitter Tolerance (Includes data to clock skew, pulse position variation.) | IOSET1 |       | 0.25  | ns   |



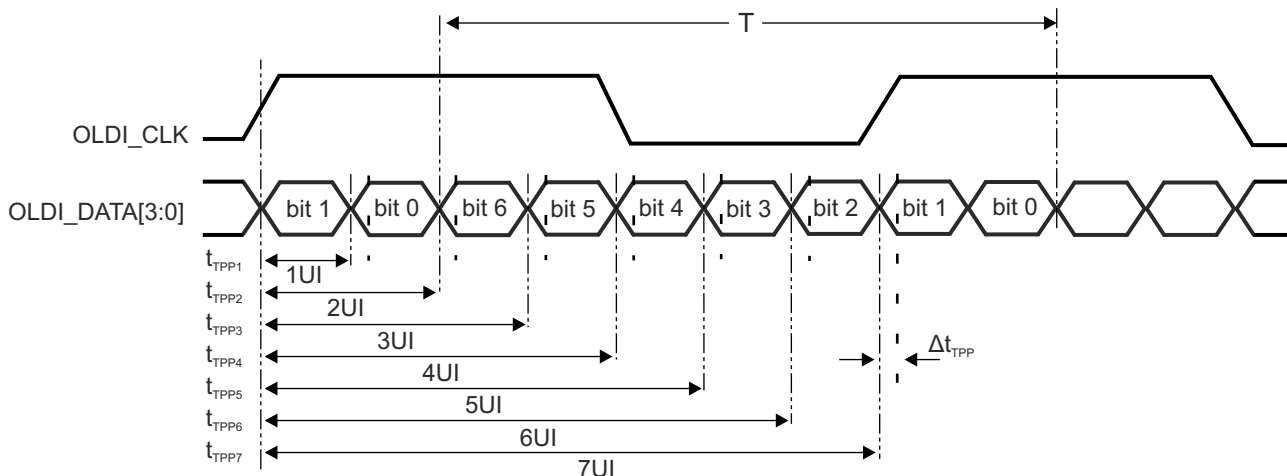


图 7-106. OLDI Transmitter Pulse Positions

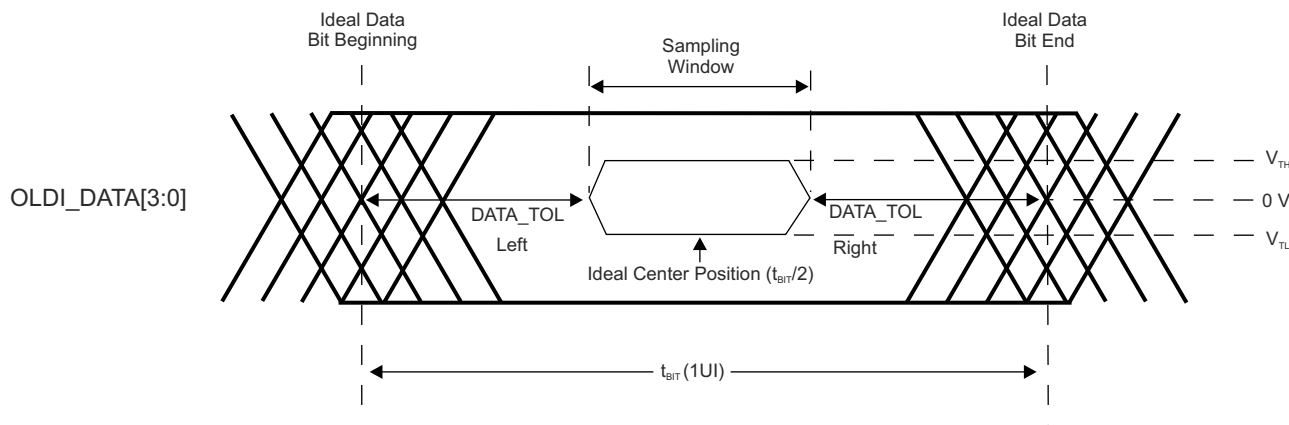


图 7-107. OLDI Data Output Jitter

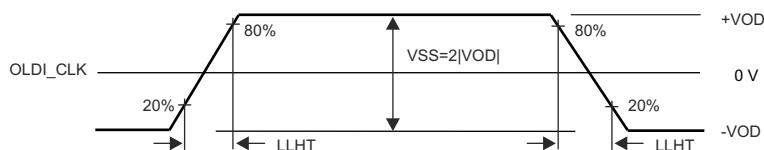


图 7-108. LVDS Output Transition Times

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.21 PCIE

The PCI-Express Subsystem is compliant with the PCIe® Base Specification, Revision 4.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

### 7.10.5.22 Timers

For more details about features and additional description information on the device Timers, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

表 7-90 represents Timers timing conditions.

表 7-90. Timers Timing Conditions

| PARAMETER                | DESCRIPTION             | MODE    | MIN | MAX | UNIT |
|--------------------------|-------------------------|---------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | CAPTURE | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | PWM     | 2   | 10  | pF   |

节 7.10.5.22.1, 节 7.10.5.22.2 和 图 7-109 present timings and switching characteristics of the Timers.

#### 7.10.5.22.1 Timing Requirements for Timers

| NO. | PARAMETER             | DESCRIPTION          | MODE    | MIN                     | MAX | UNIT |
|-----|-----------------------|----------------------|---------|-------------------------|-----|------|
| T1  | t <sub>w(TINPH)</sub> | Pulse duration, high | CAPTURE | 2.5 + 4P <sup>(1)</sup> |     | ns   |
| T2  | t <sub>w(TINPL)</sub> | Pulse duration, low  | CAPTURE | 2.5 + 4P <sup>(1)</sup> |     | ns   |

(1) P = functional clock period in ns.

#### 7.10.5.22.2 Switching Characteristics for Timers

| NO. | PARAMETER             | DESCRIPTION          | MODE | MIN                      | MAX | UNIT |
|-----|-----------------------|----------------------|------|--------------------------|-----|------|
| T3  | t <sub>w(TOUTH)</sub> | Pulse duration, high | PWM  | -2.5 + 4P <sup>(1)</sup> |     | ns   |
| T4  | t <sub>w(TOUTL)</sub> | Pulse duration, low  | PWM  | -2.5 + 4P <sup>(1)</sup> |     | ns   |

(1) P = functional clock period in ns.

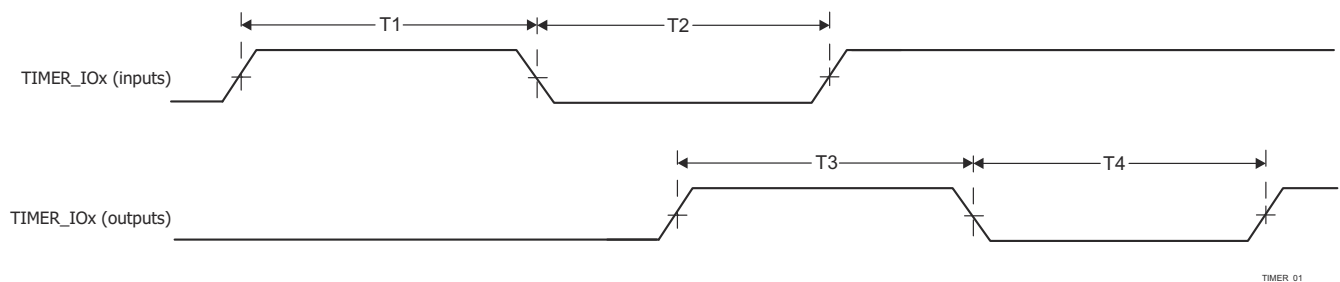


图 7-109. Timer Timing

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

### 7.10.5.23 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding sections within , [Signal Descriptions](#) and *Detailed Description*.

表 7-91 represents UART timing conditions.

表 7-91. UART Timing Conditions

| PARAMETER               | DESCRIPTION | MIN | MAX | UNIT |
|-------------------------|-------------|-----|-----|------|
| <b>INPUT CONDITIONS</b> |             |     |     |      |

表 7-91. UART Timing Conditions (continued)

| PARAMETER                | DESCRIPTION             | MIN | MAX               | UNIT |
|--------------------------|-------------------------|-----|-------------------|------|
| $SR_I$                   | Input slew rate         | 0.5 | 5                 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |                   |      |
| $C_L$                    | Output load capacitance | 1   | 30 <sup>(1)</sup> | pF   |

- (1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

节 7.10.5.23.1, 节 7.10.5.23.2, and 图 7-110 present timing requirements and switching characteristics for UART interface.

#### 7.10.5.23.1 Timing Requirements for UART

| NO. | PARAMETER      | DESCRIPTION                                | MODE | MIN                         | MAX                         | UNIT |
|-----|----------------|--------------------------------------------|------|-----------------------------|-----------------------------|------|
| 4   | $t_{w(rixd)}$  | Pulse width, receive data bit, high or low |      | 0.95U <sup>(1)</sup><br>(2) | 1.05U <sup>(1)</sup><br>(2) | ns   |
| 5   | $t_{w(rixdS)}$ | Pulse width, receive start bit, low        |      | 0.95U <sup>(1)</sup><br>(2) |                             | ns   |

- (1)  $U$  = UART baud time =  $1/\text{Programmed baud rate}$

- (2) This value defines the data valid time, where the input voltage is required to be above  $V_{IH}$  or below  $V_{IL}$ .

#### 7.10.5.23.2 UART Switching Characteristics

| NO. | PARAMETER    | DESCRIPTION                                  | MIN           | MAX           | UNIT |
|-----|--------------|----------------------------------------------|---------------|---------------|------|
|     | $f_{(baud)}$ | Maximum programmable baud rate               |               | 12            | Mbps |
| 2   | $t_{w(TX)}$  | Pulse width, transmit data bit, high or low  | $U - 2^{(1)}$ | $U + 2^{(1)}$ | ns   |
| 3   | $t_{w(RTS)}$ | Pulse width, transmit start bit, high or low | $U - 2^{(1)}$ |               | ns   |

- (1)  $U$  = UART baud time =  $1/\text{Programmed baud rate}$

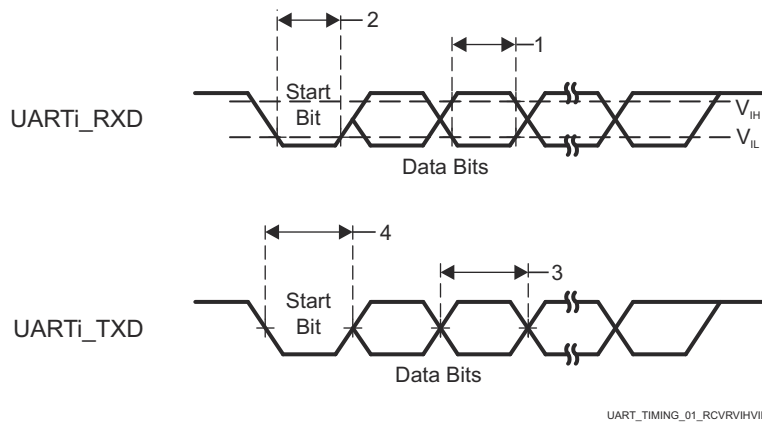


图 7-110. UART Timing

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.24 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

The USB 3.1 GEN1 Dual-Role Device Subsystem is compliant with the Universal Serial Bus (USB) 3.1 Specification, revision 1.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

## 7.10.6 Emulation and Debug

### 7.10.6.1 Trace

表 7-92. Trace Timing Conditions

| PARAMETER                            |                                              | MIN | MAX | UNIT |
|--------------------------------------|----------------------------------------------|-----|-----|------|
| <b>OUTPUT CONDITIONS</b>             |                                              |     |     |      |
| $C_L$                                | Output load capacitance                      | 2   | 5   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |                                              |     |     |      |
| $t_d$ (Trace Mismatch)               | Propagation delay mismatch across all traces |     | 200 | ps   |

表 7-93 和 图 7-111 assume testing over the recommended operating conditions and electrical characteristic conditions.

表 7-93. Trace Switching Characteristics

| NO.        | PARAMETER                                    |                                                    | MIN  | MAX | UNIT |
|------------|----------------------------------------------|----------------------------------------------------|------|-----|------|
| 1.8 V Mode |                                              |                                                    |      |     |      |
| DBTR1      | $t_{\text{c}}(\text{TRC\_CLK})$              | Cycle time, TRC_CLK                                | 6.50 |     | ns   |
| DBTR2      | $t_{\text{w}}(\text{TRC\_CLKH})$             | Pulse width, TRC_CLK high                          | 2.50 |     | ns   |
| DBTR3      | $t_{\text{w}}(\text{TRC\_CLKL})$             | Pulse width, TRC_CLK low                           | 2.50 |     | ns   |
| DBTR4      | $t_{\text{osu}}(\text{TRC\_DATAV-TRC\_CLK})$ | Output setup time, TRC_DATA valid to TRC_CLK edge  | 0.81 |     | ns   |
| DBTR5      | $t_{\text{oh}}(\text{TRC\_CLK-TRC\_DATAI})$  | Output hold time, TRC_CLK edge to TRC_DATA invalid | 0.81 |     | ns   |
| DBTR6      | $t_{\text{osu}}(\text{TRC\_CTLV-TRC\_CLK})$  | Output setup time, TRC_CTL valid to TRC_CLK edge   | 0.81 |     | ns   |
| DBTR7      | $t_{\text{oh}}(\text{TRC\_CLK-TRC\_CTLI})$   | Output hold time, TRC_CLK edge to TRC_CTL invalid  | 0.81 |     | ns   |
| 3.3 V Mode |                                              |                                                    |      |     |      |
| DBTR1      | $t_{\text{c}}(\text{TRC\_CLK})$              | Cycle time, TRC_CLK                                | 9.75 |     | ns   |
| DBTR2      | $t_{\text{w}}(\text{TRC\_CLKH})$             | Pulse width, TRC_CLK high                          | 4.13 |     | ns   |
| DBTR3      | $t_{\text{w}}(\text{TRC\_CLKL})$             | Pulse width, TRC_CLK low                           | 4.13 |     | ns   |
| DBTR4      | $t_{\text{osu}}(\text{TRC\_DATAV-TRC\_CLK})$ | Output setup time, TRC_DATA valid to TRC_CLK edge  | 1.22 |     | ns   |
| DBTR5      | $t_{\text{oh}}(\text{TRC\_CLK-TRC\_DATAI})$  | Output hold time, TRC_CLK edge to TRC_DATA invalid | 1.22 |     | ns   |
| DBTR6      | $t_{\text{osu}}(\text{TRC\_CTLV-TRC\_CLK})$  | Output setup time, TRC_CTL valid to TRC_CLK edge   | 1.22 |     | ns   |
| DBTR7      | $t_{\text{oh}}(\text{TRC\_CLK-TRC\_CTLI})$   | Output hold time, TRC_CLK edge to TRC_CTL invalid  | 1.22 |     | ns   |

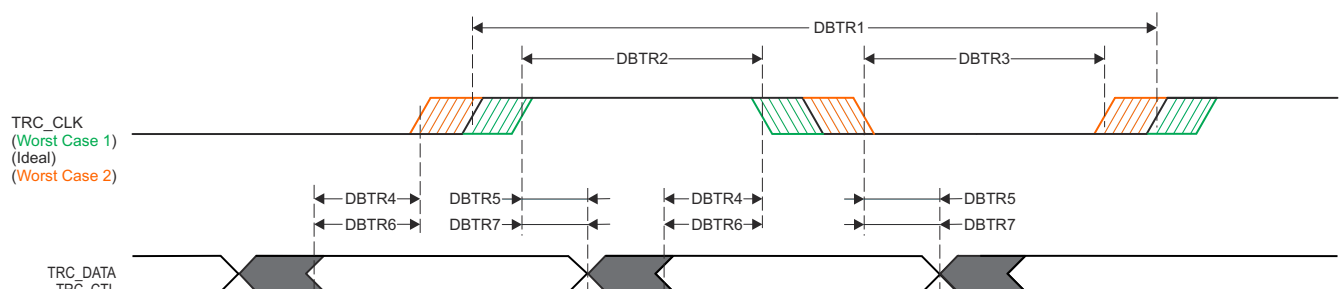


图 7-111. Trace Switching Characteristics

### 7.10.6.2 JTAG

For more details about features and additional description information on the device IEEE 1149.1 Standard – Test – Access Port, see the corresponding sections within [Signal Descriptions](#) and *Detailed Description*.

#### 备注

The JTAG signals are split across two IO power domains on the device. Timings parameters defined in this section only apply when the two IO power domains are operating at the same voltage and level-shifters are not inserted into the signal path. Values for the following timing parameters are not defined when operating the two IO power domains at different voltages since propagation delay through the device IO buffers differ when some are operating at 1.8 V while others are operating at 3.3 V. This effectively reduces timing margin beyond the values defined in this section. The JTAG interface is still expected to function when the two IO power domains are operated at different voltages, assuming the system designer has implemented appropriate level-shifters and the operating frequency is reduced to accommodate additional delay inserted by the level-shifters and IO buffers operating at different voltages.

**表 7-94. JTAG Timing Conditions**

| PARAMETER                             |                                              | MIN  | MAX                 | UNIT |
|---------------------------------------|----------------------------------------------|------|---------------------|------|
| <b>Input Conditions</b>               |                                              |      |                     |      |
| SR <sub>I</sub>                       | Input slew rate                              | 0.50 | 2.00                | V/ns |
| <b>Output Conditions</b>              |                                              |      |                     |      |
| C <sub>L</sub>                        | Output load capacitance                      | 5    | 15                  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |                                              |      |                     |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace              | 83.5 | 1000 <sup>(1)</sup> | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces |      | 100                 | ps   |

- (1) Maximum propagation delay associated with the JTAG signal traces has a significant impact on maximum TCK operating frequency. It may be possible to increase the trace delay beyond this value, but the operating frequency of TCK must be reduced to account for the additional trace delay.

#### 7.10.6.2.1 JTAG Electrical Data and Timing

节 7.10.6.2.1.1, 节 7.10.6.2.1.2, and 图 7-112 assume testing over the recommended operating conditions and electrical characteristic conditions.

##### 7.10.6.2.1.1 JTAG Timing Requirements

See 图 7-112

| NO. |                           |                                                  | MIN                 | MAX | UNIT |
|-----|---------------------------|--------------------------------------------------|---------------------|-----|------|
| J1  | t <sub>c</sub> (TCK)      | Cycle time minimum, TCK                          | 46.5 <sup>(1)</sup> |     | ns   |
| J2  | t <sub>w</sub> (TCKH)     | Pulse width minimum, TCK high                    | 18.6 <sup>(2)</sup> |     | ns   |
| J3  | t <sub>w</sub> (TCKL)     | Pulse width minimum, TCK low                     | 18.6 <sup>(2)</sup> |     | ns   |
| J4  | t <sub>su</sub> (TDI-TCK) | Input setup time minimum, TDI valid to TCK high  | 4.5                 |     | ns   |
|     | t <sub>su</sub> (TMS-TCK) | Input setup time minimum, TMS valid to TCK high  | 4.5                 |     | ns   |
| J5  | t <sub>h</sub> (TCK-TDI)  | Input hold time minimum, TDI valid from TCK high | 2                   |     | ns   |
|     | t <sub>h</sub> (TCK-TMS)  | Input hold time minimum, TMS valid from TCK high | 2                   |     | ns   |

- (1) The maximum TCK operating frequency assumes the following timing requirements and switching characteristics for the attached debugger. The operating frequency of TCK must be reduced to provide appropriate timing margin if the debugger exceeds any of these assumptions.
- Minimum TDO setup time of 4.6 ns relative to the rising edge of TCK
  - TDI and TMS output delay in the range of – 16.5 ns to 14.0 ns relative to the falling edge of TCK
- (2) P = TCK cycle time in ns

### 7.10.6.2.1.2 JTAG Switching Characteristics

See 图 7-112

| NO. | PARAMETER               |                                            | MIN | MAX | UNIT |
|-----|-------------------------|--------------------------------------------|-----|-----|------|
| J6  | $t_d(\text{TCKL-TDOI})$ | Delay time minimum, TCK low to TDO invalid | 0   |     | ns   |
| J7  | $t_d(\text{TCKL-TDOV})$ | Delay time maximum, TCK low to TDO valid   |     | 12  | ns   |

- The JTAG signals are split across two IO power domains on the device. Timings parameters defined in this table only apply when the two IO power domains are operating at the same voltage. Values for these timing parameters are not defined when operating the two IO power domains at different voltages since propagation delay through the device IO buffers differ when some are operating at 1.8V while others are operating at 3.3V. This effectively reduces timing margin beyond the values defined in this table. The JTAG interface is still expected to function when the two IO power domains are operated at different voltages, assuming the system designer has implemented appropriate level shifters and the operating frequency is reduced to accommodate additional delay inserted by the level-shifters and IO buffers operating at different voltages.

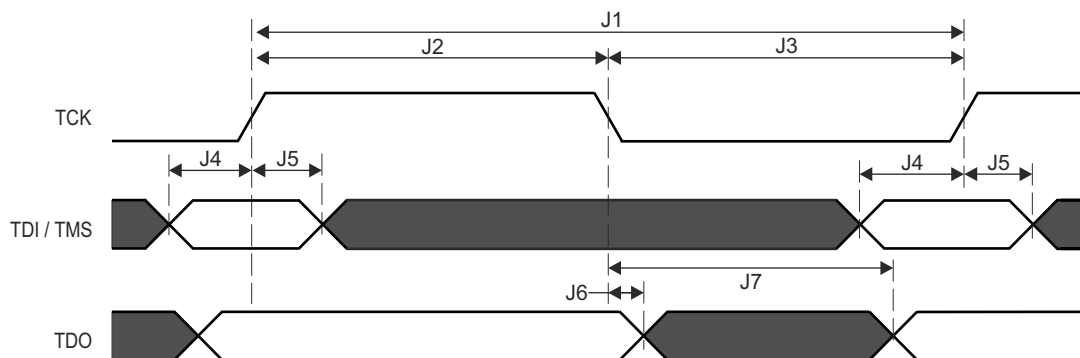


图 7-112. JTAG Timing Requirements and Switching Characteristics

## 8 Detailed Description

### 8.1 Overview

The AM69 processor family is based on the evolutionary Jacinto 7 architecture, targeted at ADAS and Autonomous Vehicle (AV) applications and built on extensive market knowledge accumulated over a decade of TI's leadership in the ADAS processor market. The AM69 provides high performance compute for both traditional and deep learning algorithms at industry leading power/performance ratios with a high level of system integration to enable scalability and lower costs for advanced automotive platforms supporting multiple sensor modalities in centralized ECUs or stand-alone sensors. Key cores include next generation DSP with scalar and vector cores, dedicated deep learning and traditional algorithm accelerators, latest Arm and GPU processors for general compute, an integrated next generation imaging subsystem (ISP), video codec, Ethernet hub and isolated MCU island. All protected by automotive grade safety and security hardware accelerators.

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#### 备注

For more information on features, subsystems, and architecture of superset device System on Chip (SoC), see the device TRM.

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### 8.2 功能方框图

图 8-1 是器件的功能方框图。

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#### 备注

要了解 TI 软件开发套件 (SDK) 目前支持哪些器件功能，请参阅 [AM69 软件构建表 \(PROCESSOR-SDK-AM69\)](#) 和 [AM69A 软件构建表 \(PROCESSOR-SDK-AM69A\)](#)。

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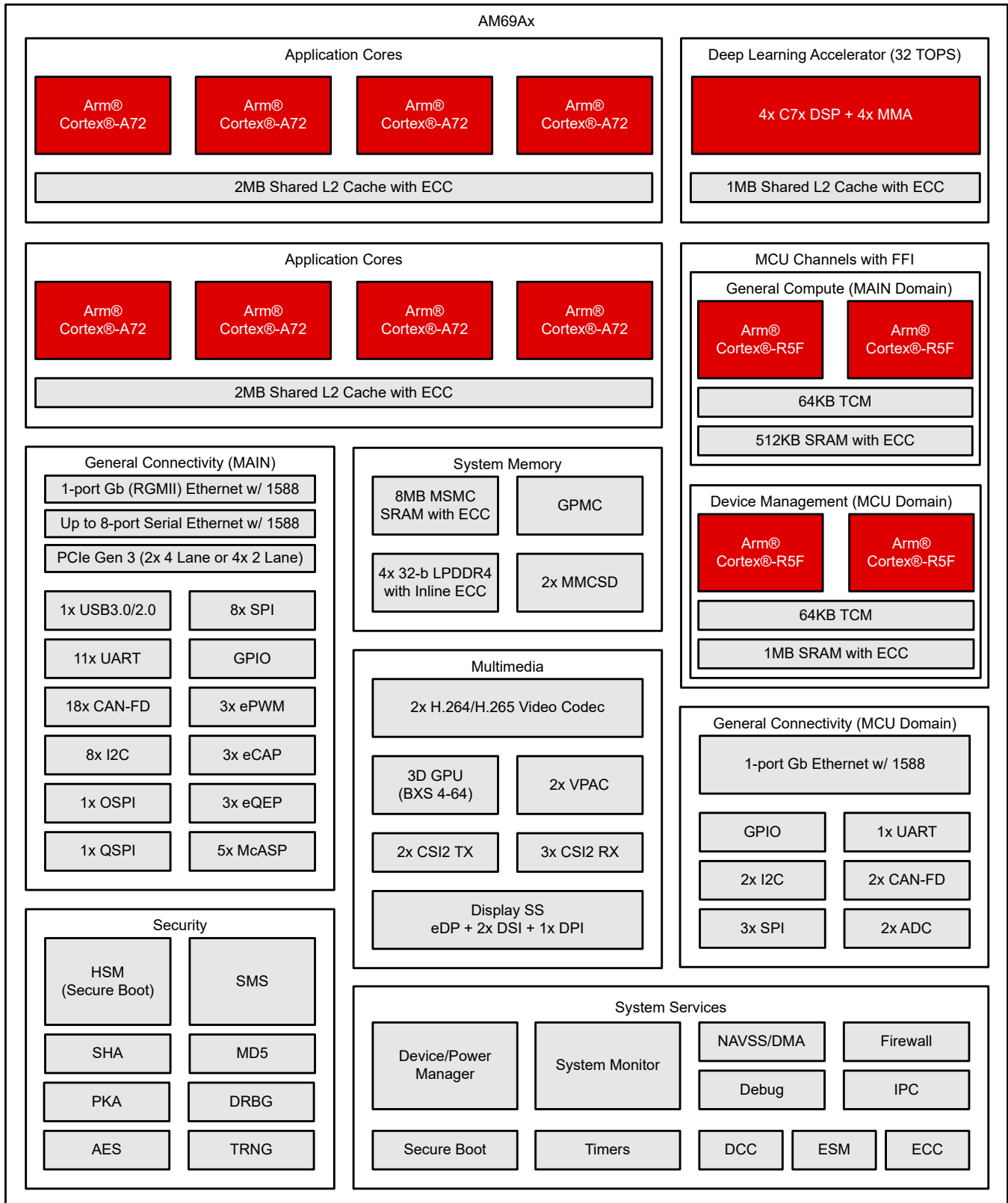


**图 8-1. 功能方框图**



## 8.3 Processor Subsystems

### 8.3.1 Arm Cortex-A72

The device implements one dual-core Arm® Cortex®-A72 MPU, which is integrated inside the Compute Cluster, along with other modules. The Cortex-A72 cores are general-purpose processors that can be used for running customer applications.

The A72SS is built around the Arm Cortex-A72 MPCore (A72 cluster), which is provided by Arm and configured by TI. It is based on the symmetric multiprocessor (SMP) architecture, and thus it delivers high performance and optimal power management and debug capabilities.

The A72 processor is a multi-issue out-of-order superscalar execution engine with integrated L1 instruction and data caches, compatible with Armv8-A architecture. The Armv8-A architecture brings a number of new features. These include 64-bit data processing, extended virtual addressing and 64-bit general purpose registers.

For more information, see *Dual-A72 MPU Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

### 8.3.2 Arm Cortex-R5F

The MCU\_ARMSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for split/lock operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC.

For more information, see *Dual-R5F MCU Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

### 8.3.3 DSP C71x

The TMS320C71x is the next-generation fixed and floating-point DSP platform. The C71x DSP is a new core in the Texas Instruments' DSP family. The C71x DSP supports vector signal processing, providing significant lift in DSP processing power over a broad range of general signal processing tasks in comparison to the C6x DSP family. In addition, the C71x provides several specialized functions which accelerate targeted functions by more than 30 times. Besides expanding vector processing capabilities, the new C71x core also incorporates advanced techniques to improve control code efficiency and ease of programming such as branch prediction, protected pipeline, precise exception and virtual memory management.

For more information, see *C71x DSP Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

## 8.4 Accelerators and Coprocessors

### 8.4.1 GPU

The Graphics Processing Unit (GPU) accelerates 3-dimensional (3D) and 2-dimensional (2D) graphics and compute applications.

The GPU module is a scalable architecture which efficiently processes a number of different workload concurrently:

- 3D Graphic Workload, which involves vertex data and pixel data processing for rendering of 3D scenes.
- 2D Graphic Workload, which involves pixel data processing for rendering 2D objects.
- Compute Applications Workload, which involves general purpose data processing.

For more information, see *Graphics Accelerator (GPU)* section in *Processors and Accelerators* chapter in the device TRM.

### 8.4.2 VPAC

The Vision Pre-processing Accelerator (VPAC) is a set of common vision primitive functions, performing memory-to-memory (M2M) pixel data processing tasks, such as: color processing and enhancement, noise filtering, wide dynamic range (WDR) processing, lens distortion correction, pixel remap for dewarping, on-the-fly scale generation, on-the-fly pyramid generation. The VPAC offloads these common tasks from the main SoC processors (ARM, DSP, etc.), so these CPUs can be utilized for differentiated high-level algorithms. The VPAC is designed to support multiple cameras by working in time-multiplexing mode. The VPAC works as front end to vision processing and prepares frame/scales for further processing by other vision accelerators or processor cores in the SoC.

For more information, see *Vision Pre-processing Accelerator (VPAC)* section in *Processors and Accelerators* chapter in the device TRM.

### 8.4.3 DMPAC

The Depth and Motion Perception Accelerator (DMPAC) is a power efficient hardware accelerator that computes dense stereo depth maps (*depth*) and dense optical flow vectors (*motion*) from camera inputs.

The image/video sensor-based environmental perception (also known as scene understanding) is at the core of many emerging applications in automotive, industrial and consumer electronics. Typically, this involves detection of all objects in the scene along with their 3D position and motion with regards to the observer or the car by analyzing one or many related input video streams. Various computer vision algorithms are used to achieve these tasks.

A very robust method of obtaining the 3D depth from images is to use two cameras in a stereo setup - two cameras with known relative positions and camera parameters. The two images of the same scene, captured from two different camera poses/perspectives, are analyzed to find disparities among every pixel positions in the images. This is known as the Stereo Disparity map. The disparity values of every pixel can be used to obtain the 3D positions of the object/space they belong to via triangulation.

On the other hand, by analyzing two images from a single camera, captured at two different time instances (that is, two temporal frames in a video), one can determine where each pixel in a past frame moved to in the future frame. This is known as the Optical Flow vector. The flow vectors for each pixel position can be used to obtain 3D structure of the scene, identify moving objects and determine their relative speed and direction of motion.

The DMPAC is dedicated to the aforesaid image processing tasks. The stereo and optical flow processing is partitioned into two top level sub-blocks: the Dense Optical Flow (DOF) engine and the Stereo Disparity Engine (SDE). The DOF and SDE blocks share a common shared local memory, DMA, external messaging and control infrastructure.

For more information, see *Depth and Motion Perception Accelerator (DMPAC)* section in *Processors and Accelerators* chapter in the device TRM.

## 8.5 Other Subsystems

### 8.5.1 MSMC

The Multicore Shared Memory Controller (MSMC) forms the heart of the compute cluster (COMPUTE\_CLUSTER0) providing high-bandwidth resource access both to and from all of the connected processing elements and the rest of the system. MSMC serves as the data-movement backbone of the compute cluster.

For more information, see *Multicore Shared Memory Controller (MSMC)* section in *Device Configuration* chapter in the device TRM.

### 8.5.2 NAVSS

#### 8.5.2.1 NAVSS0

Main SoC Navigator Subsystem (NAVSS0) consists of DMA/Queue Management components - UDMA and Ring Accelerator (UDMASS), Peripherals (Module subsystem [MODSS]), Virtualization translation (VirtSS), and a North Bridge (NBSS).

#### 8.5.2.2 MCU\_NAVSS

MCU Navigator Subsystem (MCU NAVSS) has a subset of the modules of the main NAVSS and is instantiated in the MCU domain.

MCU Navigator Subsystem consists of DMA/Queue Management components - UDMA and Ring Accelerator (UDMASS), and Peripherals (Module subsystem [MODSS]).

For more information, see *Main Navigator Subsystem (NAVSS)* and *MCU Navigator Subsystem (MCU NAVSS)* sections in the device TRM.

### 8.5.3 PDMA Controller

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers accessed via a standard non-coherent bus fabric. The PDMA module is intended to be located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured Transfer Request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer UDMA-P destination channel which then performs the movement of the data into memory. Likewise, a remote UDMA-P source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (UDMA-P + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

For more information, see *PDMA Controller* section in *DMA Controllers* chapter in the device TRM.

### 8.5.4 Power Supply

The device requires 6 power supply types and 1 internal LDO connection type, see [Power Supply Signal Descriptions](#)

- Digital IO Voltages
- Digital Low Voltages

- Digital AVS Voltage
- Analog PHY & CLK Voltages
- Analog Low Voltages
- Efuse Programming Voltages
- LDO Bulk Filter Capacitors

Common device power supply input types can be grouped together into power rails. All power rails must be supplied by power resources designed to support the most stringent power supply voltage specification and total load current demands. Two recommended Power Distribution Networks (PDNs) have been defined that either combine or isolate MCU and Main domains, (refer to *Power Supply Mapping*).

It is possible that a few power supply inputs may not be needed in some systems. In such cases, all unused supply inputs, other than VPP\_CORE & VPP\_MCU, must be connected to a valid power rail with a proper voltage level in order to ensure device reliability (refer to [Recommended Operating Conditions](#)). The following examples are given for reference:

1. If MCU Island safety monitor or MCU Only low power processing are not used, then VDD\_MCU supply can be combined with the VDD\_CORE supply with compatible operating voltage specification.
2. If UHS-I SD Card or USB2.0 interface is not needed, then VDDSHV5 (MMC1 interface) and VDDA\_USB\_3P3 (USB PHY interface) can be combined with VDD\_IO\_3V3 digital IO power rail.
3. If General Purpose device type is used, then Efuse programming voltages VPP\_CORE & VPP\_MCU are not needed and should be left unconnected.

## 8.5.5 Peripherals

### 8.5.5.1 ADC

The Analog-to-Digital Converter (ADC) module contains a single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels).

For more information, see *Analog-to-Digital Converter (ADC)* section in *Peripherals* chapter in the device TRM.

### 8.5.5.2 ATL

The Audio Tracking Logic (ATL) is used by HD Radio™ applications to synchronize the digital audio output to the baseband clock. This same IP can also be used generically to track errors between two reference signals (such as frame syncs) and generate a modulated clock output (using software-controlled cycle stealing) which averages to some desired frequency. This process can be used as a hardware assist for asynchronous sample rate conversion algorithms.

For more information, see *Audio Tracking Logic (ATL)* section in *Peripherals* chapter in the device TRM.

### 8.5.5.3 CSI

#### 8.5.5.3.1 Camera Streaming Interface Receiver (CSI\_RX\_IF) and MIPI DPHY Receiver (DPHY\_RX)

The integration of the CSI\_RX\_IF module allows the device to stream video inputs from multiple cameras to the image processing accelerator (VPAC) or to internal memory. The video input may also be retransmitted via the transmitter CSI (CSI\_TX\_IF) for debug and test purposes.

For more information, see *Camera Streaming Interface (CSI)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.3.2 Camera Streaming Interface Transmitter (CSI\_TX\_IF)

The integration of the CSI\_TX\_IF module allows the device to stream out video data from memory, or retransmit from the CSI receivers as an optional loopback output for diagnostics, debug, and test purposes.

For more information, see *Camera Streaming Interface (CSI)* section in *Peripherals* chapter in the device TRM.

### 8.5.5.4 CPSW2G

The two-port Gigabit Ethernet MAC (MCU\_CPSW0) subsystem provides Ethernet packet communication for the device and is configured in a similar manner as an Ethernet switch. MCU\_CPSW0 features the Reduced Gigabit Media Independent Interface (RGMI), Reduced Media Independent Interface (RMII), and the Management Data Input/Output (MDIO) interface for physical layer device (PHY) management.

For more information, see *Gigabit Ethernet Switch (CPSW0)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.5 CPSW9G

The 9-port Gigabit Ethernet Switch (CPSW0) subsystem provides Ethernet packet communication for the device and can be configured as an Ethernet switch. CPSW0 features the Serial Gigabit Media Independent Interface (SGMII), Reduced Gigabit Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII) and the Management Data Input/Output (MDIO) interface for physical layer device (PHY) management.

For more information, see *Gigabit Ethernet Switch (MCU\_CPSW0)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.6 DCC

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programmed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

For more information, see *Dual Clock Comparator (DCC)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.7 DDRSS

The DDR subsystem in this device comprises DDR controller, DDR PHY and wrapper logic to integrate these blocks in the device. The DDR subsystem is referred to as DDRSS0 and is used to provide an interface to external SDRAM devices which can be utilized for storing program or data. DDRSS0 is accessed via MSMC, and not directly through the system interconnect.

For more information, see *DDR Subsystem (DDRSS)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.8 DSS

The DSS is a flexible composition-enabled display subsystem, that supports multiple high resolution display outputs. It consists of one Display Controller (DISPC) and one Frame Buffer Decompression Core (FBDC). The DISPC supports a multi-layer blending and transparency for each of its display outputs. The DISPC also supports a write-back pipeline with scaling to enable memory-to-memory composition and/or to capture a display output for Ethernet video encoding.

For more information, see *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.

##### 8.5.5.8.1 DSI

The MIPI DSI v1.3.1 Controller (DSITX) implements the stream arbitration and low-level protocol layer functionalities required by MIPI DSI 1.3 standard. It supports up to 4 x 2.5 Gbps D-PHY data lanes in a single-link configuration and handles the byte lane mapping per use case (1, 2, 3, or 4-lanes). The accompanying DSI (Physical Layer) D-PHY module (DPHYTX) provides the video output interfacing by implementing a four-lane MIPI D-PHY transmitter.

For more information, see *Display Subsystem (DSS) and Display Peripherals* section in *Peripherals* chapter in the device TRM.

##### 8.5.5.8.2 eDP

The VESA DP1.4/eDP1.4 Compliant Transmitter Host Controller (EDP) can output up to 4 video streams (through Multiple Stream Transport / MST) and one audio stream through the 4-lane accompanying SerDes module. It provides up to 25.92 Gbps of application bandwidth. An additional eDP (Physical Layer) auxiliary PHY (AUXPHY) module implements a doubly-terminated differential pair required for 1 Mbps data rates over a long (15m) cable.

For more information, see *Display Subsystem (DSS) and Display Peripherals* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.9 VPFE

The Video Processing Front End (VPFE) is an input interface module that receives raw (unprocessed) image/video data or YUV digital video data from external imaging peripherals (such as image sensors, video decoders, etc) and performs DMA transfers to store the captured data in the system DDR memory.

For more information, see *Video Processing Front End (VPFE)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.10 eCAP

The enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors.

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.11 EPWM

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description the letter x within a signal or module name is used to indicate a generic EPWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the EPWM\_x instance. Thus, EPWM1A and EPWM1B belong to EPWM1, EPWM2A and EPWM2B belong to EPWM2, and so forth.

Additionally, the EPWM integration allows this synchronization scheme to be extended to the capture peripheral modules (ECAP). The number of modules is device-dependent and based on target application needs. Modules can also operate stand-alone.

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.12 ELM

The Error Location Module (ELM) is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

For more information, see *Error Location Module (ELM)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.13 ESM

The Error Signaling Module (ESM) aggregates safety-related events and/or errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with a safety event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in safe, known state.

For more information, see *Error Signaling Module (ESM)* section in *Peripherals* chapter in the device TRM.



#### 8.5.5.14 eQEP

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.15 GPIO

The General-Purpose Input/Output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, the user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.16 GPMC

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.17 Hyperbus

The Hyperbus module is a part of the device Flash Subsystem (FSS).

The Hyperbus module is low pin count memory interface that provides high read/write performance. The Hyperbus module connects to hyperbus memory (HyperFlash or HyperRAM) and uses simple hyperbus protocol for read and write transactions.

There is one Hyperbus™ module inside the device. The Hyperbus module includes one Hyperbus Memory Controller (HBMC).

For more information, see *Hyperbus Interface* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.18 I2C

The device contains ten multimaster Inter-Integrated Circuit (I2C) controllers each of which provides an interface between a local host (LH), such as an Arm or a Digital Signal Processor (DSP), and any I<sup>2</sup>C-bus-compatible device that connects via the I<sup>2</sup>C serial bus. External components attached to the I<sup>2</sup>C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I<sup>2</sup>C interface.

Each multimaster I2C module can be configured to act like a slave or master I<sup>2</sup>C-compatible device.

The WKUP\_I2C0, MCU\_I2C0, I2C0, and I2C1 controllers have dedicated I<sup>2</sup>C compliant open drain buffers, and support high speed mode (up to 3.4 Mbps in 1.8 V mode and up to 400 kbps in 3.3 V mode). The MCU\_I2C1,

I2C2, I2C3, I2C4, I2C5, and I2C6 controllers are multiplexed with standard LVCMOS I/O, connected to emulate open drain, and support fast mode (up to 400 kbps in 1.8 V/3.3 V mode). The I2C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic 1.

For more information, see *Inter-Integrated Circuit (I2C) Interface* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.19 I3C

The device contains three Improved Inter-Integrated Circuit (I3C) controllers each of which provides an interface between a local host (LH), such as an Arm, and any I3C-bus-compatible device that connects via the I3C serial bus.

For more information, see *Improved Inter-Integrated Circuit (I3C) Interface* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.20 MCAN

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control. CAN has high immunity to electrical interference. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

For more information, see *Modular Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.21 MCASP

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although inter-component digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.22 MCRC Controller

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a predetermined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system. Channel 1 can also be put into data trace mode, where MCRC controller compresses each data being read through CPU read data bus.

For more information, see *MCRC Controller* section in *Interprocessor Communication* chapter in the device TRM.

#### 8.5.5.23 MCSPI

The MCSPI module is a multichannel transmit/receive, master/slave synchronous serial bus.

There are total of eleven MCSPI modules in the device.



For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.24 MMC/SD

The MMCSD Host Controller provides an interface to eMMC 5.1 (embedded MultiMedia Card), SD 4.10 (Secure Digital), and SDIO 4.0 (Secure Digital IO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more information, see *Multimedia Card/Secure Digital (MMC/SD) Interface* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.25 OSPI

The Octal Serial Peripheral Interface (OSPI) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices. This module has a memory mapped register interface, which provides a direct memory interface for accessing data from external flash devices, simplifying software requirements.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signalling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device master at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.26 PCIE

The Peripheral Component Interconnect Express (PCIe) subsystem is built around a multi-lane dual-mode PCIe controller that provides low pin-count, high reliability, and high-speed data transfers at rates of up to 8.0 Gbps per lane for serial links on backplanes and printed wiring boards.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.27 SerDes

SerDes'es goal is to convert device (SoC) parallel data into serialized data that can be output over a highspeed electrical interface. In the opposite direction, SerDes converts high-speed serial data into parallel data that can be processed by the device. To this end, the SerDes contains a variety of functional blocks to handle both the external analog interface as well as the internal digital logic.

For more information, see *Serializer/Deserializer (SerDes)* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.28 WWDT

The Windowed Watchdog Timer provides timer functionality for operating systems and for benchmarking code. The module incorporates several counters, which define the timebases needed for scheduling in the operating system. The module is implemented with an RTI module, but only WWDT is supported.

This module is specifically designed to fulfill the requirements for OSEK ( "Offene Systeme und deren Schnittstellen für die Elektronik im Kraftfahrzeug" ; "Open Systems and the Corresponding Interfaces for Automotive Electronics" ) as well as OSEK/Time compliant operating systems.

For more information, see *Real Time Interrupt (RTI) Module* section in *Peripherals* chapter in the device TRM.

#### 8.5.5.29 Timers

All timers include specific functions to generate accurate tick interrupts to the operating system.

Each timer can be clocked from several different independent clocks. The selection of clock source is made from registers in the MCU\_CTRL\_MMR0/CTRL\_MMR0.

In the MCU domain the device provides 10 timer pins to be used as MCU Timer Capture inputs or as MCU Timer PWM outputs. In order to provide maximum flexibility, these 10 pins may be used with any of MCU\_TIMER0 through MCU\_TIMER9 instances. System level muxes are used to control the capture source pin for each MCU\_TIMER[9-0] and the MCU\_TIMER[9-0] source for each MCU\_TIMER\_IO[1-0] PWM output.

In the MAIN domain the device provides 8 timer pins to be used as Timer Capture inputs or as Timer PWM outputs. For maximum flexibility, these 8 pins may be used with any of TIMER0 through TIMER19 instances. System level muxes are used to control the capture source pin for each TIMER[19-0] and the TIMER[19-0] source for each TIMER\_IO[7-0] PWM output.

Each odd numbered timer instance from each of the domains may be optionally cascaded with the previous even numbered timer instance from the same domain to form up to a 64-bit timer. For example, TIMER1 may be cascaded to TIMER0, MCU\_TIMER1 may be cascaded to MCU\_TIMER0, etc.

When cascaded, TIMERi acts as a 32-bit prescaler to TIMERi+1, as well as MCU\_TIMERn acts as a 32-bit prescaler to MCU\_TIMERn+1. TIMERi / MCU\_TIMERn must be configured to generate a PWM output edge at the desired rate to increment the TIMERi+1/ MCU\_TIMERn+1 counter.

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

### 8.5.5.30 UART

The UART is a slave peripheral that utilizes the DMA for data transfer or interrupt polling via host CPU. There are twelve UART modules in the device. All UART modules support IrDA and CIR modes when 48 MHz function clock is used. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

For more information, see *Universal Synchronous/Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

### 8.5.5.31 USB

Similar to earlier versions of USB bus, USB 3.0 is a general-purpose cable bus, supporting data exchange between a host device and a wide range of simultaneously accessible peripherals.

The device supports two identical USB subsystems:

- USB3SS0 is SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with on-chip SS (USB3.0) PHY and HS/FS/LS (1) (USB2.0) PHY
- USB3SS1 is SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with on-chip SS (USB3.0) PHY and HS/FS/LS (USB2.0) PHY

For more information, see *Universal Serial Bus (USB) Subsystem* section in *Peripherals* chapter in the device TRM.

### 8.5.5.32 UFS

The Universal Flash Storage (UFS) interface is a standard-based serial interface engine.

There is one UFS module inside the device - UFS0. The UFS module includes one UFS 2.1 host controller (HC) with an integrated M-PHY.

The UFS module complies with the standards as listed in 表 8-1.

表 8-1. UFS Standards

| DOCUMENT   | VERSION          | DESCRIPTION                                            |
|------------|------------------|--------------------------------------------------------|
| JESD220-1A | v1.1             | Universal Flash Storage (UFS) Unified Memory Extension |
| JESD220-2  | v1.0             | Universal Flash Storage (UFS) Card Extension           |
| JESD220C   | v2.1, March 2016 | Universal Flash Storage (UFS)                          |

表 8-1. UFS Standards (continued)

| DOCUMENT   | VERSION                   | DESCRIPTION                                                                            |
|------------|---------------------------|----------------------------------------------------------------------------------------|
| JESD223-1B | v1.1A                     | Universal Flash Storage Host Controller Interface (UFSHCI) Unified Memory Extension    |
| JESD223C   | v2.1, March 2016          | Universal Flash Storage Host Controller Interface (UFSHCI)                             |
| JESD224    | March 2013                | Universal Flash Storage (UFS) Test                                                     |
|            | November, 2001            | Federal Information Processing Standards (FIPS) 197 Advanced Encryption Standard (AES) |
|            | v3.1, 2014                | MIPI® Alliance Specification for M-PHY                                                 |
|            | v1.60, 2013               | MIPI Alliance Specification for Unified Protocol (UniProSM)                            |
|            | Revision 24, August 2010  | Small Computer System Interface (SCSI) Block Commands - 3                              |
|            | Revision 27, October 2010 | SCSI Primary Commands - 4                                                              |

For more information, see *Universal Flash Storage (UFS) Interface* section in *Peripherals* chapter in the device TRM.

## 9 Applications, Implementation, and Layout

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### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

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## 10 Device Connection and Layout Fundamentals

### 10.1 Power Supply Decoupling and Bulk Capacitors

#### 10.1.1 Power Distribution Network Implementation Guidance

The [Sitara Processor Power Distribution Networks: Implementation and Analysis](#) provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI supports *only* designs that follow the board design guidelines contained in the application report.

### 10.2 External Oscillator

For more information about External Oscillators, see [Clock Specifications](#).

### 10.3 JTAG and EMU

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the [XDS Target Connection Guide](#).

For more recommendations on EMU routing, see [Emulation and Trace Headers Technical Reference Manual](#)

### 10.4 Reset

The device incorporates four external reset pins (MCU\_PORz, MCU\_RESETz, PORz, and RESET\_REQz) and two reset status pins (MCU\_RESETSTATz and RESETSTATz). These pins can be driven by an external power good circuitry or Power Management IC (PMIC). MCU\_PORz and Main PORz pins should be held active low during the entire power-up phase, and until all power supplies as well as the HFOSC0 clock are stable.

All MCU domain resets act as master resets to the whole device, whereas Main domain resets only reset Main domain (MCU domain is reset isolated from all Main domain resets).

### 10.5 Unused Pins

For more information about Unused Pins, see [Pin Connectivity Requirements](#)

### 10.6 Hardware Design Guide for Jacinto™ 7 Devices

The Hardware Design Guide for Jacinto™ 7 Devices document describes hardware system design considerations for the Jacinto™ 7 family of processors. This design guide is intended to be used as an aid during the development of application hardware.

## 11 Peripheral- and Interface-Specific Design Information

### 11.1 LPDDR4 Board Design and Layout Guidelines

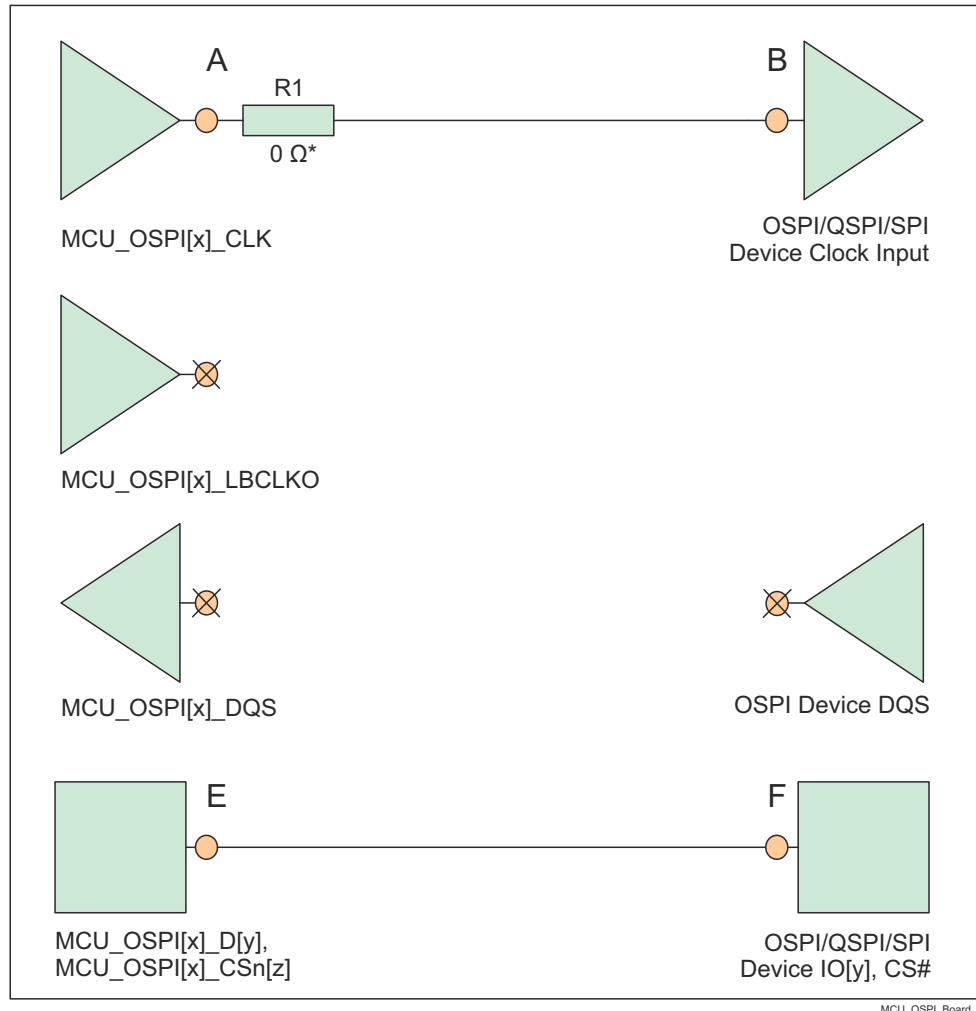
The goal of the [Jacinto 7 DDR Board Design and Layout Guidelines](#) is to make the LPDDR4 system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using LPDDR4 memories that follow the guidelines in this document.

### 11.2 OSPI and QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the OSPI and QSPI interfaces.

#### 11.2.1 No Loopback and Internal Pad Loopback

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The signal propagation delay from the MCU\_OSPI[x]\_CLK signal to the flash device must be < 450 ps (~7cm as stripline or ~8cm as microstrip)
- 50  $\Omega$  PCB routing is recommended along with series terminations, as shown in [图 11-1](#)
- Propagation delays and matching:
  - A to B < 450 ps
  - Matching skew: < 60 ps



\* 0 Ω resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK pin, is placeholder for fine tuning, if needed.

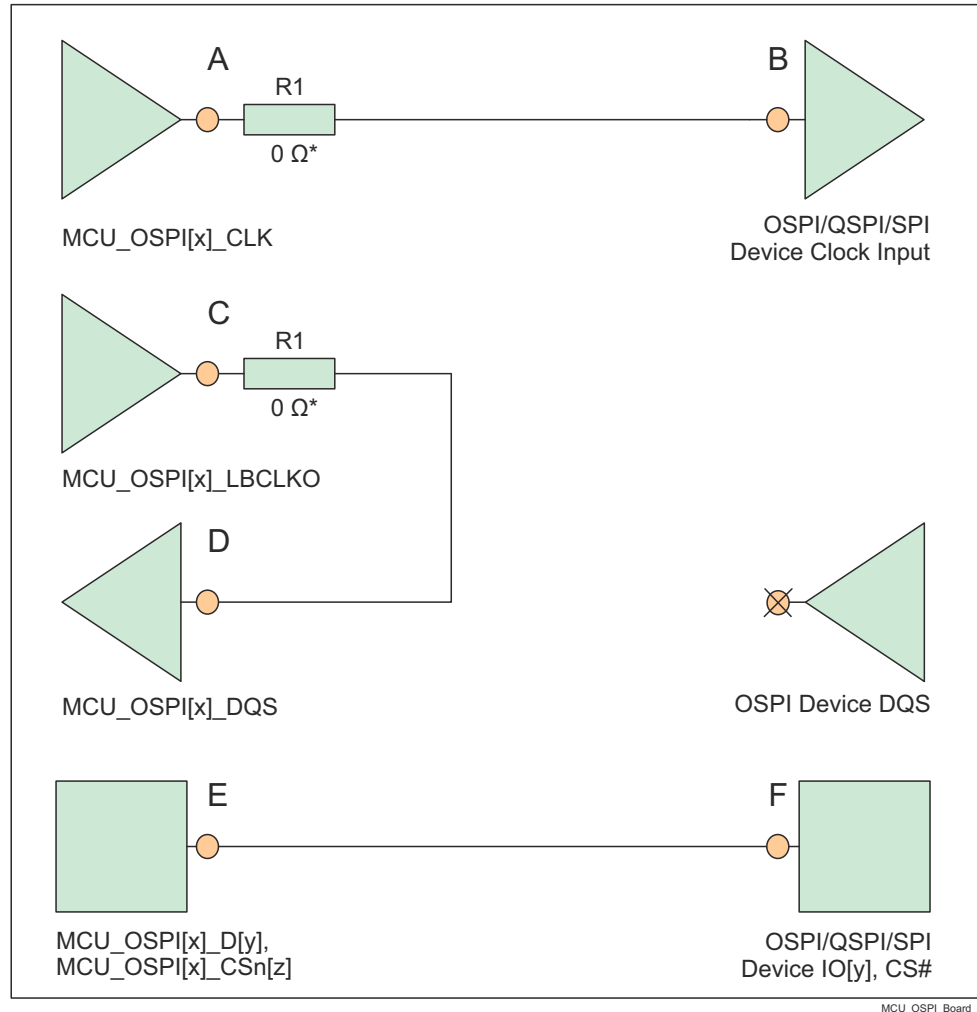
图 11-1. OSPI Interface High Level Schematic

### 11.2.2 External Board Loopback

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The MCU\_OSPI[x]\_LBCLKO output signal must be looped back into the MCU\_OSPI[x]\_DQS input
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to half of the signal propagation delay from the MCU\_OSPI[x]\_LBCLKO pin to the MCU\_OSPI[x]\_DQS pin ((C to D)/2). See the note below.
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) must be approximately equal to the signal propagation delay of the control and data signals between the flash device and the SoC device (E to F, or F to E)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 图 11-2
- Propagation delays and matching:
  - A to B = E to F = (C to D) / 2
  - Matching skew: < 60 ps

### 备注

The OSPI Board Loopback Hold time requirement (described in [OSPI](#)) is larger than the Hold time provided by a typical flash device. Therefore, the length of MCU\_OSPI[x]\_LBCLKO pin to the MCU\_OSPI[x]\_DQS pin (C to D) can be shortened to compensate.



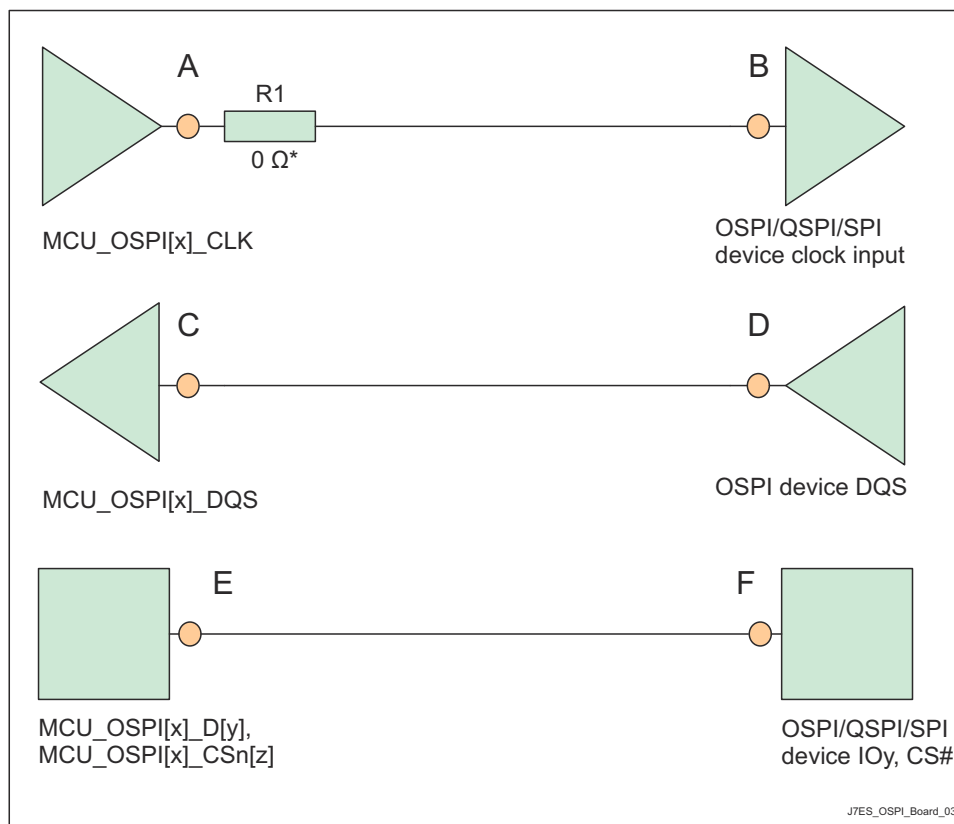
\* 0 Ω resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK and MCU\_OSPI[x]\_LBCLKO pins, is a placeholder for fine tuning, if needed.

图 11-2. OSPI Interface High Level Schematic

#### 11.2.3 DQS (only available in Octal Flash devices)

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The DQS pin of the flash devices must be connected to MCU\_OSPI[x]\_DQS signal
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to the signal propagation delay from the MCU\_OSPI[x]\_DQS pin to the DQS output pin (C to D)
- 50 Ω PCB routing is recommended along with series terminations, as shown in [图 11-3](#)
- Propagation delays and matching:
  - A to B = C to D
  - Matching skew: < 60 ps





\*  $0\ \Omega$  resistor (R1), located as close as possible to the `MCU_OSPI[x]_CLK` pin, is a placeholder for fine tuning, if needed.

图 11-3. OSPI Interface High Level Schematic

### 11.3 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the 图 11-4), which limits the voltage applied to the actual device pin (`USB0_VBUS`). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of zener diode at 5 V should be less than 100 nA.<sup>(1)</sup>

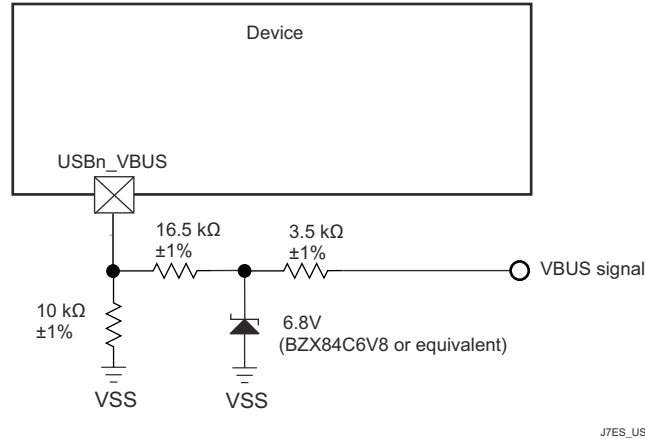


图 11-4. USB VBUS Detect Voltage Divider / Clamp Circuit

The USB0\_VBUS pin can be considered to be fail-safe because the external circuit in 图 11-4 limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

#### 11.4 System Power Supply Monitor Design Guidelines using VMON/POK

The VMON1\_ER\_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system. This supply is monitored by comparing the output of an external voltage divider circuit sourced by this supply with an internal voltage reference, with a power fail event being triggered when the voltage applied to VMON1\_ER\_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit. When designing the resistor divider circuit it is important to understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON1\_ER\_VSYS input threshold which has a nominal value of 0.45 V, with a variation of  $\pm 3\%$ . Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON1\_ER\_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON1\_ER\_VSYS input leakage current may be in the range of 10 nA to 2.5  $\mu$ A when applying 0.45 V.

#### 备注

The resistor voltage divider shall be designed such that its output voltage never exceeds the maximum value defined in [Recommended Operating Conditions](#) during normal operating conditions.

图 11-5 presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5 V - 10%, or 4.5 V.

For this example, it is important to understand which variables effect the maximum trigger threshold when selecting resistor values. It is obvious a device which has a VMON1\_ER\_VSYS input threshold of 0.45 V + 3% needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but how these contributions effect the maximum trigger point may not be obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON1\_ER\_VSYS pin is 2.5  $\mu$ A. When implementing a resistor divider where R1 = 4.81 K $\Omega$  and R2 = 40.2 K $\Omega$ , the result is a maximum trigger threshold of 4.523 V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45 V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input

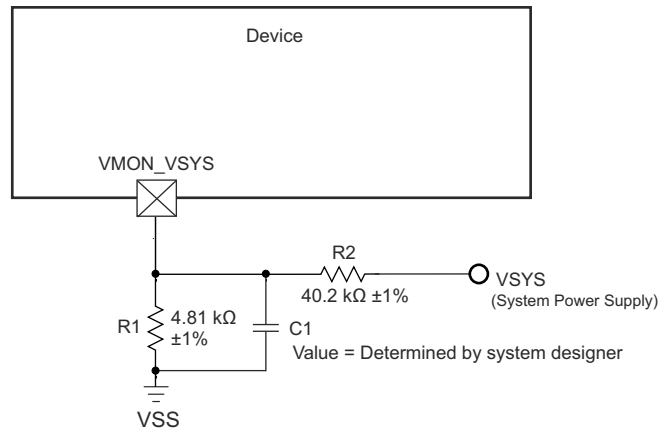
leakage current is 10 nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.008 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.008 V to 4.523 V. Approximately 250 mV of this range is introduced by VMON1\_ER\_VSYS input threshold accuracy of  $\pm 3\%$ , approximately 150 mV of this range is introduced by resistor tolerance of  $\pm 1\%$ , and approximately 100 mV of this range is introduced by loading error when VMON1\_ER\_VSYS input leakage current is 2.5  $\mu$ A.

The resistor values selected in this example produces approximately 100  $\mu$ A of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above could be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer should also consider implementing a noise filter on the voltage divider output since VMON1\_ER\_VSYS has minimum hysteresis and a high-bandwidth response to transients. This could be done by installing a capacitor across R1 as shown in [Figure 11-5](#). However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.

[Figure 11-5](#) presents an example, when the system power supply voltage is nominally 5 V and the desired trigger threshold is -10% or 4.5 V.



SPRSP56\_VMON\_ER\_MON\_01

**图 11-5. System Supply Monitor Voltage Divider Circuit**

The **VMON2\_IR\_VCPU** pin provides a way to monitor VDD\_CPU power supply. Must be externally connected as close as possible to VDD\_CPU pin on the board. SoCs that have a **VMON6\_IR\_VEXT0P8** can optionally monitor other domains such as VDD\_CORE or VDD\_MCU. Similarly, those signals should be as close as possible to VDD\_CORE or VDD\_MCU pin on the board.

The **VMON3\_IR\_VEXT1P8** and **VMON4\_IR\_VEXT1P8** pins provide a way to monitor an external 1.8-V power supply. The **VMON5\_IR\_VEXT3P3** pin provides a way to monitor an external 3.3-V power supply. An internal resistor divider with software control is implemented inside the SoC. Software can program the internal resistor divider to create appropriate under voltage and over voltage interrupts. These pins should not be sourced from an external resistor divider. If the monitored voltage requires adjustment, be sure to buffer the divided voltage prior connecting to monitor pin.

## 11.5 High Speed Differential Signal Routing Guidance

The [High Speed Interface Layout Guidelines](#) provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application report.

## 11.6 Thermal Solution Guidance

The [Thermal Design Guide for DSP and ARM Application Processors](#) provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

## 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 12.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, AM69). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM69 devices in the ALY package type, see the Package Option Addendum of this document, the TI website ([ti.com](http://ti.com)), or contact your TI sales representative.

## 12.1.1 Standard Package Symbolization

### 备注

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

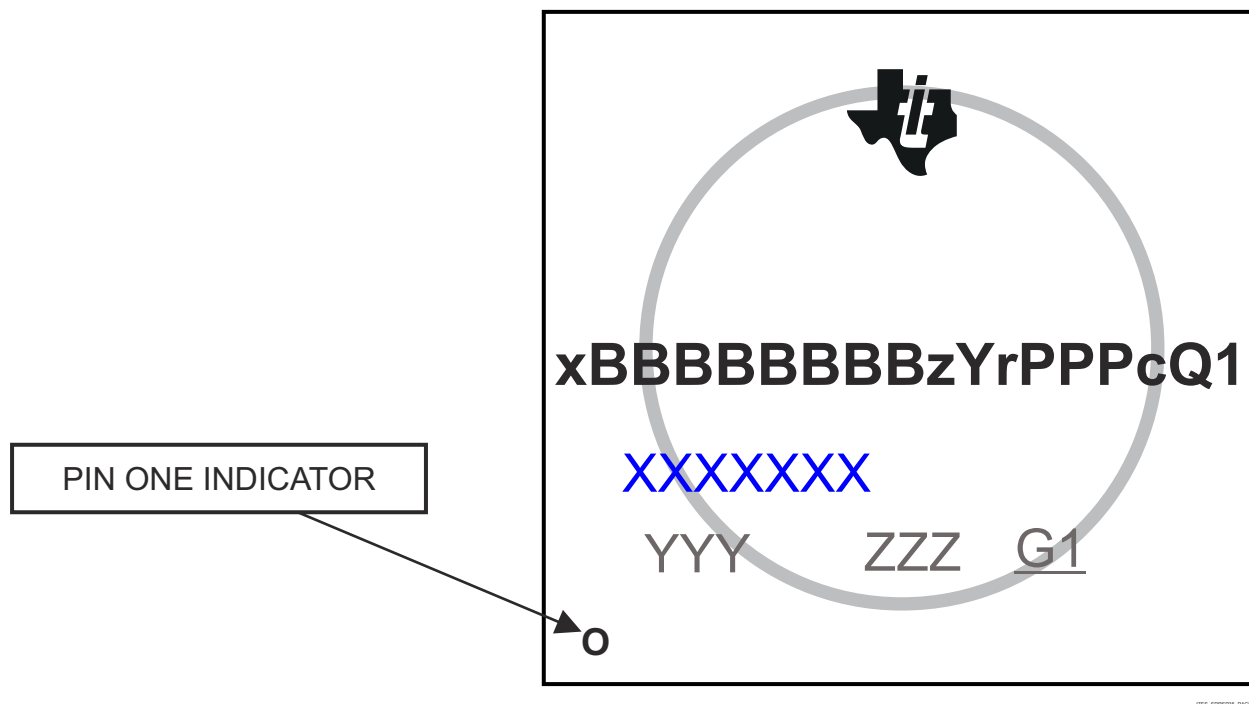


图 12-1. Printed Device Reference

## 12.1.2 Device Naming Convention

### 备注

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

表 12-1. Nomenclature Description

| FIELD<br>PARAMETER | FIELD<br>DESCRIPTION                                 | VALUE                | DESCRIPTION                                                                                   |
|--------------------|------------------------------------------------------|----------------------|-----------------------------------------------------------------------------------------------|
| a                  | Device evolution stage                               | X                    | Prototype                                                                                     |
|                    |                                                      | P                    | Preproduction (production test flow, no reliability data)                                     |
|                    |                                                      | BLANK <sup>(1)</sup> | Production                                                                                    |
| BBBBBBB            | Base production part number                          | AM69A98              | See <a href="#">Device Comparison</a>                                                         |
|                    |                                                      | AM69A94              |                                                                                               |
|                    |                                                      | AM69A78              |                                                                                               |
|                    |                                                      | AM6958               |                                                                                               |
|                    |                                                      | AM6934               |                                                                                               |
| r                  | Device revision                                      | A                    | SR1.0                                                                                         |
| Z                  | Device Speed Grade                                   | T                    | See <a href="#">Speed Grade Maximum Frequency</a> .                                           |
|                    |                                                      | OTHER                | Alternate speed grade                                                                         |
| f                  | Features<br>(see <a href="#">Device Comparison</a> ) | G                    | Base, no additional Features                                                                  |
| Y                  | Functional Safety <sup>(3)</sup>                     | G                    | Non-Functional Safety                                                                         |
| y                  | Security                                             | G                    | Non-Secure                                                                                    |
|                    |                                                      | Other                | Secure                                                                                        |
| t                  | Temperature <sup>(2)</sup>                           | A                    | - 40°C to 105°C - Extended Industrial (see <a href="#">Recommended Operation Conditions</a> ) |
|                    |                                                      | H                    | 0°C to 95°C - Commercial (see <a href="#">Recommended Operation Conditions</a> )              |
|                    |                                                      | I                    | - 40°C to 125°C - Automotive (see <a href="#">Recommended Operation Conditions</a> )          |
| PPP                | Package Designator                                   | ALY                  | FCBGA (1414-pin; 23 mm x 23 mm)                                                               |
| Q1                 | Automotive Designator                                | Q1                   | Auto Qualified (Q100)                                                                         |
|                    |                                                      | BLANK <sup>(1)</sup> | Standard                                                                                      |
| xxxxxxx            | Lot Trace Code (LTC)                                 |                      |                                                                                               |
| YYY                | Production Code, For TI use only                     |                      |                                                                                               |
| ZZZ                | Production Code, For TI use only                     |                      |                                                                                               |
| O                  | Pin one designator                                   |                      |                                                                                               |
| G1                 | ECAT - Green package designator                      |                      |                                                                                               |

(1) BLANK in the symbol or part number is collapsed so there are no gaps between characters.

(2) Applies to device max junction temperature.

(3) Functional Safety is not supported on this device family, if interested in this feature, please see the [TDA4VH device family](#).

## 12.2 Tools and Software

The following products support development for AM69 platforms:

### Development Tools

**Code Composer Studio™ Integrated Development Environment** Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

**Pin mux tool** The Pin MUX Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customer's custom software. Version 4 of the Pin Mux utility adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at [ti.com](http://ti.com). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

## 12.3 支持资源

**TI E2E™ 支持论坛**是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 12.4 Trademarks

eMMC™ is a trademark of MultiMediaCard Association.

Jacinto™, C7000™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.

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安全数字® is a registered trademark of SD Card Association.

MIPI® is a registered trademark of MIPI Alliance, Inc.

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## 12.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.6 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。



## 13 Mechanical, Packaging, and Orderable Information

### 13.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| XAM6958ATGGHAALY  | ACTIVE        | FCBGA        | ALY                | 1414 | 1              | TBD             | Call TI                              | Call TI              | -40 to 105   |                         | <a href="#">Samples</a> |
| XAM69A98ATNGHAALY | ACTIVE        | FCBGA        | ALY                | 1414 | 1              | TBD             | Call TI                              | Call TI              | -40 to 105   |                         | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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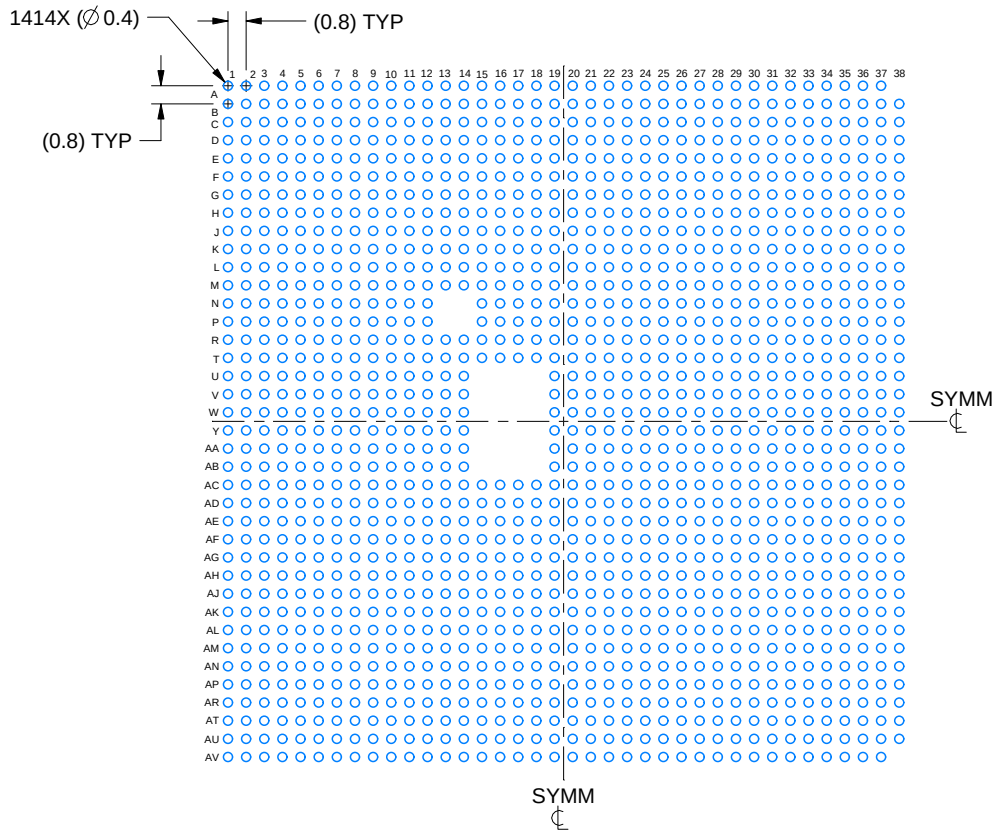


# EXAMPLE BOARD LAYOUT

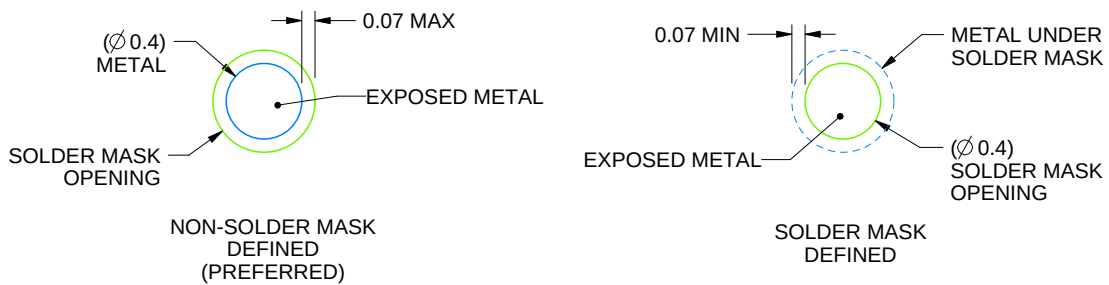
ALY1414A

FCBGA - 3.341 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:3X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

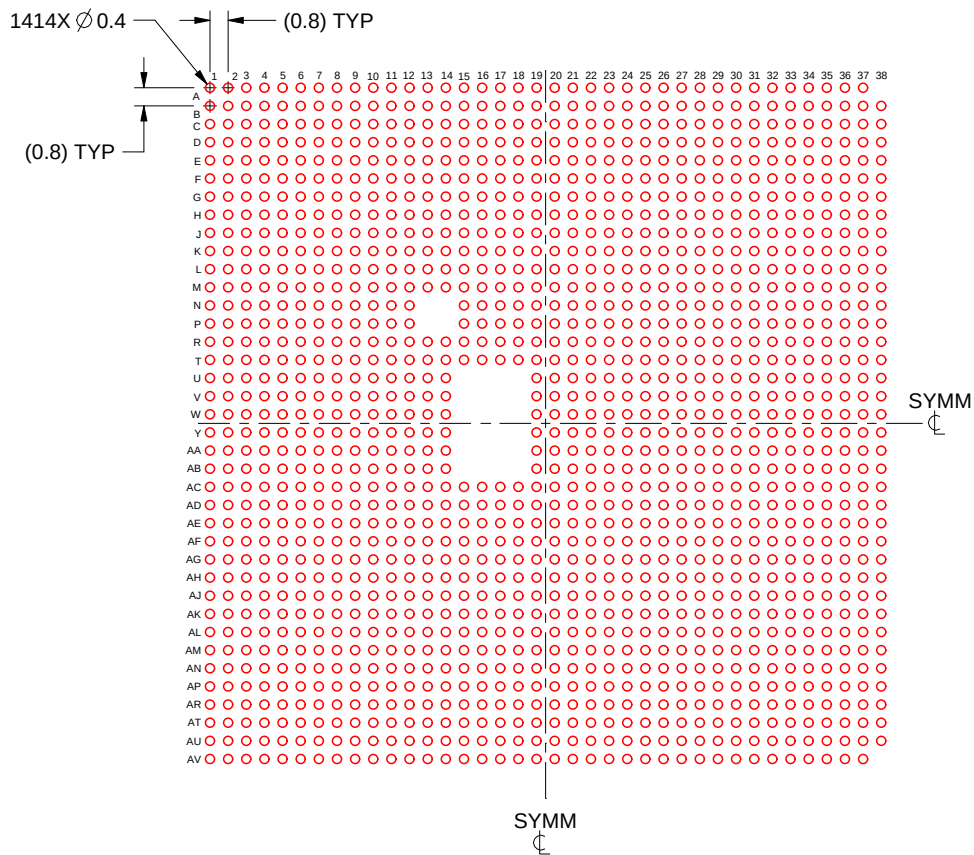
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ALY1414A

FCBGA - 3.341 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
 BASED ON 0.15 mm THICK STENCIL  
 SCALE: 3X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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