TPSM8683x 4.5V 至 28V 输入、8A 同步降压电源模块

1 特性

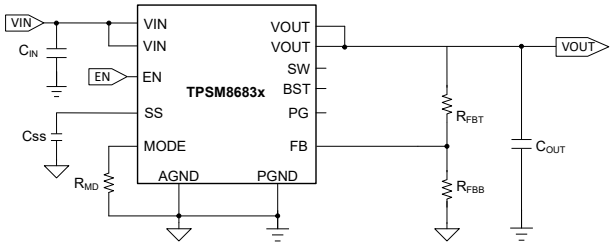
- 输入电压范围为 4.5V 至 28V
- 0.6V 至 5.5V 输出电压范围
- 8A 持续输出电流能力
- 集成 MOSFET、电感器和基本无源器件
- 在 25°C 下，具有 0.6V ±1% 的基准电压
- D-CAP3™ 控制模式，用于快速瞬态响应
- TPSM86838 具有 FCCM，用于实现伪固定频率和较低的输出纹波
- TPSM86837 具有 Eco-mode，可实现较高的轻负载效率
- 可调节软启动时间（通过 SS 电容器调节）
- 内置输出放电功能
- 可选 800kHz 和 1200kHz 开关频率
- 电源正常状态指示器，可监测输出电压
- 支持高达 98% 的负荷运行
- 非闭锁 UV、OV、OT 和 UVLO 保护
- –40°C 至 +150°C 的工作结温范围
- 19 引脚 5.0mm × 5.5mm QFN HotRod™ 封装

2 应用

- 工业应用：医疗应用、工厂自动化和控制（IPC、机器人）、测试和测量、专业音频视频
- 适用于 12V、19V 和 24V 电源总线应用的空间受限 POL

3 说明

TPSM8683x 是一款高效、高压输入、易于使用的同步降压电源模块。该器件集成了功率 MOSFET、屏蔽式电感器和基本无源器件，更大限度地减小了设计尺寸。



简化版原理图

该器件具有 4.5V 至 28V 的宽工作输入电压范围，非常适合由 12V、19V、24V 总线电源轨供电的系统。TPSM8683x 支持高达 8A 的持续输出电流，相应的输出电压介于 0.6V 和 5.5V 之间。

TPSM8683x 使用 DCAP3 控制模式来提供快速瞬态响应、良好的线性调整率和负载调整率，无需外部补偿，并支持低等效串联电阻 (ESR) 输出电容器（如 MLCC）。

TPSM86838 在轻负载期间以强制连续导通模式 (FCCM) 运行，并且在所有负载条件下均可保持较低的输出纹波。TPSM86837 以 Eco-mode 运行，可在轻负载条件下实现高效率。

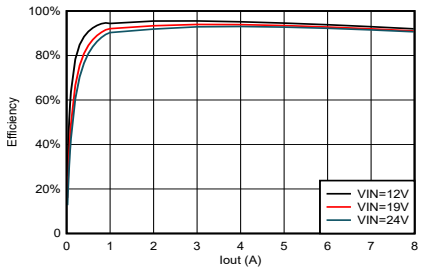
TPSM8683x 提供完整的非锁存 OV（过压）、UV（欠压）、OC（过流）、OT（过热）以及 UVLO（欠压锁定）保护，并具有电源正常状态指示器和输出放电功能特性。

TPSM8683x 可采用 19 引脚 5.0mm × 5.5mm HotRod QFN 封装，额定结温范围为 –40°C 至 150°C。

器件信息

器件型号	模式	封装和封装尺寸(1) (2)
TPSM86838	FCCM	RCG（B3QFN，19），5.0mm× 5.5mm
TPSM86837	ECO	

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



TPSM86838 效率，Vout = 5V，Fsw = 800kHz

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

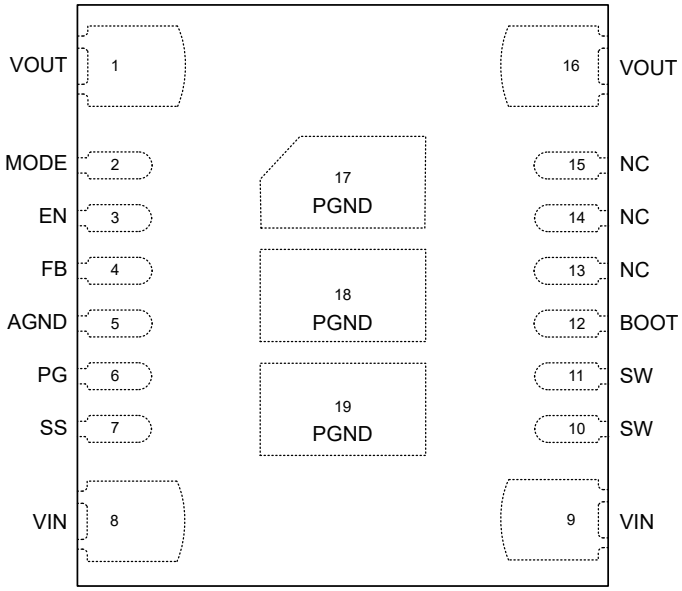


图 4-1. 19-Pin B3QFN RCG Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VOUT	1, 16	O	Output voltage. These pins are connected to the internal buck inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
MODE	2	I	Switching frequency selection pin. Connect this pin to a resistor to AGND for different switching frequency options shown in 表 6-1.
EN	3	I	Enable input control. Driving EN high or leaving this pin floating enables the module. A resistor divider can be used to imply an UVLO function.
FB	4	I	Feedback input. Connect the midpoint of the feedback resistor divider to this pin. Connect the upper resistor (RFBT) of the feedback divider to VOUT at the desired point of regulation. Connect the lower resistor (RFBB) of the feedback divider to AGND. Do not leave open or connect to ground.
AGND	5	G	Ground of internal analog circuitry. Connect AGND to PGND plane at a single point.
PG	6	O	Open-drain power-good monitor output that asserts low if the output voltage is out of PG threshold due to overvoltage, undervoltage, thermal shutdown, EN shutdown, or during soft start.
SS	7	I	Soft-start time selection pin. Connecting an external capacitor to AGND to set the soft-start time. A minimum 22nF ceramic capacitor must be connected at this pin, which sets the minimum soft-start time to approximately 2.2ms. Do not float.
VIN	8, 9	P	Input supply voltage. A 100nF input capacitor is internally connected from this pin to PGND within the module. Externally, connect input capacitors between these pins and PGND in close proximity to the device.
SW	10, 11	O	Switching node. *Do not place any external component on this pin or connect to any signal.* The amount of copper placed on this pin must be kept to a minimum to prevent issues with noise and EMI.
BOOT	12	I/O	Bootstrap pin for the internal high-side gate driver. A 100nF bootstrap capacitor is internally connected from this pin to SW within the module to provide the bootstrap voltage. *Do not place any external component on this pin or connect to any signal.*
NC	13, 14, 15	—	No connection. Tie to GND for better thermal performance.

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表 4-1. Pin Functions（续）

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
PGND	17, 18, 19	G	Power ground. This pin is the return current path for the power stage of the device. Connect these pads to the input supply return, the load return, and the capacitors associated with the VIN and VOUT pins.

(1) I = input, O = output, G = ground, P = power

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5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	32	V
	BOOT	–0.3	SW + 6	V
	BOOT-SW	–0.3	6	V
	EN, FB, MODE	–0.3	6	V
	PGND, AGND	–0.3	0.3	V
Output voltage	SW	–2	32	V
	SW (< 10ns transient)	–5	35	V
	PG	–0.3	6	V
Mechanical vibration	MIL-STD-883D, Method 2007.2, 20Hz to 2kHz		20	G
Mechanical shock	MIL-STD-883D, Method 2002.3, 1ms, 1/2 sine, mounted		500	G
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Input voltage	V_{IN}	4.5		28	V
	BOOT	–0.1		SW + 5.5	V
	BOOT-SW	–0.1		5.5	V
	EN, FB, MODE	–0.1		5.5	V
	PGND, AGND	–0.1		0.1	V
Output voltage	SW	–1		28	V
	PG	–0.1		5.5	V
Operating junction temperature, T_J		–40		150	°C

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5.4 Thermal Information

THERMAL METRIC[1]		TPSM8683x RCG (B3QFN) 19 PINS	UNIT
Eff $R_{\theta JA}$	Effective Junction-to-ambient thermal resistance (TPSM8683x EVM)	24	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC)	36	°C/W
Ψ_{JT}	Junction-to-top characterization parameter[2]	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter[3]	12	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-top board characterization parameter, Ψ_{JT}, estimates the junction temperature, T_J , of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \Psi_{JT} \times P_{DIS} + T_T$; where P_{DIS} is the power dissipated in the device and T_T is the temperature of the top of the device.
(3) The junction-to-top board characterization parameter, Ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \Psi_{JB} \times P_{DIS} + T_B$; where P_{DIS} is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

5.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that do not degrade the parametric or functional specifications of the device for the life of the product containing it. Typical values correspond to T_J = 25°C, V_{IN} = 24V. Minimum and maximum limits are based on T_J = –40°C to +150°C, V_{IN} = 4.5V to 28V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Quiescent current, operating [1]	T_J = 25°C, V_{EN} = 5V, V_{FB} = 0.7V (TPSM86838)		350		µA
		T_J = 25°C, V_{EN} = 5V, V_{FB} = 0.65V (TPSM86837)		45		µA
I_{SD}	Shutdown supply current	T_J = 25°C, V_{EN} = 0V		3		µA
UVLO						
UVLO	V_{IN} undervoltage lockout	Wake up V_{IN} voltage	4.0	4.2	4.4	V
		Shutdown V_{IN} voltage	3.5	3.65	3.8	V
		Hysteresis V_{IN} voltage		550		mV
ENABLE(EN PIN)						
I_{EN_INPUT}	Input current	V_{EN} = 1.1V		1		µA
I_{EN_HYS}	Hysteresis current	V_{EN} = 1.3V		3		µA
V_{EN_ON}	Enable threshold	EN rising		1.18	1.26	V
V_{EN_OFF}		EN falling	1	1.07		V
FEEDBACK VOLTAGE						
V_{FB}	Feedback voltage	V_{OUT} = 5V, continuous mode operation, T_J = 25°C	0.594	0.6	0.606	V
		V_{OUT} = 5V, continuous mode operation, T_J = –40°C to 150°C	0.591	0.6	0.609	V
CURRENT LIMIT						
I_{LS_OCL}	Low-side MOSFET valley current limit		8	9.6	11.1	A

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5.5 Electrical Characteristics（续）

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that do not degrade the parametric or functional specifications of the device for the life of the product containing it. Typical values correspond to T_J = 25°C, V_{IN} = 24V. Minimum and maximum limits are based on T_J = –40°C to +150°C, V_{IN} = 4.5V to 28V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{HS_OCL}	High-side MOSFET peak current limit		12.75	15	17.25	A
I_{NOC}	Reverse current limit for FCCM		3			A
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	V_{IN} = 24V, V_{OUT} = 5V, continuous mode operation, Mode setting to 800kHz		800		kHz
$t_{ON(MIN)}$	Minimum on time[2]			50		ns
$t_{OFF(MIN)}$	Minimum off time[2]	T_J = 25°C		150		ns
SOFT START						
I_{SS}	Soft-start charging current			6		uA
POWER GOOD						
V_{PGTH}	PG lower threshold - falling	% of V_{FB}		85%		
	PG lower threshold - rising	% of V_{FB}		90%		
	PG upper threshold - falling	% of V_{FB}		110%		
	PG upper threshold - rising	% of V_{FB}		115%		
t_{PG_DLY}	PG delay	PG from low-to-high		64		us
		PG from high-to-low		32		us
V_{OVP}	Output OVP threshold	OVP detect(L->H)		125%		
t_{OVP_DEG}	OVP Prop deglitch	T_J = 25°C		32		us
V_{UVP}	Output UVP threshold	Hiccup detect(H->L)		65%		
t_{UVP_WAIT}	UV protection hiccup wait time			256		us
t_{UVP_HICCUP}	UV protection hiccup time before recovery			10.5		*t_{SS}
THERMAL SHUTDOWN						
Thermal shutdown threshold[3]		Temperature rising	150	165		°C
		Hysteresis		30		°C
SW DISCHARGE RESISTANCE						
V_{OUT} discharge resistance		V_{EN} = 0, V_{SW} = 0.5V, T_J = 25°C		200		Ω

(1) Not representative of the total input current of the system when in regulation. Specified by design and characterization test.
(2) Not production tested. Specified by design.
(3) Not production tested. Specified by design and engineering sample correlation.

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5.6 Typical Characteristics

V_{IN} = 12V (unless otherwise noted)

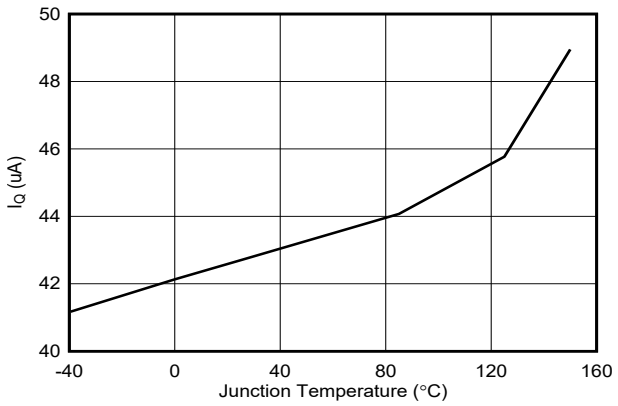


图 5-1. TPSM86837 Quiescent Current vs Temperature

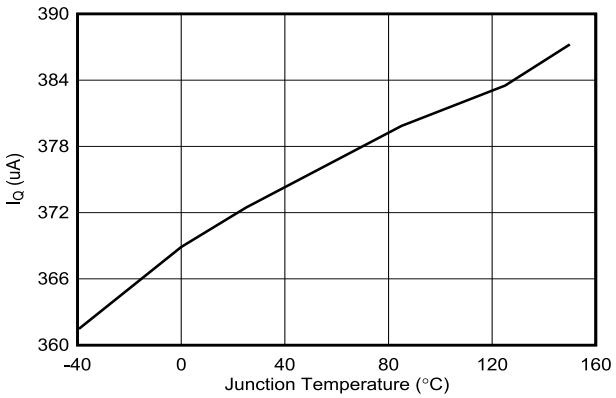


图 5-2. TPSM86838 Quiescent Current vs Temperature

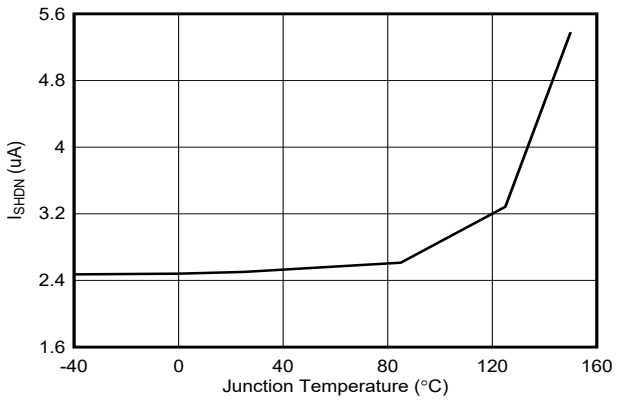


图 5-3. Shutdown Current vs Temperature

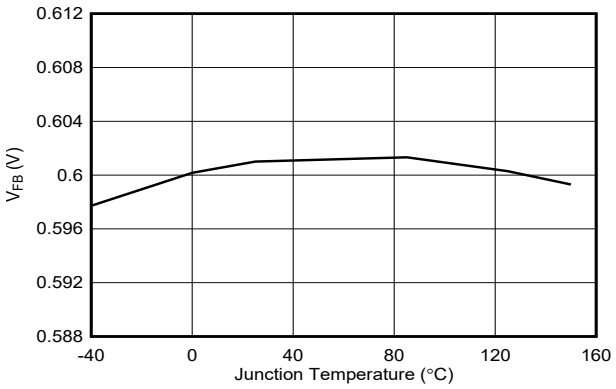


图 5-4. Feedback Voltage vs Temperature

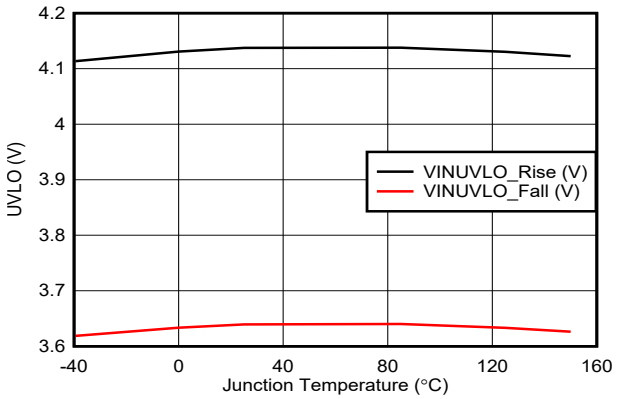


图 5-5. VIN UVLO Threshold vs Temperature

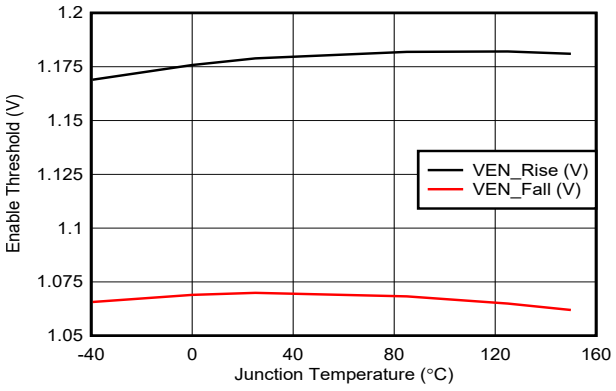


图 5-6. EN Threshold vs Temperature

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5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

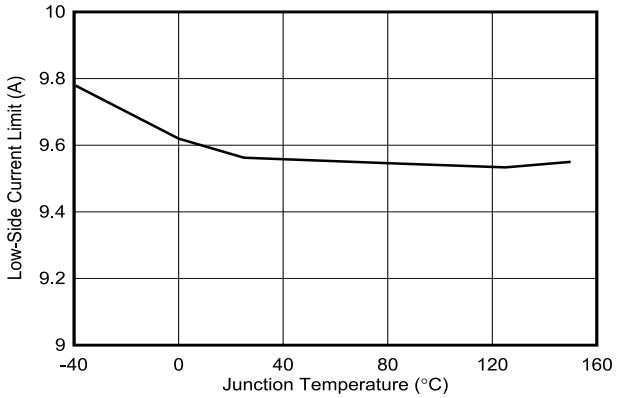


图 5-7. Low-Side Valley Current Limit vs Temperature

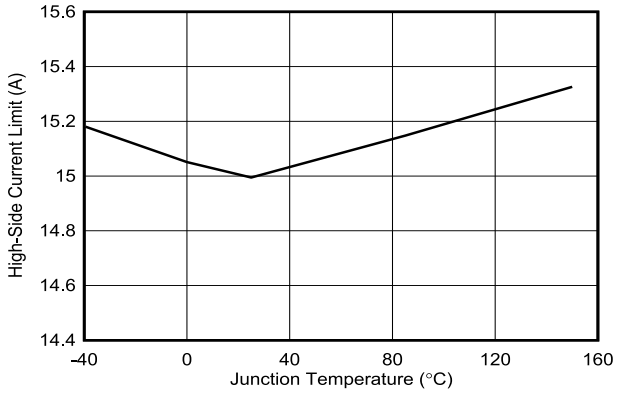


图 5-8. High-Side Peak Current Limit vs Temperature

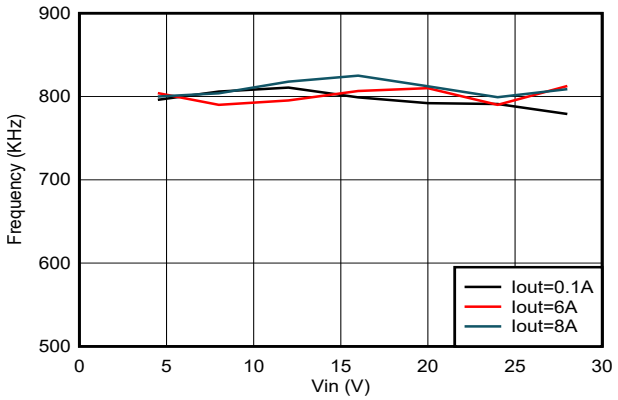


图 5-9. TPSM86838 Switching Frequency vs Input Voltage, Fsw = 800kHz, Vo = 1.8V

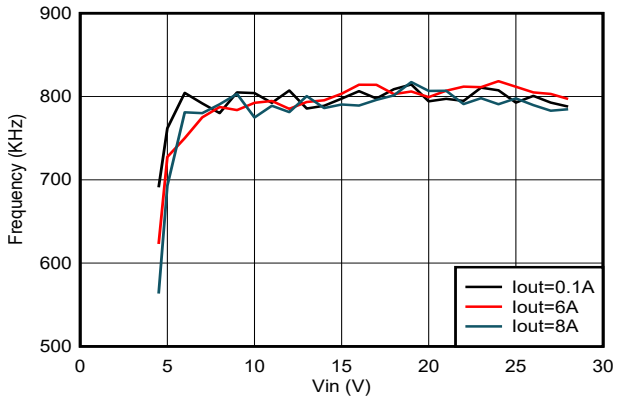


图 5-10. TPSM86838 Switching Frequency vs Input Voltage, Fsw = 800kHz, Vo = 3.3V

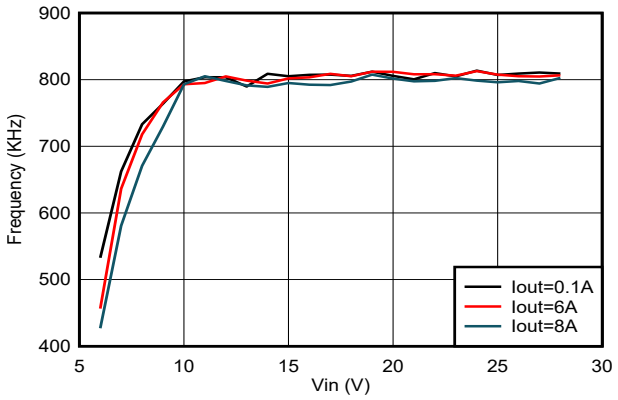


图 5-11. TPSM86838 Switching Frequency vs Input Voltage, Fsw = 800kHz, Vo = 5V

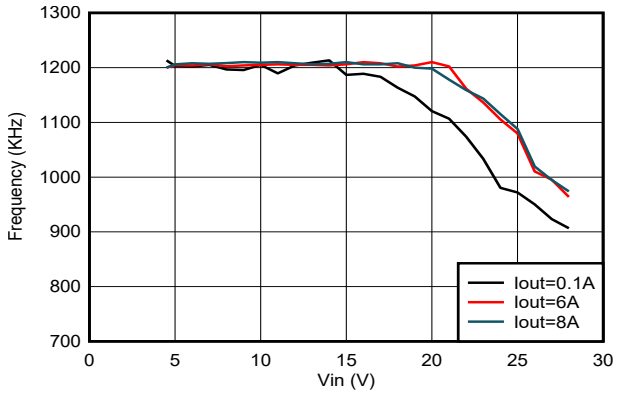


图 5-12. TPSM86838 Switching Frequency vs Input Voltage, Fsw = 1200kHz, Vo = 1.8V

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5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

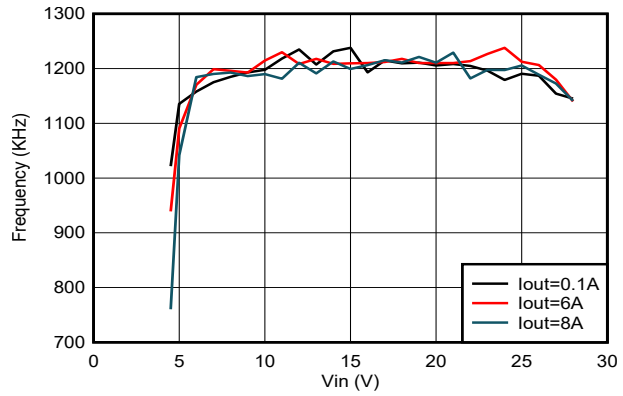


图 5-13. TPSM86838 Switching Frequency vs Input Voltage, Fsw = 1200kHz, Vo = 3.3V

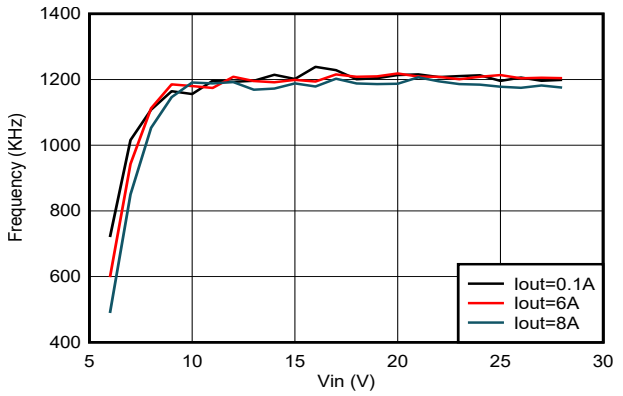


图 5-14. TPSM86838 Switching Frequency vs Input Voltage, Fsw = 1200kHz, Vo = 5V

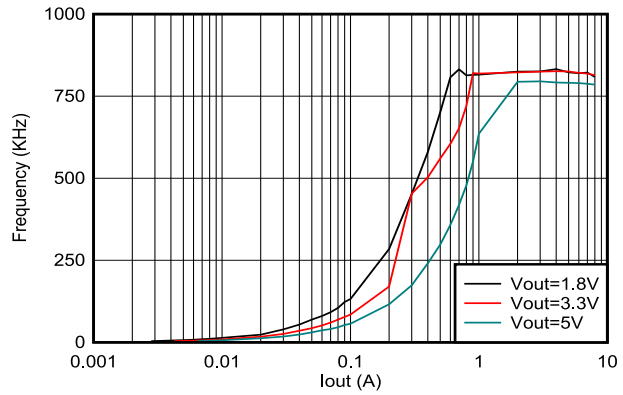


图 5-15. TPSM86837 Switching Frequency vs Output Current, Fsw = 800kHz, Vin = 24V

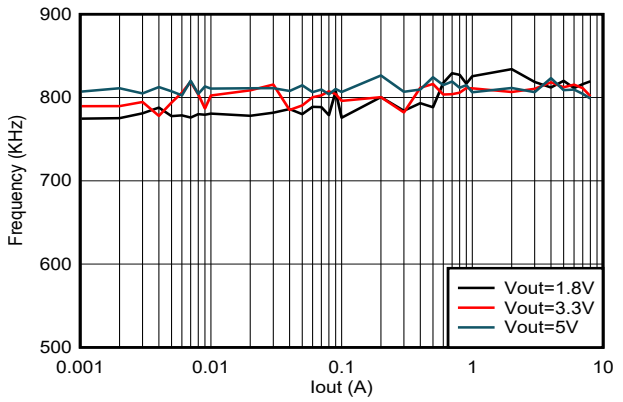


图 5-16. TPSM86838 Switching Frequency vs Output Current, Fsw = 800kHz, Vin = 24V

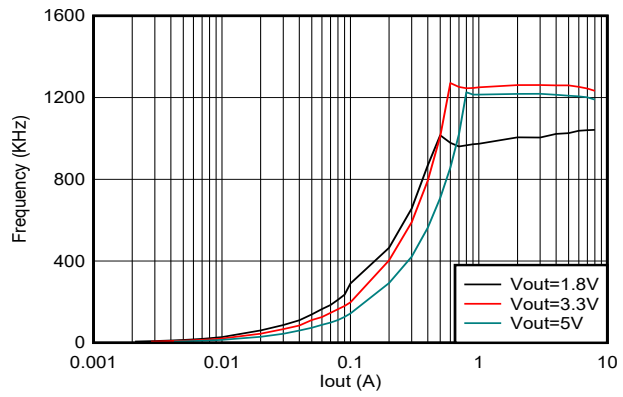


图 5-17. TPSM86837 Switching Frequency vs Output Current, Fsw = 1200kHz, Vin = 24V

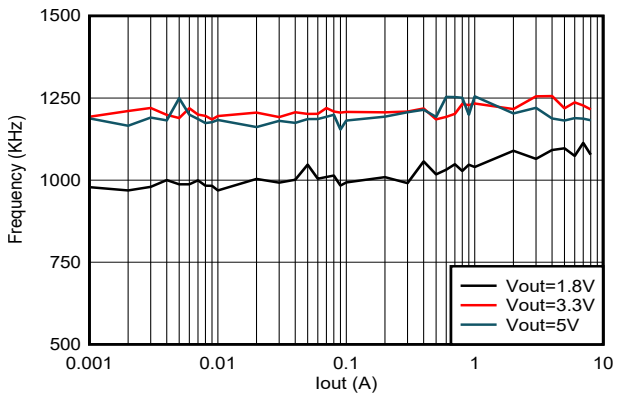


图 5-18. TPSM86838 Switching Frequency vs Output Current, Fsw = 1200kHz, Vin = 24V

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5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

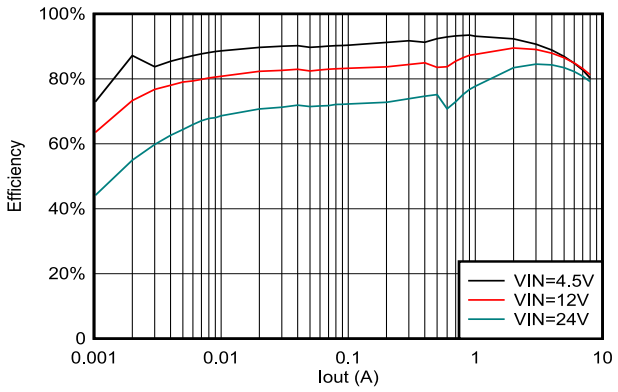


图 5-19. TPSM86837 Efficiency, VOUT = 1.8V, Fsw = 800kHz

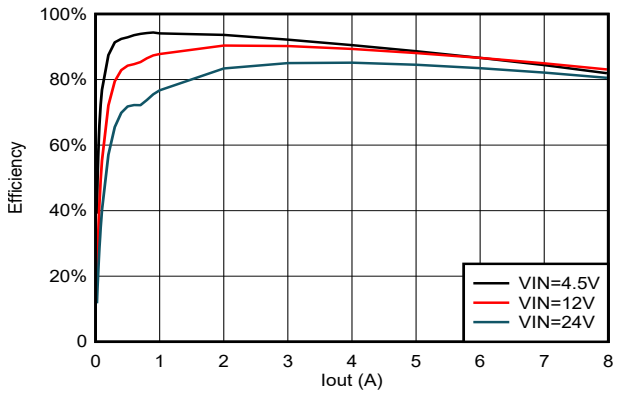


图 5-20. TPSM86838 Efficiency, VOUT = 1.8V, Fsw = 800kHz

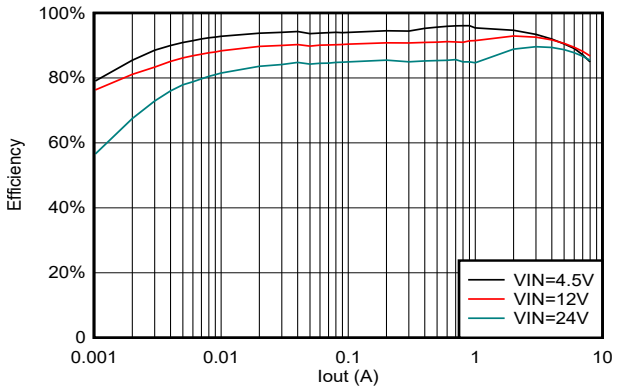


图 5-21. TPSM86837 Efficiency, VOUT = 3.3V, Fsw = 800kHz

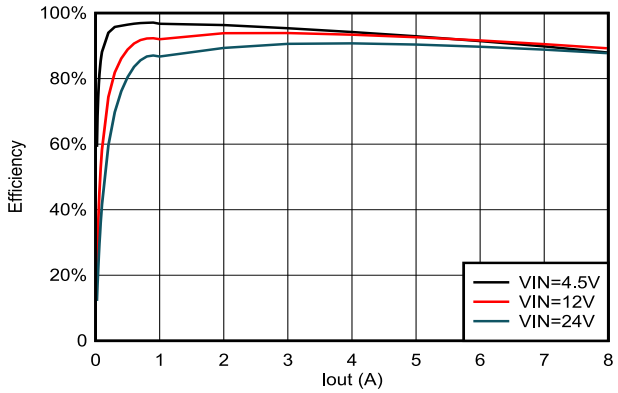


图 5-22. TPSM86838 Efficiency, VOUT = 3.3V, Fsw = 800kHz

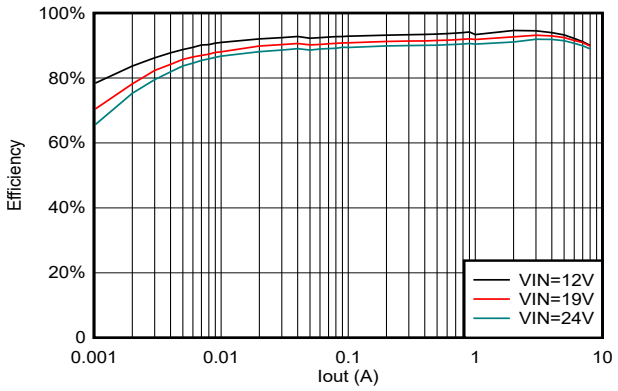


图 5-23. TPSM86837 Efficiency, VOUT = 5V, Fsw = 800kHz

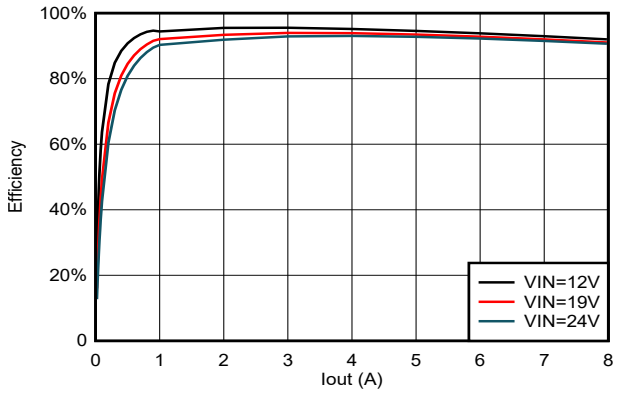


图 5-24. TPSM86838 Efficiency, VOUT = 5V, Fsw = 800kHz

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5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

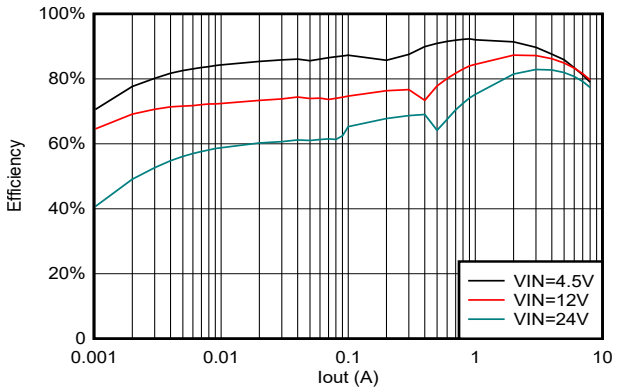


图 5-25. TPSM86837 Efficiency, VOUT = 1.8V, Fsw = 1200kHz

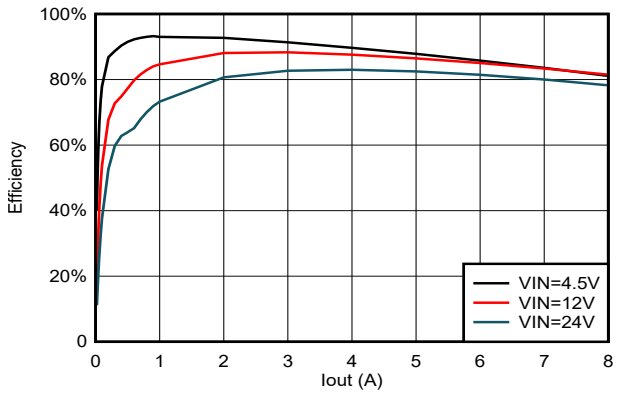


图 5-26. TPSM86838 Efficiency, VOUT = 1.8V, Fsw = 1200kHz

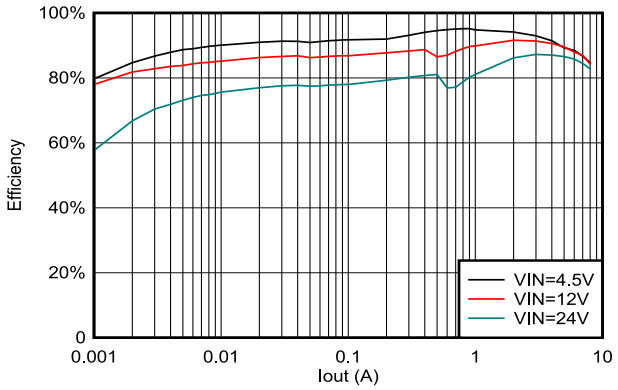


图 5-27. TPSM86837 Efficiency, VOUT = 3.3V, Fsw = 1200kHz

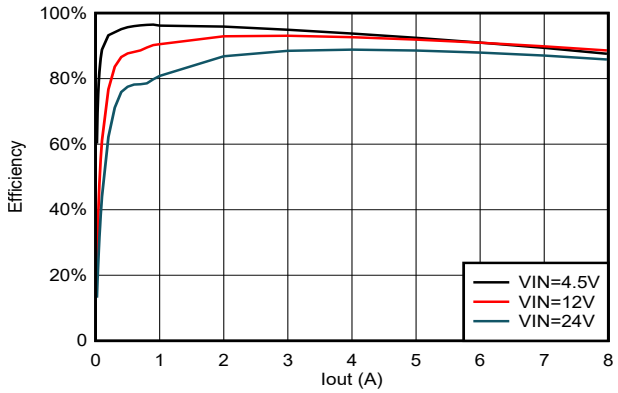


图 5-28. TPSM86838 Efficiency, VOUT = 3.3V, Fsw = 1200kHz

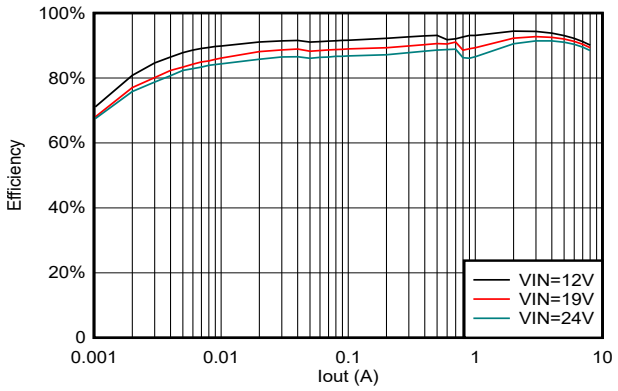


图 5-29. TPSM86837 Efficiency, VOUT = 5V, Fsw = 1200kHz

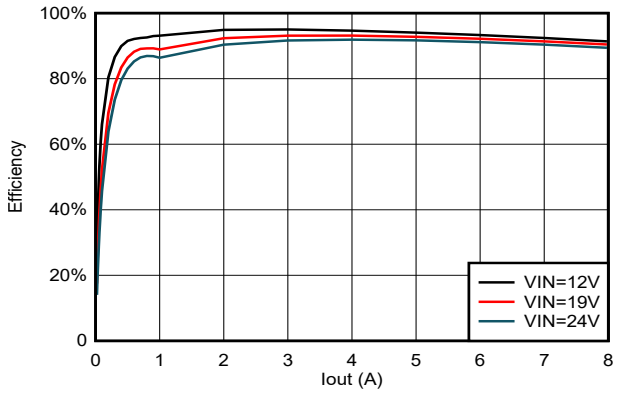


图 5-30. TPSM86838 Efficiency, VOUT = 5V, Fsw = 1200kHz

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6 Detailed Description

6.1 Overview

The TPSM8683x is an easy-to-use, synchronous buck DC/DC power module designed for a wide variety of applications where reliability, small design size, and low EMI signature are of paramount importance. With integrated power MOSFETs, a shielded buck inductor, and basic passives, the TPSM8683x is a 8A synchronous buck module operating from 4.5V to 28V input voltage (V_{IN}), and the output voltage ranges from 0.6V to 5.5V. The proprietary D-CAP3 control mode enables low external component count, ease of design, optimization of the power design for power, size, and efficiency. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. TPSM86837 operates in Eco-mode to attain high efficiency at light load. TPSM86838 operates in FCCM mode which has the quasi-fixed switching frequency at both light and heavy load. The TPSM8683x is able to adapt both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The TPSM8683x incorporates specific features to improve EMI performance in noise-sensitive applications:

- An optimized package and pinout design enables a shielded switch-node layout that mitigates radiated EMI.
- Parallel input and output paths with symmetrical capacitor layouts minimize parasitic inductance, switch voltage ringing, and radiated field coupling
- Integrated power MOSFETs with enhanced gate drive control enable low-noise PWM switching.

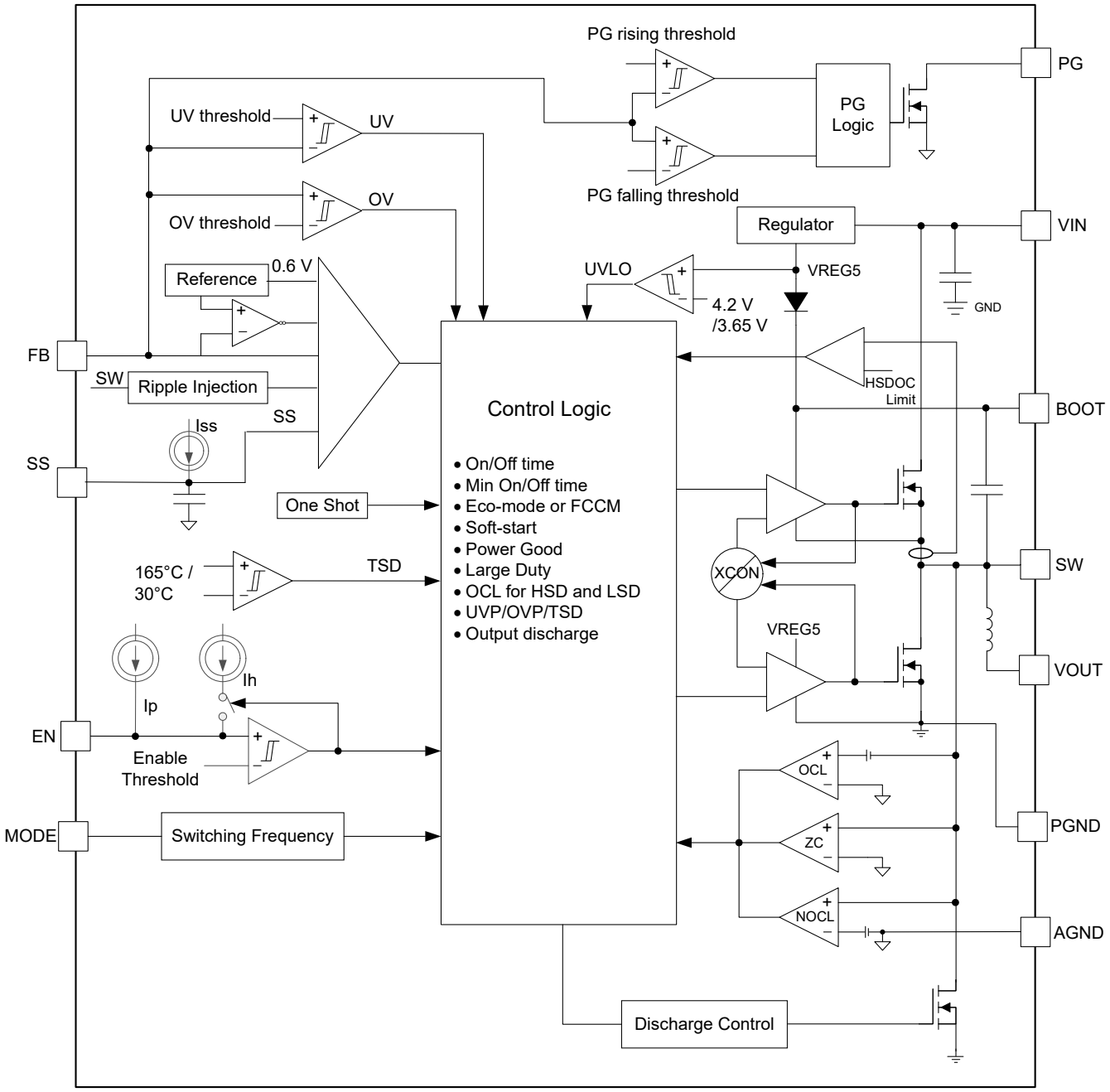
The TPSM8683x module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing programmable non-latched input undervoltage lockout (UVLO)
- Non-latched overvoltage protections
- Hiccup-mode overcurrent protection with cycle-by-cycle valley current limits
- Thermal shutdown with automatic recovery.

Leveraging a pin arrangement designed for simple layout that requires only a few external components, the TPSM8683x is specified to maximum junction temperatures of 150°C.

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6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 The Adaptive On-Time Control and PWM Operation

The main control loop of the TPSM8683x is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. The D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for quasi-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The D-CAP3 control mode is stable even with virtually no ripple at the output. The TPSM8683x also includes an error amplifier that makes the output voltage very accurate. No external current sense network or loop compensation is required for D-CAP3 control mode.

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At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and is inversely proportional to the module input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence called adaptive on-time control. When the feedback voltage falls below the reference voltage, the one-shot timer is reset and the high-side MOSFET is turned on again. An internal ripple generation circuit is added to the reference voltage for emulating the output ripple, and this action enables the use of very low-ESR output capacitors, such as multi-layered ceramic caps (MLCC).

6.3.2 Mode Selection

TPSM8683x has a MODE pin to configure the switching frequency, as shown in 表 6-1. The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options list in 表 6-1.The voltage on the MODE pin can be set by connecting a resistor to AGND. A guideline for the MODE resistor in 1% resistors in shown in 表 6-1. The MODE pin setting can be reset only by a VIN or EN power cycling.

图 6-1 shows the typical start-up sequence of the device after the enable signal triggers the EN turn-on threshold. After the voltage of internal VCC crosses the UVLO rising threshold, the MODE setting is read. After this process, the MODE is latched and does not change until VIN or EN toggles to restart-up this device. Then after a delay, the internal soft-start function begins to ramp up and Vout ramps up smoothly. When Vout is up to the reference voltage, PGOOD turns to high after a delay.

表 6-1. MODE Pin Settings for TPSM8683x

MODE Pin	Switching Frequency
R = 162kohm	800kHz
R = 374kohm	1200kHz

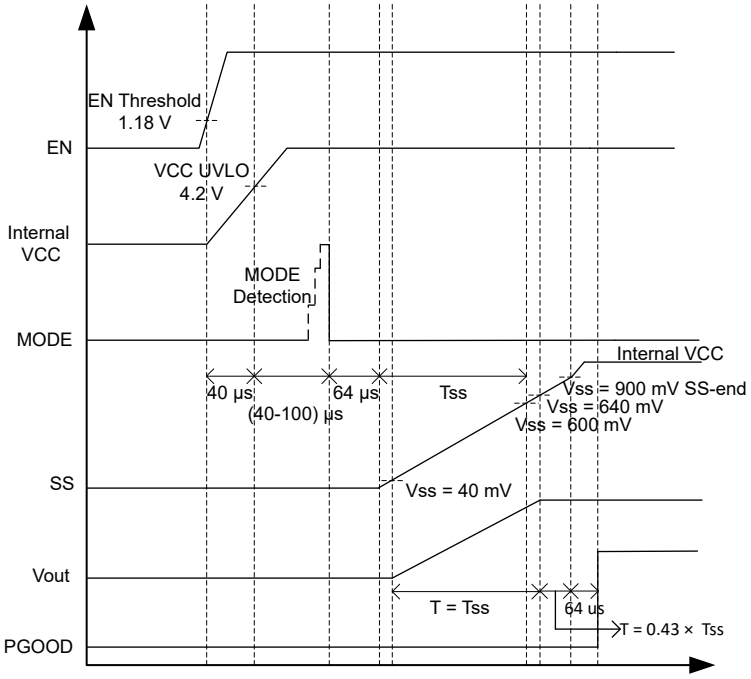


图 6-1. Power-Up Sequence

6.3.2.1 FCCM Control and Eco-mode Control

TPSM86838 operates in forced continuous conduction mode (FCCM) in light load conditions and allows the inductor current to become negative. In FCCM, the switching frequency is maintained at a quasi-fixed level over the entire load range, which is designed for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load compared with that under Eco-mode. This

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mode also can help to avoid switching frequency dropping into audible range that can introduce some audible *noise*.

TPM86837 is set to Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to a point that the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as in the continuous conduction mode so that longer time is needed to discharge the output capacitor with smaller load current to the level of the reference voltage. This process makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation IOUT(LL) current can be calculated by 方程式 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times Fsw} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

6.3.3 Soft Start and Prebiased Soft Start

The TPSM8683x has an adjustable soft-start time that can be set by connecting a capacitor between SS and AGND. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and AGND. 方程式 2 calculates the soft-start time (T_{SS}) :

$$T_{ss} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (2)$$

If the external capacitor (C_{SS}) has pre-stored voltage at start-up, the device initially discharges the external capacitor voltage to lower voltage then charge again to prevent inrush start-up.

If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme make sure that the converters ramp up smoothly into regulation point.

6.3.4 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operating. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the standby operation.

The EN pin has an internal pullup current source which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, open-drain or open-collector output logic can be used to interface with the pin.

The TPSM8683x implements internal undervoltage lockout (UVLO) circuitry on the V_{IN} pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN} UVLO threshold. The internal V_{IN} UVLO threshold has a hysteresis of 550mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in 图 6-2. When using the external UVLO function, TI recommends setting the hysteresis at a value greater than 500mV.

The EN pin has a small pullup current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because the pullup current increases by I_h when the EN pin crosses the enable threshold. Use 方程式 3 and 方程式 4 to calculate the values of R1 and R2 for a specified UVLO threshold. After R1, R2 are settled down, the V_{EN} voltage can be calculated by 方程式 5, which must be lower than 5.5V with maximum V_{IN}.

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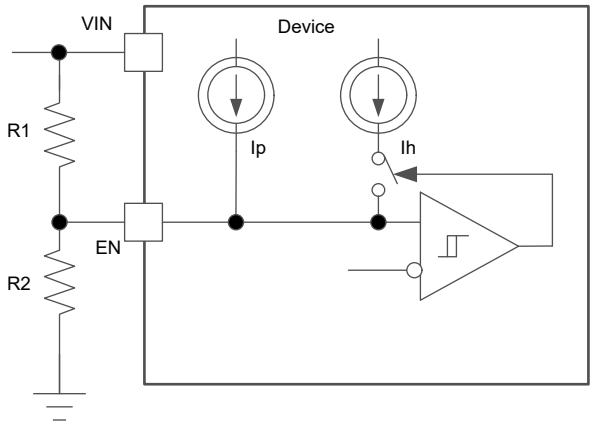


图 6-2. Adjustable VIN Undervoltage Lockout

$$R_1 = \frac{V_{START} \times \frac{V_{ENfalling}}{V_{ENrising}} - V_{STOP}}{I_p \times \left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h} \quad (3)$$

$$R_2 = \frac{R_1 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R_1 \times \left(I_p + I_h\right)} \quad (4)$$

$$V_{EN} = \frac{R_2 \times V_{IN} + R_1 \times R_2 \times \left(I_p + I_h\right)}{R_1 + R_2} \quad (5)$$

Where

- I_p = 1μA
- I_h = 3μA
- $V_{ENfalling}$ = 1.07V
- $V_{ENrising}$ = 1.18V

6.3.5 Output Overcurrent Limit and Undervoltage Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle low-side MOSFET valley current detection and high-side MOSFET peak current detection. The switching current is monitored by measuring the MOSFET drain to source voltage. This voltage is proportional to the switching current. To improve accuracy, the voltage sensing is temperature compensated.

There are some important considerations for this type of overcurrent limit. When the load current is higher than the I_{LS_LIMIT} added by one half of the peak-to-peak inductor ripple current, or higher than I_{HS_LIMIT} subtracted by one half of the peak-to-peak inductor ripple current, the OCP is triggered and the current is being limited, output voltage tends to drop because the load demand is higher than what the module can support. When the output voltage falls below 65% of the target voltage, the UVP comparator detects this fall and shuts down the device after a deglitch wait time of 256 us and then re-start after the hiccup time of 10.5 cycles of soft-start time. When the overcurrent condition is removed, the output recovers.

6.3.6 Overvoltage Protection

When the output voltage becomes higher than 125% of the target voltage, the OVP is triggered. The output is discharged after a deglitch time of 32us and both the high-side MOSFET driver and the low-side MOSFET driver turn off. When the overvoltage condition is removed, the output voltage recovers.

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6.3.7 UVLO Protection

Undervoltage Lockout protection(UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut down. This protection is non-latched.

6.3.8 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 165°C (typical), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and the discharge path is turned on. When T_J decreases below the hysteresis amount, the module resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 30°C is implemented on the thermal shutdown temperature.

6.3.9 Output Voltage Discharge

The TPSM8683x has a built-in discharge function by using an integrated MOSFET with 200Ω $R_{DS(on)}$, which is connected to the output terminal SW. The discharge is slow due to the lower current capability of the MOSFET. The discharge path turns on when the device is turned off due to UV, OV, OT, and EN shutdown conditions.

6.3.10 Power Good

The TPSM8683x has a built-in power-good (PG) function to indicate whether the output voltage has reached an appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor (to any voltage below 5.5V). TI recommends a pullup resistor of 100 kΩ to pull the pin up to 5V voltage. The pin can sink 10mA of current and maintain the specified logic low level. After the FB pin voltage is between 90% and 110% of the internal reference voltage (V_{REF}) and after a deglitch time of 64µs, the PG turns to high impedance status. The PG pin is pulled low after a deglitch time of 32µs when FB pin voltage is lower than 85% of the internal reference voltage or greater than 115% of the internal reference voltage, or in events of thermal shutdown, EN shutdown, UVLO conditions. V_{IN} must remain present for the PG pin to stay Low. The PG pin logic are shown in 表 6-2.

表 6-2. Power-Good Pin Logic Table

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN = High)	V_{FB} does not trigger V_{PGTH}	√	
	V_{FB} triggers V_{PGTH}		√
Shutdown (EN = Low)			√
UVLO	$2V < V_{IN} < V_{UVLO}$		√
Thermal shutdown	$T_J > T_{SD}$		√
Power supply removal	$V_{IN} < 2V$	√	

6.3.11 Large Duty Operation

The TPSM8683x can support large duty operations by smoothly dropping down the switching frequency. The switching frequency is allowed to smoothly drop to make T_{ON} extended to implement the large duty operation and also improve the performance of the load transient performance. The TPSM8683x can support up to 98% duty cycle operation.

6.4 Device Functional Modes

6.4.1 Standby Operation

The TPSM8683x can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 3µA (typical) when in standby condition.

6.4.2 Light Load Operation

TPSM86837 operates in Eco-mode, which maintains high efficiency at light loading. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point

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where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as the on-time was in continuous conduction mode so that discharging the output capacitor with smaller load current to the level of the reference voltage takes longer. This fact makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

TPSM86838 operates in forced CCM (FCCM) mode. The switching frequency is maintained at an almost constant level over the entire load range which is designed for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

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7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The schematic of 图 7-1 shows a typical application for TPSM8683x. This design converts an input voltage range of 4.5V to 28V down to 1.8V with a maximum output current of 8A.

7.2 Typical Application

The application schematic in 图 7-1 shows the TPSM8683x 4.5V to 28V Input, 1.8V output module design meeting the requirements for 8A output. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

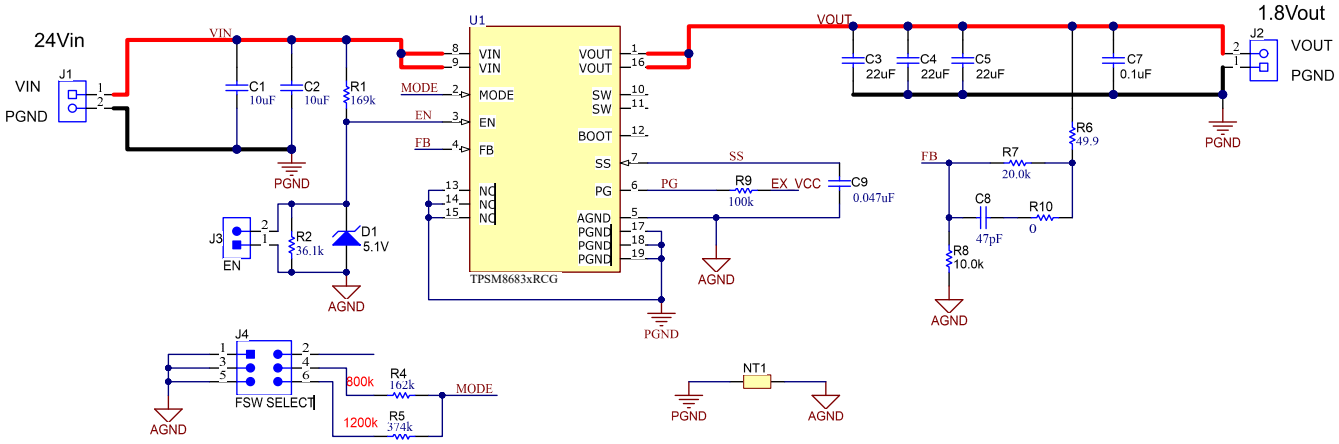


图 7-1. TPSM8683x 1.8V, 8A Reference Design

7.2.1 Design Requirements

表 7-1 shows the design parameters for this application.

表 7-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	24V nominal, 4.5V to 28V
Output voltage	1.8V
Transient response, 8A load step	ΔV_{OUT} = ±5%
Output ripple voltage	20mV
Output current rating	8A
Operating frequency	800kHz

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7.2.2 Detailed Design Procedure

7.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the V_{FB} pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 方程式 6 to calculate V_{OUT}. R_6 is optional and can be used to measure the control loop frequency response.

To improve efficiency at very light loads consider using larger value resistors. If the resistance is too high, the device is more susceptible to noise and voltage errors from the V_{FB} input current are more noticeable. Please note that TI does not recommend dynamically adjusting output voltage.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R7}{R8}\right) \quad (6)$$

7.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (7)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. D-CAP3 control mode introduces a high frequency zero that reduces the gain roll off to –20dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 方程式 7 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement, use the values recommended in 表 7-2.

表 7-2. Recommended Component Values

Switching Frequency (kHz)	Output Voltage (V)(1)	R7 (kΩ)(2)	R8 (kΩ)	C_{OUT} (µF)(3)		C8 (pF)(4)
				Typical	Maximum	
800	1.05	7.5	10	22uF × 3	22uF × 10	
	1.8	20	10	22uF × 3	22uF × 10	30-100 (47 typical)
	3.3	45.3	10	22uF × 3	22uF × 10	30-100 (47 typical)
	5	73.2	10	22uF × 2	22uF × 10	30-100 (47 typical)
1200	1.05	7.5	10	22uF × 3	22uF × 10	
	1.8	20	10	22uF × 3	22uF × 10	30-100 (47 typical)
	3.3	45.3	10	22uF × 3	22uF × 10	30-100 (47 typical)
	5	73.2	10	22uF × 2	22uF × 10	100-200 (150 typical)

(1) Please use the recommended C_{OUT} of the higher and closest output rail for unlisted output rails.
(2) R7 = 0 Ω for V_{OUT} = 0.6V.
(3) COUT in this data sheet is using Murata GRM32ER71E226KE15L 25VDC capacitor. TI recommends to use the same effective output capacitance. The effective capacitance is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. A careful study of bias and temperature variation of any capacitor bank must

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be made to make sure that the minimum value of effective capacitance is provided. Refer to the information of DC bias and temperature characteristics from manufacturers of ceramic capacitors. Higher than Cout_max capacitance is allowed by careful tuning the feedforward compensation.

(4) R10 and C8 can be used to improve the load transient response or improve the loop-phase margin. The *Optimizing Transient Response of Internally Compensated DCDC Converters with Feed-forward Capacitor* application report is helpful when experimenting with a feed-forward capacitor.

The capacitor value and ESR determines the amount of output voltage ripple. The TPSM8683x is intended for use with ceramic or other low ESR capacitors. Use 方程式 8 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times Fsw} \quad (8)$$

For this design, three MuRata GRM32ER71E226KE15L 25VDC 22µF output capacitors are used so that the effective capacitance is 68µF at DC biased voltage of 1.8V.

7.2.2.3 Input Capacitor Selection

The TPSM8683x requires input decoupling capacitors, and a bulk capacitor is needed depending on the application. TI recommends at least two 10µF ceramic capacitors for the decoupling capacitor. The capacitor voltage rating must be greater than the maximum input voltage. Use 方程式 9 to calculate the input voltage ripple.

$$\Delta V_{IN} = \frac{I_{OUTMAX} \times 0.25}{C_{IN} \times Fsw} \quad (9)$$

The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. Use 方程式 10 to calculate the input ripple current:

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}} \times \frac{V_{IN(MIN)} - V_{OUT}}{V_{IN(MIN)}}} \quad (10)$$

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7.2.3 Application Curves

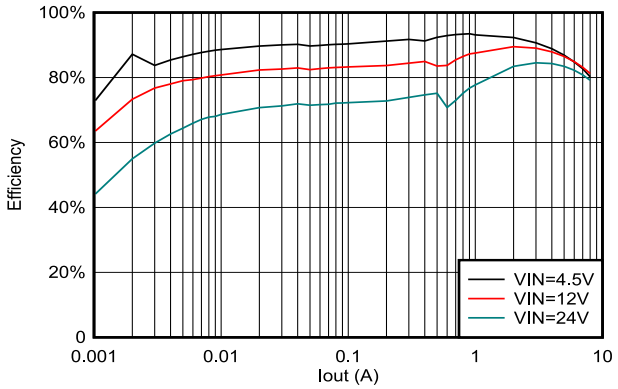


图 7-2. TPSM86837 Efficiency

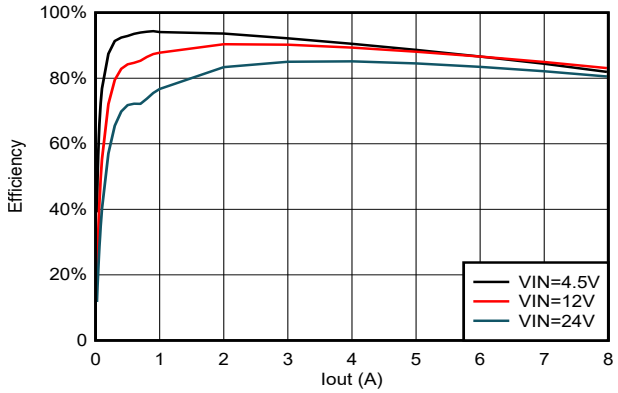


图 7-3. TPSM86838 Efficiency

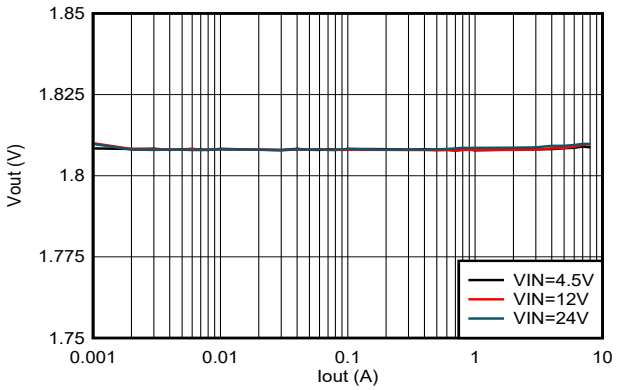


图 7-4. TPSM86838 Load Regulation

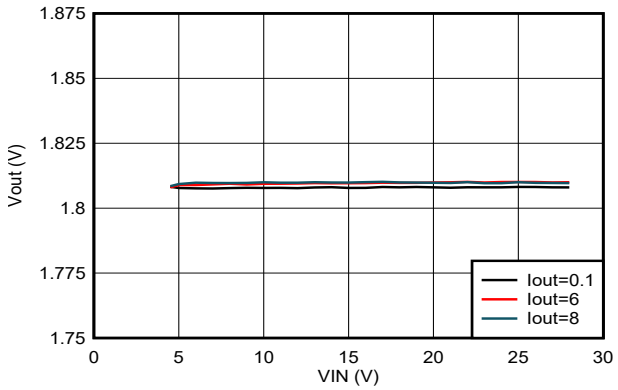


图 7-5. TPSM86838 Line Regulation

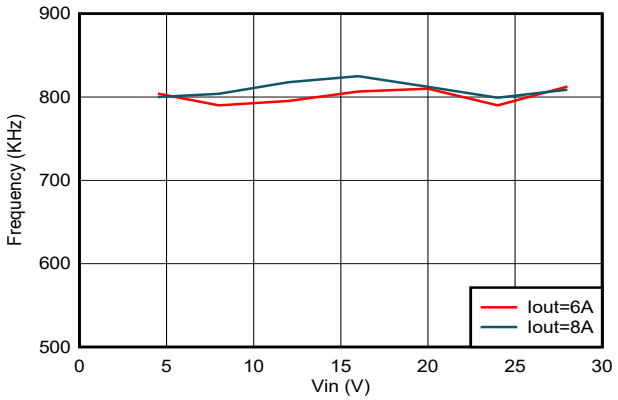


图 7-6. Switching Frequency vs Input Voltage

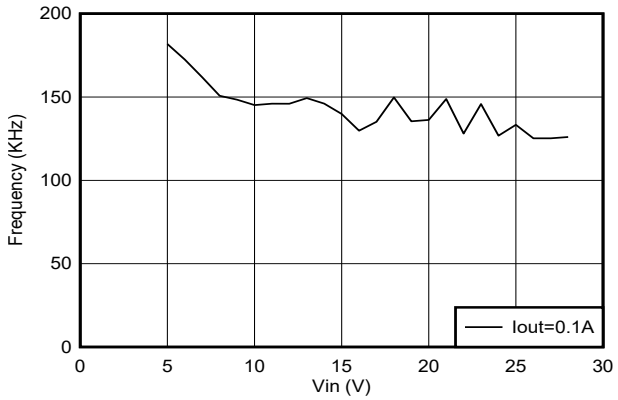


图 7-7. TPSM86837 Switching Frequency vs Input Voltage

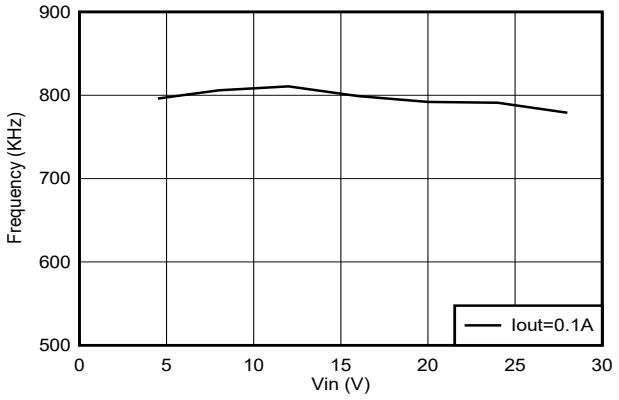


图 7-8. TPSM86838 Switching Frequency vs Input Voltage

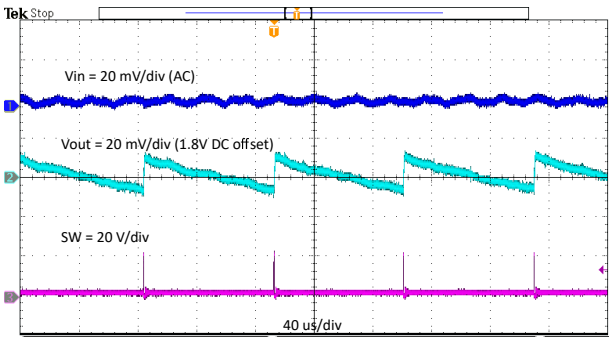


图 7-9. TPSM86837 Steady State Waveform, I_{OUT} = 0.01A

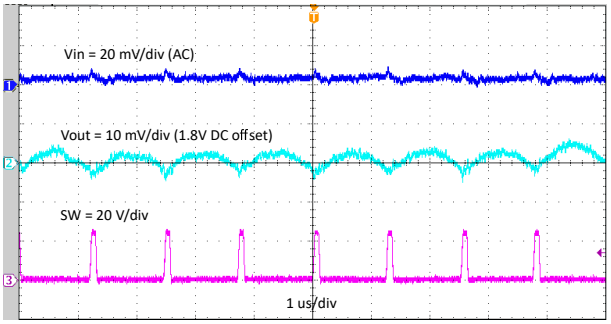


图 7-10. TPSM86838 Steady State Waveform, I_{OUT} = 0.01A

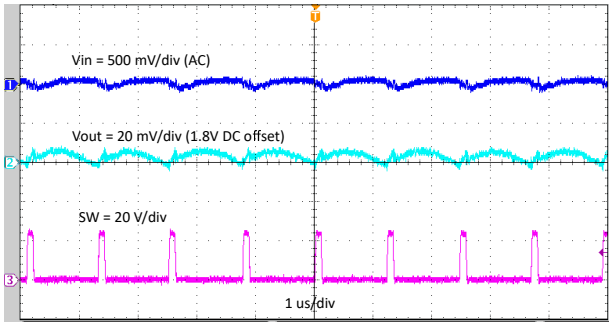


图 7-11. Steady State Waveform, I_{OUT} = 8A

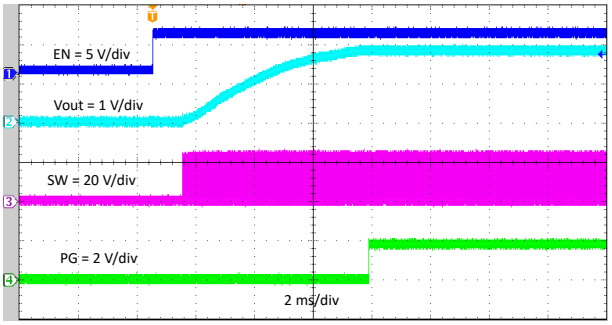


图 7-12. Enable Relative to EN

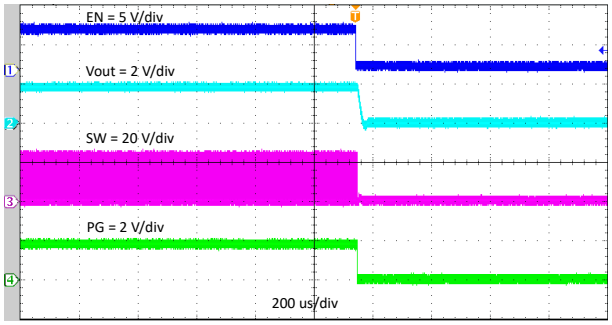


图 7-13. Disable Relative to EN

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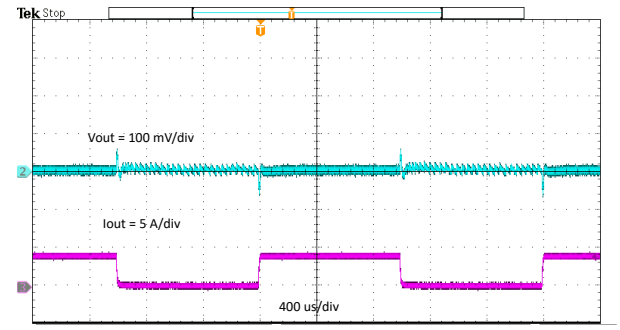


图 7-14. TPSM86837 Transient Response 0A to 4A

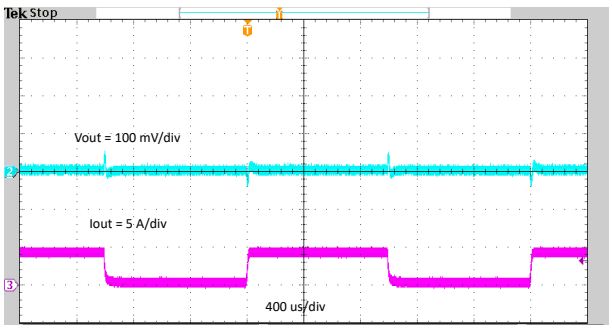


图 7-15. TPSM86838 Transient Response 0A to 4A

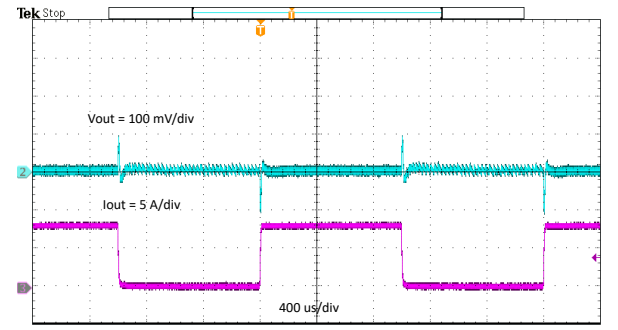


图 7-16. TPSM86837 Transient Response 0A to 8A

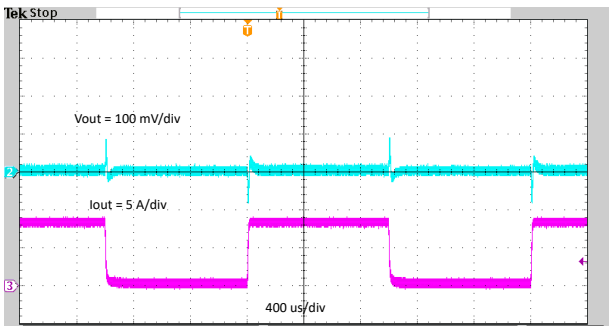


图 7-17. TPSM86838 Transient Response 0A to 8A

7.3 Power Supply Recommendations

The TPSM8683x is designed to operate from input supply voltage in the range of 4.5V to 28V. Buck modules require the input voltage to be higher than the output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPSM8683x circuit, TI recommends some additional input bulk capacitance.

7.3.1 Application Thermal Considerations

The power module integrates the main power dissipating elements, the power switches and magnetics, all into one package, which enables smaller design size and simplifies the development. Therefore, in addition to the IC losses, the heat generated from the inductor direct current resistance (DCR) and core losses add to the total power dissipated in the package. Under the same operating conditions as the discrete counterparts (which have an external inductor), the module has the challenge of dissipating more heat through a smaller surface area. There is a constraint on the maximum output current that modules can deliver at higher operating ambient temperatures due to limitations in maximum temperature ratings for both the inductor and IC.

The temperature rise of module can be calculated by using efficiency and EVM effective $R_{\theta JA}$. 方程式 11 calculates the power loss from the data sheet efficiency curves:

$$Power\ Loss = \left(V_{OUT} \times I_{OUT}\right) \times \left(\frac{1}{\eta} - 1\right) \quad (11)$$

Where η is the application conditions efficiency. As an example, 图 7-2 shows the efficiency curve at 25°C for the 24Vin, 1.8Vout, 800kHz condition. At 8A load, with nearly 81% efficiency, 方程式 11 calculates the power loss as 3.378W. Multiplying by the EVM effective $R_{\theta JA}$ 24 °C/W gives a temperature rise of 81°C.

The maximum temperature rating for TPSM8683x is 150°C. Subtracting this temperature rise from the 150°C maximum temperature results in a maximum ambient temperature of 69°C. Consider operation within this ambient temperature.

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7.4 Layout

7.4.1 Layout Guidelines

The following list summarizes the essential guidelines for PCB layout and component placement to optimize DC/DC module performance, including thermals and EMI signature.

1. Use a four-layer PCB with two-ounce copper thickness for good thermal performance and with maximum ground plane.
2. Place input capacitors as close as possible to the VIN pins. Note the dual and symmetrical arrangement of the input capacitors based on the VIN1 and VIN2 pins located on each side of the module package. The high-frequency currents are split in two and effectively flow in opposing directions such that the related magnetic fields contributions cancel each other, leading to improved EMI performance.
   - Use low-ESR 1206 or 1210 ceramic capacitors with X7R or X7S dielectric.
   - Make ground return paths for the input capacitors consist of localized top-side planes that connect to the PGND pads under the module.
   - Make VIN traces as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation. Even though the VIN pins are connected internally, use a wide polygon plane on a bottom PCB layer to connect these pins together and to the input supply.
3. Place output capacitors as close as possible to the VOUT pins. A similar dual and symmetrical arrangement of the output capacitors enables magnetic field cancellation and EMI mitigation.
   - Make ground return paths for the output capacitors consist of localized top-side planes that connect to the PGND pads under the module.
   - Make VOUT traces as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation. Even though the VOUT pins are connected internally, use a wide polygon plane on a bottom PCB layer to connect these pins together and to the load, thus reducing conduction loss and thermal stress.
4. Keep the FB trace as short as possible by placing the feedback resistors close to the FB pin. Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. FB is the input to the voltage-loop error amplifier and represents a high-impedance node sensitive to noise. Route a trace from the upper feedback resistor to the required point of output voltage regulation. Place the voltage feedback loop away from the high-voltage switching trace, and preferably has ground shield.
5. Provide enough PCB area for proper heatsinking. Use sufficient copper area to achieve a low thermal impedance commensurate with the maximum load current and ambient temperature conditions. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pads (PGND) of the package to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes.

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7.4.2 Layout Example

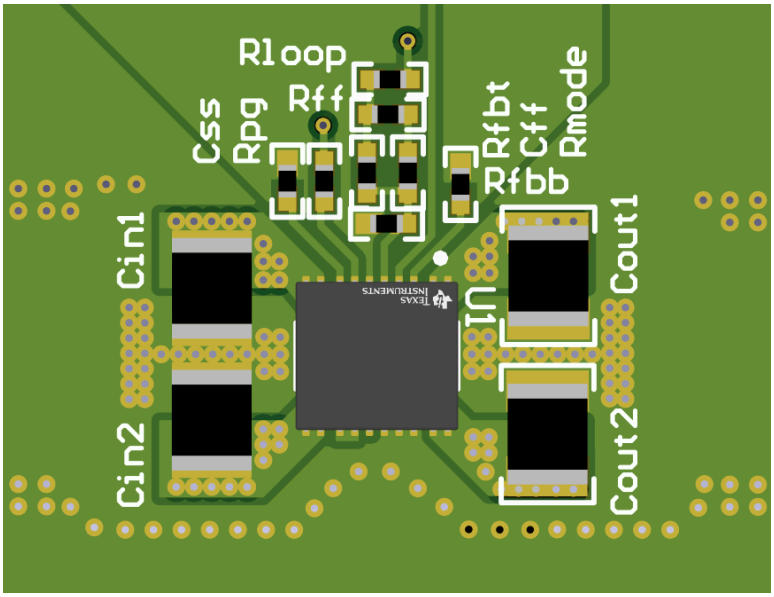


图 7-18. TPSM8683x Layout

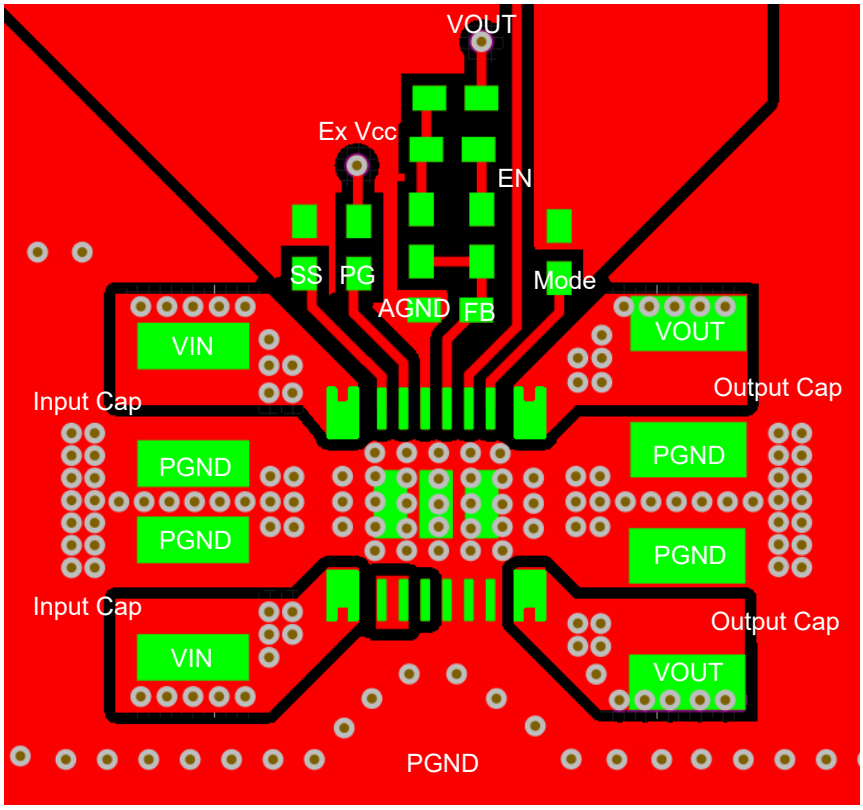


图 7-19. TPSM8683x Top Layer Design

8 Device and Documentation Support

8.1 Device Support

8.1.1 第三方产品免责声明

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPSM86838 Buck Module Evaluation Module* EVM user's guide
- Texas Instruments, *Optimizing Transient Response of Internally Compensated DCDC Converters with Feed-forward Capacitor* application report

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 2023) to Revision B (May 2024)	Page
• 通篇添加了 TPSM86837	1

Changes from Revision * (October 2023) to Revision A (December 2023)	Page
• 将文档状态从“预告信息”更改为“量产数据”	1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM86837RCGR	ACTIVE	B3QFN	RCG	19	1000	RoHS & Green	NIPDAU	Level-3-245C-168 HR	-40 to 150	TPSM86837	Samples
TPSM86838RCGR	ACTIVE	B3QFN	RCG	19	1000	RoHS & Green	NIPDAU	Level-3-245C-168 HR	-40 to 150	TPSM86838	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

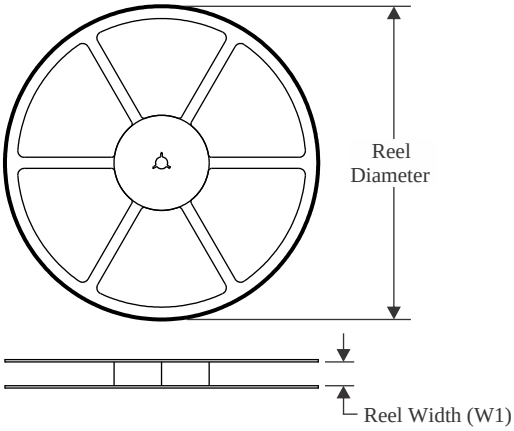
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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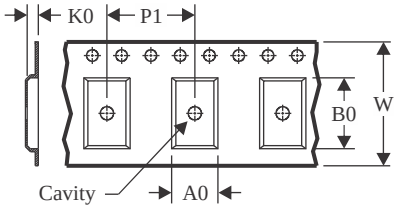
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

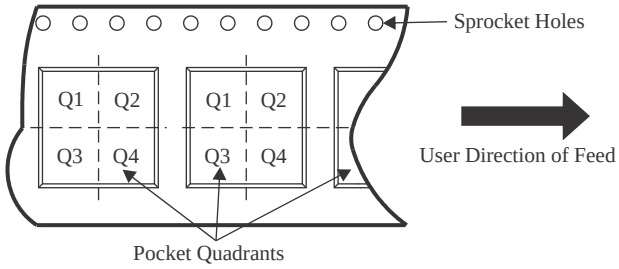


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

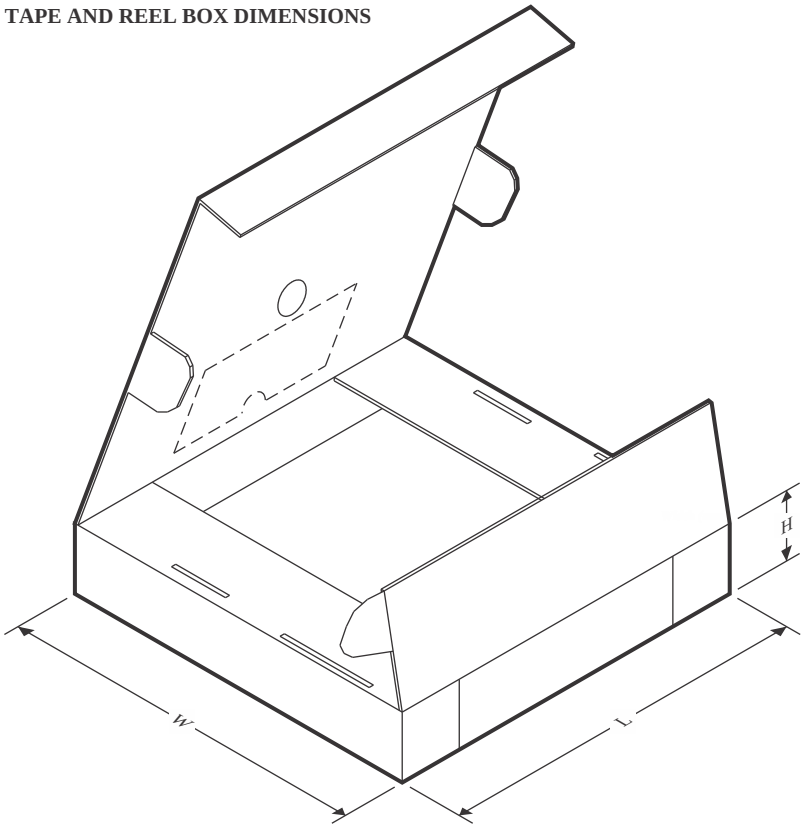
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM86837RCGR	B3QFN	RCG	19	1000	330.0	16.4	5.28	5.78	4.28	8.0	16.0	Q1
TPSM86838RCGR	B3QFN	RCG	19	1000	330.0	16.4	5.28	5.78	4.28	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

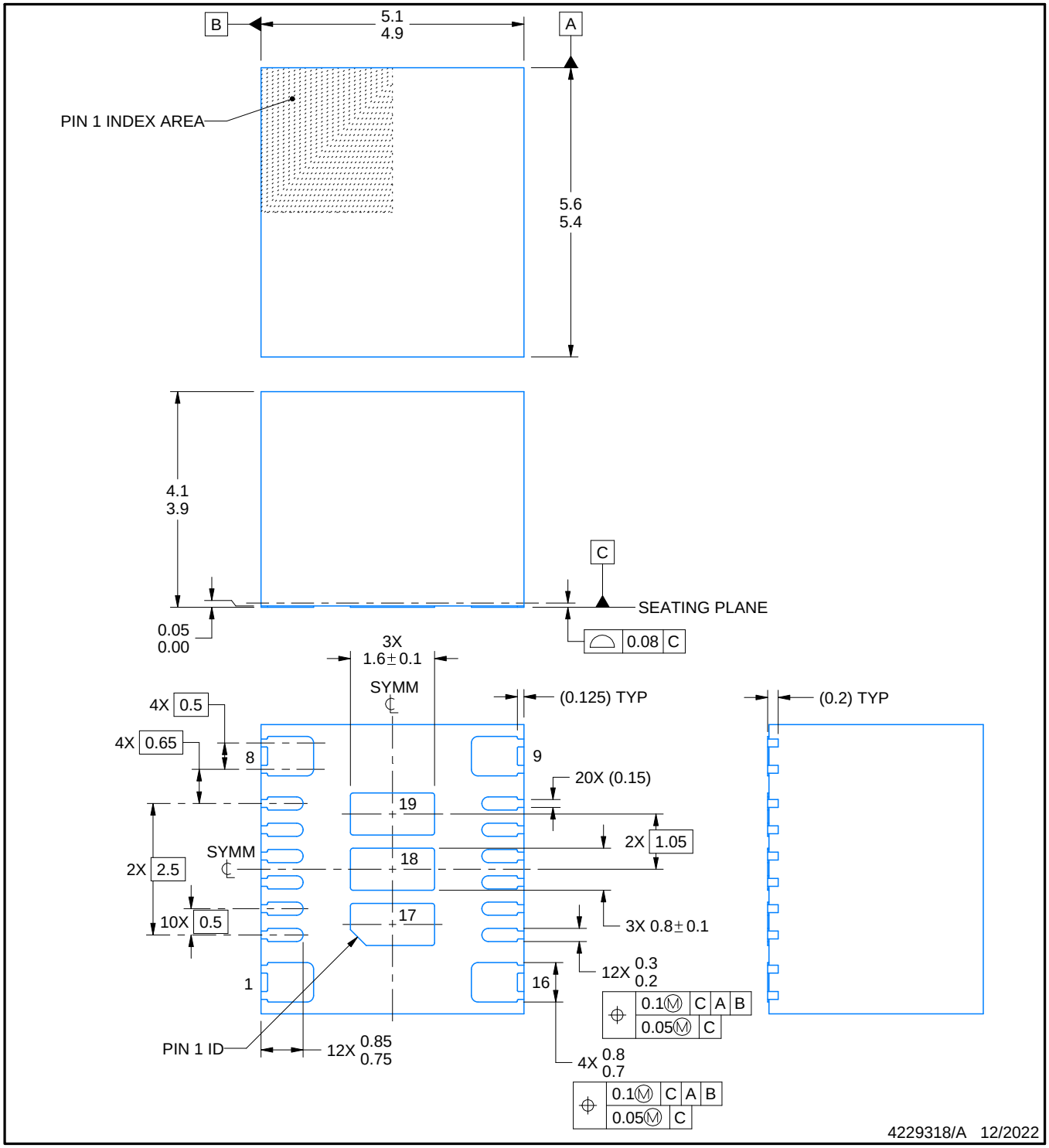
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM86837RCGR	B3QFN	RCG	19	1000	336.0	336.0	48.0
TPSM86838RCGR	B3QFN	RCG	19	1000	336.0	336.0	48.0

PACKAGE OUTLINE

RCG0019A

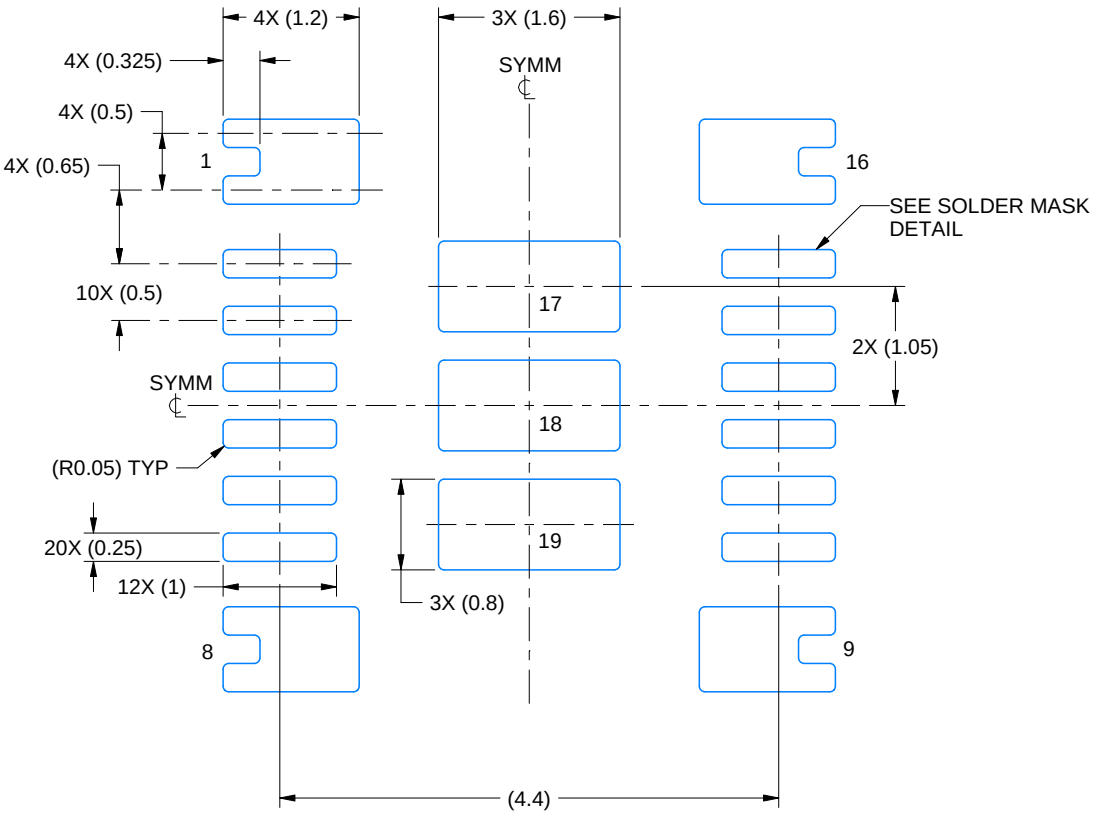
B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

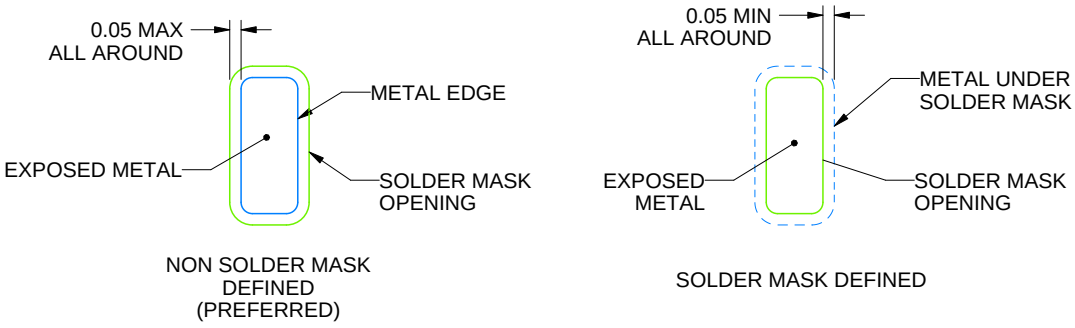


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS
NOT TO SCALE

4229318/A 12/2022

NOTES: (continued)

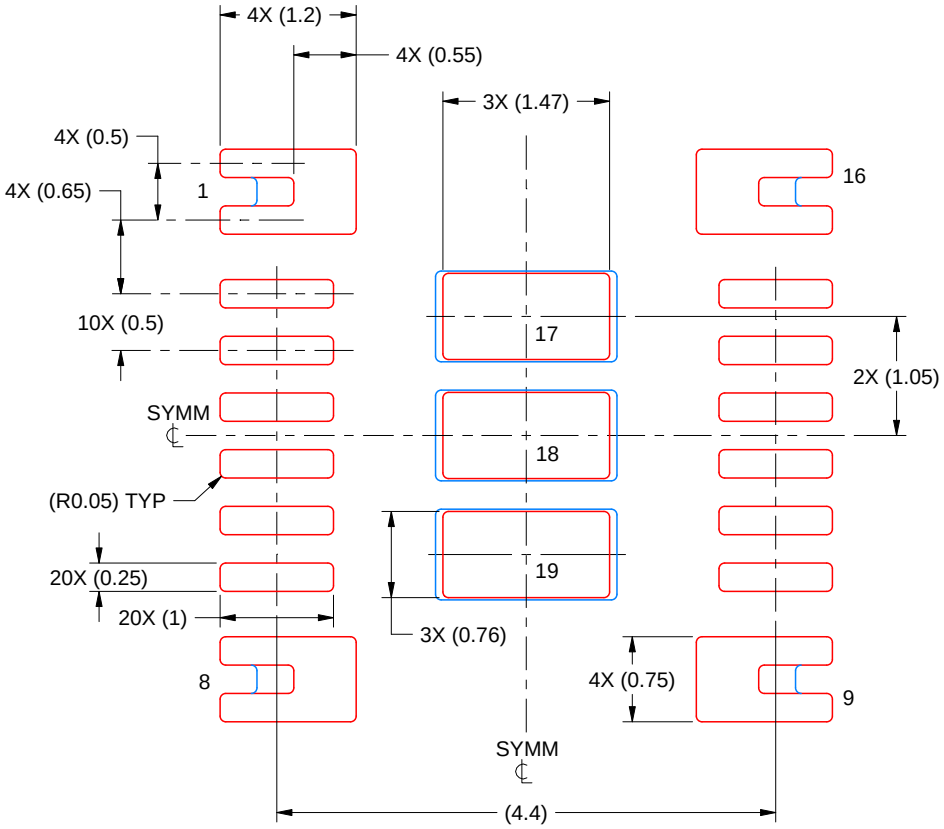
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RCG0019A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 8, 9 & 16: 90%
PADS 17, 18 & 19: 82%

4229318/A 12/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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