具有四个引脚可选增益设置的 INA225-Q1 AEC-Q100、36V 双向电流检测放大器

1 特性

- 符合 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 +125°C
  - HBM ESD 分类等级 2
  - CDM ESD 分类等级 C4B
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 宽共模范围：0V 至 36V
- 失调电压：±150μV（上限，所有增益）
- 失调电压漂移：0.5μV/°C（上限）
- 温度范围内的增益精度（上限）：
  - 25V/V、50V/V：±0.15%
  - 100V/V±0.2%
  - 200V/V：±0.3%
  - 10ppm/°C 增益漂移
- 带宽：250kHz（增益 = 25V/V）
- 可编程增益：
  - G1 = 25V/V
  - G2 = 50V/V
  - G3 = 100V/V
  - G4 = 200V/V
- 静态电流：350μA（最大值）
- 封装：8 引脚 VSSOP

2 应用

- 汽车照明
- 车身控制模块
- 电机控制
- 阀门控制
- 仪表组
- 中央控制模块

3 说明

INA225-Q1 是一款电压输出、电流感测放大器，能够在 0V 至 36V 共模电压上感测电流感测电阻的压降，并且与电源电压无关。此器件是一款双向、电流分流监控器，允许外部基准用于测量双向流入电流感测电阻器的电流。

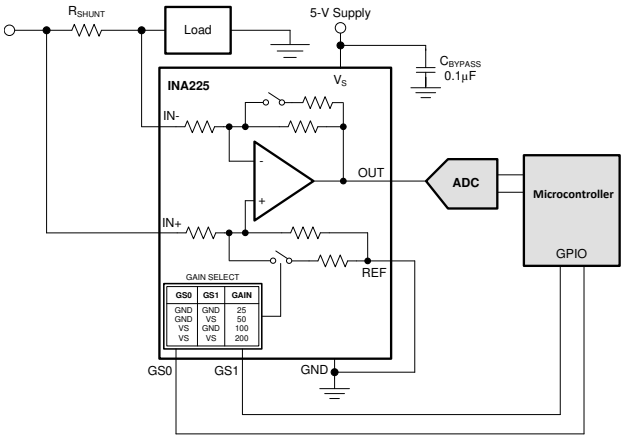
使用两个增益选择端子（GS0 和 GS1）可选择四个离散增益电平，从而对 25V/V、50V/V、100V/V 和 200V/V 增益进行编程。使用低偏移、零漂移架构和精密增益值，可在分流器上的压降上限低至 10mV 满量程的情况下进行电流检测，同时在整个工作温度范围内保持非常高精度的测量水准。

此器件由一个 +2.7V 至 +36V 的单电源供电，最大电源电流为 350μA。此器件的额定扩展工作温度范围为 -40 °C 至 +125 °C，采用超薄小外形尺寸封装 (VSSOP)-8 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
INA225-Q1	VSSOP (8)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



典型应用

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4 Revision History

Changes from Revision * (February 2015) to Revision A (March 2021) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 向 *特性* 添加了“功能安全”要点 1
- 为重要图形添加了标题 1
- Added 25 kΩ value to R_{INT} in *Input Filtering* 16

5 Pin Configuration and Functions

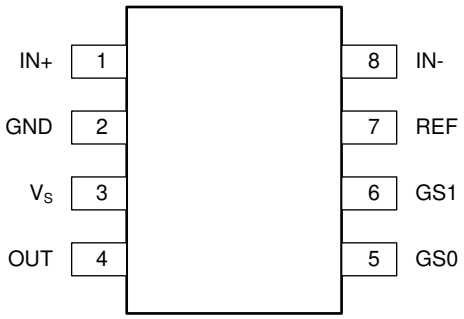


图 5-1. DGK Package VSSOP-8 (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN+	Analog input	Connect to supply side of shunt resistor.
2	GND	Analog	Ground
3	V_S	Analog	Power supply, 2.7 V to 36 V
4	OUT	Analog output	Output voltage
5	GS0	Digital input	Gain select. Connect to V_S or GND. 表 7-3 lists terminal settings and the corresponding gain value.
6	GS1	Digital input	Gain select. Connect to V_S or GND. 表 7-3 lists terminal settings and the corresponding gain value.
7	REF	Analog input	Reference voltage, 0 V to V_S
8	IN–	Analog input	Connect to load side of shunt resistor.

6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
Supply voltage			+40	V
Analog inputs, V_{IN+}, V_{IN-} (2)	Differential (V_{IN+}) – (V_{IN-})	–40	+40	V
	Common-mode(3)	GND – 0.3	+40	V
REF, GS0, and GS1 inputs		GND – 0.3	(V_S) + 0.3	V
Output		GND – 0.3	(V_S) + 0.3	V
Temperature	Operating, T_A	–55	+150	°C
	Junction, T_J		+150	°C
	Storage, T_{stg}	–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and V_{IN-} are the voltages at the IN+ and IN– terminals, respectively.
(3) Input voltage at any terminal may exceed the voltage shown if the current at that terminal is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Operating supply voltage		5		V
T_A	Operating free-air temperature	–40		+125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA225-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	84.7	
ψ_{JT}	Junction-to-top characterization parameter	6.5	
ψ_{JB}	Junction-to-board characterization parameter	83.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = +25 °C, $V_{SENSE} = V_{IN+} – V_{IN–}$, V_S = +5 V, V_{IN+} = 12 V, and $V_{REF} = V_S / 2$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{CM}	Common-mode input range	T_A = –40 °C to +125 °C	0		36	V
CMR	Common-mode rejection	V_{IN+} = 0 V to +36 V, V_{SENSE} = 0 mV, T_A = –40 °C to +125 °C	95	105		dB
V_{OS}	Offset voltage, RTI(1)	V_{SENSE} = 0 mV		±75	±150	µV
dV_{OS}/dT	RTI vs. temperature	T_A = –40 °C to +125 °C		0.2	0.5	µV/°C
PSRR	Power-supply rejection ratio	V_{SENSE} = 0 mV, V_{REF} = 2.5 V, V_S = 2.7 V to 36 V		±0.1	±1	µV/V
I_B	Input bias current	V_{SENSE} = 0 mV	55	72	85	µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV		±0.5		µA
V_{REF}	Reference input range	T_A = –40 °C to +125 °C	0		V_S	V
OUTPUT						
G	Gain			25, 50, 100, 200		V/V
E_G	Gain error	Gain = 25 V/V and 50 V/V, V_{OUT} = 0.5 V to V_S – 0.5 V, T_A = –40 °C to +125 °C		±0.05%	±0.15%	
		Gain = 100 V/V, V_{OUT} = 0.5 V to V_S – 0.5 V, T_A = –40 °C to +125 °C		±0.1%	±0.2%	
		Gain = 200 V/V, V_{OUT} = 0.5 V to V_S – 0.5 V, T_A = –40 °C to +125 °C		±0.1%	±0.3%	
	Gain error vs. temperature	G = 25 V/V, 50 V/V, 100 V/V, T_A = –40 °C to +125 °C		3	10	ppm/°C
		G = 200 V/V, T_A = –40 °C to +125 °C		5	15	
	Nonlinearity error	V_{OUT} = 0.5 V to V_S – 0.5 V		±0.01%		
	Maximum capacitive load	No sustained oscillation		1		nF
VOLTAGE OUTPUT(2)						
	Swing to V_S power-supply rail	R_L = 10 kΩ to GND, T_A = –40 °C to +125 °C		V_S – 0.05	V_S – 0.2	V
	Swing to GND(3)	V_{REF} = V_S / 2, all gains, R_L = 10 kΩ to GND, T_A = –40 °C to +125 °C		V_{GND} + 5	V_{GND} + 10	mV
		V_{REF} = GND, gain = 25 V/V, R_L = 10 kΩ to GND, T_A = –40 °C to +125 °C		V_{GND} + 7		mV
		V_{REF} = GND, gain = 50 V/V, R_L = 10 kΩ to GND, T_A = –40 °C to +125 °C		V_{GND} + 15		mV
		V_{REF} = GND, gain = 100 V/V, R_L = 10 kΩ to GND, T_A = –40 °C to +125 °C		V_{GND} + 30		mV
		V_{REF} = GND, gain = 200 V/V, R_L = 10 kΩ to GND, T_A = –40 °C to +125 °C		V_{GND} + 60		mV
FREQUENCY RESPONSE						
BW	Bandwidth	Gain = 25 V/V, C_{LOAD} = 10 pF		250		kHz
		Gain = 50 V/V, C_{LOAD} = 10 pF		200		kHz
		Gain = 100 V/V, C_{LOAD} = 10 pF		125		kHz
		Gain = 200 V/V, C_{LOAD} = 10 pF		70		kHz
SR	Slew rate			0.4		V/µs
NOISE, RTI(1)						
	Voltage noise density			50		nV/√Hz

At T_A = +25 °C, V_{SENSE} = V_{IN+} – $V_{IN–}$, V_S = +5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT						
C_i	Input capacitance			3		pF
	Leakage input current	$0 \le V_{IN} \le V_S$		1	2	µA
V_{IL}	Low-level input logic level		0		0.6	V
V_{IH}	High-level input logic level		2		V_S	V
POWER SUPPLY						
V_S	Operating voltage range	T_A = –40 °C to +125 °C	+2.7		+36	V
I_Q	Quiescent current	V_{SENSE} = 0 mV		300	350	µA
	I_Q over temperature	T_A = –40 °C to +125 °C			375	µA
TEMPERATURE RANGE						
	Specified range		–40		+125	°C
	Operating range		–55		+150	°C

(1) RTI = referred-to-input.
(2) See Typical Characteristic curve, *Output Voltage Swing vs. Output Current* (图 6-10).
(3) See Typical Characteristic curve, *Unidirectional Output Voltage Swing vs. Temperature* (图 6-14).

6.6 Typical Characteristics

At T_A = +25 °C, V_S = +5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, unless otherwise noted.

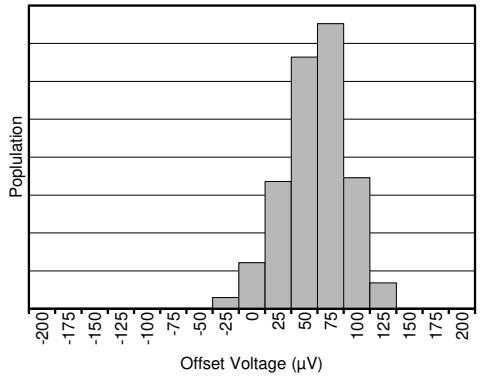


图 6-1. Input Offset Voltage Production Distribution

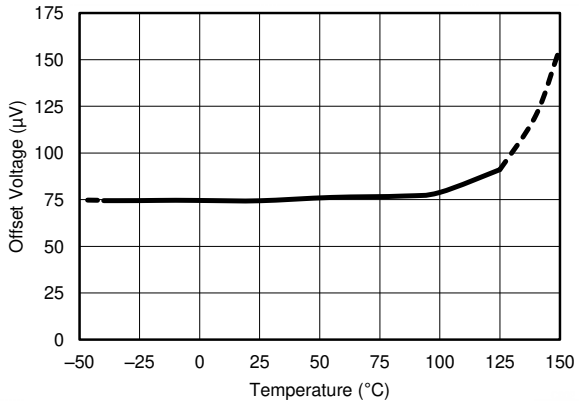


图 6-2. Input Offset Voltage vs. Temperature

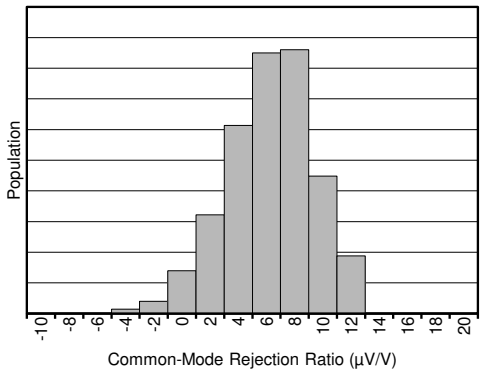


图 6-3. Common-Mode Rejection Production Distribution

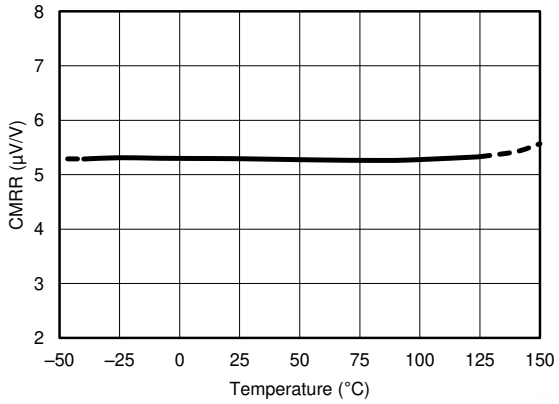


图 6-4. Common-Mode Rejection Ratio vs. Temperature

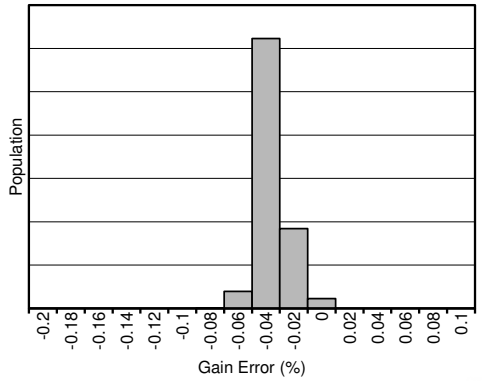


图 6-5. Gain Error Production Distribution (Gain = 25 V/V)

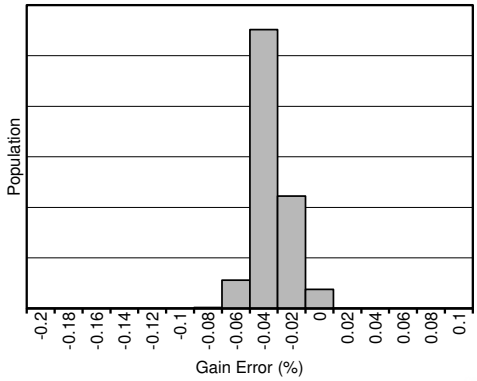


图 6-6. Gain Error Production Distribution (Gain = 50 V/V)

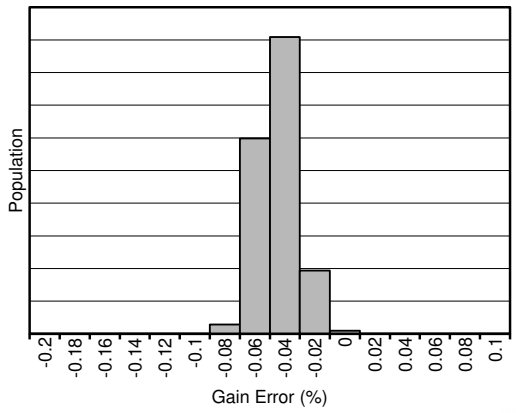


图 6-7. Gain Error Production Distribution (Gain = 100 V/V)

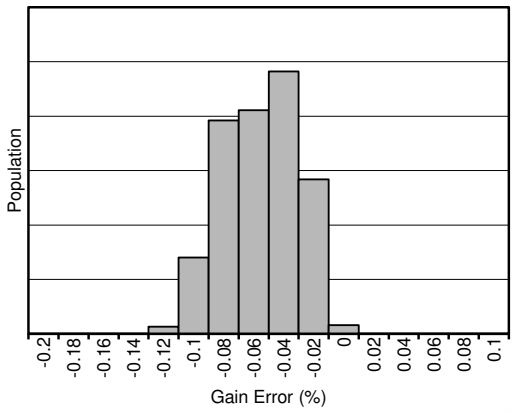


图 6-8. Gain Error Production Distribution (Gain = 200 V/V)

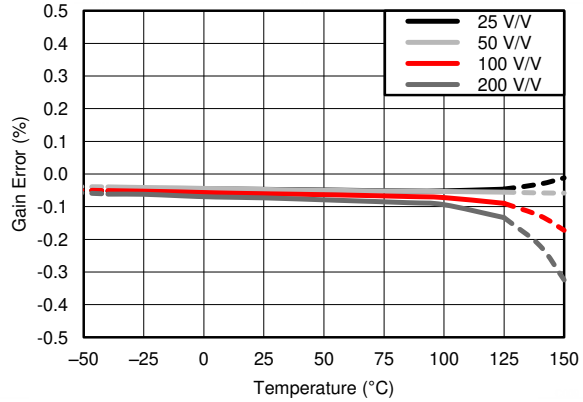
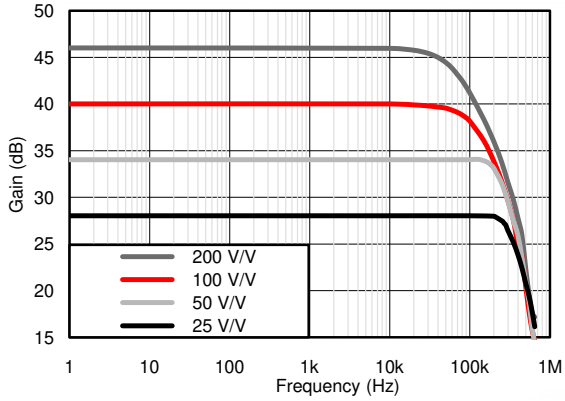
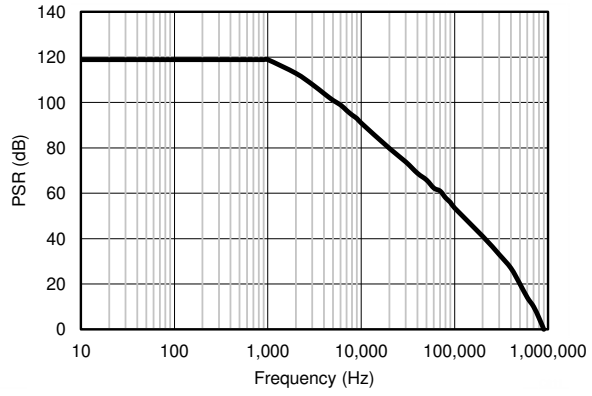


图 6-9. Gain Error vs. Temperature



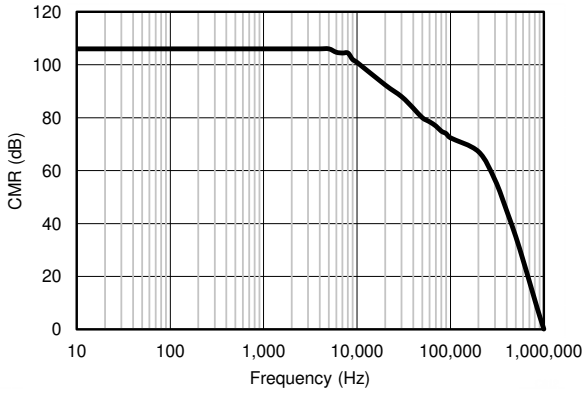
V_{CM} = 0 V V_{SENSE} = 15 mV_{PP}

图 6-10. Gain vs. Frequency



V_{CM} = 0 V V_{REF} = 2.5 V V_{SENSE} = 0 mV, Shorted
V_S = 5 V + 250-mV Sine Disturbance

图 6-11. Power-Supply Rejection Ratio vs. Frequency



V_S = 5 V V_{REF} = 2.5 V V_{SENSE} = 0 mV, Shorted
V_{CM} = 1-V Sine Wave

图 6-12. Common-Mode Rejection Ratio vs. Frequency

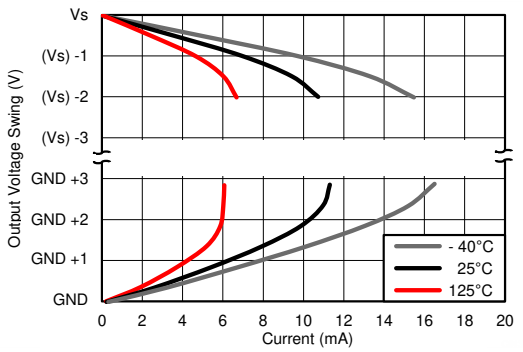
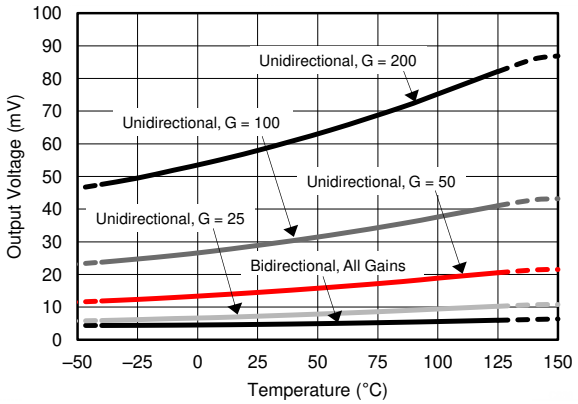


图 6-13. Output Voltage Swing vs Output Current



Unidirectional, REF = GND　　Bidirectional, REF > GND

图 6-14. Unidirectional Output Voltage Swing vs. Temperature

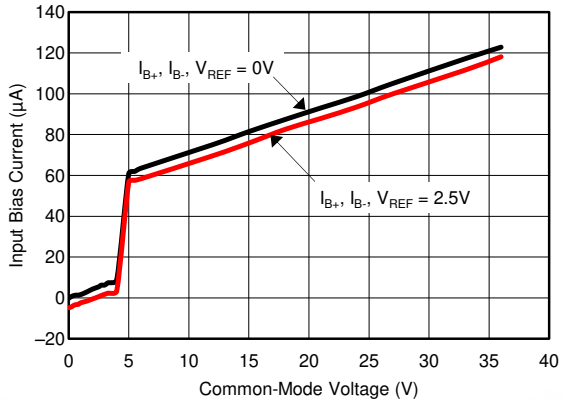


图 6-15. Input Bias Current vs. Common-Mode Voltage (Supply Voltage = +5 V)

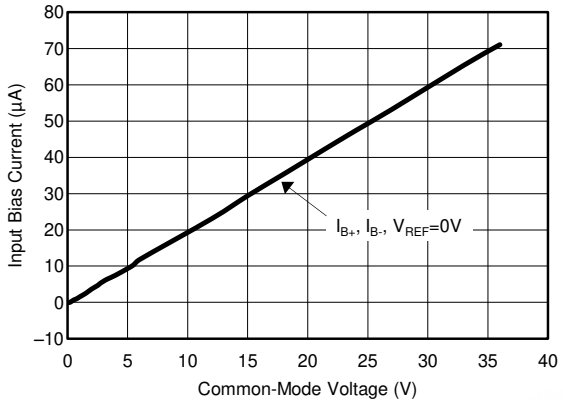
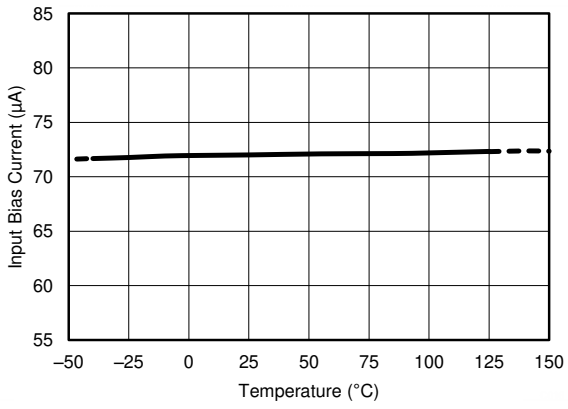


图 6-16. Input Bias Current vs. Common-Mode Voltage (Supply Voltage = 0 V, Shutdown)



V_S = 5 V　　V_{CM} = 12 V

图 6-17. Input Bias Current vs. Temperature

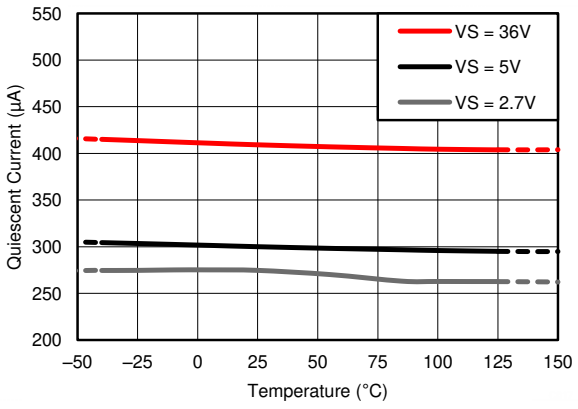


图 6-18. Quiescent Current vs. Temperature

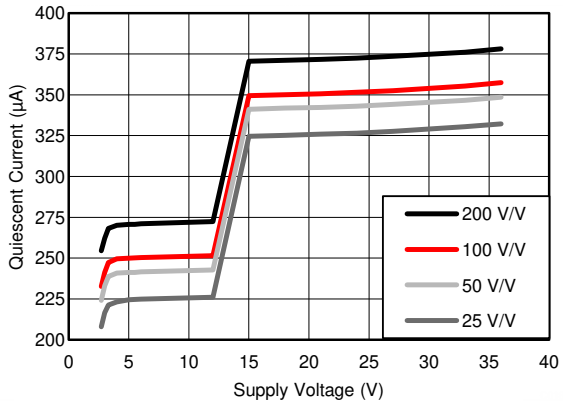
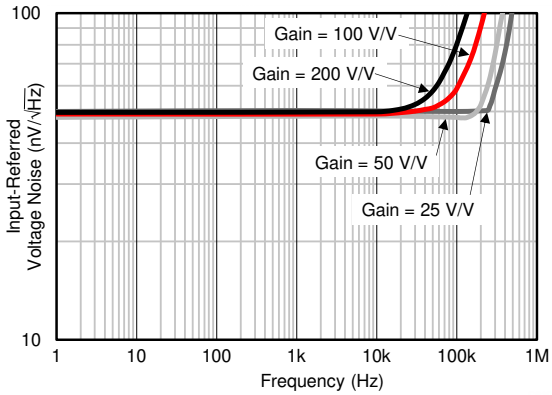
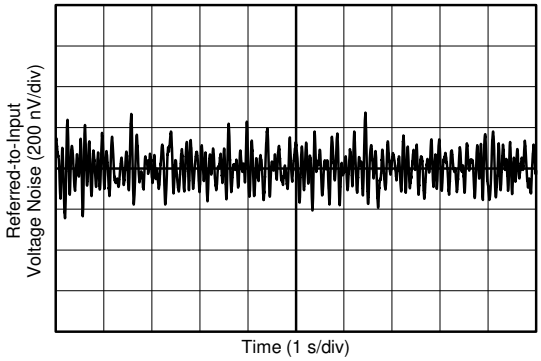


图 6-19. Quiescent Current vs. Supply Voltage



V_S = ± 2.5 V V_{REF} = 0 V V_{SENSE} = 0 mV, Shorted

图 6-20. Input-Referred Voltage Noise vs. Frequency



V_S = ± 2.5 V V_{CM} = 0 V V_{SENSE} = 0 mV, Shorted

图 6-21. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

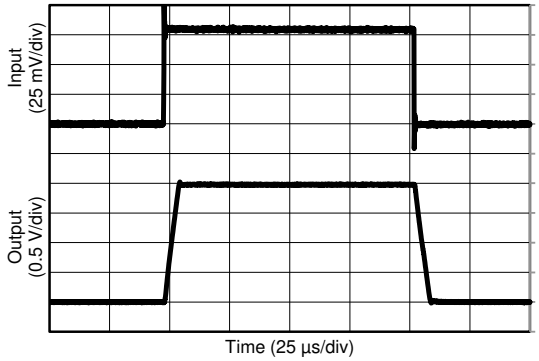


图 6-22. Step Response (Gain = 25 V/V, 2-V_{PP} Output Step)

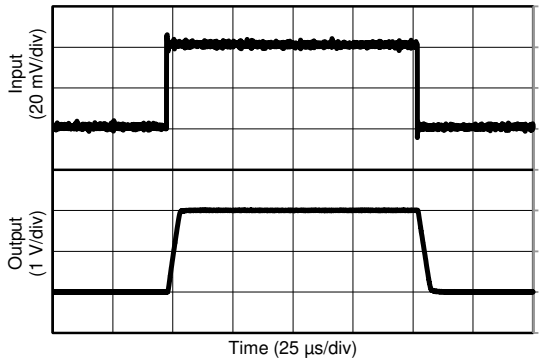


图 6-23. Step Response (Gain = 50 V/V, 2-V_{PP} Output Step)

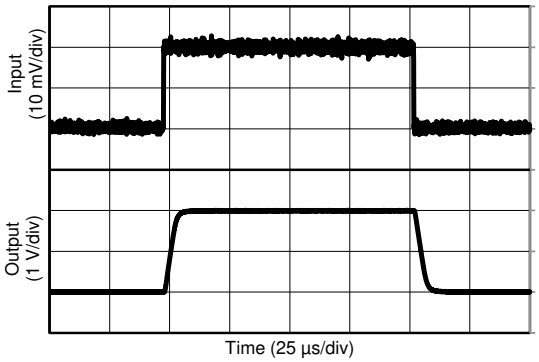


图 6-24. Step Response (Gain = 100 V/V, 2-V_{PP} Output Step)

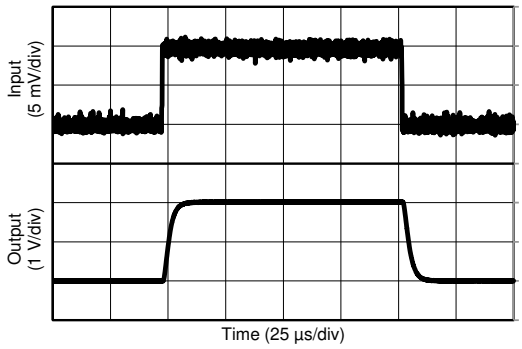
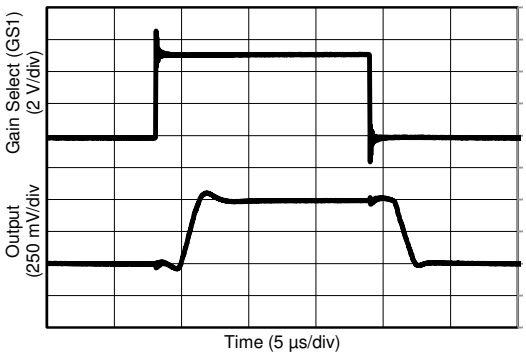
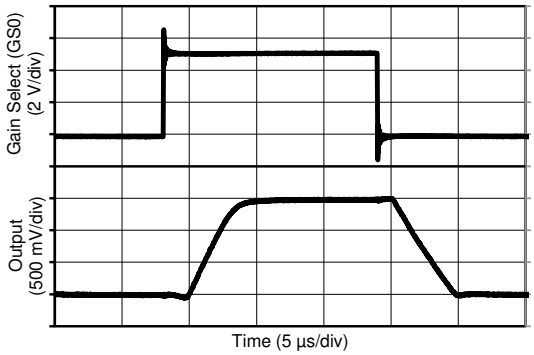


图 6-25. Step Response (Gain = 200 V/V, 2-V_{PP} Output Step)



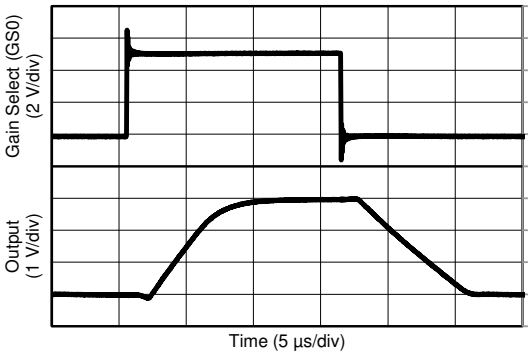
V_{DIFF} = 20 mV V_{OUT} at 25-V/V Gain = 500 mV
V_{OUT} at 50-V/V Gain = 1 V

图 6-26. Gain Change Output Response (Gain = 25 V/V to 50 V/V)



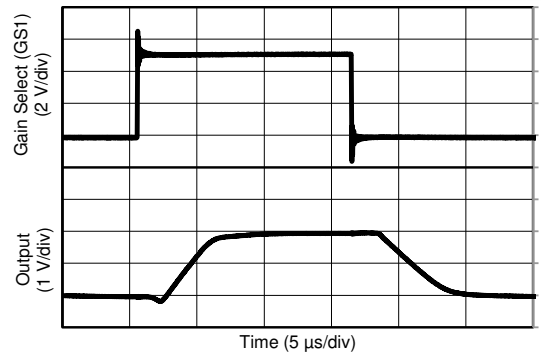
V_{DIFF} = 20 mV V_{OUT} at 25-V/V Gain = 500 mV
V_{OUT} at 100-V/V Gain = 2 V

图 6-27. Gain Change Output Response (Gain = 25 V/V to 100 V/V)



V_{DIFF} = 20 mV V_{OUT} at 50-V/V Gain = 1 V
V_{OUT} at 200-V/V Gain = 4 V

图 6-28. Gain Change Output Response (Gain = 50 V/V to 200 V/V)



V_{DIFF} = 20 mV V_{OUT} at 100-V/V Gain = 2 V
V_{OUT} at 200-V/V Gain = 4 V

图 6-29. Gain Change Output Response (Gain = 100 V/V to 200 V/V)

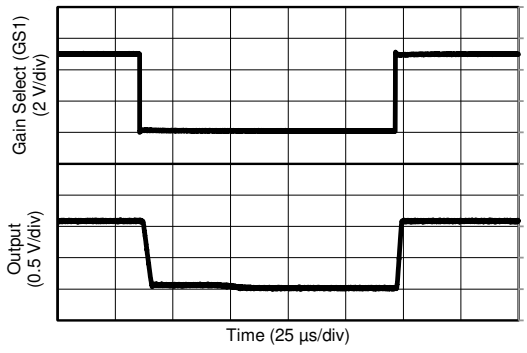


图 6-30. Gain Change Output Response From Saturation (Gain = 50 V/V to 25 V/V)

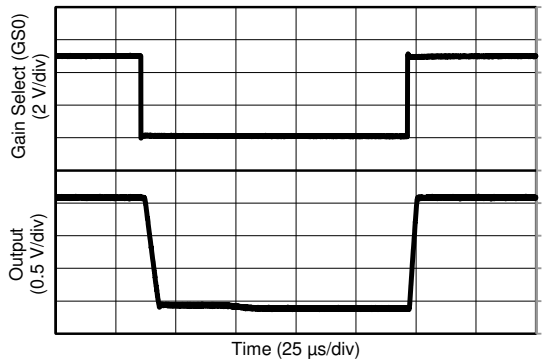


图 6-31. Gain Change Output Response From Saturation (Gain = 100 V/V to 25 V/V)

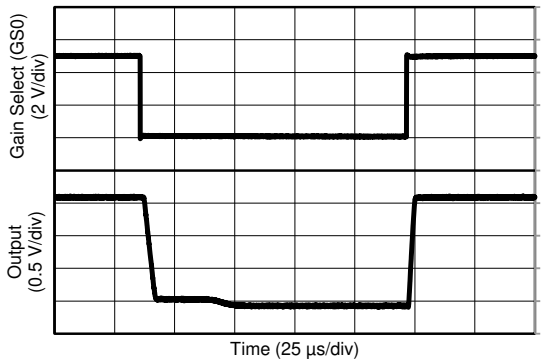


图 6-32. Gain Change Output Response From Saturation (Gain = 200 V/V to 50 V/V)

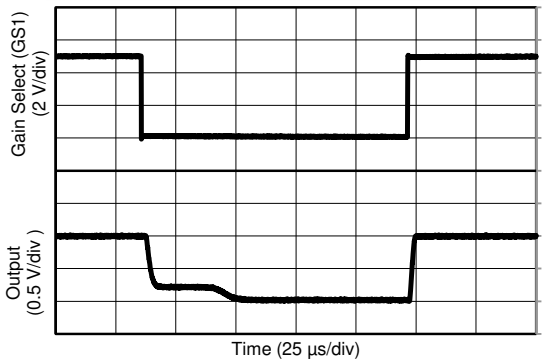


图 6-33. Gain Change Output Response From Saturation (Gain = 200 V/V to 100 V/V)

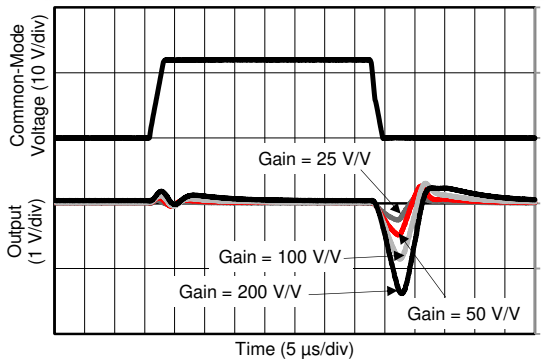


图 6-34. Common-Mode Voltage Transient Response

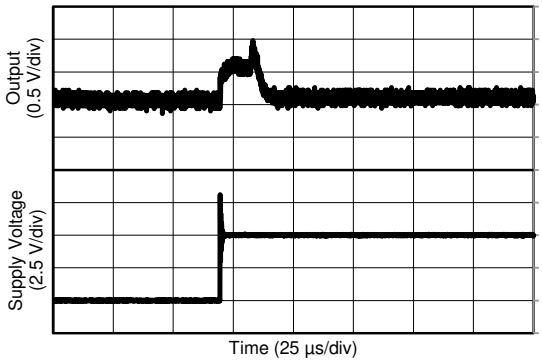


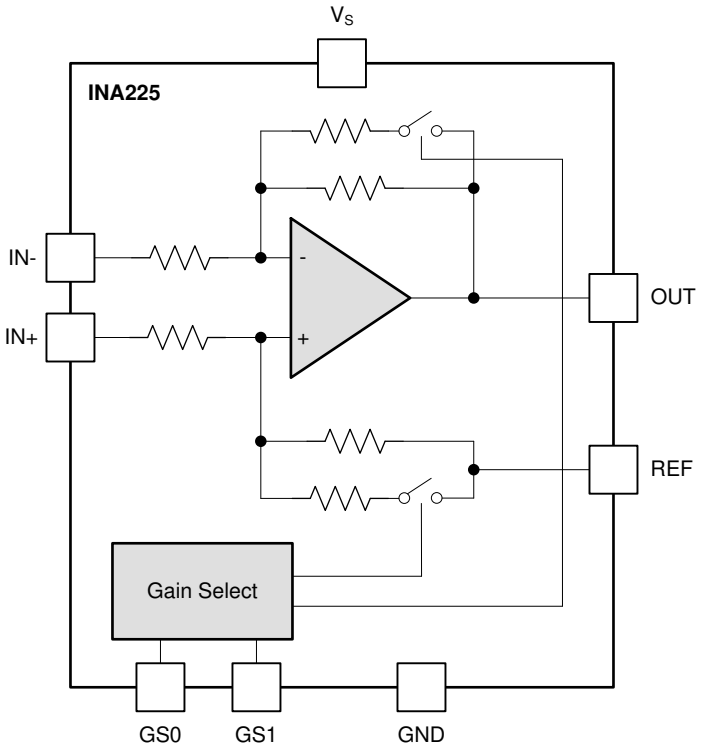
图 6-35. Start-Up Response

7 Detailed Description

7.1 Overview

The INA225-Q1 is a 36-V, common-mode, zero-drift topology, current-sensing amplifier. This device features a significantly higher signal bandwidth than most comparable precision, current-sensing amplifiers, reaching up to 125 kHz at a gain of 100 V/V. A very useful feature present in the device is the built-in programmable gain selection. To increase design flexibility with the device, a programmable gain feature is added that allows changing device gain during operation in order to accurately monitor wider dynamic input signal ranges. Four discrete gain levels (25 V/V, 50 V/V, 100 V/V, and 200 V/V) are available in the device and are selected using the two gain-select terminals, GS0 and GS1.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Selecting A Shunt Resistor

The device measures the differential voltage developed across a resistor when current flows through it. This resistor is commonly referred to as a *current-sensing resistor* or a *current-shunt resistor*, with each term commonly used interchangeably. The flexible design of the device allows a wide range of input signals to be measured across this current-sensing resistor.

Selecting the value of this current-sensing resistor is based primarily on two factors: the required accuracy of the current measurement and the allowable power dissipation across the resistor. The larger the voltage developed across this resistor the more accurate of a measurement that can be made because of the fixed internal amplifier errors. These fixed internal amplifier errors, which are dominated by the internal offset voltage of the device, result in a larger measurement uncertainty when the input signal gets smaller. When the input signal gets larger, the measurement uncertainty is reduced because the fixed errors become a smaller percentage of the signal being measured.

A system design trade-off for improving the measurement accuracy through the use of the larger input signals is the increase in the power dissipated across the current-sensing resistor. Increasing the value of the current-shunt resistor increases the differential voltage developed across the resistor when current passes through it. However, the power that is then dissipated across this component also increases. Decreasing the value of

the current-shunt resistor value reduces the power dissipation requirements of the resistor, but increases the measurement errors resulting from the decreasing input signal. Finding the optimal value for the shunt resistor requires factoring both the accuracy requirement of the application and allowable power dissipation into the selection of the component. An increasing amount of very low ohmic value resistors are becoming available with values reaching down to 200 µΩ with power dissipations of up to 5 W, thus enabling very large currents to be accurately monitored using sensing resistors.

The maximum value for the current-sensing resistor that can be chosen is based on the full-scale current to be measured, the full-scale input range of the circuitry following the device, and the device gain selected. The minimum value for the current-sensing resistor is typically a design-based decision because maximizing the input range of the circuitry following the device is commonly preferred. Full-scale output signals that are significantly less than the full input range of the circuitry following the device output can limit the ability of the system to exercise the full dynamic range of system control based on the current measurement.

7.3.1.1 Selecting A Current-Sense Resistor Example

The example in 表 7-1 is based on a set of application characteristics, including a 10-A full-scale current range and a 4-V full-scale output requirement. The calculations for selecting a current-sensing resistor of an appropriate value are shown in 表 7-1.

表 7-1. Calculating the Current-Sense Resistor, R_{SENSE}

PARAMETER		EQUATION	RESULT
I_{MAX}	Full-scale current		10 A
V_{OUT}	Full-scale output voltage		4 V
Gain	Gain selected	Initial selection based on default gain setting.	25 V/V
V_{DIFF}	Ideal maximum differential input voltage	$V_{Diff} = V_{OUT} / Gain$	160 mV
R_{SHUNT}	Shunt resistor value	$R_{SHUNT} = V_{Diff} / I_{MAX}$	16 mΩ
P_{RSENSE}	Current-sense resistor power dissipation	$R_{SENSE} \times I_{MAX}^2$	1.6 W
V_{OS} Error	Offset voltage error	$(V_{OS} / V_{DIFF}) \times 100$	0.094%

7.3.1.2 Optimizing Power Dissipation versus Measurement Accuracy

The example shown in 表 7-1 results in a maximum current-sensing resistor value of 16 mΩ to develop the 160 mV required to achieve the 4-V full-scale output with the gain set to 25 V/V. The power dissipated across this 16-mΩ resistor at the 10-A current level is 1.6 W, which is a fairly high power dissipation for this component. Adjusting the device gain allows alternate current-sense resistor values to be selected to ease the power dissipation requirement of this component.

Changing the gain setting from 25 V/V to 100 V/V, as shown in 表 7-2, decreases the maximum differential input voltage from 160 mV down to 40 mV, thus requiring only a 4-mΩ current-sensing resistor to achieve the 4-V output at the 10-A current level. The power dissipated across this resistor at the 10-A current level is 400 mW, significantly increasing the availability of component options to select from.

The increase in gain by a factor of four reduces the power dissipation requirement of the current-sensing resistor by this same factor of four. However, with this smaller full-scale signal, the measurement uncertainty resulting from the device fixed input offset voltage increases by the same factor of four. The measurement error resulting from the device input offset voltage is approximately 0.1% at the 160-mV full-scale input signal for the 25-V/V gain setting. Increasing the gain to 100 V/V and decreasing the full-scale input signal to 40 mV increases the offset induced measurement error to 0.38%.

表 7-2. Accuracy and RSENSE Power Dissipation vs. Gain Setting

PARAMETER		EQUATION	RESULT
I_{MAX}	Full-scale current		10 A
V_{OUT}	Full-scale output voltage		4 V
Gain	Gain selected		100 V/V
V_{DIFF}	Ideal maximum differential input voltage	$V_{Diff} = V_{OUT} / Gain$	40 mV
R_{SENSE}	Current-sense resistor value	$R_{SENSE} = V_{Diff} / I_{MAX}$	4 mΩ
P_{RSENSE}	Current-sense resistor power dissipation	$R_{SENSE} \times I_{MAX}^2$	0.4 W
V_{OS} Error	Offset voltage error	$(V_{OS} / V_{DIFF}) \times 100$	0.375%

7.3.2 Programmable Gain Select

The device features a terminal-controlled gain selection in determining the device gain setting. Four discrete gain options are available (25 V/V, 50 V/V, 100 V/V, and 200 V/V) on the device and are selected based on the voltage levels applied to the gain-select terminals (GS0 and GS1). These terminals are typically fixed settings for most applications but the programmable gain feature can be used to adjust the gain setting to enable wider dynamic input range monitoring as well as to create an automatic gain control (AGC) network.

表 7-3 shows the corresponding gain values and gain-select terminal values for the device.

表 7-3. Gain Select Settings

GAIN	GS0	GS1
25 V/V	GND	GND
50 V/V	GND	V_S
100 V/V	V_S	GND
200 V/V	V_S	V_S

7.4 Device Functional Modes

7.4.1 Input Filtering

An obvious and straightforward location for filtering is at the device output; however, this location negates the advantage of the low output impedance of the internal buffer. The input then represents the best location for implementing external filtering. 图 7-1 shows the typical implementation of the input filter for the device.

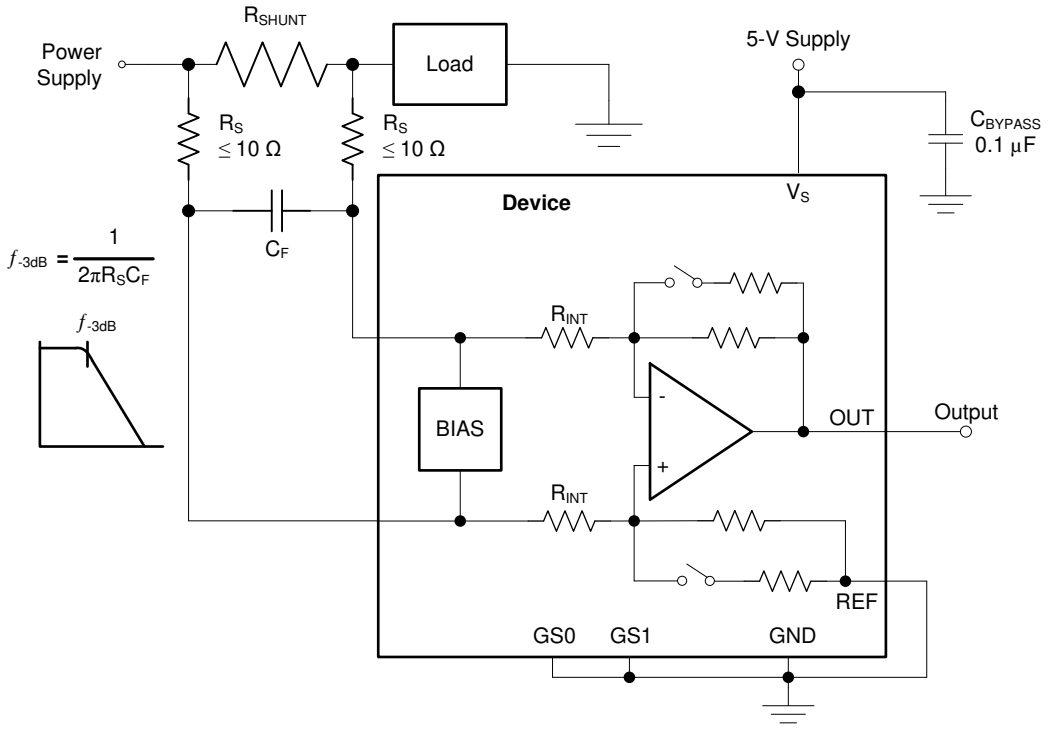


图 7-1. Input Filter

Care must be taken in the selection of the external filter component values because these components can affect device measurement accuracy. Placing external resistance in series with the input terminals creates an additional error so these resistors should be kept as low of a value as possible with a recommended maximum value of
10 Ω or less. Increasing the value of the input filter resistance beyond 10 Ω results in a smaller voltage signal present at the device input terminals than what is developed across the current-sense shunt resistor.

The internal bias network shown in 图 7-1 creates a mismatch in the two input bias current paths when a differential voltage is applied between the input terminals. Under normal conditions, where no external resistance is added to the input paths, this mismatch of input bias currents has little effect on device operation or accuracy. However, when additional external resistance is added (such as for input filtering), the mismatch of input bias currents creates unequal voltage drops across these external components. The mismatched voltages result in a signal reaching the input terminals that is lower in value than the signal developed directly across the current-sensing resistor.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value (R_S) and the internal input resistors (R_{INT} = 25 kΩ). The reduction of the shunt voltage reaching the device input terminals appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance.

The amount of error these external filter resistors introduce into the measurement can be calculated using the simplified gain error factor in 方程式 1, where the gain error factor is calculated with 方程式 2.

$$\text{Gain Error Factor} = \frac{50{,}000}{(41 \times R_S) + 50{,}000} \quad (1)$$

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \quad (2)$$

where:

- R_{INT} is the internal input impedance, and
- R_S is the external series resistance.

For example, using the gain error factor (方程式 1), a 10-Ω series resistance results in a gain error factor of 0.992. The corresponding gain error is then calculated using 方程式 3, resulting in a gain error of approximately 0.81% solely because of the external 10-Ω series resistors. Using 100-Ω filter resistors increases this gain error to approximately 7.58% from these resistors alone.

$$\text{Gain Error (\%)} = 1 - \text{Gain Error Factor} \quad (3)$$

7.4.2 Shutting Down the Device

Although the device does not have a shutdown terminal, the low-power consumption allows for the device to be powered from the output of a logic gate or transistor switch that can turn on and turn off the voltage connected to the device power-supply terminal.

However, in current-shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the device simplified schematic in shutdown mode, as shown in 图 7-2.

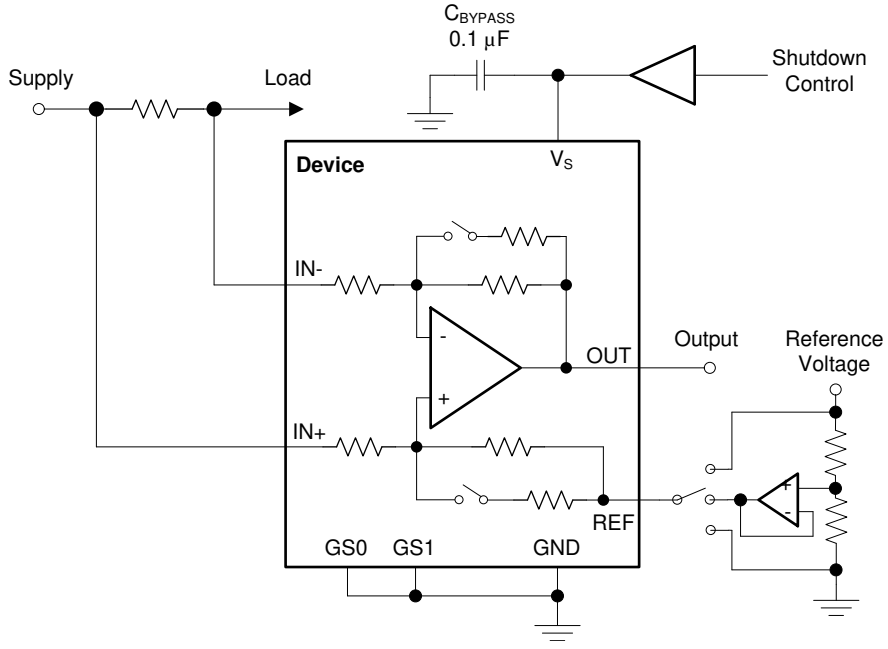


图 7-2. Shutting Down the Device

Note that there is typically a 525-kΩ impedance (from the combination of the 500-kΩ feedback and 25-kΩ input resistors) from each device input to the REF terminal. The amount of current flowing through these terminals depends on the respective configuration. For example, if the REF terminal is grounded, calculating the effect

of the 525-kΩ impedance from the shunt to ground is straightforward. However, if the reference or op amp is powered while the device is shut down, the calculation is direct. Instead of assuming 525 kΩ to ground, assume 525 kΩ to the reference voltage. If the reference or op amp is also shut down, some knowledge of the reference or op amp output impedance under shutdown conditions is required. For instance, if the reference source behaves similar to an open circuit when un-powered, little or no current flows through the 525-kΩ path.

7.4.3 Using the Device with Common-Mode Transients Above 36 V

With a small amount of additional circuitry, the device can be used in circuits subject to transients higher than 36 V (such as automotive applications). Use only zener diodes or zener-type transient absorbers (sometimes referred to as *transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors, as shown in 图 7-3, as a working impedance for the zener. Keeping these resistors as small as possible is preferable, most often around 10 Ω. This value limits the impact on accuracy with the addition of these external components, as described in the *Input Filtering* section. Larger values can be used if necessary with the result having an impact on gain error. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional zener diodes of the lowest power rating available. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

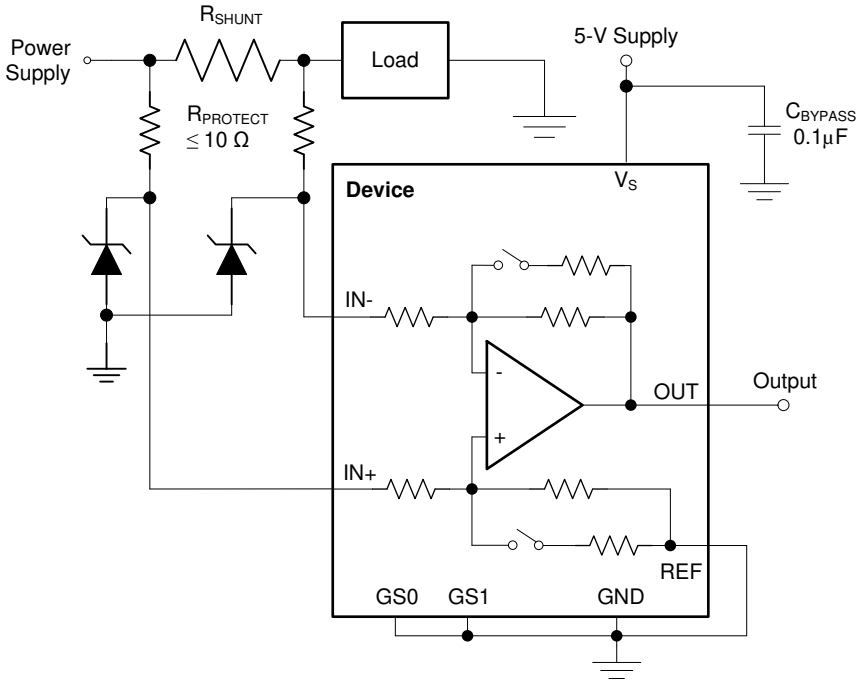


图 7-3. Device Transient Protection

8 Applications and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The INA225-Q1 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference terminal to adjust the functionality of the output signal offers multiple configurations discussed throughout this section.

8.2 Typical Applications

8.2.1 Microcontroller-Configured Gain Selection

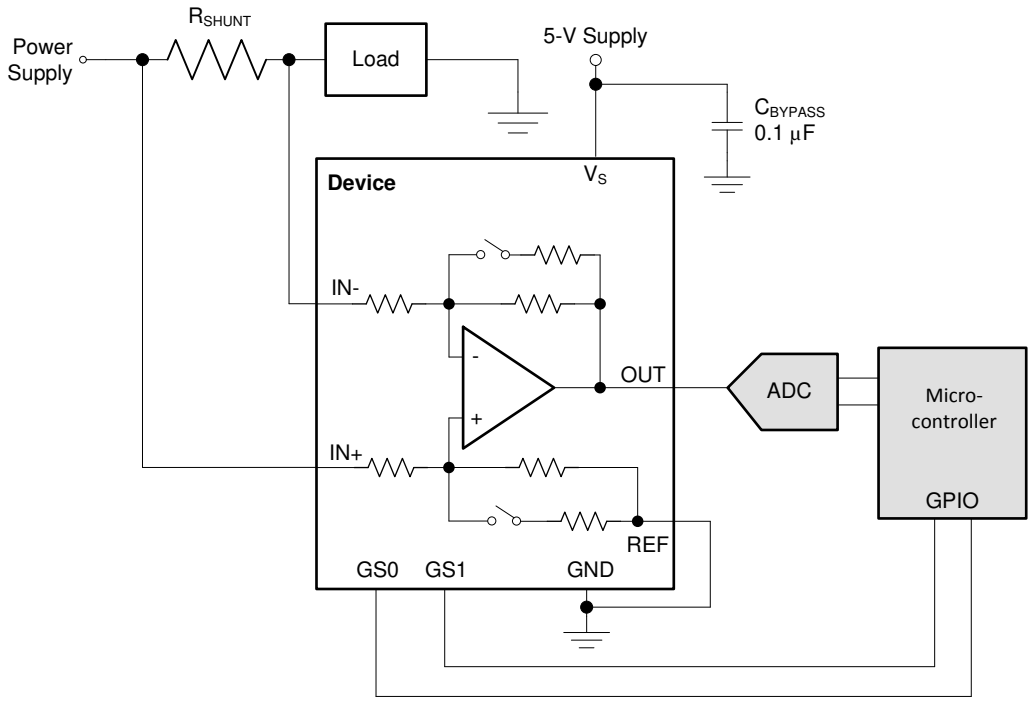


图 8-1. Microcontroller-Configured Gain Selection Schematic

8.2.1.1 Design Requirements

图 8-1 shows the typical implementation of the device interfacing with an analog-to-digital converter (ADC) and microcontroller.

8.2.1.2 Detailed Design Procedure

In this application, the device gain setting is selected and controlled by the microcontroller to ensure the device output is within the linear input range of the ADC. Because the output range of the device under a specific gain setting approaches the linear output range of the INA225-Q1 itself or the linear input range of the ADC, the microcontroller can adjust the device gain setting to ensure the signal remains within both the device and the ADC linear signal range.

8.2.1.3 Application Curve

图 8-2 illustrates how the microcontroller can monitor the ADC measurements to determine if the device gain setting should be adjusted to ensure the output of the device remains within the linear output range as well as the linear input range of the ADC. When the output of the device rises to a level near the desired maximum voltage level, the microcontroller can change the GPIO settings connected to the G0 and G1 gain-select terminals to adjust the device gain setting, thus resulting in the output voltage dropping to a lower output range. When the input current increases, the output voltage increases again to the desired maximum voltage level. The microcontroller can again change the device gain setting to drop the output voltage back to a lower range.

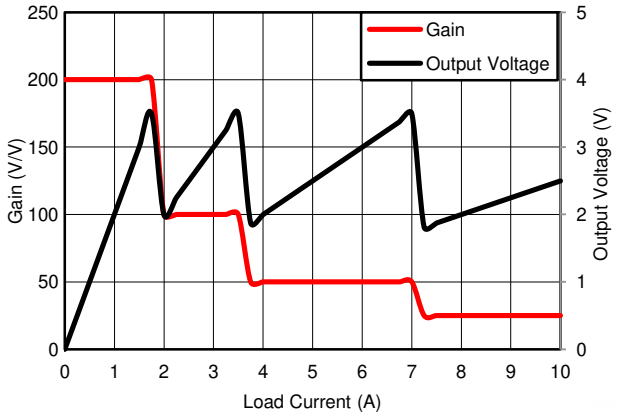


图 8-2. Microcontroller-Configured Gain Selection Response

8.2.2 Unidirectional Operation

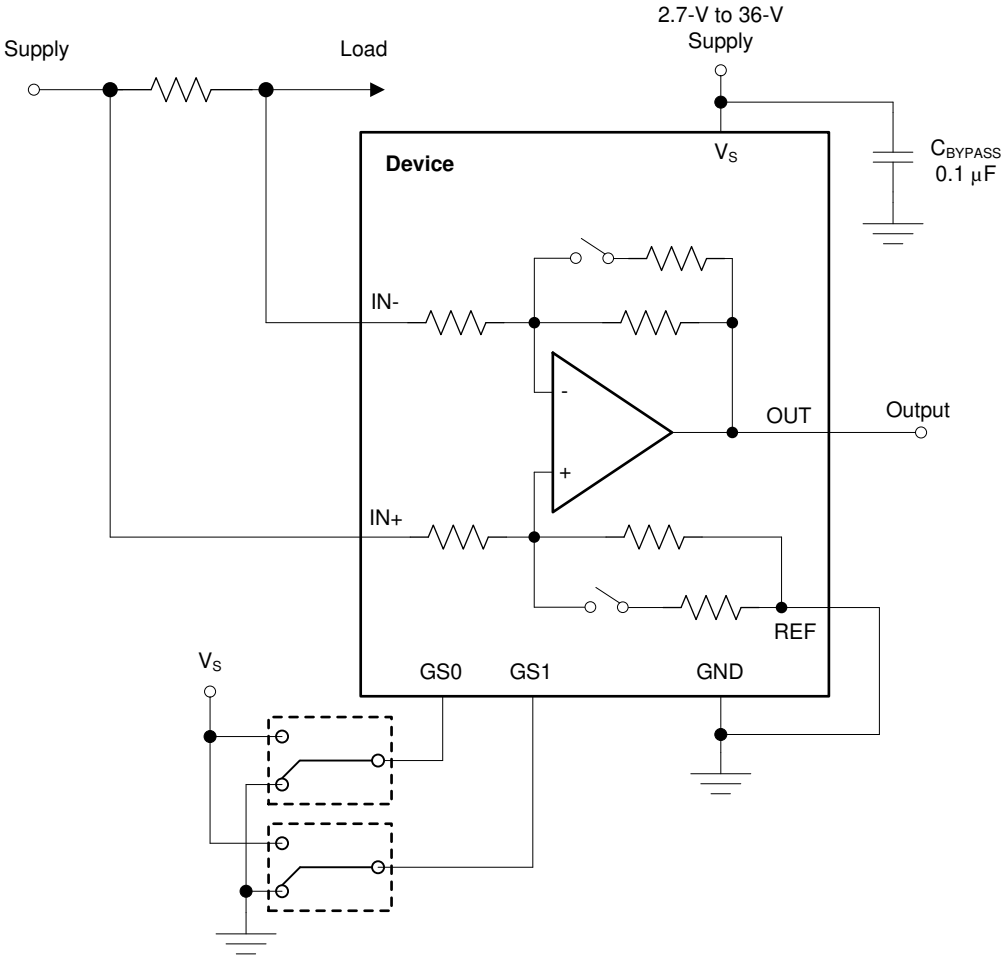


图 8-3. Unidirectional Application Schematic

8.2.2.1 Design Requirements

The device can be configured to monitor current flowing in one direction or in both directions, depending on how the REF terminal is configured. For measuring current in one direction, only the REF terminal is typically connected to ground as shown in 图 8-3. With the REF terminal connected to ground, the output is low with no differential input signal applied. When the input signal increases, the output voltage at the OUT terminal increases above ground based on the device gain setting.

8.2.2.2 Detailed Design Procedure

The linear range of the output stage is limited in how close the output voltage can approach ground under zero input conditions. Resulting from an internal node limitation when the REF terminal is grounded (unidirectional configuration) the device gain setting determines how close to ground the device output voltage can achieve when no signal is applied; see 图 6-14. To overcome this internal node limitation, a small reference voltage (approximately 10 mV) can be applied to the REF terminal to bias the output voltage above this voltage level. The device output swing capability returns to the 10-mV saturation level with this small reference voltage present.

At the lowest gain setting, 25 V/V, the device is capable of accurately measuring input signals that result in output voltages below this 10-mV saturation level of the output stage. For these gain settings, a reference voltage can be applied to bias the output voltage above this lower saturation level to allow the device to monitor these smaller input signals. To avoid common-mode rejection errors, buffer the reference voltage connected to the REF terminal.

A less frequently-used output biasing method is to connect the REF terminal to the supply voltage, V_S. This method results in the output voltage saturating at 200 mV below the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the REF terminal is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– terminal. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF terminal must not exceed the device supply voltage.

8.2.2.3 Application Curve

An example output response of a unidirectional configuration is shown in 图 8-4. With the REF terminal connected directly to ground, the output voltage is biased to this zero output level. The output rises above the reference voltage for positive differential input signals but cannot fall below the reference voltage for negative differential input signals because of the grounded reference voltage.

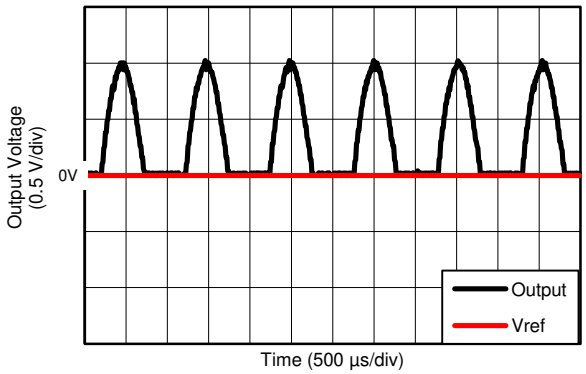


图 8-4. Unidirectional Application Output Response

8.2.3 Bidirectional Operation

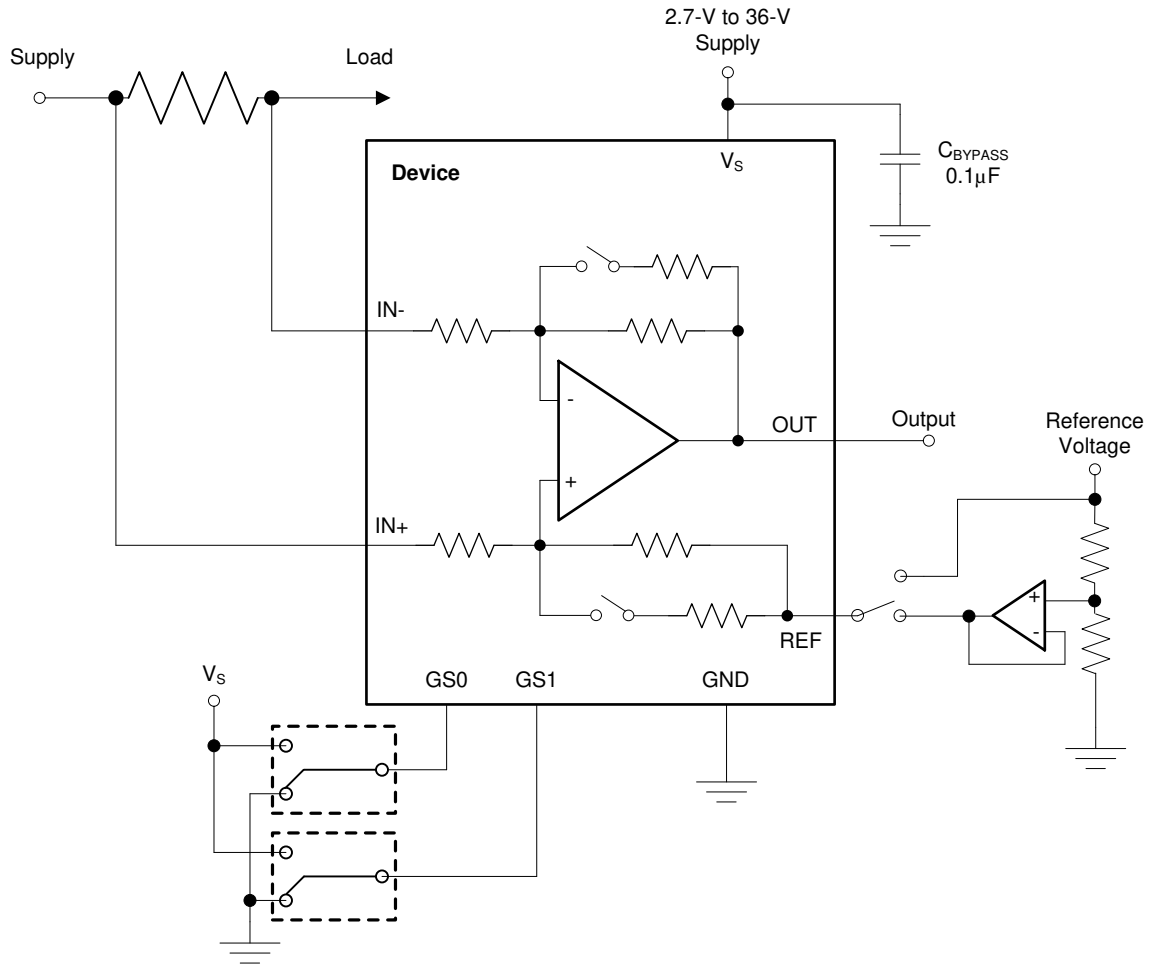


图 8-5. Bidirectional Application Schematic

8.2.3.1 Design Requirements

The device is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flow-through resistor can change directions.

8.2.3.2 Detailed Design Procedure

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF terminal, as shown in 图 8-5. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– terminal) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF terminal can be set anywhere between 0 V to V_S. For bidirectional applications, V_{REF} is typically set at mid-scale for equal range in both directions. In some cases, however, V_{REF} is set at a voltage other than half-scale when the bidirectional current is non-symmetrical.

8.2.3.3 Application Curve

An example output response of a bidirectional configuration is shown in 图 8-6. With the REF terminal connected to a reference voltage, 2.5 V in this case, the output voltage is biased upwards by this reference level. The output rises above the reference voltage for positive differential input signals and falls below the reference voltage for negative differential input signals.

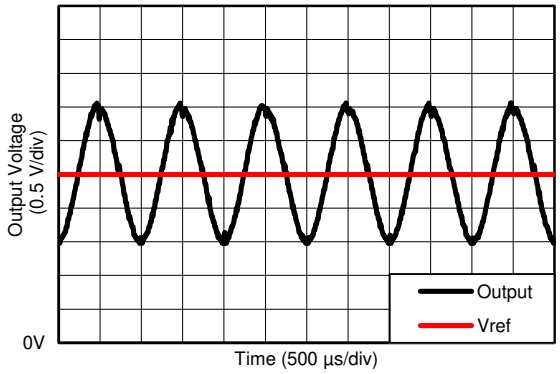


图 8-6. Bidirectional Application Output Response

9 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power supply voltage, V_S. For example, the voltage applied to the V_S power supply terminal can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as +36 V. Note also that the device can withstand the full –0.3-V to +36-V range at the input terminals, regardless of whether the device has power applied or not.

Power-supply bypass capacitors are required for stability and should be placed as closely as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

- Connect the input terminals to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input terminals. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input terminals. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- The power-supply bypass capacitor should be placed as closely as possible to the supply and ground terminals. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

10.2 Layout Example

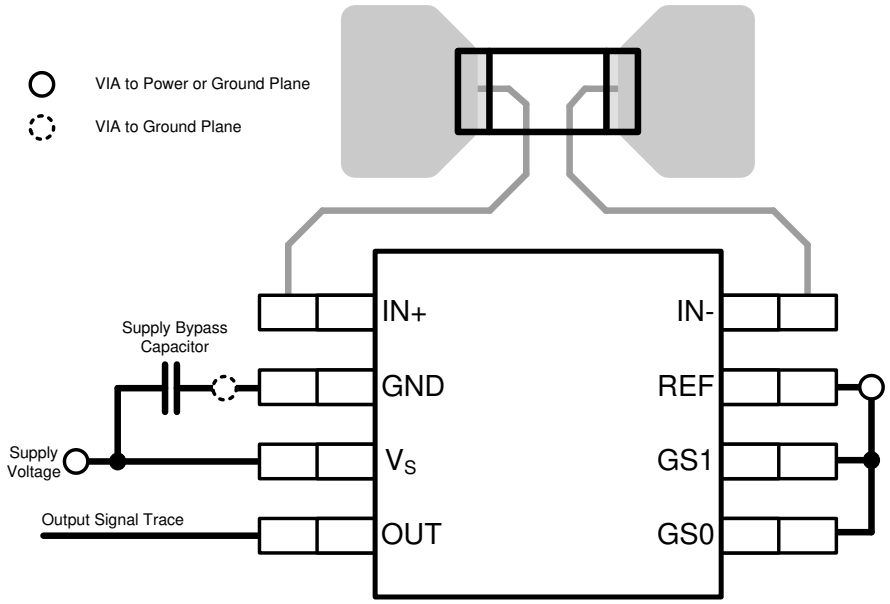


图 10-1. Recommended Layout

备注

The layout shown has REF connected to ground for unidirectional operation. Gain-select terminals (GS0 and GS1) are also connected to ground, indicating a 25-V/V gain setting.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- INA225EVM User's Guide, SBOU140

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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11.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA225AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	IAAQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

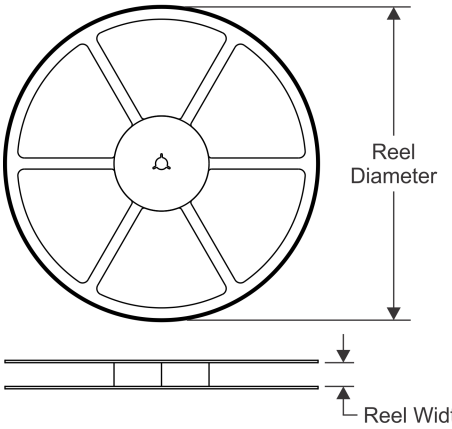
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

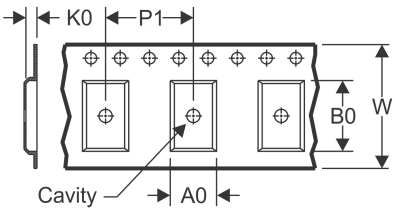
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

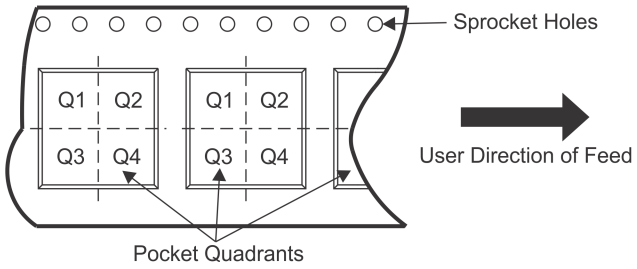


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

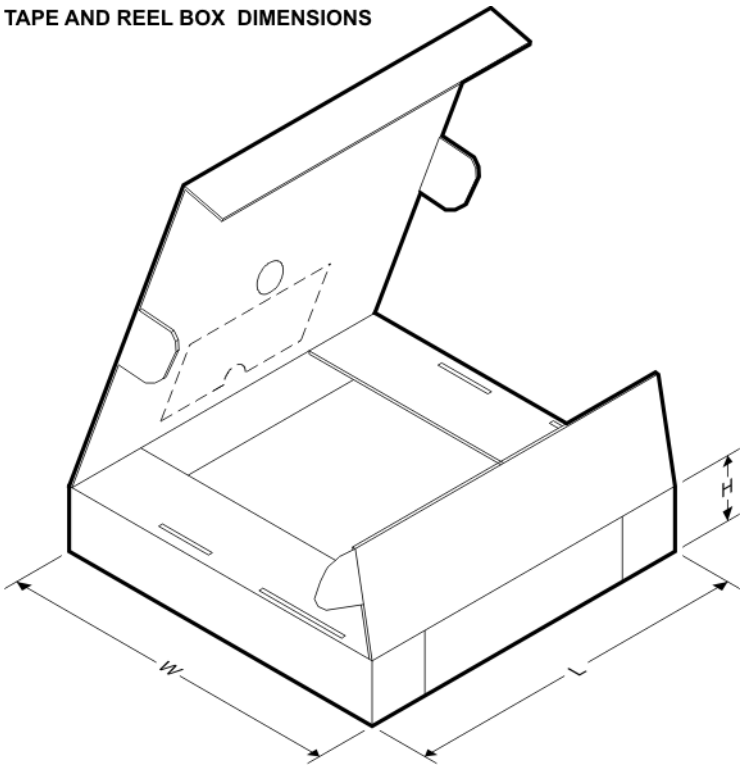
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA225AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

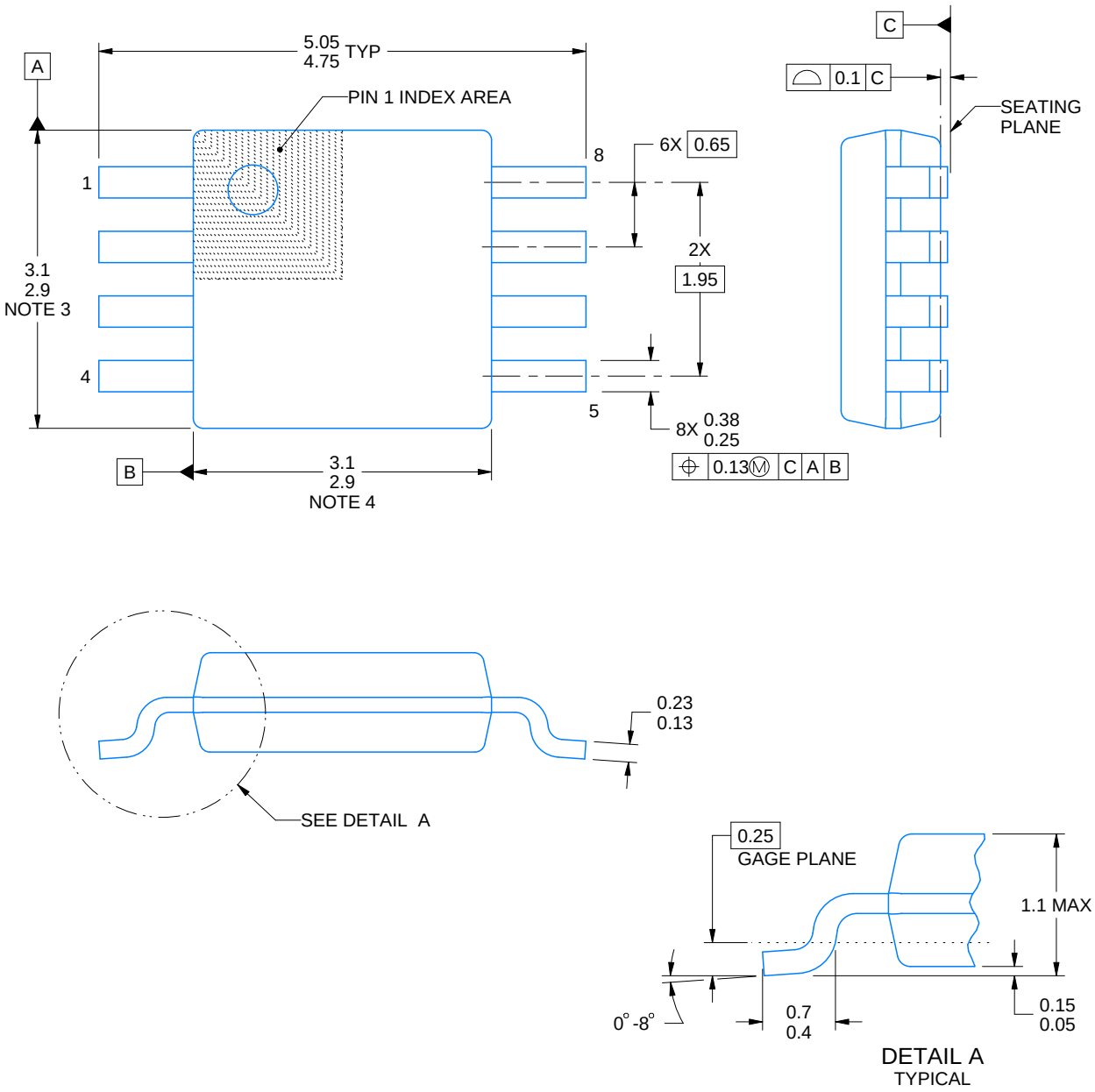
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA225AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

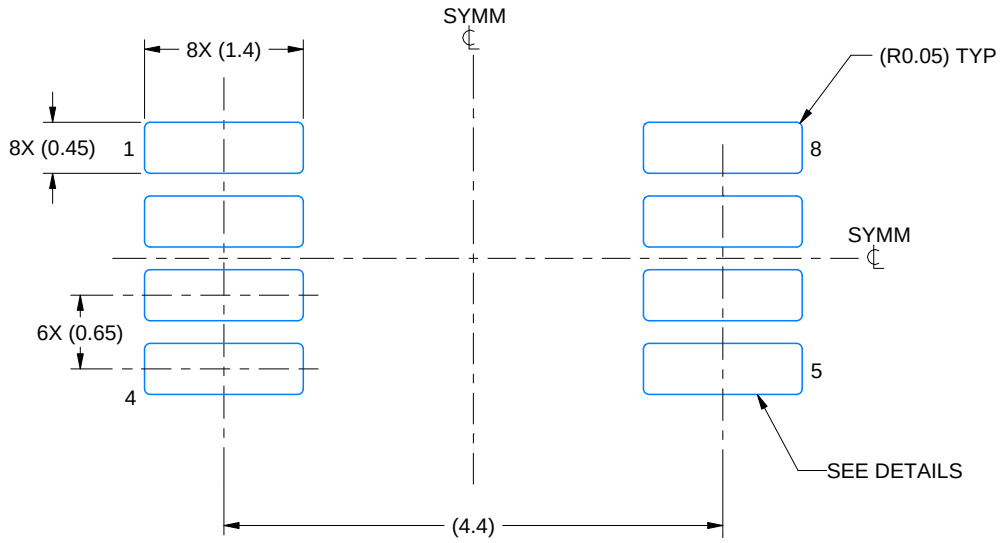
SMALL OUTLINE PACKAGE



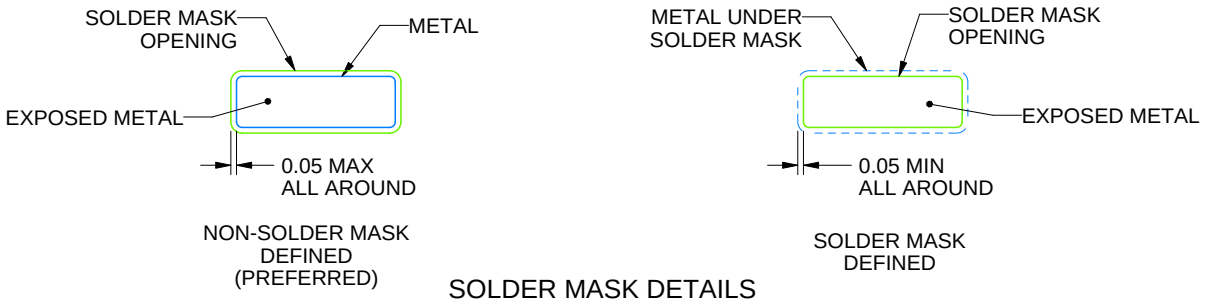
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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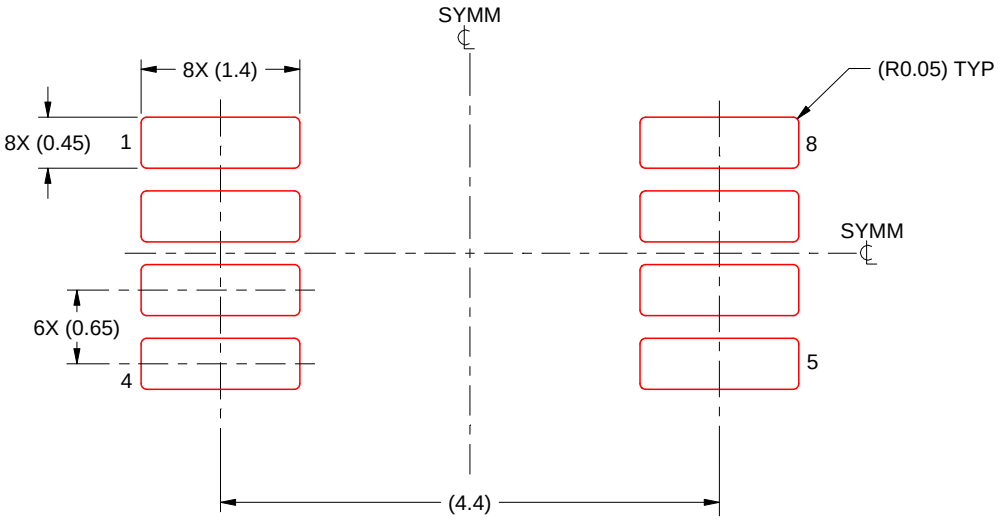
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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