

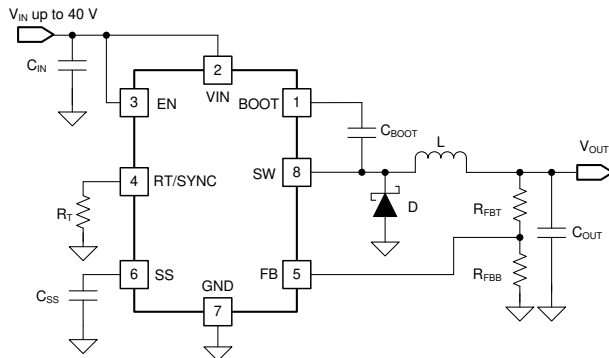
## LV14540 SIMPLE SWITCHER® 40V、5A、2MHz 同步降压转换器

## 1 特性

- 输入电压范围：4V 至 40V
- 5A 持续输出电流
- 100mΩ 高侧 MOSFET
- 最短导通时间：100ns
- 电流模式控制
- 可调节开关频率范围：200kHz 至 2MHz
- 与外部时钟频率同步
- 内置补偿功能，便于使用
- 支持高占空比运行
- 精密使能输入
- 关断电流：1μA
- 热保护、过压保护和短路保护
- 采用 PowerPAD™ 集成电路封装的 8 引脚 HSOIC

## 2 应用

- 汽车电池稳压
- 工业电源
- 电信和数据通信系统
- 电池供电型系统



简化原理图

## 3 说明

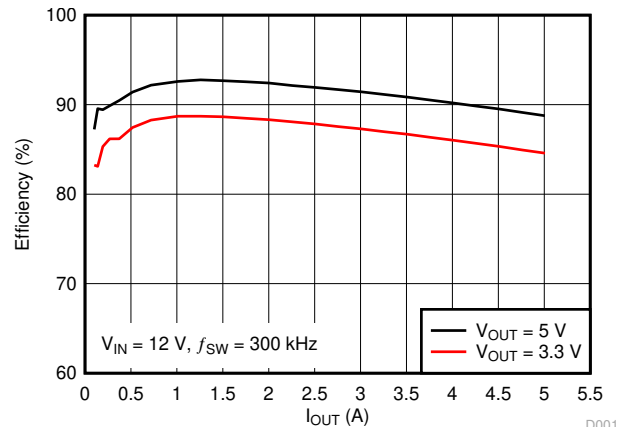
LV14540 是一款配有集成型高侧 MOSFET 的 40V、5A 降压稳压器。该器件具有 4V 至 40V 的宽输入范围，适用于从工业到汽车各类应用中非稳压电源的电源调节。该稳压器的可调开关频率范围较宽，这使得效率或外部元件尺寸能够得到优化。内部环路补偿意味着用户不用承担设计环路补偿组件的枯燥工作。内部环路补偿还能够更大限度地减少器件的外部元件。利用精密使能端输入可以简化稳压器控制和系统电源时序。此外，该器件还内置多种保护特性：逐周期电流限制保护、应对功耗过大的热感测和热关断保护、以及输出过压保护。

## 封装信息

| 器件型号    | 封装 <sup>(1)</sup> | 封装尺寸 <sup>(2)</sup> |
|---------|-------------------|---------------------|
| LV14540 | DDA ( HSOIC , 8 ) | 4.89mm x 3.90mm     |

(1) 有关更多信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



效率与输出电流之间的关系

D001



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## 4 Pin Configuration and Functions

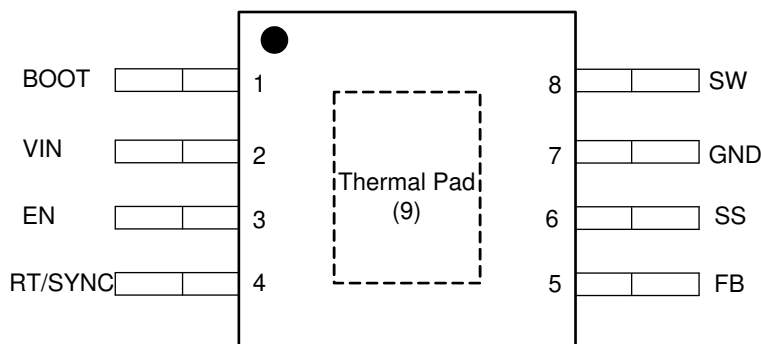


图 4-1. 8-Pin HSOIC DDA Package (Top View)

表 4-1. Pin Functions

| PIN         |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------------|-----|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME        | NO. |                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| BOOT        | 1   | P                   | Bootstrap capacitor connection for high-side MOSFET driver. Connect a high quality 0.1 $\mu$ F capacitor from BOOT to SW.                                                                                                                                                                                                                                                                                                                                                                                                              |
| VIN         | 2   | P                   | Connect to power supply and bypass capacitors $C_{IN}$ . Path from VIN pin to high frequency bypass $C_{IN}$ and GND must be as short as possible.                                                                                                                                                                                                                                                                                                                                                                                     |
| EN          | 3   | A                   | Enable pin, with internal pullup current source. Pull below 1.2V to disable. Float or connect to VIN to enable. Adjust the input undervoltage lockout with two resistors. See the <a href="#">Enable and Adjustable Undervoltage Lockout</a> section.                                                                                                                                                                                                                                                                                  |
| RT/SYNC     | 4   | A                   | Resistor Timing or External Clock input. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to frequency programming by resistor. |
| FB          | 5   | A                   | Feedback input pin, connect to the feedback divider to set $V_{OUT}$ . Do not short this pin to ground during operation.                                                                                                                                                                                                                                                                                                                                                                                                               |
| SS          | 6   | A                   | Soft-start control pin. Connect to a capacitor to set soft-start time.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| GND         | 7   | G                   | System ground pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| SW          | 8   | P                   | Switching output of the regulator. Internally connected to high-side power MOSFET. Connect to power inductor.                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Thermal Pad | 9   | G                   | Major heat dissipation path of the die. Must be connected to ground plane on PCB.                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

(1) A = Analog, P= Power, G = Ground

## 5 Specifications

### 5.1 Absolute Maximum Ratings

Over junction temperature range of  $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$  (unless otherwise noted) <sup>(1)</sup>

|                  |                      | MIN   | MAX | UNIT               |
|------------------|----------------------|-------|-----|--------------------|
| Input voltages   | VIN, EN to GND       | - 0.3 | 45  | V                  |
|                  | BOOT to GND          | - 0.3 | 50  |                    |
|                  | SS to GND            | - 0.3 | 5   |                    |
|                  | FB to GND            | - 0.3 | 7   |                    |
|                  | RT/SYNC to GND       | - 0.3 | 3.6 |                    |
| Output voltages  | BOOT to SW           |       | 6.5 | V                  |
|                  | SW to GND            | - 3   | 45  |                    |
| T <sub>J</sub>   | Junction temperature | - 40  | 150 | $^{\circ}\text{C}$ |
| T <sub>stg</sub> | Storage temperature  | - 65  | 150 | $^{\circ}\text{C}$ |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

|                                            |                                                                                | VALUE | UNIT |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                            | Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  (unless otherwise noted)

|                |                                                | MIN  | MAX  | UNIT               |
|----------------|------------------------------------------------|------|------|--------------------|
| Buck regulator | VIN                                            | 4    | 40   | V                  |
|                | VOUT                                           | 0.8  | 32   |                    |
|                | BOOT                                           |      | 45   |                    |
|                | SW                                             | - 1  | 40   |                    |
|                | FB                                             | 0    | 5    |                    |
| Control        | EN                                             | 0    | 40   | V                  |
|                | RT/SYNC                                        | 0    | 3.3  |                    |
|                | SS                                             | 0    | 3    |                    |
| Frequency      | Switching frequency range at RT mode           | 200  | 2000 | kHz                |
|                | Switching frequency range at SYNC mode         | 250  | 2000 |                    |
| Temperature    | Operating junction temperature, T <sub>J</sub> | - 40 | 125  | $^{\circ}\text{C}$ |

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | LV14540     | UNIT |
|-------------------------------|----------------------------------------------|-------------|------|
|                               |                                              | DDA (HSOIC) |      |
|                               |                                              | 8 PINS      |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 42.5        | °C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 9.9         |      |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 25.4        |      |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 56.1        |      |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 3.8         |      |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 25.5        |      |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature ( $T_J$ ) range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^{\circ}\text{C}$ , and are provided for reference purposes only. Unless otherwise specified, the following conditions apply:  $V_{IN} = 4\text{ V}$  to  $40\text{ V}$ .

| PARAMETER                      |                                             | TEST CONDITIONS                                                              | MIN   | TYP   | MAX   | UNIT |
|--------------------------------|---------------------------------------------|------------------------------------------------------------------------------|-------|-------|-------|------|
| POWER SUPPLY (VIN PIN)         |                                             |                                                                              |       |       |       |      |
| V <sub>IN</sub>                | Operation input voltage                     |                                                                              | 4     |       | 40    | V    |
| UVLO                           | Undervoltage lockout thresholds             | Rising threshold                                                             | 3.5   | 3.7   | 3.9   | V    |
|                                |                                             | Hysteresis                                                                   |       | 285   |       | mV   |
| I <sub>SHDN</sub>              | Shutdown supply current                     | V <sub>EN</sub> = 0 V, T <sub>J</sub> = 25°C, 4.0 V ≤ V <sub>IN</sub> ≤ 40 V |       | 1     | 3.0   | μ A  |
| I <sub>Q</sub>                 | Operating quiescent current (non-switching) | V <sub>FB</sub> = 1.0 V, T <sub>J</sub> = 25°C                               |       | 300   |       | μ A  |
| ENABLE (EN PIN)                |                                             |                                                                              |       |       |       |      |
| V <sub>EN_TH</sub>             | EN threshold voltage                        |                                                                              | 1.05  | 1.20  | 1.38  | V    |
| I <sub>EN_PIN</sub>            | EN PIN current                              | Enable threshold +50 mV                                                      |       | - 4.6 |       | μ A  |
|                                |                                             | Enable threshold -5 mV                                                       |       | - 1.0 |       |      |
| I <sub>EN_HYS</sub>            | EN hysteresis current                       |                                                                              |       | - 3.6 |       | μ A  |
| EXTERNAL SOFT-START            |                                             |                                                                              |       |       |       |      |
| I <sub>SS</sub>                | SS pin current                              | T <sub>A</sub> = 25°C                                                        |       | 3     |       | μ A  |
| VOLTAGE REFERENCE (FB PIN)     |                                             |                                                                              |       |       |       |      |
| V <sub>FB</sub>                | Feedback voltage                            | T <sub>J</sub> = 25°C                                                        | 0.744 | 0.750 | 0.756 | V    |
|                                |                                             | T <sub>J</sub> = - 40°C to 125°C                                             | 0.735 | 0.750 | 0.765 | V    |
| HIGH-SIDE MOSFET               |                                             |                                                                              |       |       |       |      |
| R <sub>DS_ON</sub>             | On-resistance                               | V <sub>IN</sub> = 12 V, BOOT to SW = 5.8 V                                   |       | 100   | 180   | mΩ   |
| High-side MOSFET CURRENT LIMIT |                                             |                                                                              |       |       |       |      |
| I <sub>LIMIT</sub>             | Current limit                               | V <sub>IN</sub> = 12 V, T <sub>A</sub> = 25°C, Open Loop                     | 6.2   | 7.9   | 9.7   | A    |
| THERMAL PERFORMANCE            |                                             |                                                                              |       |       |       |      |
| T <sub>SHDN</sub>              | Thermal shutdown threshold                  |                                                                              |       | 170   |       | °C   |
| T <sub>HYS</sub>               | Hysteresis                                  |                                                                              |       | 12    |       |      |

## 5.6 Switching Characteristics

Over the recommended operating junction temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  (unless otherwise noted)

| PARAMETER              |                                 | TEST CONDITION                                                                                 | MIN | TYP | MAX | UNIT          |
|------------------------|---------------------------------|------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| $f_{\text{SW}}$        | Switching frequency             | $R_T = 49.9\text{ k}\Omega$ , 1% accuracy                                                      | 400 | 500 | 600 | kHz           |
| $V_{\text{SYNC\_HI}}$  | SYNC clock high level threshold |                                                                                                | 1.7 |     |     | V             |
| $V_{\text{SYNC\_LO}}$  | SYNC clock low level threshold  |                                                                                                |     |     | 0.5 |               |
| $T_{\text{SYNC\_MIN}}$ | Minimum SYNC input pulse width  | Measured at 500 kHz, $V_{\text{SYNC\_HI}} > 3\text{ V}$ , $V_{\text{SYNC\_LO}} < 0.3\text{ V}$ |     | 30  |     | ns            |
| $T_{\text{LOCK\_IN}}$  | PLL lock in time                | Measured at 500 kHz                                                                            |     | 100 |     | $\mu\text{s}$ |
| $T_{\text{ON\_MIN}}$   | Minimum controllable on time    | $V_{\text{IN}} = 12\text{ V}$ , BOOT to SW = 5.8 V, $I_{\text{Load}} = 1\text{ A}$             |     | 100 |     | ns            |
| $D_{\text{MAX}}$       | Maximum duty cycle              | $f_{\text{SW}} = 200\text{ kHz}$                                                               |     | 97% |     | %             |

## 5.7 Typical Characteristics

Unless otherwise specified the following conditions apply:  $V_{IN} = 12\text{ V}$ ,  $f_{SW} = 300\text{ kHz}$ ,  $L = 6.5\text{ }\mu\text{H}$ ,  $C_{OUT} = 47\text{ }\mu\text{F} \times 4$ ,  $T_A = 25^\circ\text{C}$

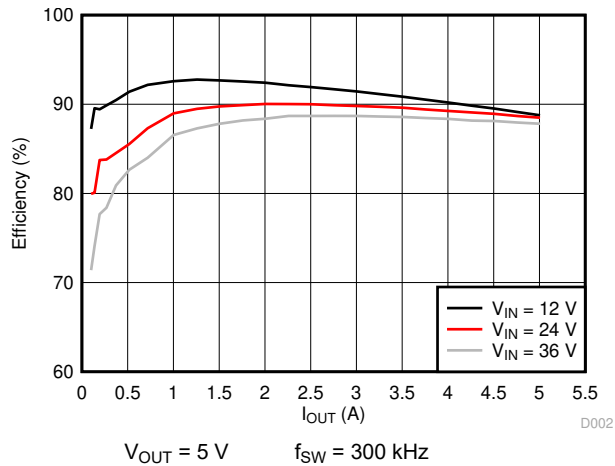


图 5-1. Efficiency versus Load Current

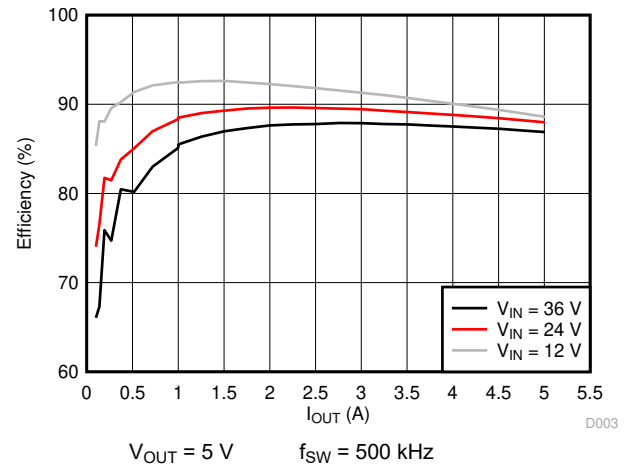


图 5-2. Efficiency versus Load Current

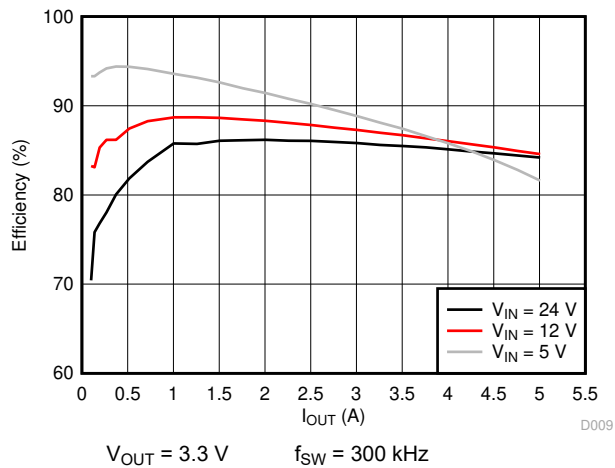


图 5-3. Efficiency versus Load Current

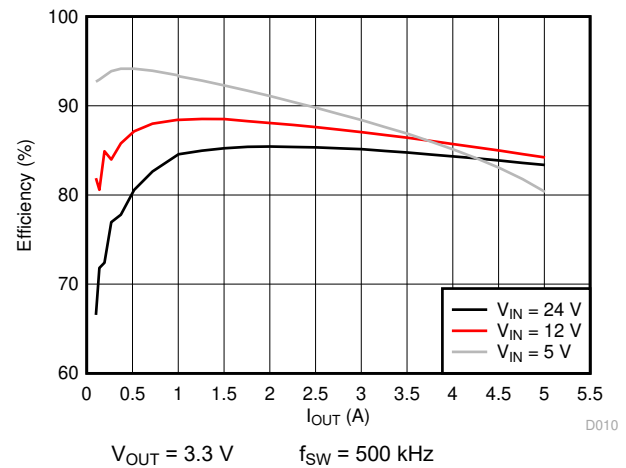


图 5-4. Efficiency versus Load Current

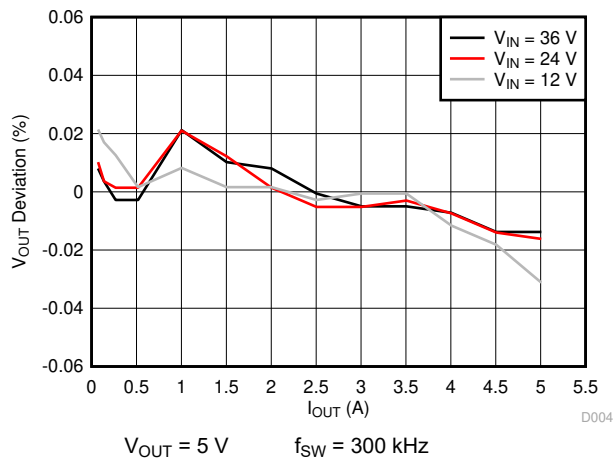


图 5-5. Load Regulation

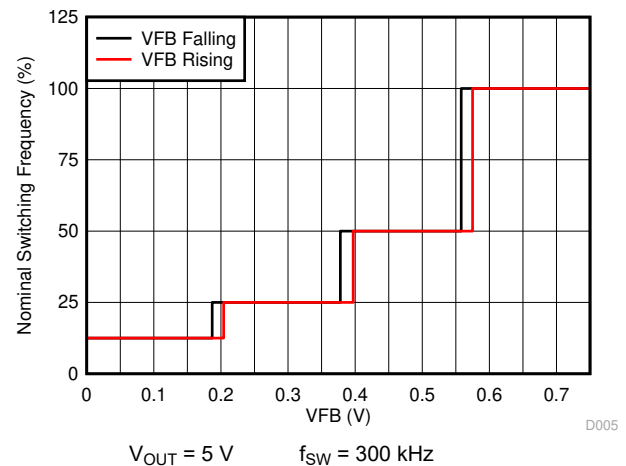


图 5-6. Frequency versus  $V_{FB}$

## 5.7 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply:  $V_{IN} = 12\text{ V}$ ,  $f_{SW} = 300\text{ kHz}$ ,  $L = 6.5\text{ }\mu\text{H}$ ,  $C_{OUT} = 47\text{ }\mu\text{F} \times 4$ ,  $T_A = 25^\circ\text{C}$

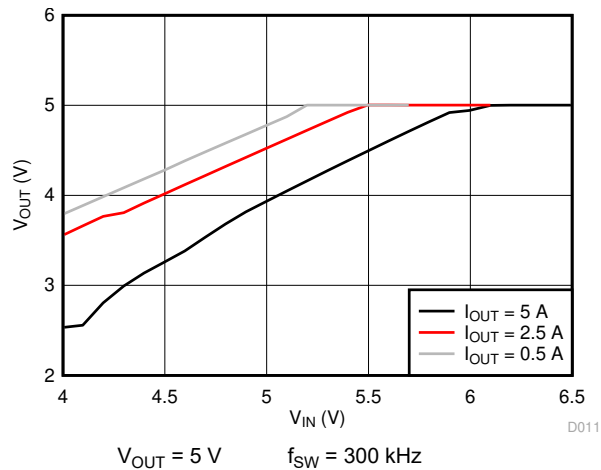


图 5-7. Dropout Curve

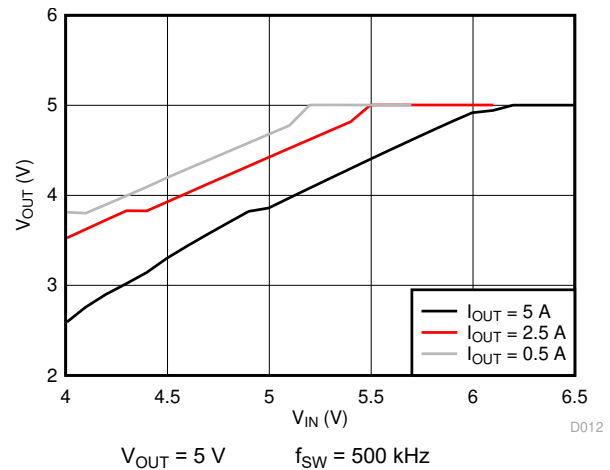


图 5-8. Dropout Curve

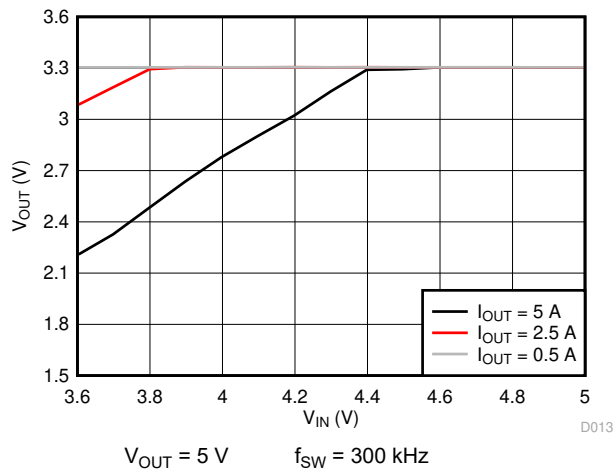


图 5-9. Dropout Curve

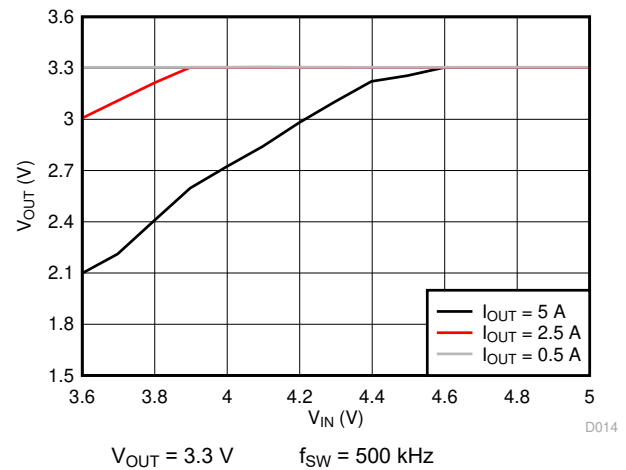


图 5-10. Dropout Curve

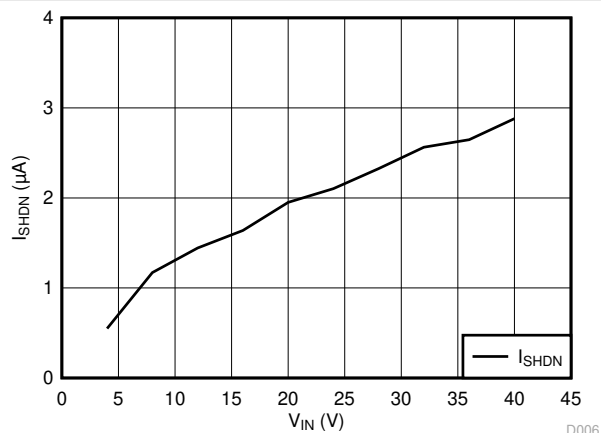


图 5-11. Shut-down Current

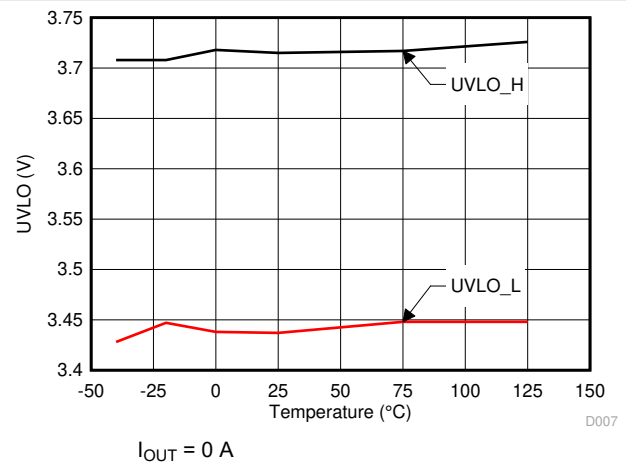


图 5-12. UVLO Threshold

## 6 Detailed Description

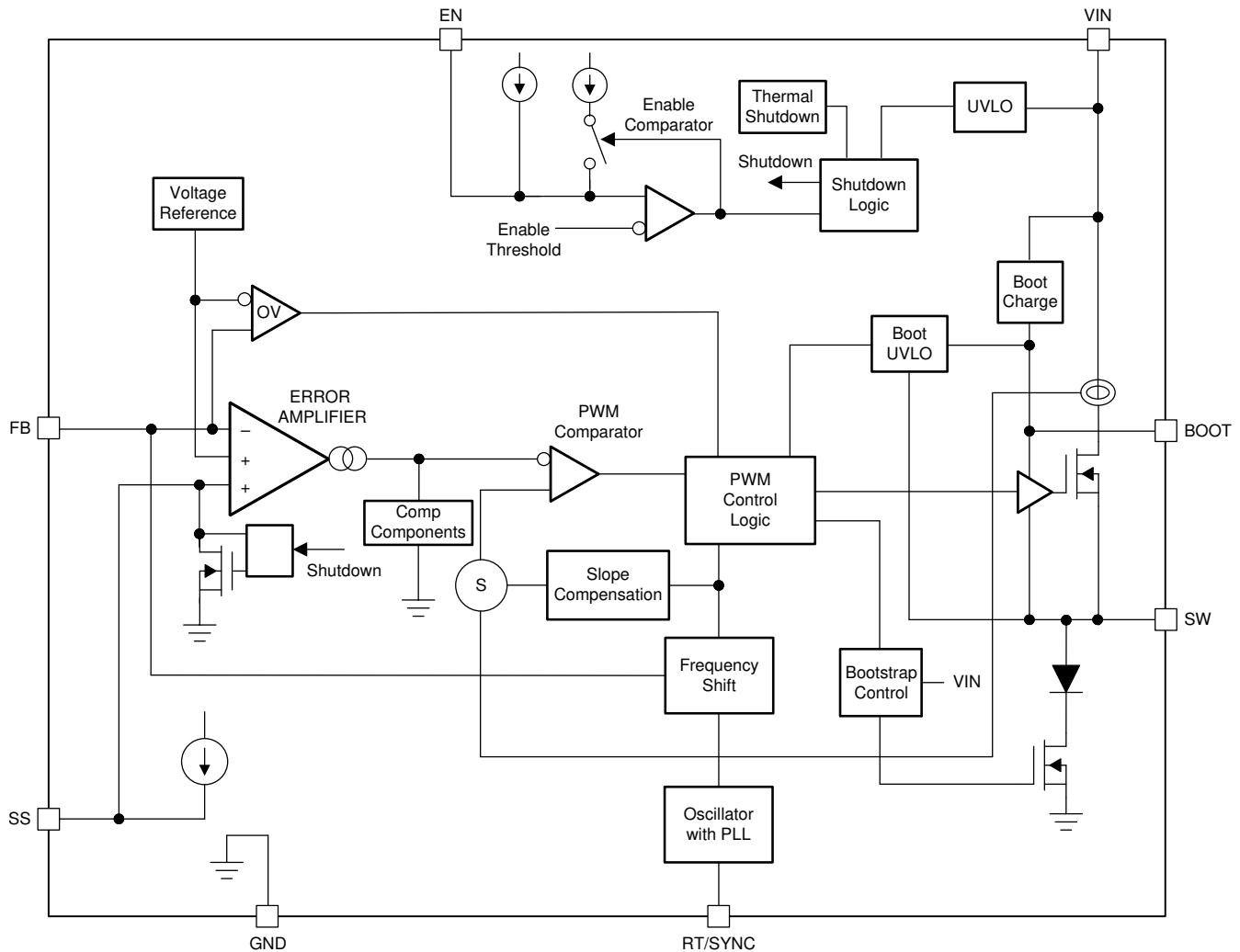
### 6.1 Overview

The LV14540 SIMPLE SWITCHER® regulator is an easy-to-use step-down DC/DC converter that operates from 4.0 V to 40 V supply voltage. It integrates a 100 m $\Omega$  (typical) high-side MOSFET and is capable of delivering up to 5 A DC load current with exceptional efficiency and thermal performance in a very small design size. The operating current is typically 120  $\mu$ A under no-load condition (not switching). When the device is disabled, the supply current is typically 1  $\mu$ A. An extended family is available in 2 A and 3.5 A load options in pin-to-pin compatible packages.

The LV14540 implements constant frequency peak current mode control with pulse skipping mode at light load to achieve high efficiency. The device is internally compensated, which reduces design time, and requires fewer external components. The switching frequency is programmable from 200 kHz to 2 MHz by an external resistor,  $R_T$ . The LV14540 is also capable of synchronization to an external clock within the 250 kHz to 2 MHz frequency range, which allows the device to be designed to fit small board space at higher frequency, or high efficient power conversion at lower frequency.

Other optional features are included for more comprehensive system requirements, including precision enable, adjustable soft-start time, and approximately 97% duty cycle by a BOOT capacitor recharge circuit. These features provide a flexible and easy to use platform for a wide range of applications. Protection features include over temperature shutdown,  $V_{OUT}$  overvoltage protection (OVP),  $V_{IN}$  undervoltage lockout (UVLO), cycle-by-cycle current limit, and short-circuit protection with frequency fold-back.

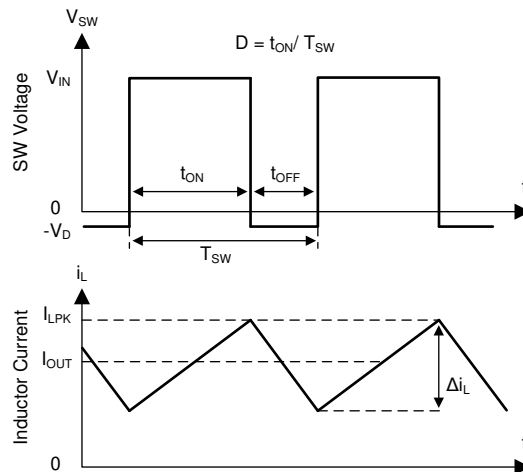
## 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Fixed Frequency Peak Current Mode Control

The following operation description of the LV14540 refers to the [节 6.2](#) and the waveforms in [图 6-1](#). LV14540 output voltage is regulated by turning on the high-side N-MOSFET with controlled ON time. During high-side switch ON time, the SW pin voltage swings up to approximately  $V_{IN}$ , and the inductor current,  $i_L$ , increases with linear slope  $(V_{IN} - V_{OUT}) / L$ . When high-side switch is off, inductor current discharges through freewheel diode with a slope of  $-V_{OUT} / L$ . The control parameter of Buck converter is defined as Duty Cycle  $D = t_{ON} / T_{SW}$ , where  $t_{ON}$  is the high-side switch ON time and  $T_{SW}$  is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle  $D$ . In an ideal buck converter where losses are ignored,  $D$  is proportional to the output voltage and inversely proportional to the input voltage:  $D = V_{OUT} / V_{IN}$ .



**图 6-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)**

The LV14540 employs fixed frequency peak current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency at normal load condition. At very light load, the LV14540 operates in pulse skipping mode to maintain high efficiency and the switching frequency decrease with reduced load current.

### 6.3.2 Slope Compensation

The LV14540 adds a compensating ramp to the MOSFET switch current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycle greater than 50%. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

### 6.3.3 Pulse Skipping Mode

The LV14540 operates in pulse skipping mode (PSM) at light load current to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switching current at the end of any switching cycle is below the current threshold of 300 mA, the device enters PSM. The PSM current threshold is the peak switch current level corresponding to a nominal internal COMP voltage of 400 mV.

When in PSM, the internal COMP voltage is clamped at 400 mV, the high-side MOSFET is inhibited, and the device draws about 120  $\mu$ A input quiescent current. Because the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the internal COMP voltage. The high-side MOSFET is enabled and switching resumes when the error amplifier lifts internal COMP voltage above 400 mV. The output voltage recovers to the regulated value, and internal COMP voltage eventually falls below the PSM threshold at which time the device again enters PSM.

### 6.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The LV14540 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1  $\mu$ F. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or higher for stable performance overtemperature and voltage.

When operating with a low voltage difference from input to output, the high-side MOSFET of the LV14540 operates at approximately 97% duty cycle. When the high-side MOSFET is continuously on for 5 or 6 switching cycles (5 or 6 switching cycles for frequency lower than 1 MHz, and 10 or 11 switching cycles for frequency

higher than 1 MHz) and the voltage from BOOT to SW drops below 3.2 V, the high-side MOSFET is turned off and an integrated low side MOSFET pulls SW low to recharge the BOOT capacitor.

Since the gate drive current sourced from the BOOT capacitor is small, the high-side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 97%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side diode voltage and the printed circuit board resistance.

### 6.3.5 Adjustable Output Voltage

The internal voltage reference produces a precise 0.75 V (typical) voltage reference over the operating temperature. The output voltage is set by a resistor divider from output voltage to the FB pin. It is recommended to use 1% tolerance or better and temperature coefficient of 100 ppm or lower divider resistors. Select the low-side resistor  $R_{FBB}$  for the desired divider current and use [方程式 1](#) to calculate high-side  $R_{FBT}$ . Larger value divider resistors are good for efficiency at light load. However, if the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current can become noticeable. TI recommends  $R_{FBB}$  in the range from 10 k $\Omega$  to 100 k $\Omega$  for most applications.

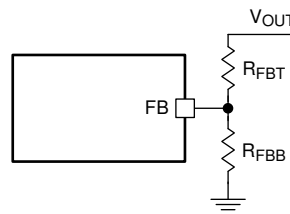


图 6-2. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - 0.75}{0.75} R_{FBB} \quad (1)$$

### 6.3.6 Enable and Adjustable Undervoltage Lockout

The LV14540 is enabled when the VIN pin voltage rises above 3.7 V (typical) and the EN pin voltage exceeds the enable threshold of 1.2 V (typical). The LV14540 is disabled when the VIN pin voltage falls below 3.42 V (typical) or when the EN pin voltage is below 1.2 V. The EN pin has an internal pullup current source (typically  $I_{EN} = 1 \mu A$ ) that enables operation of the LV14540 when the EN pin is floating.

Many applications will benefit from the employment of an enable divider  $R_{ENT}$  and  $R_{ENB}$  in [图 6-3](#) to establish a precision system UVLO level for the stage. System UVLO can be used for supplies operating from utility power as well as battery power. It can be used for sequencing, making sure of reliable operation, or supply protection, such as a battery. An external logic signal can also be used to drive EN input for system sequencing and protection.

When EN terminal voltage exceeds 1.2 V, an additional hysteresis current (typically  $I_{HYS} = 3.6 \mu A$ ) is sourced out of the EN terminal. When the EN terminal is pulled below 1.2 V,  $I_{HYS}$  current is removed. This additional current facilitates adjustable input voltage UVLO hysteresis. Use [方程式 2](#) and [方程式 3](#) to calculate  $R_{ENT}$  and  $R_{ENB}$  for desired UVLO hysteresis voltage.

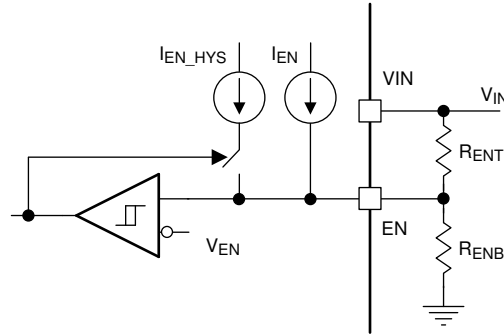


图 6-3. System UVLO by Enable Dividers

$$R_{ENT} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (2)$$

$$R_{ENB} = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{R_{ENT}} + I_{EN}} \quad (3)$$

where  $V_{START}$  is the desired voltage threshold to enable LV14540,  $V_{STOP}$  is the desired voltage threshold to disable device.

### 6.3.7 External Soft Start

The LV14540 has soft-start pin for programmable output ramp-up time. The soft-start feature is used to prevent inrush current impacting the LV14540 and the load when power is first applied. The soft-start time can be programmed by connecting an external capacitor  $C_{SS}$  from SS pin to GND. An internal current source (typically  $I_{SS} = 3 \mu A$ ) charges  $C_{SS}$  and generates a ramp from 0V to  $V_{REF}$ . The soft-start time can be calculated by 方程式 4:

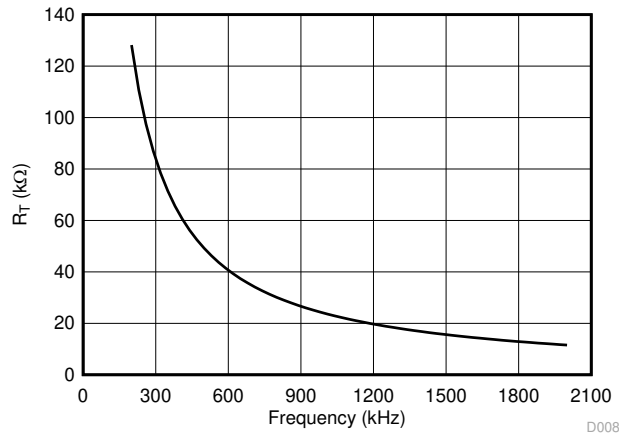
$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (4)$$

The internal soft start resets while the device is disabled or in thermal shutdown.

### 6.3.8 Switching Frequency and Synchronization (RT/SYNC)

The switching frequency of the LV14540 can be programmed by the resistor  $R_T$  from the RT/SYNC pin and GND pin. The RT/SYNC pin cannot be left floating or shorted to ground. To determine the timing resistance for a given switching frequency, use 方程式 5 or the curve in 图 6-4. 表 6-1 gives typical  $R_T$  values for a given  $f_{SW}$ .

$$R_T(k\Omega) = 42904 \times f_{SW}(kHz)^{-1.088} \quad (5)$$

图 6-4.  $R_T$  versus Frequency Curve表 6-1. Typical Frequency Setting  $R_T$  Resistance

| $f_{sw}$ (kHz) | $R_T$ (kΩ) |
|----------------|------------|
| 200            | 133        |
| 350            | 73.2       |
| 500            | 49.9       |
| 750            | 32.4       |
| 1000           | 23.2       |
| 1500           | 15.0       |
| 1912           | 11.5       |
| 2000           | 11.0       |

The LV14540 switching action can also be synchronized to an external clock from 250 kHz to 2 MHz. Connect a square wave to the RT/SYNC pin through either circuit network shown in 图 6-5. The internal oscillator is synchronized by the falling edge of the external clock. The recommendations for the external clock include a high level no lower than 1.7 V, a low level no higher than 0.5 V, and a pulse width greater than 30 ns. When using a low impedance signal source, the frequency setting resistor  $R_T$  is connected in parallel with an AC coupling capacitor  $C_{COUP}$  to termination resistor  $R_{TERM}$  (for example, 50  $\Omega$ ). The two resistors in series provide the default frequency setting resistance when the signal source is turned off. A 470 pF ceramic capacitor can be used for  $C_{COUP}$ . 图 6-6, 图 6-7, and 图 6-8 show the device synchronized to an external system clock.

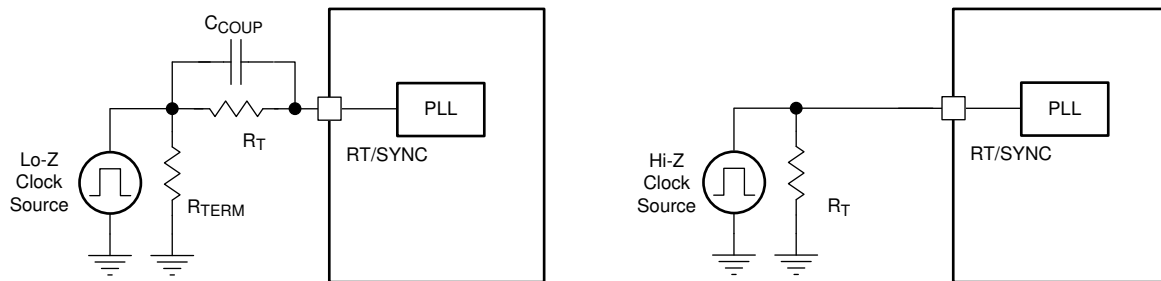


图 6-5. Synchronizing to an External Clock

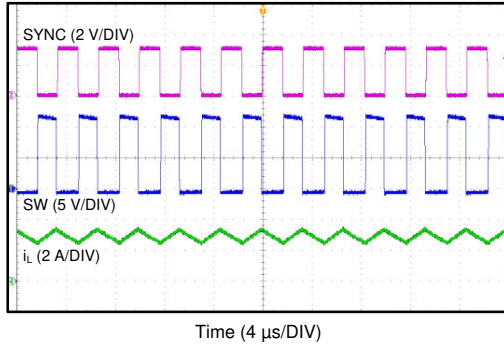


图 6-6. Synchronizing in CCM

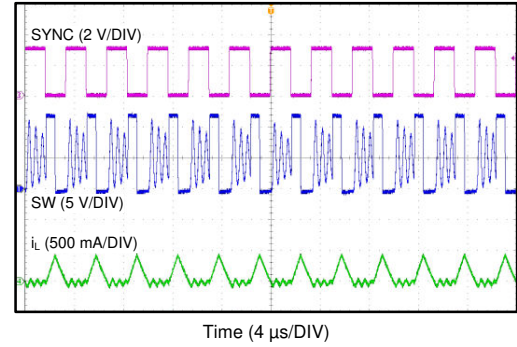


图 6-7. Synchronizing in DCM

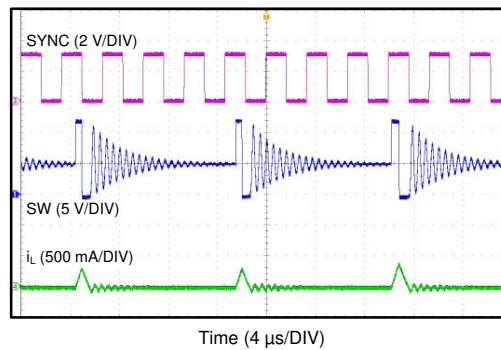


图 6-8. Synchronizing in PSM

方程式 6 calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step-down ratio. Setting the switching frequency above this value causes the regulator to skip switching pulses to achieve the low duty cycle required at maximum input voltage.

$$f_{SW(max)} = \frac{1}{t_{ON}} \times \left( \frac{I_{OUT} \times R_{IND} + V_{OUT} + V_D}{V_{IN\_MAX} - I_{OUT} \times R_{DS\_ON} + V_D} \right) \quad (6)$$

where

- $I_{OUT}$  = Output current
- $R_{IND}$  = Inductor series resistance
- $V_{IN\_MAX}$  = Maximum input voltage
- $V_{OUT}$  = Output voltage
- $V_D$  = Diode voltage drop
- $R_{DS\_ON}$  = High-side MOSFET switch on resistance
- $t_{ON}$  = Minimum on-time

### 6.3.9 Overcurrent and Short-Circuit Protection

The LV14540 is protected from overcurrent condition by cycle-by-cycle current limiting on the peak current of the high-side MOSFET. High-side MOSFET overcurrent protection is implemented by the nature of the Peak Current Mode control. The high-side switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. Refer to the 节 6.2 for more details. The peak current of high-side switch is

limited by a clamped maximum peak current threshold which is constant. So the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

The LV14540 also implements a frequency foldback to protect the converter in severe overcurrent or short conditions. The oscillator frequency is divided by 2, 4, and 8 as the FB pin voltage decrease to 75%, 50%, and 25% of  $V_{REF}$ . The frequency foldback increases the off-time by increasing the period of the switching cycle so that it provides more time for the inductor current to ramp down and leads to a lower average inductor current. Lower frequency also means lower switching loss. Frequency foldback reduces power dissipation and prevents overheating and potential damage to the device.

### 6.3.10 Overvoltage Protection

The LV14540 employs an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. The OVP feature minimizes output overshoot by turning off high-side switch immediately when FB voltage reaches to the rising OVP threshold which is nominally 109% of the internal voltage reference  $V_{REF}$ . When the FB voltage drops below the falling OVP threshold which is nominally 107% of  $V_{REF}$ , the high-side MOSFET resumes normal operation.

### 6.3.11 Thermal Shutdown

The LV14540 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 170°C (typical). The high-side MOSFET stops switching when the thermal shutdown activates. After the die temperature falls below 158°C (typical), the device reinitiates the power up sequence controlled by the internal soft-start circuitry.

## 6.4 Device Functional Modes

### 6.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LV14540. When  $V_{EN}$  is below 1.0 V, the device is in shutdown mode. The switching regulator is turned off and the quiescent current drops to 1.0  $\mu$ A typically. The LV14540 also employs undervoltage lockout protection. If  $V_{IN}$  voltage is below the UVLO level, the regulator turns off.

### 6.4.2 Active Mode

The LV14540 is in active mode when  $V_{EN}$  is above the precision enable threshold and  $V_{IN}$  is above the UVLO level. The simplest way to enable the LV14540 is to connect the EN pin to VIN pin. This connection allows self start-up when the input voltage is in the operation range: 4.0 V to 40 V. Please refer to [Figure 6.3.6](#) for details on setting these operating levels.

In active mode, depending on the load current, the LV14540 is in one of three modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple.
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation.
3. Sleep-mode when the internal COMP voltage drops to 400 mV at very light load.

### 6.4.3 CCM Mode

CCM operation is employed in the LV14540 when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode and the maximum output current of 5 A can be supplied by the LV14540.

### 6.4.4 Light Load Operation

When the load current is lower than half of the peak-to-peak inductor current in CCM, the LV14540 operates in DCM. At even lighter current loads, sleep-mode is activated to maintain high efficiency operation by reducing switching and gate drive losses.

## 7 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 7.1 Application Information

The LV14540 is a step-down DC-to-DC regulator. The device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 5A. The following design procedure can be used to select components for the LV14540. This section presents a simplified discussion of the design process.

### 7.2 Typical Application

The LV14540 only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. A schematic of 5 V/5 A application circuit is shown in 图 7-1. The external components must fulfill the needs of the application, but also the stability criteria of the control loop of the device.

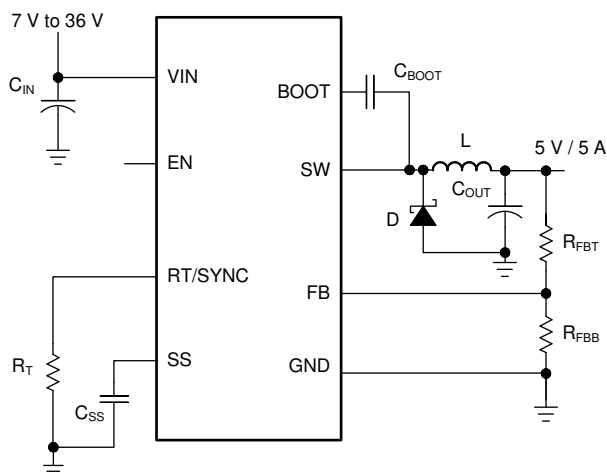


图 7-1. Application Circuit, 5V Output

#### 7.2.1 Design Requirements

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level:

|                                     |                           |
|-------------------------------------|---------------------------|
| Input voltage, $V_{IN}$             | 7 V to 36 V, Typical 12 V |
| Output voltage, $V_{OUT}$           | 5.0 V                     |
| Maximum output current $I_{O\_MAX}$ | 5 A                       |
| Transient response 0.5 A to 5 A     | 5%                        |
| Output voltage ripple               | 50 mV                     |
| Input voltage ripple                | 400 mV                    |
| Switching frequency $f_{SW}$        | 300 kHz                   |
| Soft-start time                     | 5 ms                      |

## 7.2.2 Detailed Design Procedure

### 7.2.2.1 Output Voltage Set-Point

The output voltage of the LV14540 is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor  $R_{FBT}$  and bottom feedback resistor  $R_{FBB}$ . 方程式 7 is used to determine the output voltage:

$$R_{FBT} = \frac{V_{OUT} - 0.75}{0.75} R_{FBB} \quad (7)$$

Choose the value of  $R_{FBT}$  to be 100 k $\Omega$ . With the desired output voltage set to 5 V and the  $V_{FB} = 0.75$  V, the  $R_{FBB}$  value can then be calculated using 方程式 7. The formula yields to a value 17.65 k $\Omega$ . Choose the closest available value of 17.8 k $\Omega$  for  $R_{FBB}$ .

### 7.2.2.2 Switching Frequency

For desired frequency, use 方程式 8 to calculate the required value for  $R_T$ .

$$R_T(\text{k}\Omega) = 42904 \times f_{SW}(\text{kHz})^{-1.088} \quad (8)$$

For 300kHz, the calculated  $R_T$  is 86.57 k $\Omega$  and standard value 86.6 k $\Omega$  can be used to set the switching frequency at 300 kHz.

### 7.2.2.3 Output Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current  $\Delta i_L$ . Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance  $L_{MIN}$ . Use 方程式 10 to calculate the minimum value of the output inductor.  $K_{IND}$  is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. A reasonable value of  $K_{IND}$  must be 20% - 40%. During an instantaneous short or over current operation event, the RMS and peak inductor current can be high. The inductor current rating must be higher than current limit.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \quad (9)$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (10)$$

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that over current protection at the full load can be falsely triggered. It also generates more conduction loss because the RMS current is slightly higher. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, it is not recommend to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose  $K_{IND} = 0.4$ . The minimum inductor value is calculated to be 7.17  $\mu\text{H}$ , and a nearest standard value is chosen: 8.2  $\mu\text{H}$ . A standard 8.2  $\mu\text{H}$  ferrite inductor with a capability of 7 A RMS current and 10 A saturation current can be used.

### 7.2.2.4 Output Capacitor Selection

The output capacitors,  $C_{OUT}$ , must be chosen with care because the output capacitors directly affects the steady state output voltage ripple, loop stability, and the voltage over/undershoot during load current transients.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (11)$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \quad (12)$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The control loop of the regulator usually needs three or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for three clock cycles to maintain the output voltage within the specified range. 方程式 13 shows the minimum output capacitance needed for specified output undershoot. When a sudden large load decrease happens, the output capacitors absorb energy stored in the inductor. The catch diode cannot sink current so the energy stored in the inductor results in an output voltage overshoot. 方程式 14 calculates the minimum capacitance required to keep the voltage overshoot within a specified range.

$$C_{OUT} > \frac{3 \times (I_{OH} - I_{OL})}{f_{SW} \times V_{US}} \quad (13)$$

$$C_{OUT} > \frac{I_{OH}^2 - I_{OL}^2}{(V_{OUT} + V_{OS})^2 - V_{OUT}^2} \times L \quad (14)$$

where

- $K_{IND}$  = Ripple ratio of the inductor ripple current ( $\Delta i_L / I_{OUT}$ )
- $I_{OL}$  = Low level output current during load transient
- $I_{OH}$  = High level output current during load transient
- $V_{US}$  = Target output voltage undershoot
- $V_{OS}$  = Target output voltage overshoot

For this design example, the target output ripple is 50 mV. Assume  $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C} = 50$  mV, and choose  $K_{IND} = 0.4$ . 方程式 11 yields ESR no larger than 25 mΩ and 方程式 12 yields  $C_{OUT}$  no smaller than 16.7 μF. For the target overshoot and undershoot range of this design,  $V_{US} = V_{OS} = 5\% \times V_{OUT} = 250$  mV. The  $C_{OUT}$  can be calculated to be no smaller than 180 μF and 79.2 μF by 方程式 13 and 方程式 14, respectively. In summary, the most stringent criteria for the output capacitor is 180 μF. Four 47 μF, 16 V, X7R ceramic capacitors with 5 mΩ ESR are used in parallel.

### 7.2.2.5 Schottky Diode Selection

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. The current rating for the diode must be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is much greater than the output voltage, the average diode current is lower. In this case, using a diode with a lower average current rating, approximately  $(1-D) \times I_{OUT}$ , is possible, however, the peak current rating must be higher than the maximum load current. A 6 A to 7 A rated diode is a good starting point.

### 7.2.2.6 Input Capacitor Selection

The LV14540 device requires high frequency input decoupling capacitor or capacitors and a bulk input capacitor, depending on the application. The typical recommended value for the high frequency decoupling capacitor is 4.7  $\mu$ F to 10  $\mu$ F. A high-quality ceramic capacitor type X5R or X7R with sufficiency voltage rating is recommended. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. Additionally, some bulk capacitance can be required, especially if the LV14540 circuit is not located within approximately 5 cm from the input voltage source. This capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace. For this design, two 2.2  $\mu$ F, X7R ceramic capacitors rated for 100 V are used. Use a 0.1  $\mu$ F for high-frequency filtering and place as close as possible to the device pins.

### 7.2.2.7 Bootstrap Capacitor Selection

Every LV14540 design requires a bootstrap capacitor ( $C_{BOOT}$ ). The recommended capacitor is 0.1  $\mu$ F and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

### 7.2.2.8 Soft-start Capacitor Selection

Use [方程式 15](#) to calculate the soft-start capacitor value:

$$C_{SS}(\text{nF}) = \frac{t_{SS}(\text{ms}) \times I_{SS}(\mu\text{A})}{V_{REF}(\text{V})} \quad (15)$$

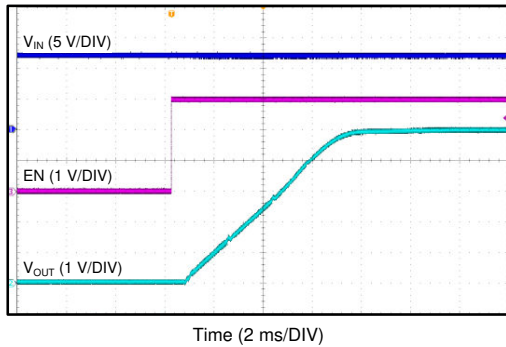
where

- $C_{SS}$  = Soft-start capacitor value
- $I_{SS}$  = Soft-start charging current (3  $\mu$ A)
- $t_{SS}$  = Desired soft-start time

For the desired soft-start time of 5 ms and soft-start charging current of 3  $\mu$ A, [方程式 15](#) yields a soft-start capacitor value of 20 nF, a standard 22 nF ceramic capacitor is used.

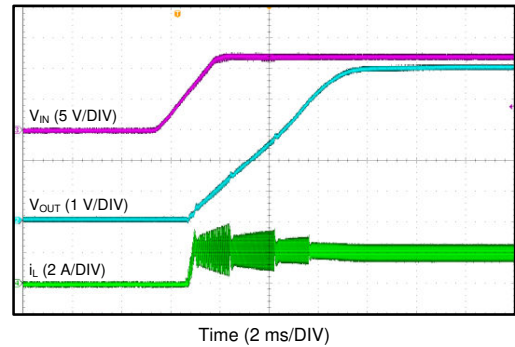
### 7.2.3 Application Curves

Unless otherwise specified, the following conditions apply:  $V_{IN} = 12\text{ V}$ ,  $f_{SW} = 300\text{ kHz}$ ,  $L = 6.5\text{ }\mu\text{H}$ ,  $C_{OUT} = 47\text{ }\mu\text{F}$   $\times 4$ ,  $T_A = 25^\circ\text{C}$



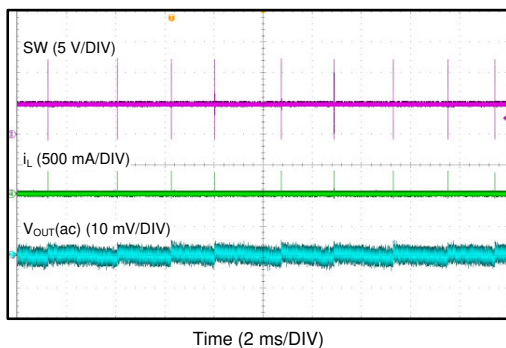
$V_{IN} = 12\text{ V}$        $V_{OUT} = 5\text{ V}$        $I_{OUT} = 2\text{ A}$

图 7-2. Start-Up by EN



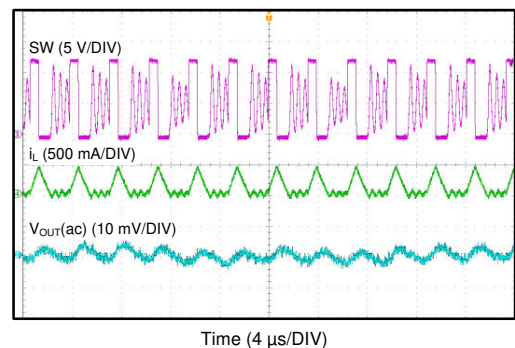
$V_{IN} = 12\text{ V}$        $V_{OUT} = 5\text{ V}$        $I_{OUT} = 2\text{ A}$

图 7-3. Start-Up by  $V_{IN}$



$V_{IN} = 12\text{ V}$        $V_{OUT} = 5\text{ V}$        $I_{OUT} = 0\text{ A}$

图 7-4. Pulse Skipping Mode



$V_{IN} = 12\text{ V}$        $V_{OUT} = 5\text{ V}$        $I_{OUT} = 100\text{ mA}$

图 7-5. DCM Mode

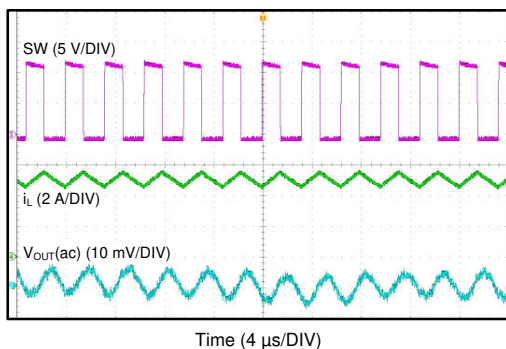
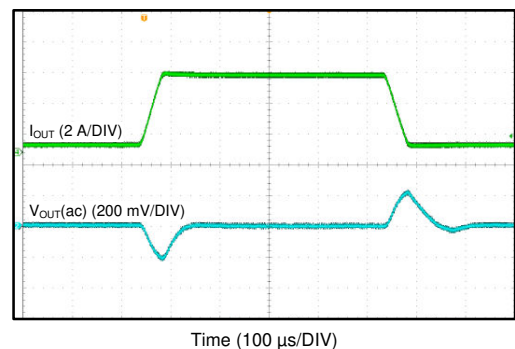


图 7-6. CCM Mode



$I_{OUT}$ : 10%  $\rightarrow$  100% Slew rate = 100 mA/  
of 5 A  $\mu\text{s}$

图 7-7. Load Transient

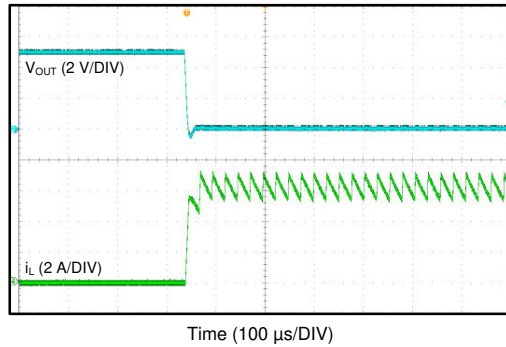

 $V_{IN} = 12\text{ V}$        $V_{OUT} = 5\text{ V}$ 

图 7-8. Output Short

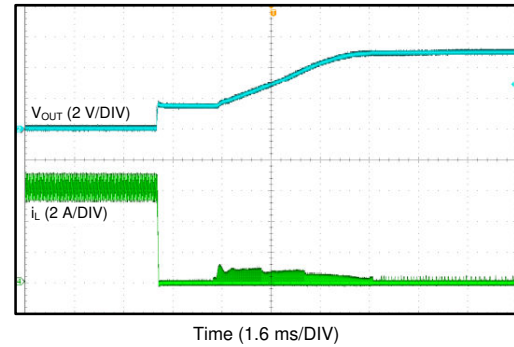

 $V_{IN} = 12\text{ V}$        $V_{OUT} = 5\text{ V}$ 

图 7-9. Output Short Recovery

### 7.3 Best Design Practices

- Do not exceed the [Absolute Maximum Ratings](#)
- Do not exceed the [Recommended Operating Conditions](#).
- Do not exceed the [ESD Ratings](#).
- Do not allow the EN input to float.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique design and PCB layout to help make the project a success.

### 7.4 Power Supply Recommendations

The LV14540 is designed to operate from an input voltage supply range between 4 V and 40 V. This input supply must be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LV14540 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LV14540, additional bulk capacitance can be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 47  $\mu\text{F}$  or 100  $\mu\text{F}$  electrolytic capacitor is a typical choice .

### 7.5 Layout

#### 7.5.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Close the feedback network, resistor  $R_{FBT}$  and  $R_{FBB}$ , to the FB pin.  $V_{OUT}$  sense path away from noisy nodes and preferably through a layer on the other side of a shielding layer.
2. Place the input bypass capacitor  $C_{IN}$  as close as possible to the VIN pin and ground. Grounding for both the input and output capacitors must consist of localized top side planes that connect to the GND pin and PAD.
3. Place the inductor L close to the SW pin to reduce magnetic and electrostatic noise.
4. Place the output capacitor,  $C_{OUT}$  close to the junction of L and the diode D. The L, D, and  $C_{OUT}$  trace must be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. Make the ground connection for the diode  $C_{IN}$  and  $C_{OUT}$  as small as possible and tied to the system ground plane in only one spot (preferably at the  $C_{OUT}$  ground point) to minimize conducted noise in the system ground plane.
6. For more detail on switching power supply layout considerations see [AN-1149 Layout Guidelines for Switching Power Supplies application report](#)

## 7.5.2 Layout Example

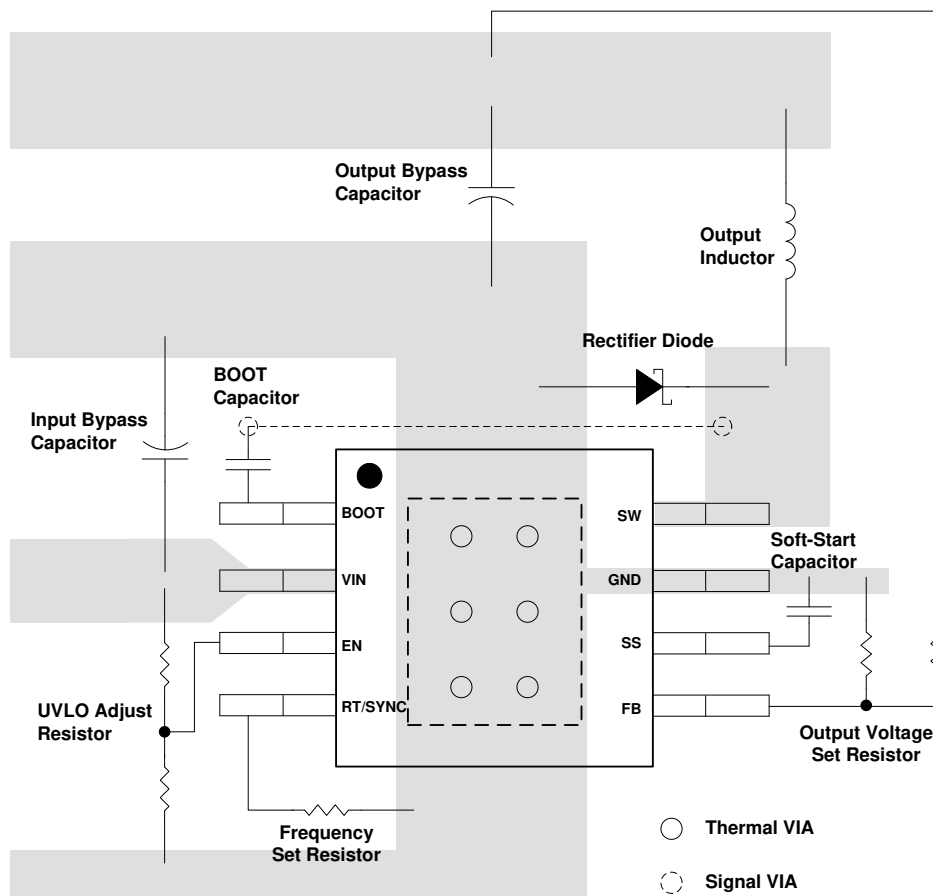


图 7-10. Layout

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, [AN-1149 Layout Guidelines for Switching Power Supplies application report](#)

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 8.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.

SIMPLE SWITCHER® is a registered trademark of TI .

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### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 术语表

[TI 术语表](#)      本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision * (June 2015) to Revision A (February 2024) | Page |
|-------------------------------------------------------------------|------|
| • 更新了整个文档中的表格、图和交叉参考的编号格式.....                                    | 1    |
| • 首次公开发布.....                                                     | 1    |
| • 通篇将 SOIC 更改为 HSOIC.....                                         | 1    |
| • 从器件名称中删除了 S.....                                                | 1    |
| • 更新了 <i>封装信息</i> 表的格式.....                                       | 1    |
| • Updated the TYPE column.....                                    | 3    |
| • Changed VIN, EN to GND MAX from 44 to 45.....                   | 4    |
| • Changed BOOT to GND MAX from 49 to 50.....                      | 4    |
| • Updated <i>ESD Ratings</i> table to current TI standards.....   | 4    |
| • Updated <a href="#">方程式 5</a> .....                             | 13   |
| • Updated <a href="#">表 6-1</a> .....                             | 13   |
| • Added the <i>Device Functional Modes</i> section.....           | 16   |
| • Updated <a href="#">方程式 8</a> .....                             | 18   |

- 
- Added the *Best Design Practices* section.....[22](#)
- 

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LV14540DDAR      | ACTIVE        | SO PowerPAD  | DDA                | 8    | 2500           | RoHS & Green    | NIPDAU   NIPDAUAG                    | Level-2-260C-1 YEAR  | -40 to 125   | 14540                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

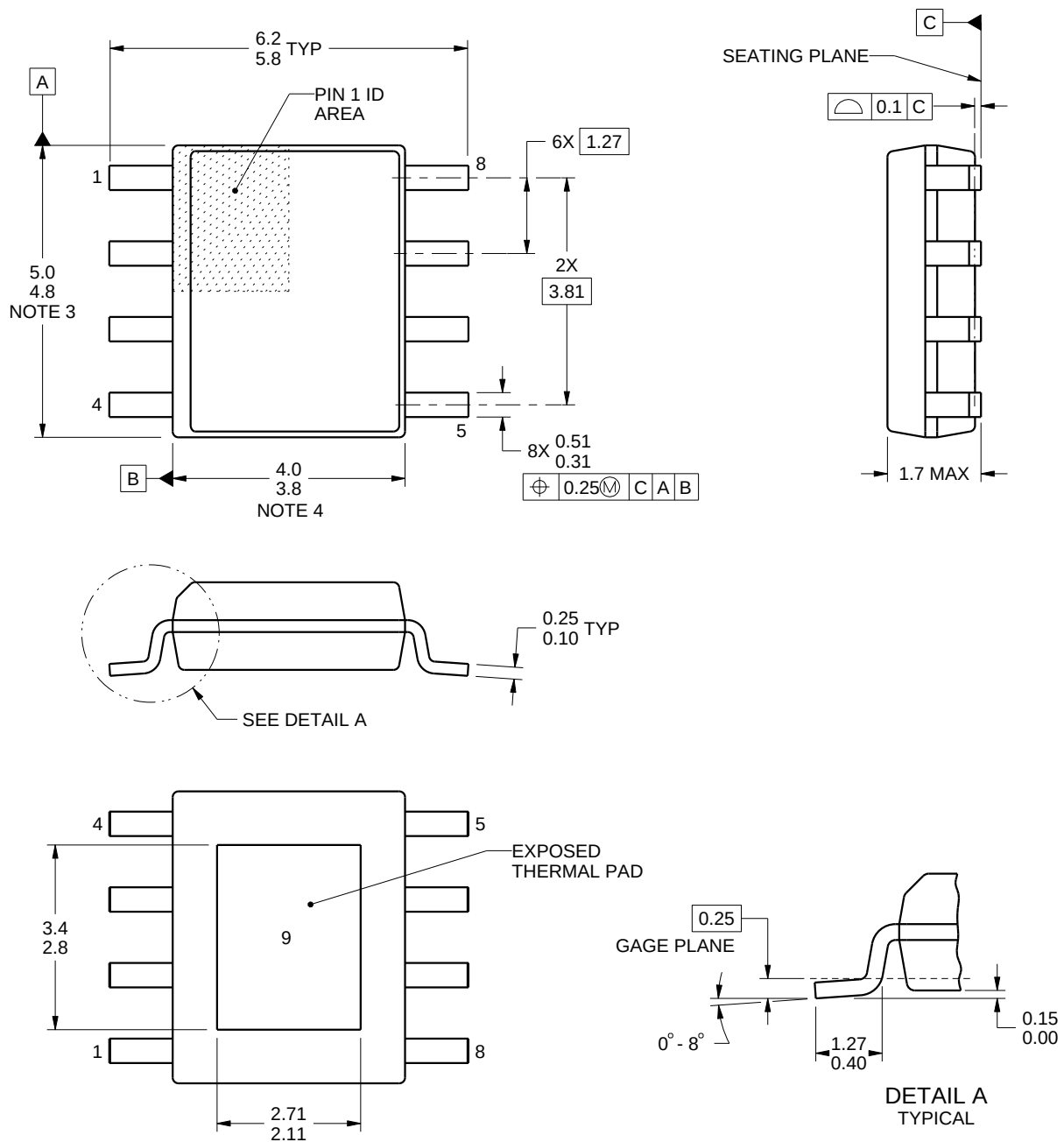
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**DDA0008B**

# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4214849/A 08/2016

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

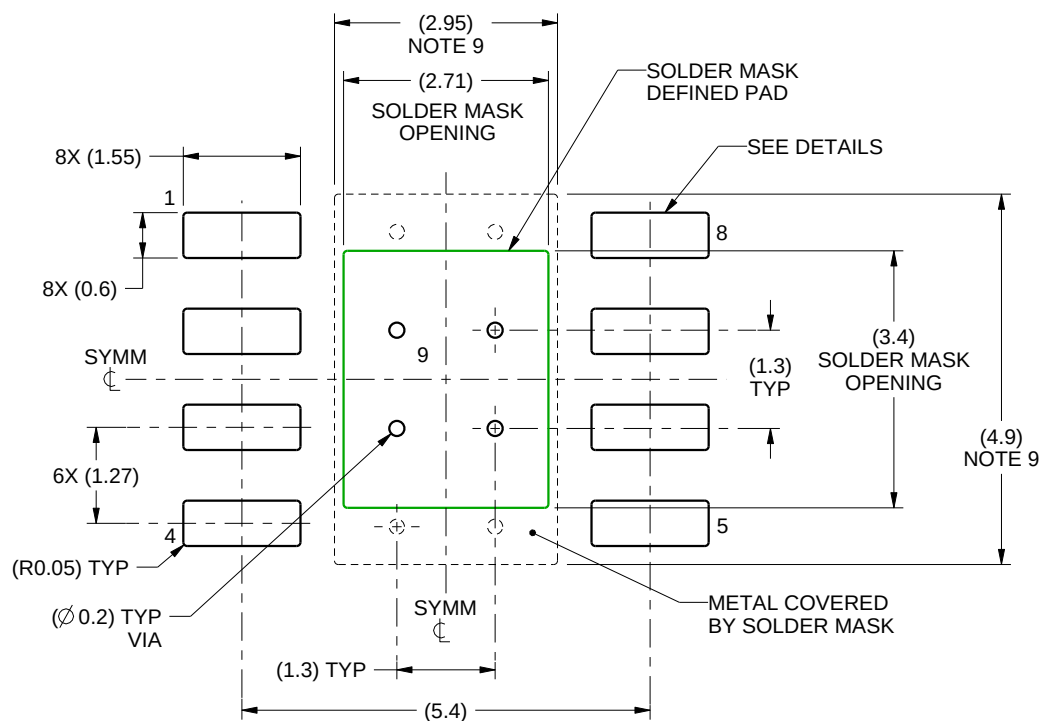
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

# EXAMPLE BOARD LAYOUT

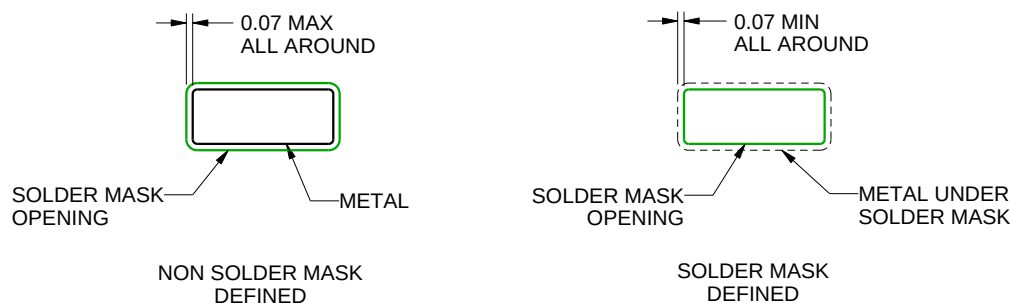
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

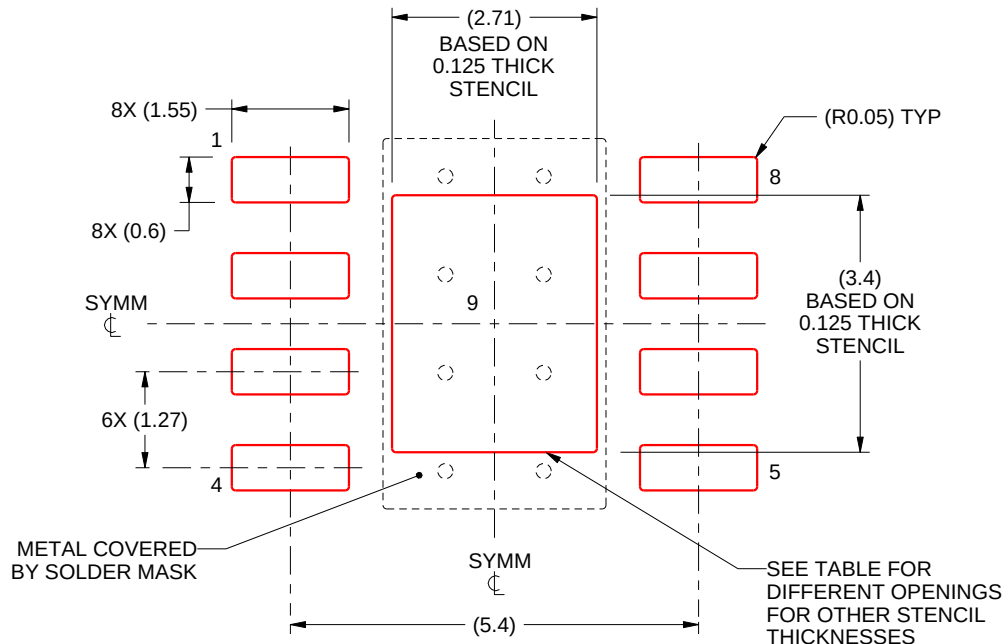
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 3.03 X 3.80            |
| 0.125             | 2.71 X 3.40 (SHOWN)    |
| 0.150             | 2.47 X 3.10            |
| 0.175             | 2.29 X 2.87            |

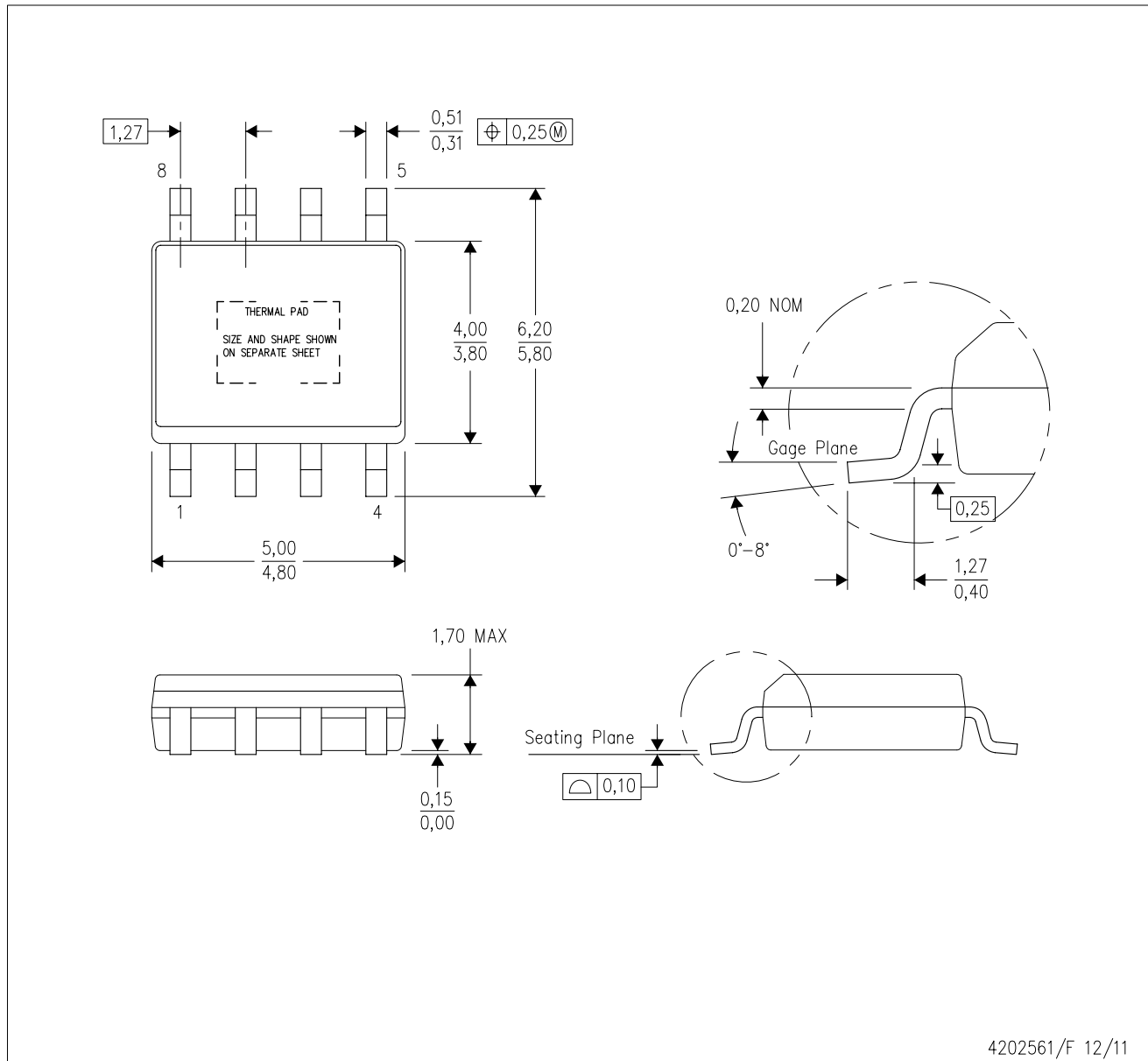
4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - This package complies to JEDEC MS-012 variation BA

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DDA (R-PDSO-G8)

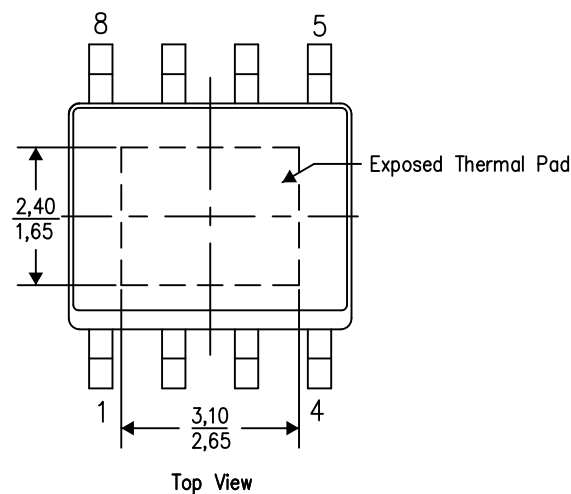
PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

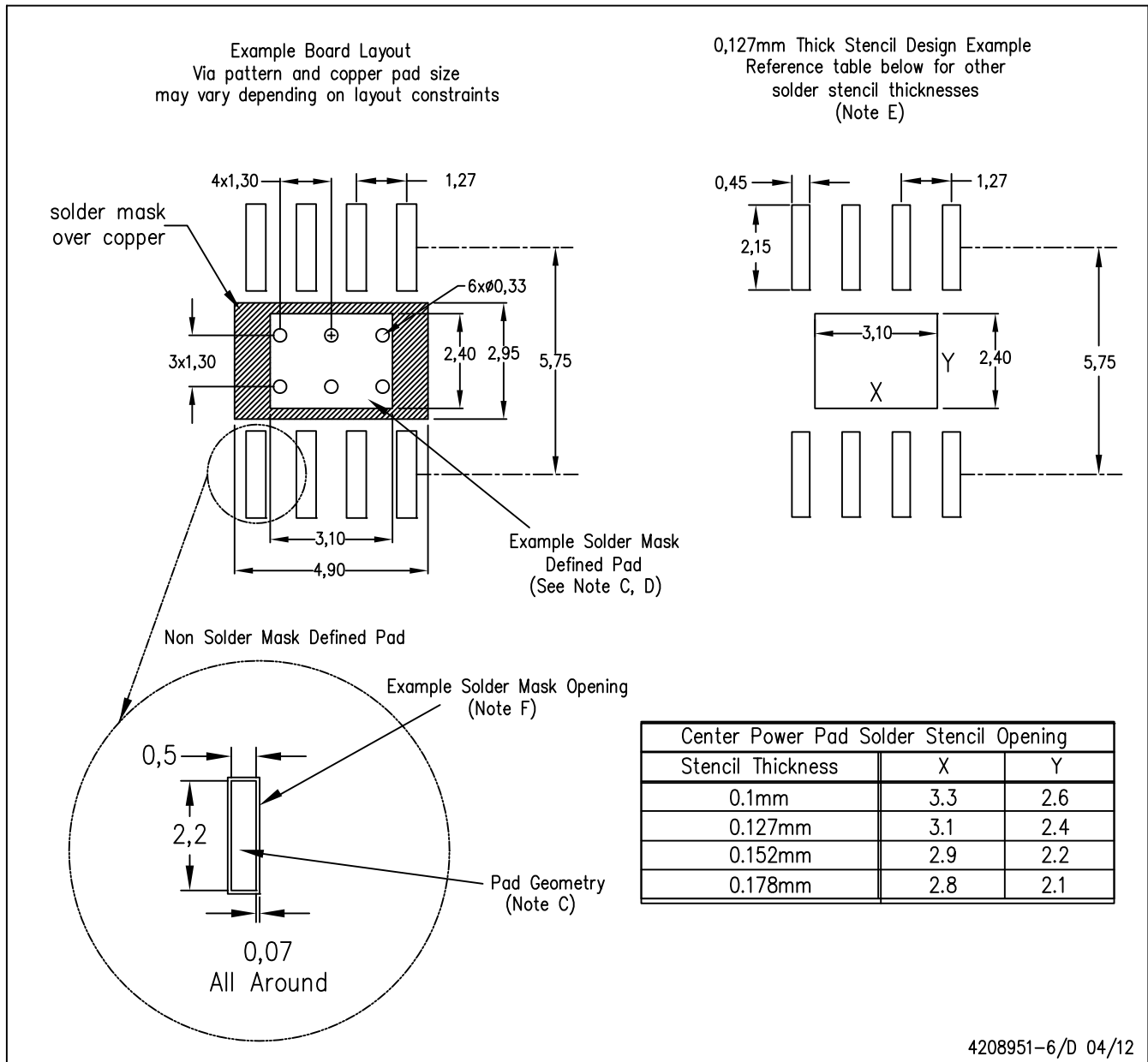
4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

## 重要声明和免责声明

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