

TPS3809xxx-Q1 3 引脚电源监控器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
 - 器件温度 1 级：-40°C 至 +125°C 环境温度范围
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C5
- 3 引脚 SOT-23 封装
- 电源电流为 9μA (典型值)
- 精密电源电压监控器：2.5V、3V、3.3V、5V
- 固定延时时间为 200ms 的上电复位发生器
- 与 MAX 809 引脚对引脚兼容

2 应用

- 汽车摄像头系统
- 远程信息处理系统
- 汽车仪表组
- 发动机控制
- 环视系统

3 说明

TPS3809 系列监控电路主要为 DSP 及基于处理器的系统提供电路初始化和计时监控功能。新款 TLV809E 器件是具有相同引脚、功能和电气参数的替代产品。

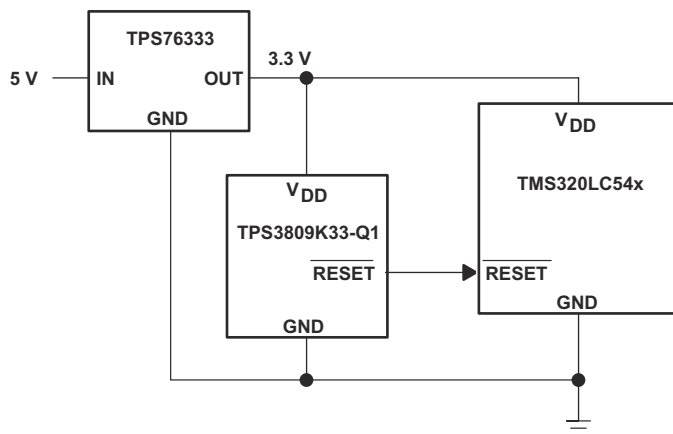
上电期间，如果电源电压 V_{DD} 大于 1.1V， $\overline{RESET}$ 就会生效。因此，只要 V_{DD} 保持在阈值电压 V_{IT} 以下，监控电路就会监测 V_{DD} ，并使 $\overline{RESET}$ 保持有效状态。内部计时器将会延迟输出恢复至无效状态（高电平）的时间，以确保系统正常复位。延时时间 $t_{d(typ)} = 200ms$ ，从 V_{DD} 上升至高于阈值电压 V_{IT} 后开始计时。电源电压降至阈值电压 V_{IT} 以下时，输出再次变为有效状态（低电平）。无需外部组件。该系列所有器件均具有由内部分压器设定的固定检测阈值电压 V_{IT} 。

该产品系列旨在用于 2.5V、3V、3.3V 和 5V 电源电压。这些电路都采用 3 引脚 SOT-23 封装。TPS3809xxx-Q1 器件的工作温度范围为 -40°C 至 +125°C，符合集成电路 AEC-Q100 应力测试认证的要求。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS3809xxx-Q1	SOT-23 (3)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (March 2016) to Revision C (December 2020)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 在说明部分添加了有关新款 TLV809E 的描述.....	1
• Renamed <i>Device Comparison</i> modified device option table and added comparison table	3
• Changed VDD from 7 to 6.5 in <i>Absolute Maximum Ratings</i>	4
• Changed V _{OL} @ 500 μ A from 0.2 to 0.3 in <i>Electrical Characteristics</i>	5
• Changed t _w pulse duration from 3 to 10 μ s in <i>Timing Requirements</i>	5
• Changed t _{P_{HL}} from 1 to 10 μ s in <i>Switching Characteristics</i>	5
• Deleted figure for Minimum Pulse Duration At V _{DD} in Typical Characteristics.....	7

Changes from Revision A (December 2002) to Revision B (February 2016)	Page
• 在项目符号中添加了符合 AEC-Q100 标准的信息.....	1
• 更改了应用列表项.....	1
• 添加了 ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• Changed device part numbers by adding -Q1 to them throughout document	5

5 Device Comparison

表 5-1. Device Threshold Options

PRODUCT	THRESHOLD VOLTAGE
TPS3809J25QDBVRQ1	2.25 V
TPS3809L30QDBVRQ1	2.64 V
TPS3809K33QDBVRQ1	2.93 V
TPS3809I50QDBVRQ1	4.55 V

表 5-2. Device Family Comparison

DEVICE	FUNCTION
TLV803	Open-Drain, RESET Output
TLV809	Push-Pull, RESET Output
TLV810	Push-Pull, RESET Output

6 Pin Configuration and Functions

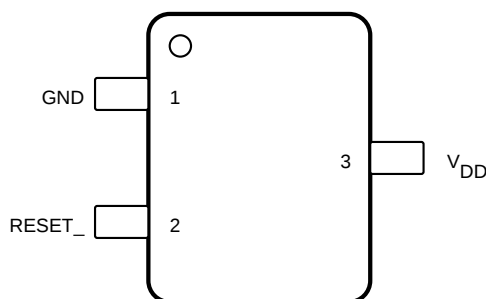


图 6-1. DBV Package
3-Pin SOT-23
Top View

6.1 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground
RESET	2	O	Reset output
V _{DD}	3	I	Supply voltage and supervising input

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V_{DD} ⁽²⁾		6.5	V
All other pins ⁽²⁾	- 0.3	6.5	V
Maximum low output current, I_{OL}		5	mA
Maximum high output current, I_{OH}		- 5	mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	- 20	20	mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	- 20	20	mA
Continuous total power dissipation			
Operating free-air temperature range, T_A	- 40	125	°C
Storage temperature, T_{stg}	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 6.5 V for more than $t = 1000$ h continuously.

7.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
	Charged-device model (CDM), per AEC Q100-011	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{DD} Supply voltage	2		6	V
T_A Operating free-air temperature	- 40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3809xxx-Q1	UNIT
		DBV (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	232.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	187.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	104.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	40.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	104.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V _{OH}	High-level output voltage	V _{DD} = 2.5 V to 6 V, I _{OH} = -500 μA		V _{DD} - 0.2		V		
		V _{DD} = 3.3 V, I _{OH} = -2 μA		V _{DD} - 0.4				
		V _{DD} = 6 V, I _{OH} = -4 mA	T _A = -40°C to +25°C	V _{DD} - 0.4				
			T _A = 125°C	V _{DD} - 0.5				
V _{OL}	Low-level output voltage	V _{DD} = 2 V to 6 V, I _{OL} = 500 μA		0.3		V		
		V _{DD} = 3.3 V, I _{OL} = 2 mA		0.4				
		V _{DD} = 6 V, I _{OL} = 4 mA		0.4				
Power-up reset voltage ⁽¹⁾		V _{DD} ≥ 1.1 V, I _{OL} = 50 μA		0.2		V		
V _{IT-}	Negative-going input threshold voltage ⁽²⁾	TPS3809J25-Q1	T _A = -40°C to +125°C		2.20	2.25	2.30	V
		TPS3809L30-Q1			2.58	2.64	2.7	
		TPS3809K33-Q1			2.87	2.93	2.99	
		TPS3809I50-Q1	T _A = -40°C to +85°C		4.45	4.55	4.65	
			T _A = -40°C to +125°C		4.4	4.55	4.65	
V _{hys}	Hysteresis	TPS3809J25-Q1			30		mV	
		TPS3809L30-Q1			35			
		TPS3809K33-Q1			40			
		TPS3809I50-Q1			60			
I _{DD}	Supply current	V _{DD} = 2 V, Output unconnected		9	15	μA		
		V _{DD} = 6 V, Output unconnected		20	30			
C _i	Input capacitance	V _I = 0 V to V _{DD}		5		pF		

(1) The lowest supply voltage at which RESET becomes active. t_r, V_{DD} $\geq$ 15 μ s/V.

(2) To ensure best stability of the threshold voltage, a bypass capacitor (0.1 μ F, ceramic) should be placed near the supply terminals.

7.6 Timing Requirements

R_L = 1 M Ω , C_L = 50 pF, T_A = 25°C

			MIN	NOM	MAX	UNIT
t _w	Pulse width at V _{DD}	V _{DD} = V _{IT-} + 0.2 V, V _{DD} = V _{IT-} - 0.2 V	10			μ s

7.7 Switching Characteristics

R_L = 1 M Ω , C_L = 50 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _d	Delay time	V _{DD} $\geq$ V _{IT-} + 0.2 V, See timing diagram, 节 7.8	120	200	280	ms
t _{PHL}	Propagation (delay) time, high-to-low-level output	V _{DD} to RESET delay V _{IL} = V _{IT-} - 0.2 V, V _{IH} = V _{IT-} + 0.2 V		10		μ s

7.8 Timing Diagrams

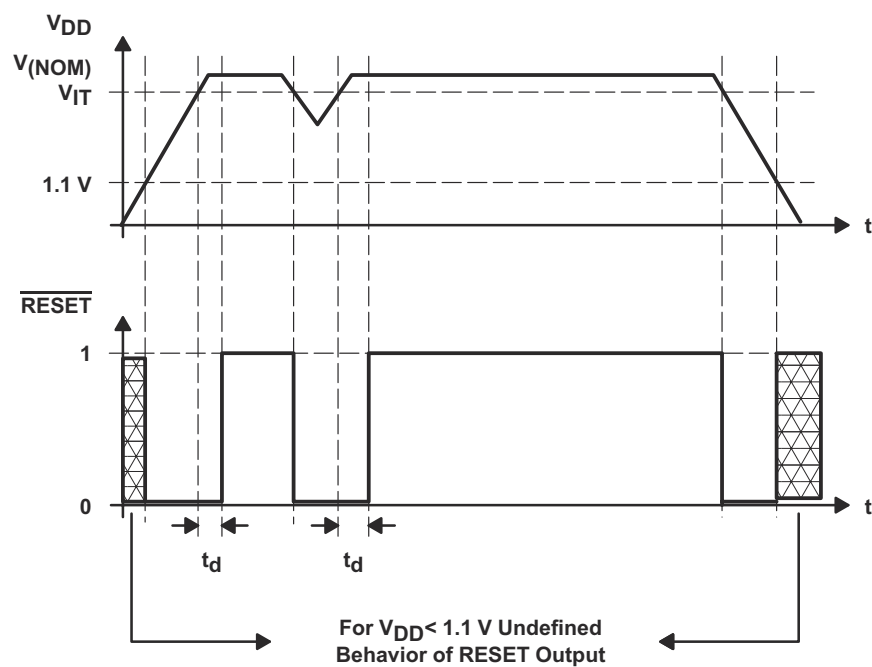


图 7-1. Timing Diagram

7.9 Typical Characteristics

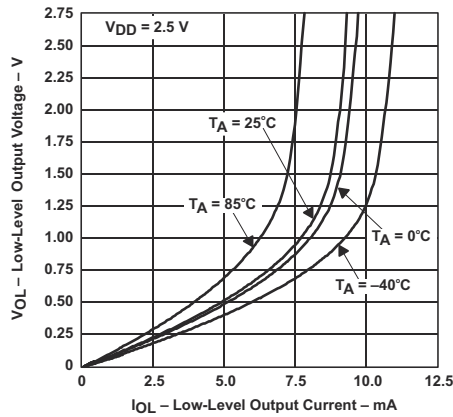


图 7-2. Low-Level Output Voltage vs Low-Level Output Current

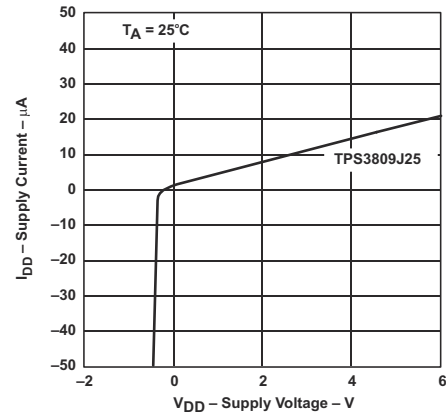


图 7-3. Supply Current vs Supply Voltage

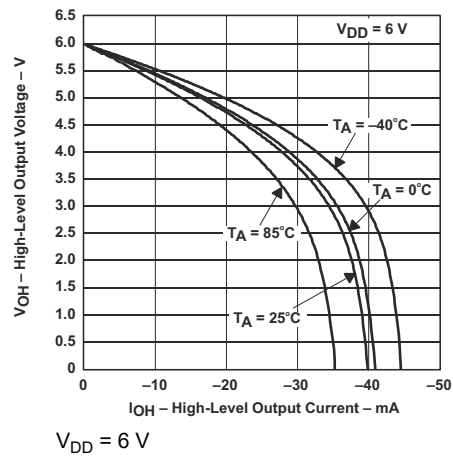


图 7-4. High-Level Output Voltage vs High-Level Output Current

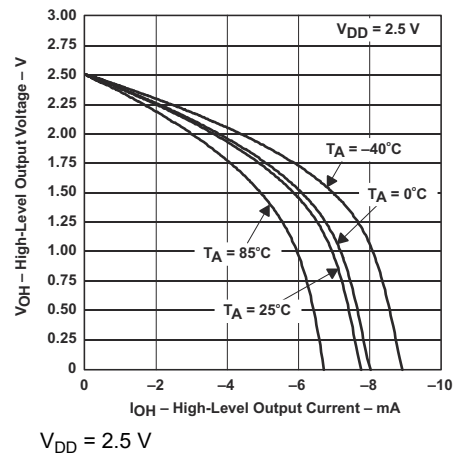


图 7-5. High-Level Output Voltage vs High-Level Output Current

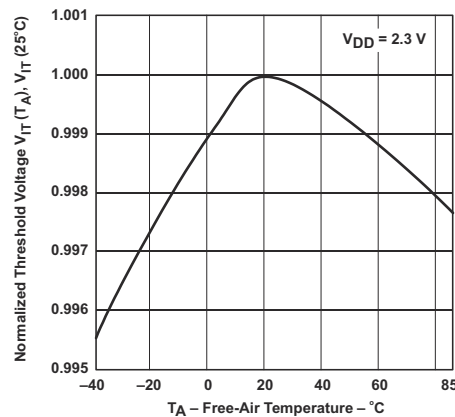


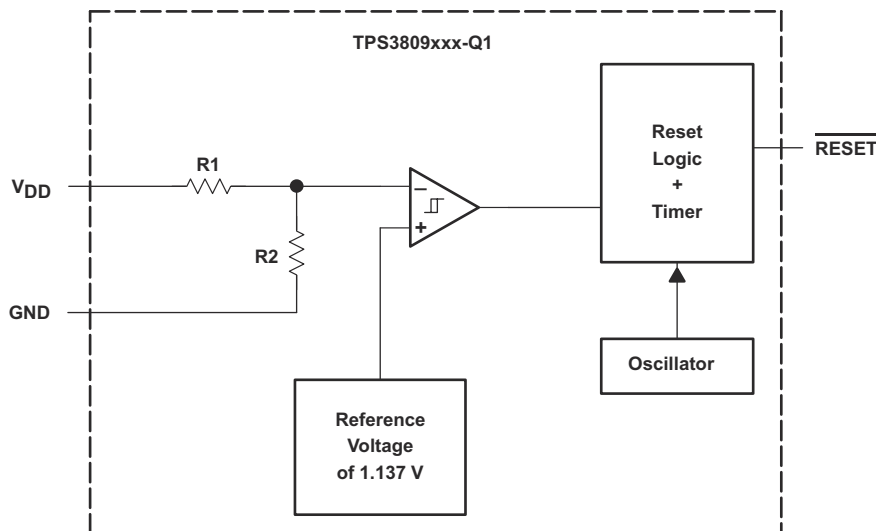
图 7-6. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

8 Detailed Description

8.1 Overview

The TPS3809xxx-Q1 device is a low-current supervisory circuit for monitoring system voltages above 2 V. The device asserts an active-low $\overline{\text{RESET}}$ signal when VDD drops below a preset threshold. The $\overline{\text{RESET}}$ output remains low until VDD returns above its threshold. The device design is also to be relatively immune to short negative transients on the VDD pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 VDD Monitoring

The VDD pin provides a terminal at which a system voltage can be monitored. If the voltage on this pin drops below V_{IT} , $\overline{\text{RESET}}$ is asserted low. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and deassertions. Refer to [§ 5](#) to determine the VDD voltage threshold for each device.

8.4 Device Functional Modes

TPS3809xxx-Q1 monitors one supply using the VDD pin. When VDD is above the V_{IT} threshold for the device, $\overline{\text{RESET}}$ will be high. When VDD is below the V_{IT} threshold for the device, $\overline{\text{RESET}}$ will be low.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TPS3809xxx-Q1 voltage supervisor device design asserts an active-low RESET signal when V_{DD} drops below a voltage threshold V_{IT} . The RESET signal remains low until the voltage returns above its threshold. The typical application is with a processor or microcontroller, which needs to be reset when the supply rail drops below a specified tolerance.

9.2 Typical Application

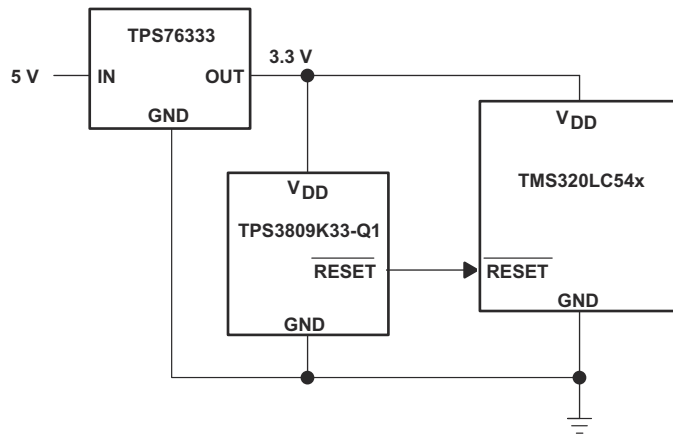


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

Each device has a fixed-voltage monitoring threshold, and the device should be chosen based on the voltage being monitored. Refer to [节 5](#) to determine the V_{DD} voltage threshold for each device. In this example, a 3.3V supply rail to a microcontroller will be monitored.

9.2.2 Detailed Design Procedure

Because a 3.3-V supply rail needs to be monitored, TPS3809K33-Q1 should be used. This device has a 2.93-V threshold for reset. Connect the 3.3-V supply to the V_{DD} pin and the reset output of the supervisor to the reset pin of the microcontroller.

9.2.3 Application Curves

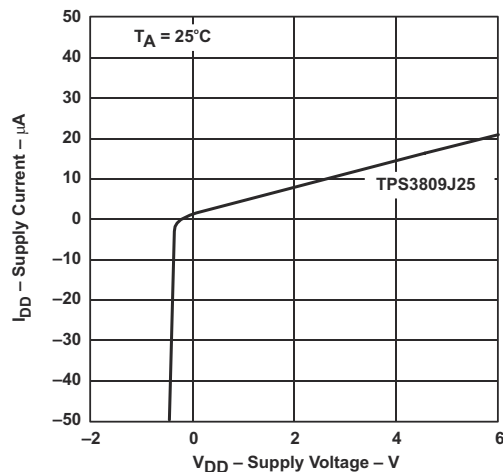


图 9-2. Supply Current vs Supply Voltage

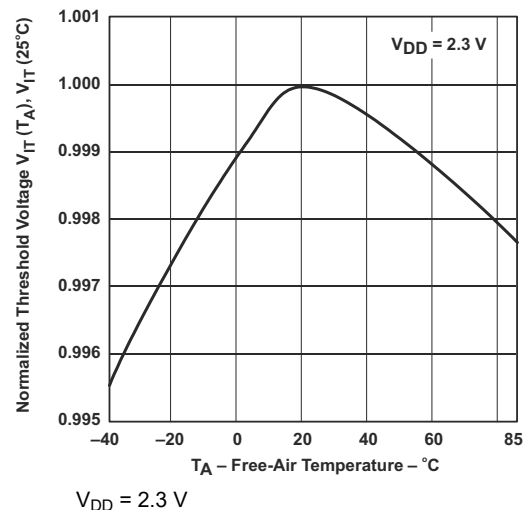


图 9-3. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

10 Power Supply Recommendations

The TPS3809xxx-Q1 device design operates from an input supply from 2 V to 6 V. TI recommends placing a 0.1- μ F capacitor near the V_{DD} pin.

11 Layout

11.1 Layout Guidelines

TI recommends placing the 0.1- μ F decoupling capacitor close to the V_{DD} pin. The V_{DD} and GND traces should be able to carry 30 μ A without a significant drop in voltage.

11.2 Layout Example

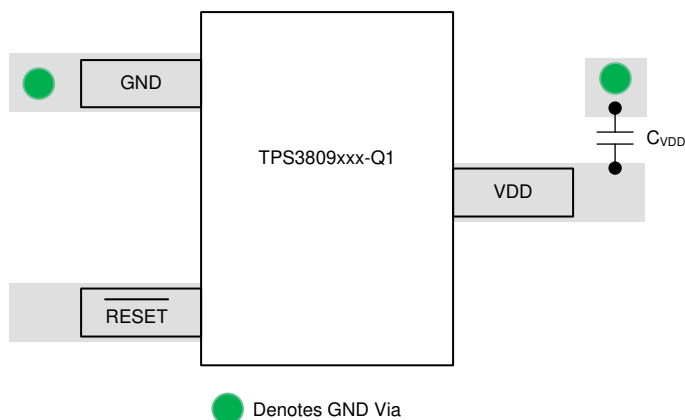


图 11-1. Layout Example

12 Device and Documentation Support

12.1 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

12.3 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.4 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
2T09I50QDBVRG4Q	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDCQ	Samples
TPS3809I50QDBVRQ1	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDCQ	Samples
TPS3809K33QDBVRQ1	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDBQ	Samples
TPS3809L30QDBVRQ1	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PDAQ	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

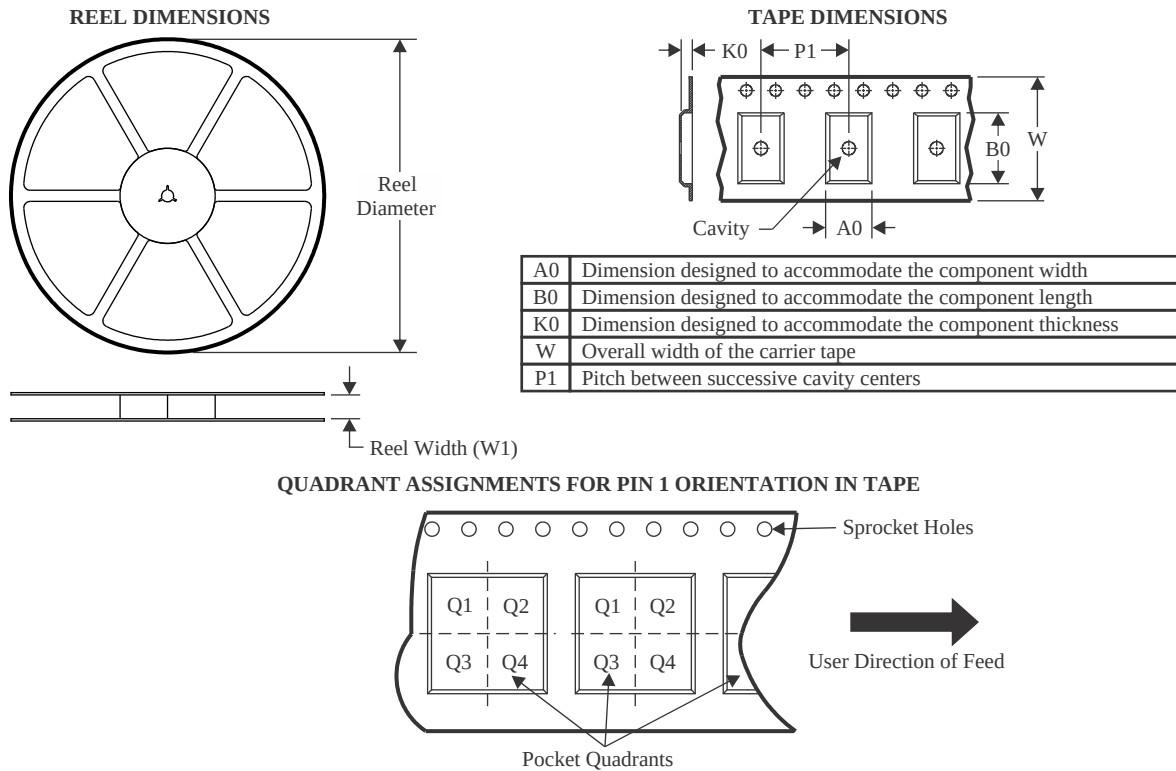
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

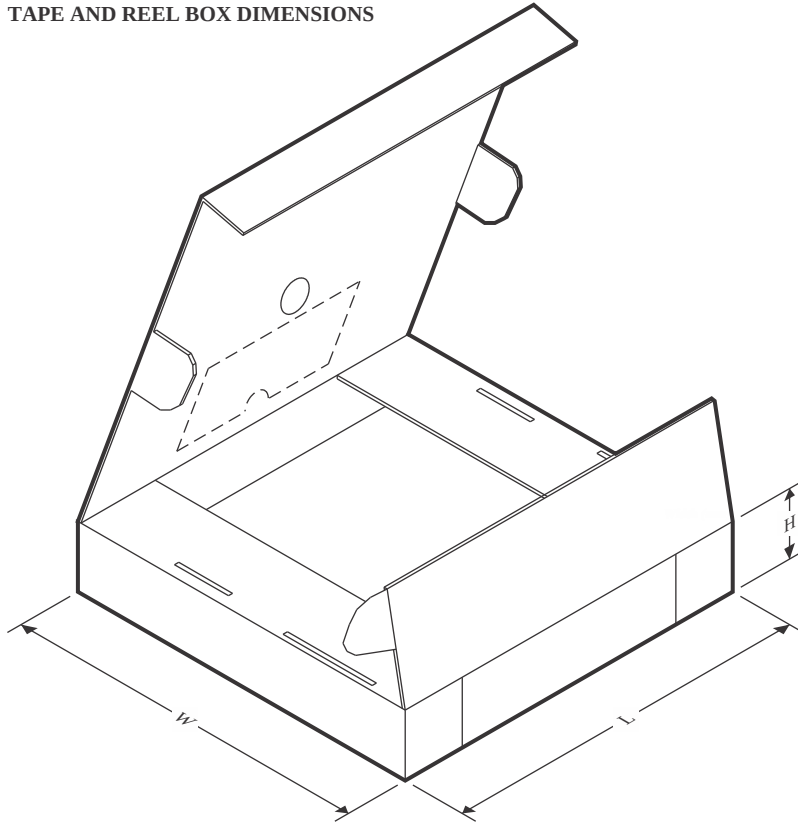
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
2T09I50QDBVRG4Q	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3809I50QDBVRQ1	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3809K33QDBVRQ1	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS3809L30QDBVRQ1	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

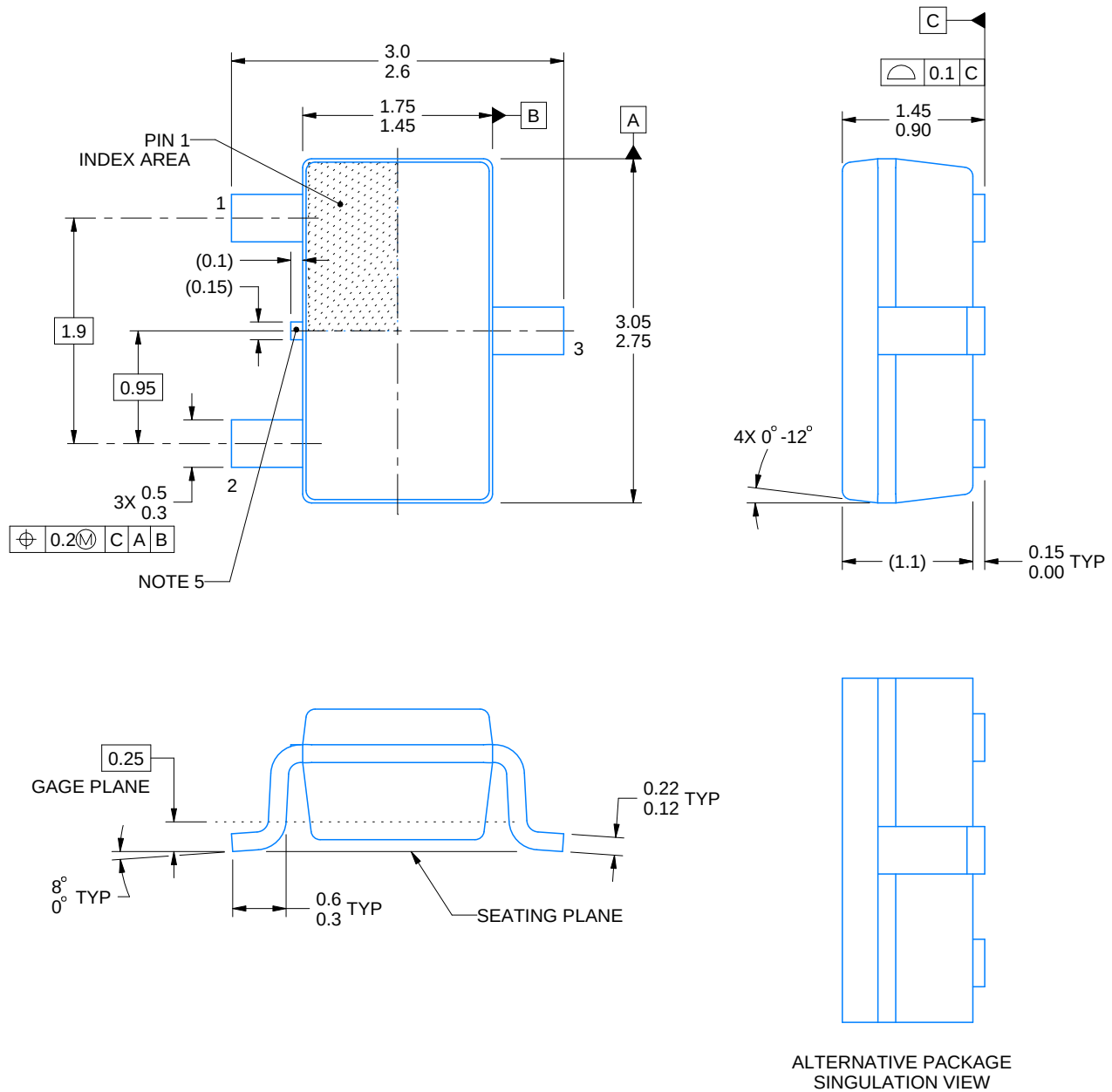


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
2T09I50QDBVRG4Q	SOT-23	DBV	3	3000	180.0	180.0	18.0
TPS3809I50QDBVRQ1	SOT-23	DBV	3	3000	180.0	180.0	18.0
TPS3809K33QDBVRQ1	SOT-23	DBV	3	3000	180.0	180.0	18.0
TPS3809L30QDBVRQ1	SOT-23	DBV	3	3000	180.0	180.0	18.0

DBV0003A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



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NOTES:

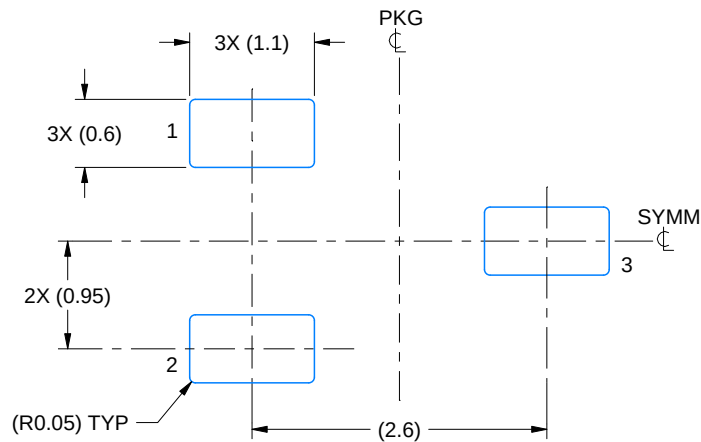
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

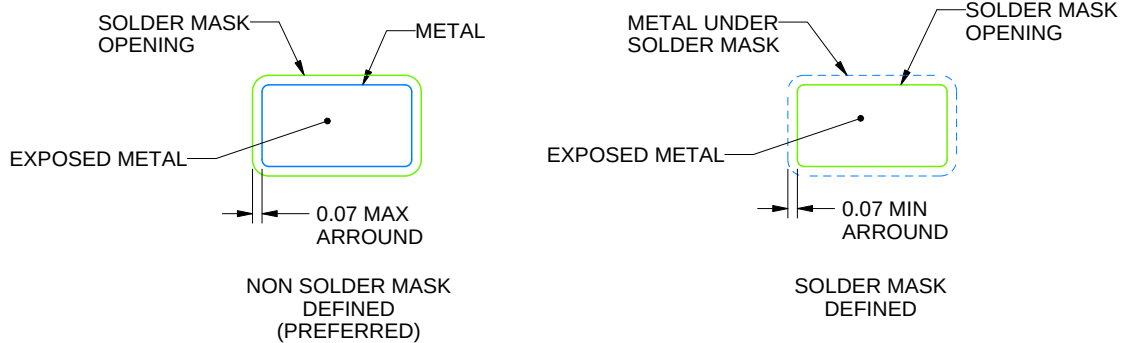
DBV0003A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

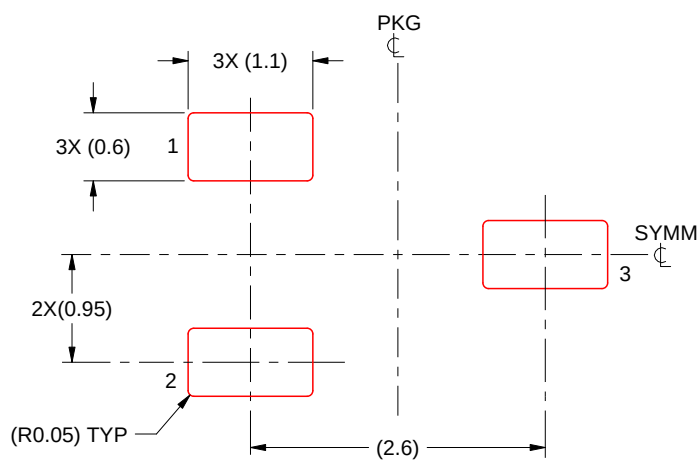
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0003A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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