

SN74AHC157-Q1 汽车类 四通道 2 位至 1 位数据选择器/多路复用器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
 - 器件温度等级 1：-40°C 至 +125°C
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C4B
- 采用具有可湿性侧面的 QFN 封装
- 工作范围为 2V 至 5.5V V_{CC}
- 低延迟，12ns ($V_{CC} = 5V$, $C_L = 50pF$)
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 具有共享数据总线的存储器器件选项
- 减少片选应用所需的输出数量
- [路由数据](#)

3 说明

SN74AHC157-Q1 是一款四通道 2 线至 1 线数据选择器多路复用器，采用 2V 至 5.5V V_{CC} 电压供电。这些 SN74AHC157-Q1 器件具有一个常见选通 ($\bar{G}$) 输入。当选通脉冲为高电平时，所有输出都为低电平。当选通脉冲为低电平时，从两个源之一选择一个 4 位字并将其发送到四个输出。该器件提供真实数据。

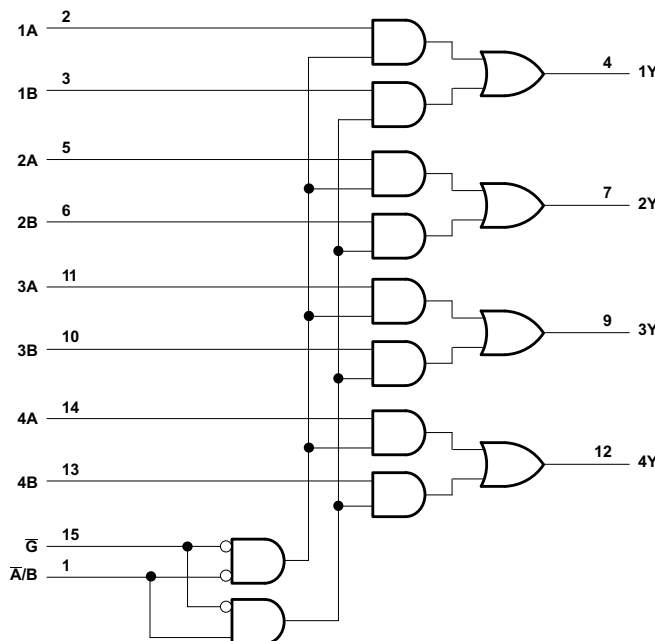
封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	封装尺寸 (标称值) ⁽³⁾
SN74AHC157-Q1	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm

(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)

(3) 封装尺寸 (长 × 宽) 为标称值，不包括引脚。



所示引脚编号用于 D、DB、DGV、J、N、NS、PW、RGY 和 W 封装。

逻辑图 (正逻辑)



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4 Pin Configuration and Functions

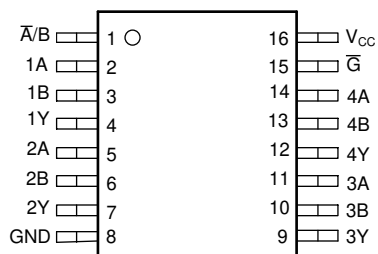


图 4-1. PW Package, 16-Pin TSSOP (Top View)

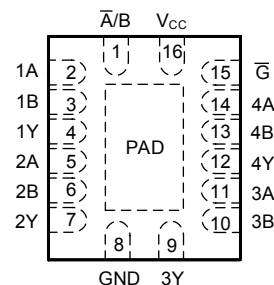


图 4-2. WBQB Package, 16-Pin WQFN (Transparent Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
A/B	1	I	Address select
1A	2	I	Channel 1, data input A
1B	3	I	Channel 1, data input B
1Y	4	I	Channel 1, data output
2A	5	O	Channel 2, data input A
2B	6	O	Channel 2, data input B
2Y	7	I	Channel 2, data output
GND	8	G	Ground
3Y	9	I	Channel 3, data output
3B	10	I	Channel 3, data input B
3A	11	I	Channel 3, data input A
4Y	12	I	Channel 4, data output
4B	13	I	Channel 4, data input B
4A	14	I	Channel 4, data input A
G	15	I	Output strobe, active low
V _{CC}	16	P	Positive supply
Thermal pad ⁽²⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.

(2) WBQB package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range ⁽²⁾		-0.5	7	V
V_O	Output voltage range ⁽²⁾		-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < -0.5V$		-20	mA
I_{OK}	Output clamp current	$V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±75	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2V$	1.5		V
		$V_{CC} = 3V$	2.1		
		$V_{CC} = 5.5V$	3.85		
V_{IL}	Low-Level input voltage	$V_{CC} = 2V$		0.5	V
		$V_{CC} = 3V$		0.9	
		$V_{CC} = 5.5V$		1.65	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2V$		-50	μA
		$V_{CC} = 3.3V \pm 0.3V$		-4	mA
		$V_{CC} = 5V \pm 0.5V$		-8	mA
I_{OL}	Low-level output current	$V_{CC} = 2V$		50	μA
		$V_{CC} = 3.3V \pm 0.3V$		4	mA
		$V_{CC} = 5V \pm 0.5V$		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3V \pm 0.3V$		100	ns/V
		$V_{CC} = 5V \pm 0.5V$		20	ns/V

5.3 Recommended Operating Conditions (续)

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
T _A	Operating free-air temperature		- 40	125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		WBQB (WQFN)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	105.6	135.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	96.6	70.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	75.4	81.3	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	19.1	22.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	75.4	80.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	56.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = - 50 μA	2V to 5.5V	V _{CC} -0.1	V _{CC}		V _{CC} -0.1	V _{CC}		V
	I _{OH} = -4mA	3V	2.58			2.48			
	I _{OH} = -8mA	4.5V	3.94			3.8			
V _{OL}	I _{OL} = 50 μA	2V to 5.5V			0.1			0.1	V
	I _{OL} = 4mA	3V			0.36			0.44	
	I _{OL} = 8mA	4.5V			0.36			0.44	
I _I	V _I = 5.5V or GND and V _{CC} = 0 V to 5.5V	0 V to 5.5V			±0.1			±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0, and V _{CC} = 5.5V	5.5V			4			40	μA
C _I	V _I = V _{CC} or GND	5V		2	10			10	pF
C _{PD}	No load, F = 1MHz	5V		87					pF

5.6 Switching Characteristics

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PHL}	A or B	Any Y	C _L = 15pF	3.3V ± 0.3V	4.2	9.3		1	11		1	11.5		ns
t _{PLH}	A or B	Any Y	C _L = 15pF	3.3V ± 0.3V	4.2	9.3		1	11		1	11.5		ns
t _{PHL}	$\overline{G}$	Any Y	C _L = 15pF	3.3V ± 0.3V	8.7	13.6		1	16		1	16		ns
t _{PLH}	$\overline{G}$	Any Y	C _L = 15pF	3.3V ± 0.3V	8.7	13.6		1	16		1	16		ns
t _{PHL}	$\overline{A/B}$	Any Y	C _L = 15pF	3.3V ± 0.3V	5.2	11		1	13		1	14		ns
t _{PLH}	$\overline{A/B}$	Any Y	C _L = 15pF	3.3V ± 0.3V	5.2	11		1	13		1	14		ns
t _{PHL}	A or B	Any Y	C _L = 50pF	3.3V ± 0.3V	6	12.8		1	14.5		1	15		ns
t _{PLH}	A or B	Any Y	C _L = 50pF	3.3V ± 0.3V	6	12.8		1	14.5		1	15		ns
t _{PHL}	$\overline{G}$	Any Y	C _L = 50pF	3.3V ± 0.3V	11.2	17.1		1	19.5		1	19.5		ns

5.6 Switching Characteristics (续)

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	$\overline{G}$	Any Y	C _L = 50pF	3.3V ± 0.3V	11.2	17.1		1	19.5		1	19.5		ns
t _{PHL}	$\overline{A/B}$	Any Y	C _L = 50pF	3.3V ± 0.3V	7.4	14.5		1	16.5		1	18.5		ns
t _{PLH}	$\overline{A/B}$	Any Y	C _L = 50pF	3.3V ± 0.3V	7.4	14.5		1	16.5		1	18.5		ns
t _{PHL}	A or B	Any Y	C _L = 15pF	5V ± 0.5V	2.9	5.9		1	7		1	7.5		ns
t _{PLH}	A or B	Any Y	C _L = 15pF	5V ± 0.5V	2.9	5.9		1	7		1	7.5		ns
t _{PHL}	$\overline{G}$	Any Y	C _L = 15pF	5V ± 0.5V	5.6	8.6		1	10		1	10		ns
t _{PLH}	$\overline{G}$	Any Y	C _L = 15pF	5V ± 0.5V	5.6	8.6		1	10		1	10		ns
t _{PHL}	$\overline{A/B}$	Any Y	C _L = 15pF	5V ± 0.5V	3.5	6.8		1	8		1	8.5		ns
t _{PLH}	$\overline{A/B}$	Any Y	C _L = 15pF	5V ± 0.5V	3.5	6.8		1	8		1	8.5		ns
t _{PHL}	A or B	Any Y	C _L = 50pF	5V ± 0.5V	4.2	7.9		1	9		1	9.5		ns
t _{PLH}	A or B	Any Y	C _L = 50pF	5V ± 0.5V	4.2	7.9		1	9		1	9.5		ns
t _{PHL}	$\overline{G}$	Any Y	C _L = 50pF	5V ± 0.5V	7.1	10.6		1	12		1	12		ns
t _{PLH}	$\overline{G}$	Any Y	C _L = 50pF	5V ± 0.5V	7.1	10.6		1	12		1	12		ns
t _{PHL}	$\overline{A/B}$	Any Y	C _L = 50pF	5V ± 0.5V	5	8.8		1	10		1	11.5		ns
t _{PLH}	$\overline{A/B}$	Any Y	C _L = 50pF	5V ± 0.5V	5	8.8		1	10		1	11.5		ns

5.7 Noise Characteristics

V_{CC} = 5V, C_L = 50 pF, T_A = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.2	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}	-0.9	-0.2		V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	4.4	4.7		V
V _{IH(D)}	High-level dynamic input voltage	3.5			V
V _{IL(D)}	Low-level dynamic input voltage			1.5	V

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

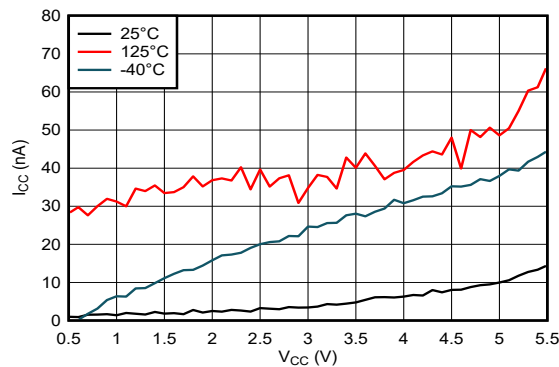


图 5-1. Supply Current Across Supply Voltage

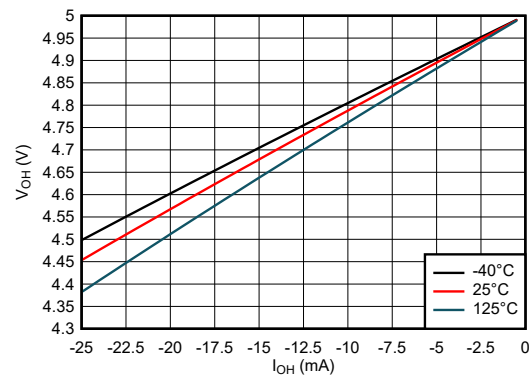


图 5-2. Output Voltage vs Current in HIGH State; 5V Supply

5.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

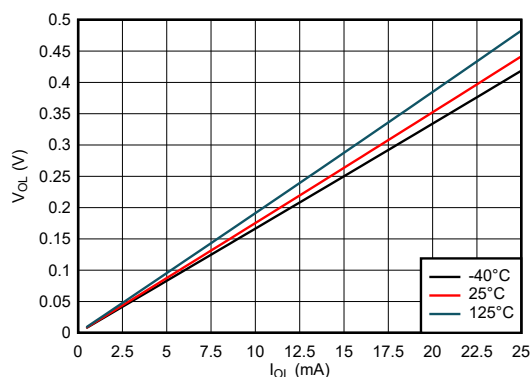


图 5-3. Output Voltage vs Current in LOW State; 5V Supply

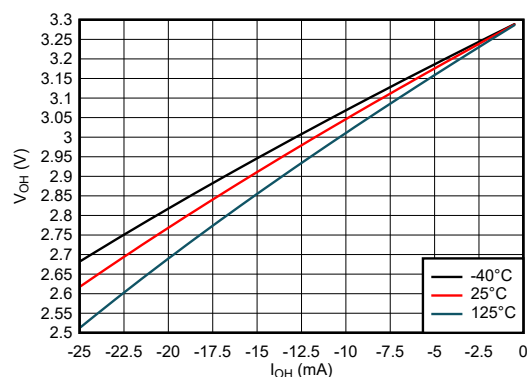


图 5-4. Output Voltage vs Current in HIGH State; 3.3V Supply

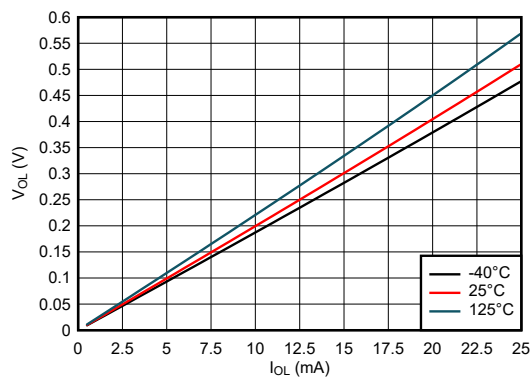


图 5-5. Output Voltage vs Current in LOW State; 3.3V Supply

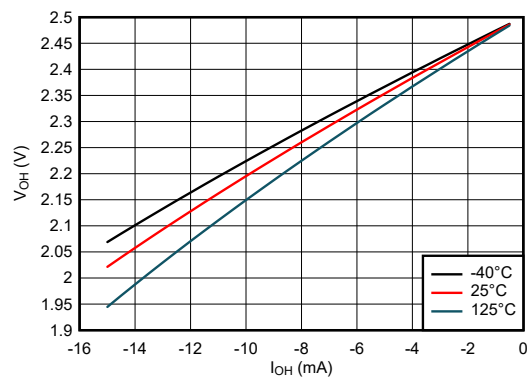


图 5-6. Output Voltage vs Current in HIGH State; 2.5V Supply

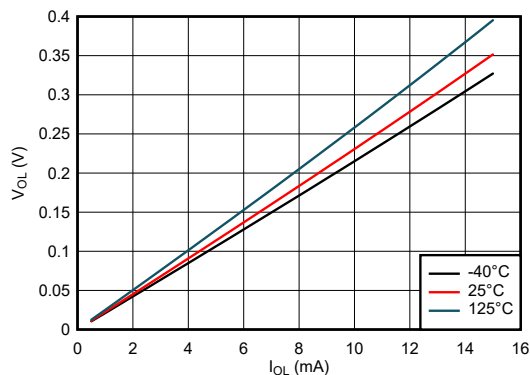
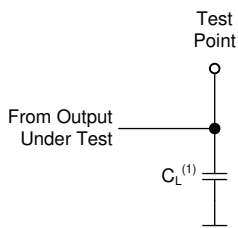


图 5-7. Output Voltage vs Current in LOW State; 2.5V Supply

6 Parameter Measurement Information

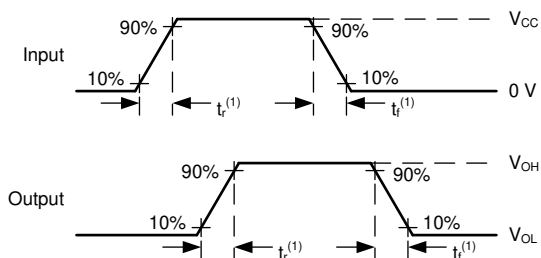
Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_i < 2.5\text{ns}$.

The outputs are measured individually with one input transition per measurement.



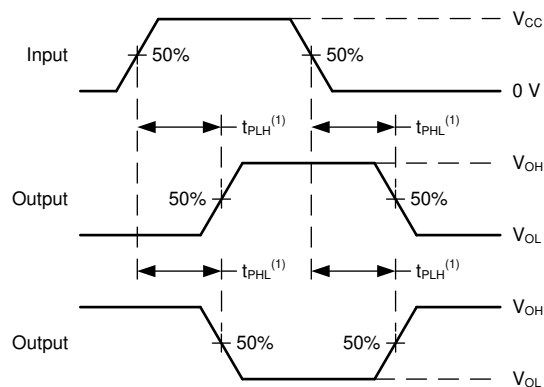
(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for Push-Pull Outputs



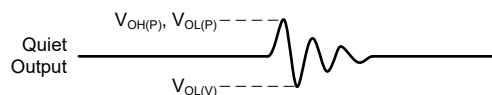
(1) The greater between t_r and t_f is the same as t_t .

图 6-3. Voltage Waveforms, Input and Output Transition Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

图 6-2. Voltage Waveforms Propagation Delays



Noise values measured with all other outputs simultaneously switching.

图 6-4. Voltage Waveforms, Noise

7 Detailed Description

7.1 Overview

The SN74AHC157-Q1 is a high speed silicon gate CMOS multiplexer an excellent choice for multiplexing and data routing applications. It contains four 2:1 multiplexers.

The SN74AHC157-Q1 operates asynchronously, with each Y output being equal to the input selected by the address input ($\overline{A/B}$). All four channels are controlled by the same address input.

The strobe ($\overline{G}$) input forces all Y outputs low, regardless of the state of other inputs.

7.2 Functional Block Diagram

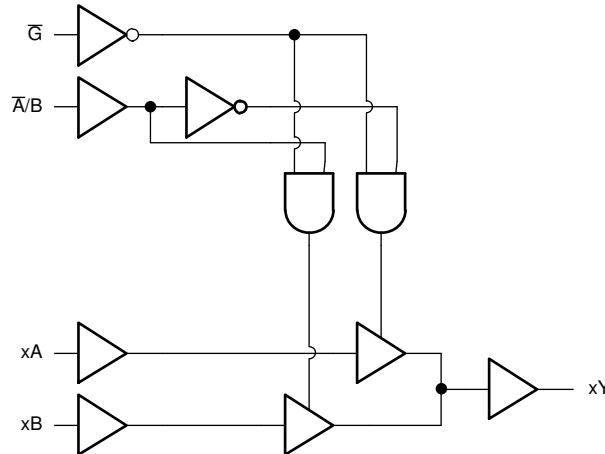


图 7-1. Logic Diagram (Positive Logic) for SN74AHC157-Q1

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10k Ω resistor, however, is recommended and will typically meet all requirements.

7.3.3 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

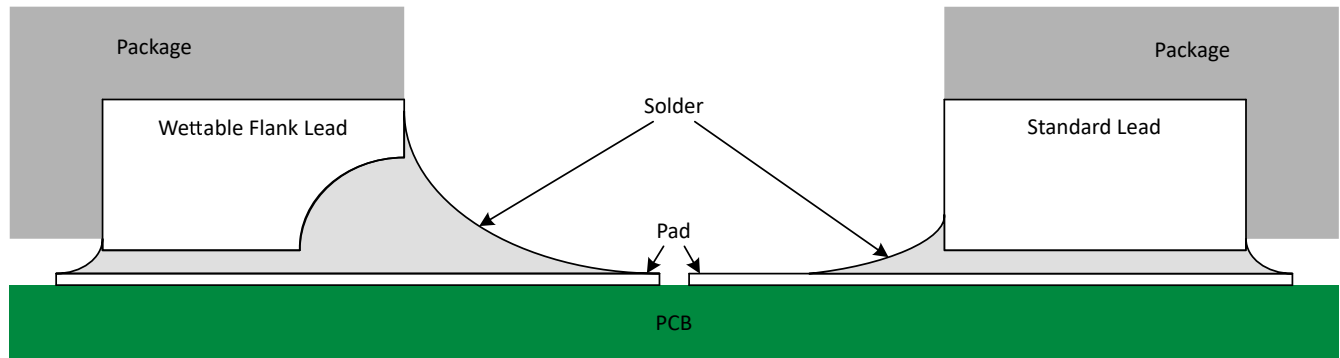


图 7-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in 图 7-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.3.4 Clamp Diode Structure

As 图 7-3 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

小心
Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

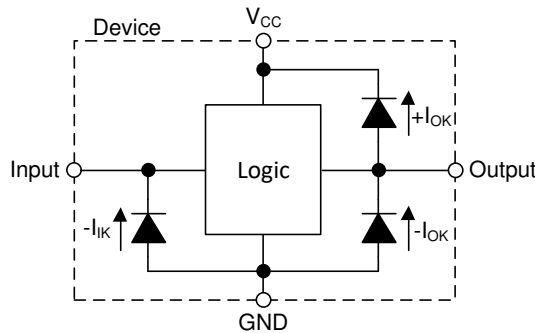


图 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS				OUTPUT
$\bar{G}$	$\bar{A}/B$	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H

表 7-1. Function Table (续)

INPUTS				OUTPUT
$\bar{G}$	$\bar{A}/B$	A	B	Y
L	H	X	L	L
L	H	X	H	H

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AHC157-Q1 is a quadruple 2-to-1 data selector/multiplexer. This application shows an example of using the device with all required connections to switch a 4-bit data bus between two source devices.

8.2 Typical Application

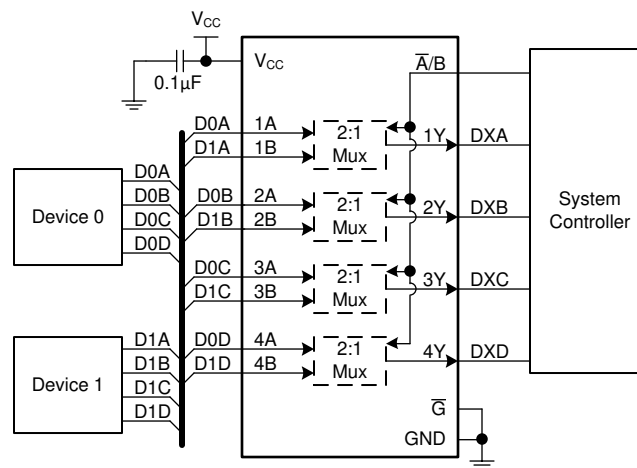


图 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHC157-Q1 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHC157-Q1 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AHC157-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AHC157-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state,

the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

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The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHC157-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A $10k\Omega$ resistor value is often used due to these factors.

The SN74AHC157-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is $\leq 50pF$. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHC157-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in $M\Omega$; much larger than the minimum calculated previously.

4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

8.2.3 Application Curve

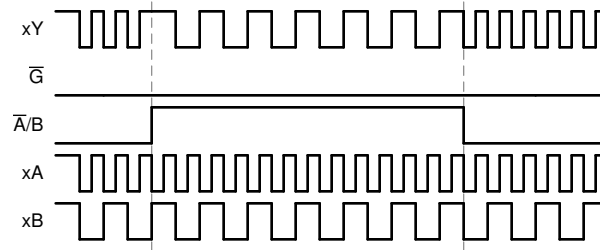


图 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\ \mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\ \mu\text{F}$ and $1\ \mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

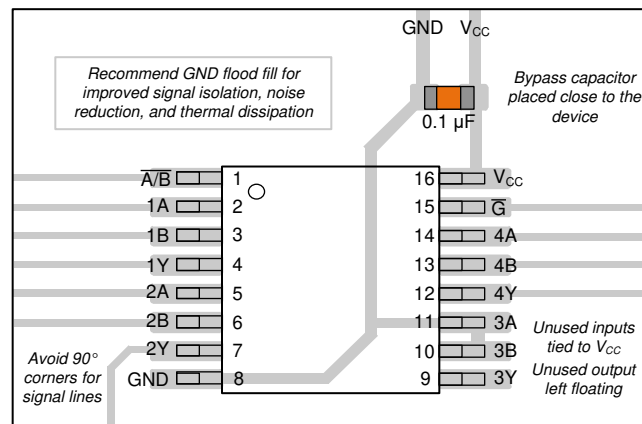


图 8-3. Example Layout for the SN74AHC157-Q1

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.3 Trademarks

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9.4 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

DATE	REVISION	NOTES
February 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAHCT157QWBQBRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AT157Q	Samples
SN74AHC157QPWRQ1	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC157Q	Samples
SN74AHC157QWBQBRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH157Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

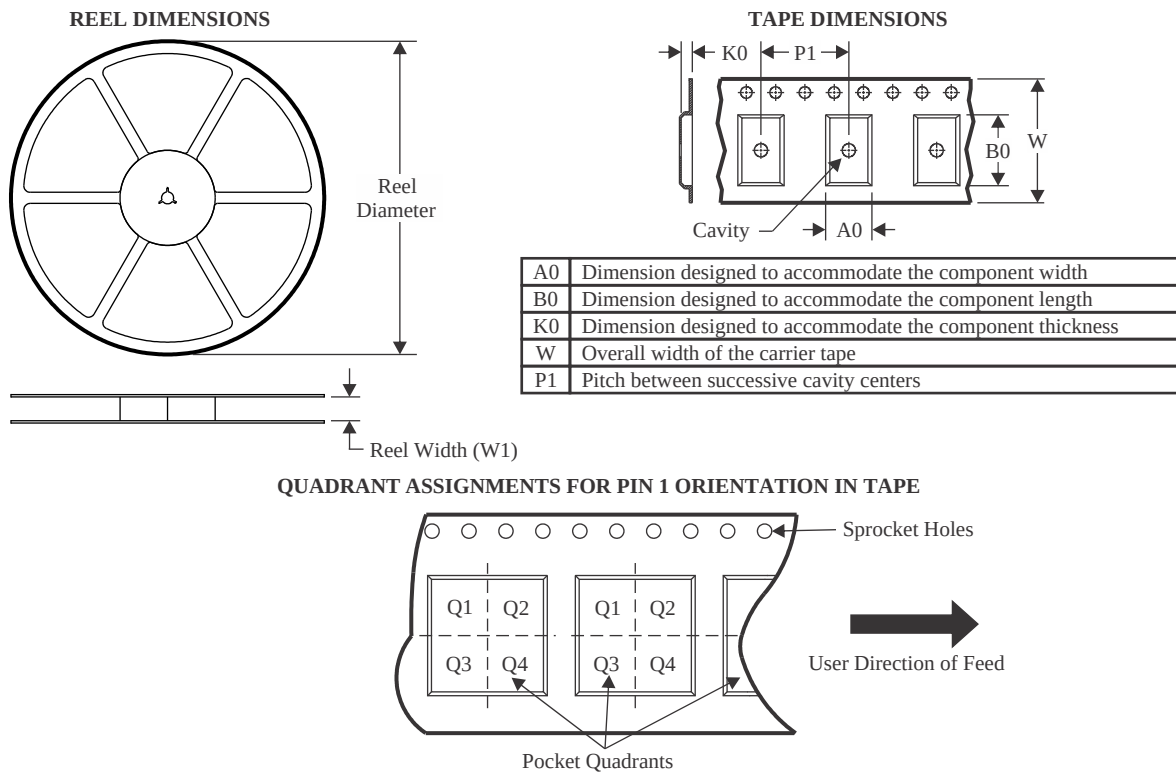
OTHER QUALIFIED VERSIONS OF SN74AHC157-Q1 :

- Catalog : [SN74AHC157](#)
- Military : [SN54AHC157](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

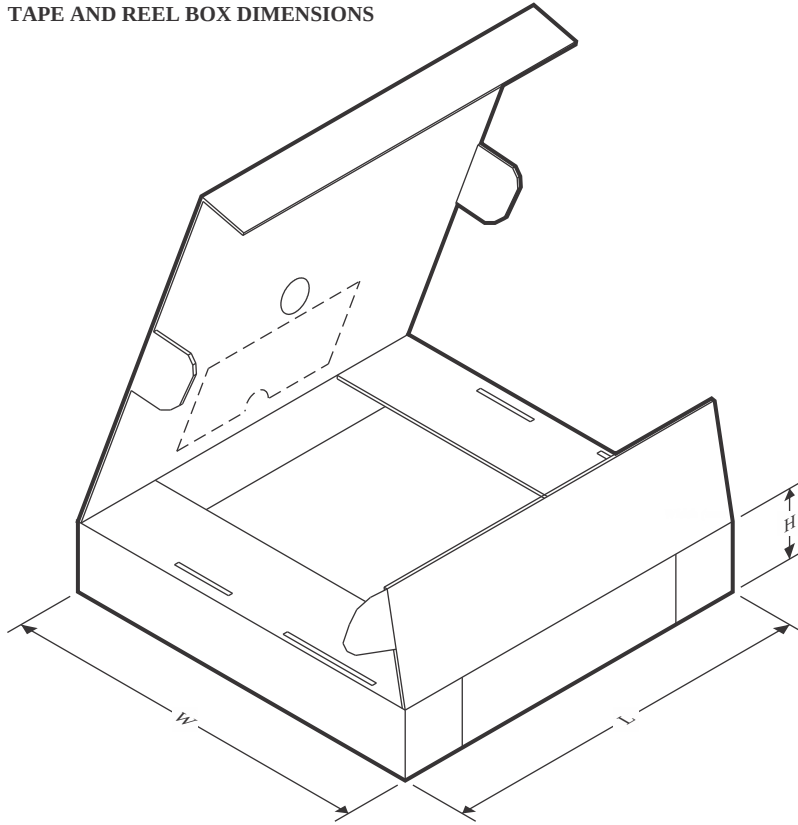
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAHCT157QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74AHC157QPWRQ1	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC157QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAHCT157QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74AHC157QPWRQ1	TSSOP	PW	16	3000	353.0	353.0	32.0
SN74AHC157QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

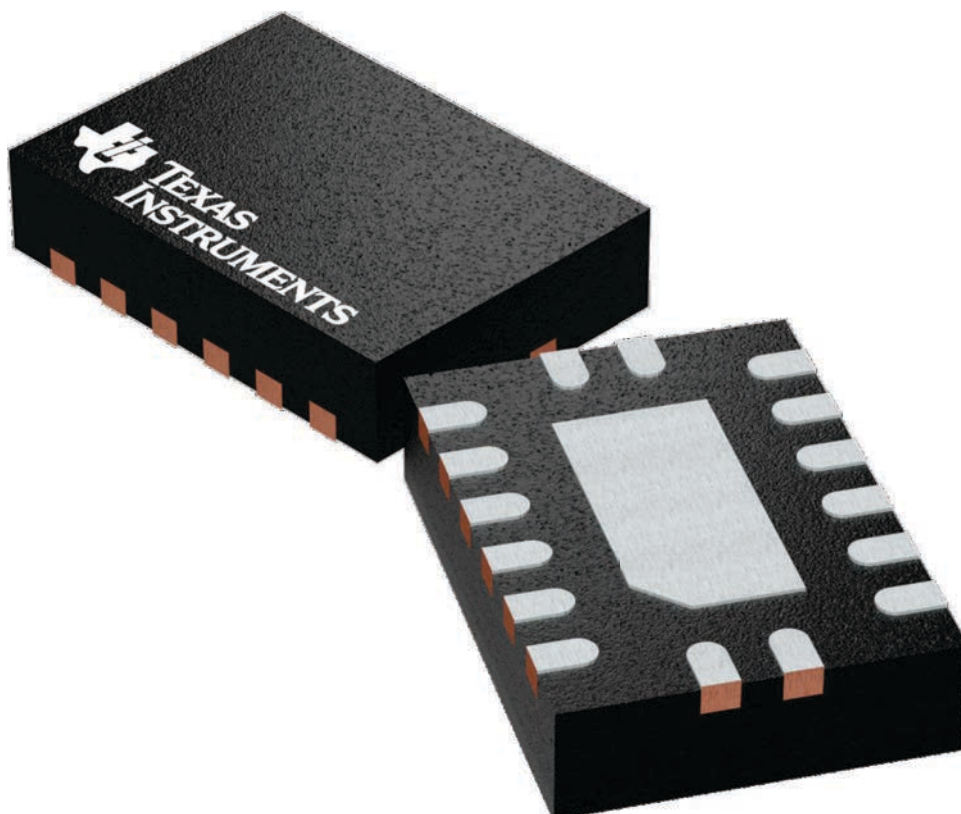
BQB 16

WQFN - 0.8 mm max height

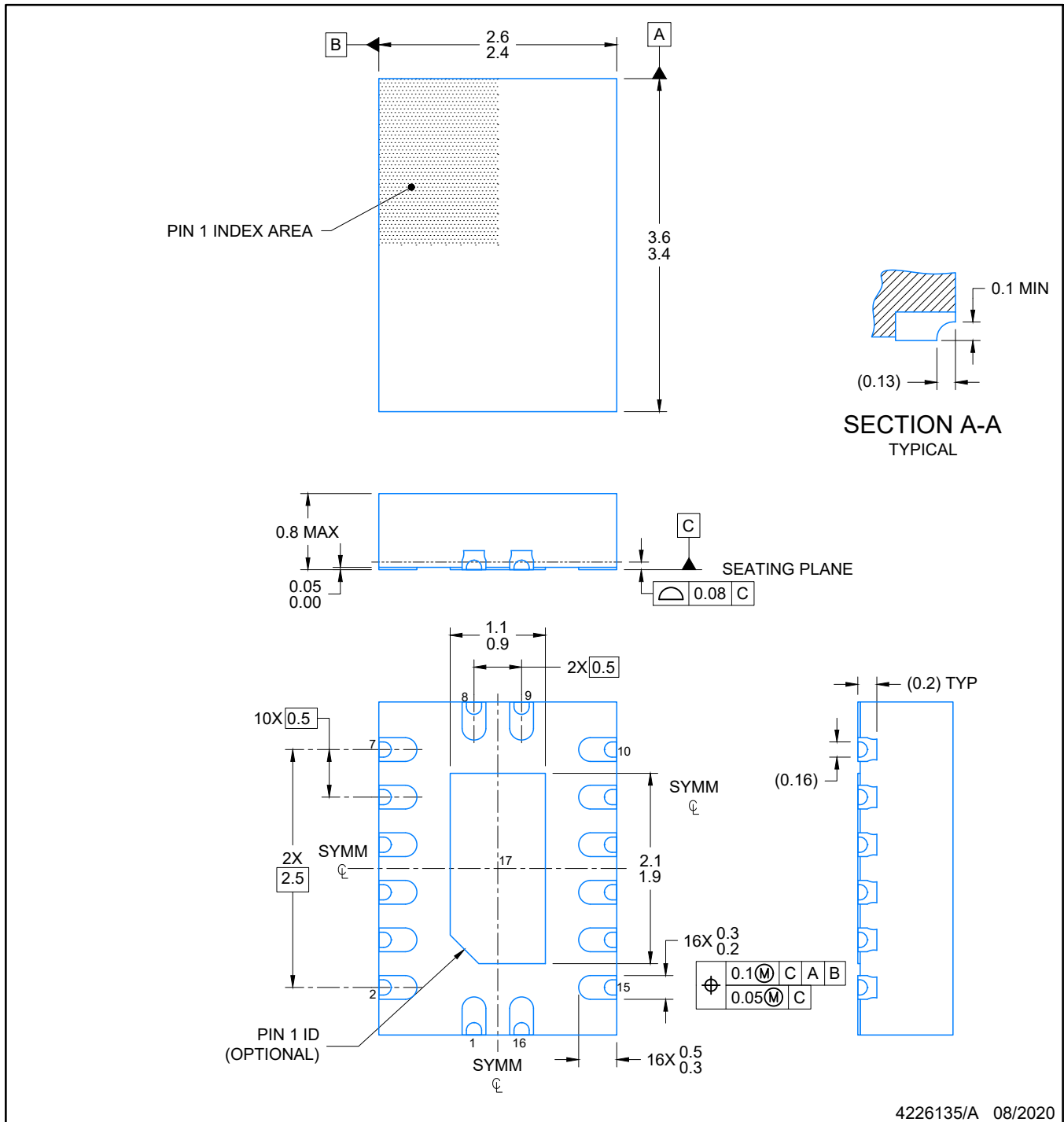
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



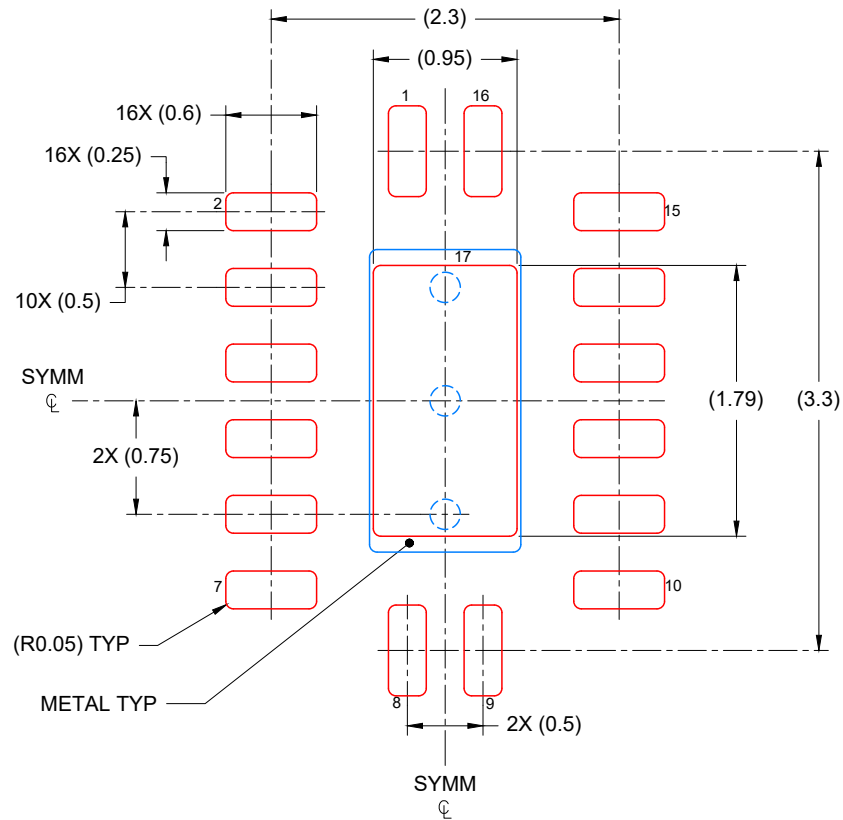
4226161/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



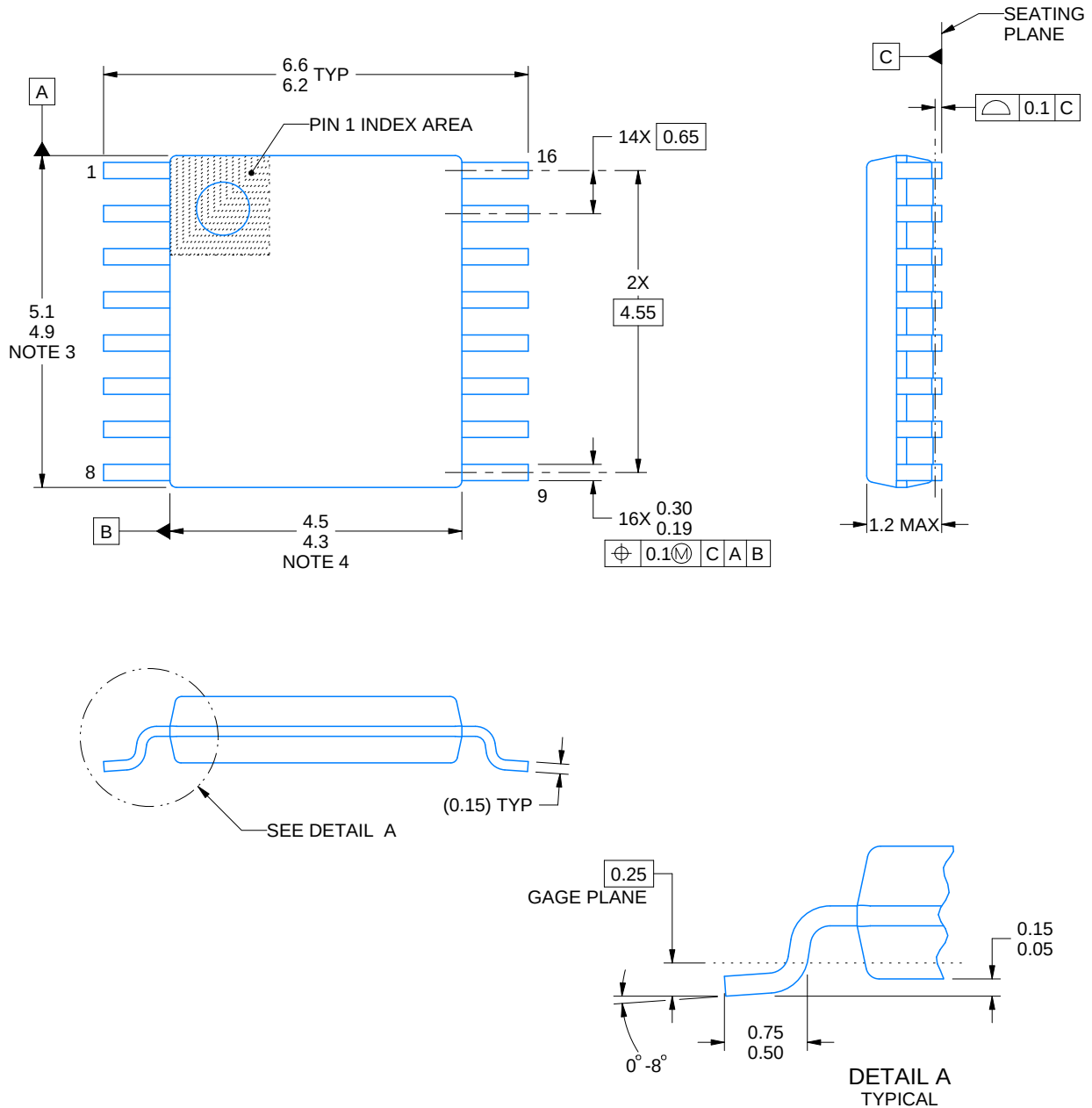
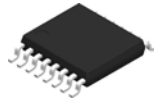
SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 85% PRINTED COVERAGE BY AREA
 SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220204/A 02/2017

NOTES:

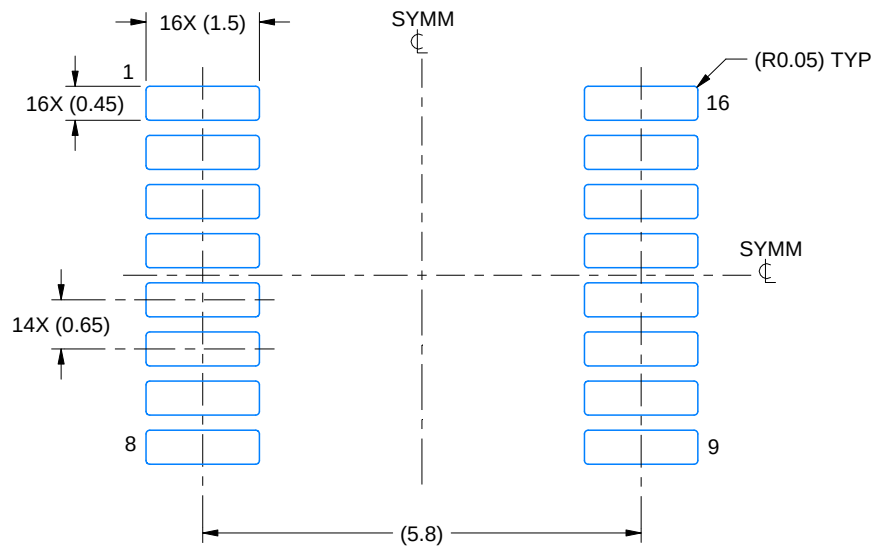
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

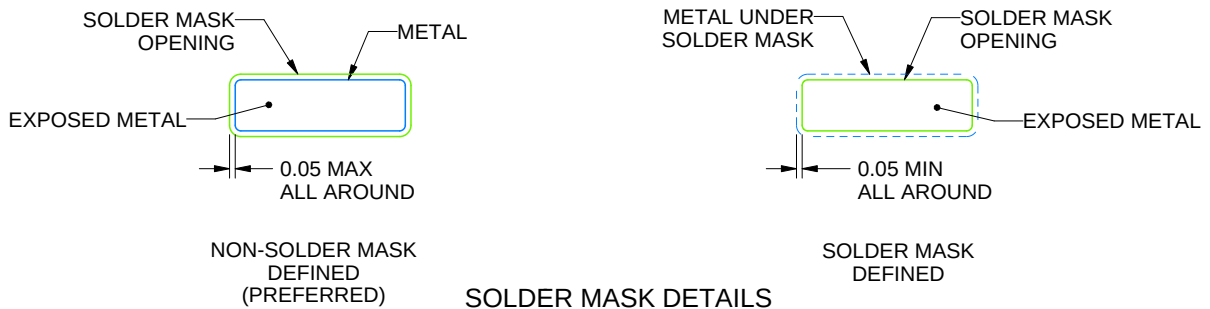
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

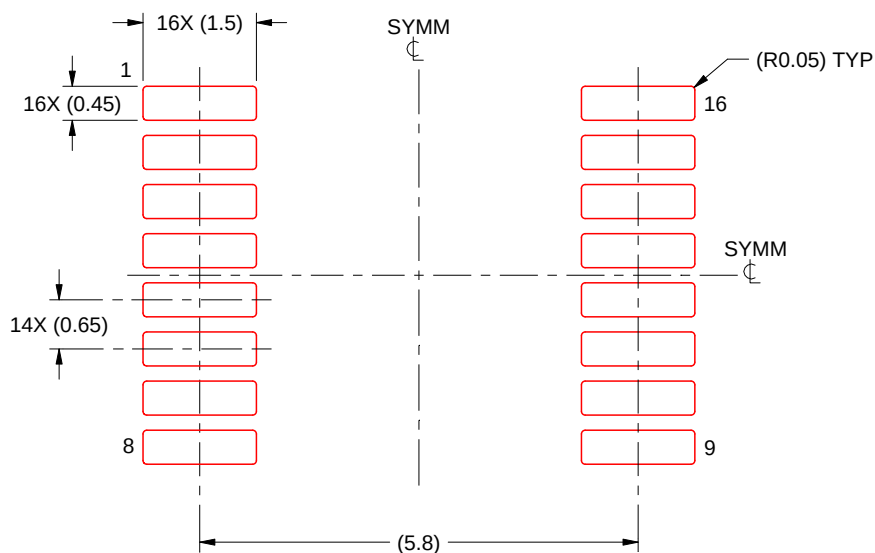
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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