

# LMKDB1xxx PCIe Gen 1 to Gen 6 Ultra Low Jitter 1:20, 1:8, 1:4, 1:2, 2:4, 2:2 LP-HCSL Clock Buffer and Clock MUX

## 1 Features

- LP-HCSL clock buffer and clock MUX that support:
  - PCIe Gen 1 to Gen 6
  - CC (Common Clock) and IR (Independent Reference) PCIe architectures
  - Input clock with or without SSC
- DB2000QL compliant:
  - All devices meet DB2000QL specifications
  - LMKDB1120 is pin-compatible to DB2000QL
- Extremely low additive jitter:
  - 31fs maximum 12kHz to 20MHz RMS additive jitter at 156.25MHz
  - 13fs maximum additive jitter for PCIe Gen 4
  - 5fs maximum additive jitter for PCIe Gen 5
  - 3fs maximum additive jitter for PCIe Gen 6
- Fail-safe input
- Flexible power-up sequence
- Automatic output disable
- Individual output enable
- SBI (Side Band Interface) for high-speed output enable or disable
- LOS (Loss of Signal) input detection
- 85Ω or 100Ω output impedance
- 1.8V / 3.3V  $\pm$  10% power supply
- –40°C to 105°C ambient temperature

## 2 Applications

- [High Performance Computing](#)
- [Server Motherboard](#)
- [NIC/SmartNIC](#)
- [Hardware Accelerator](#)

## 3 Description

The LMKDB devices are a family of extremely-low-jitter LP-HCSL buffers and MUX that support PCIe Gen 1 to Gen 6 and are DB2000QL compliant. The devices provide flexible power-up sequence, fail-safe inputs, individual output enable and disable pins, loss of input signal (LOS) detection and automatic output disable features, as well as excellent power supply noise rejection performance.

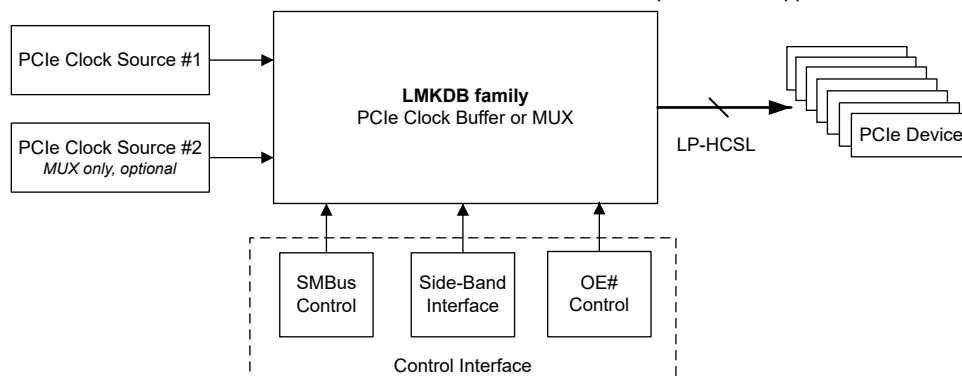
Both 1.8V and 3.3V supply voltages are supported. For LMKDB1120, 1.8V power supply saves 250mW power compared to 3.3V.

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| LMKDB1120   | NPP (TLGA, 80)         | 6mm × 6mm                   |
| LMKDB1108   | RKP (VQFN, 40)         | 5mm × 5mm                   |
| LMKDB1104   | REX (VQFN, 28)         | 4mm × 4mm                   |
| LMKDB1204   | REX (VQFN, 28)         | 4mm × 4mm                   |
| LMKDB1202   | REY (VQFN, 20)         | 3mm × 3mm                   |
| LMKDB1102   | REY (VQFN, 20)         | 3mm × 3mm                   |

(1) For all available packages, see [Section 13](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Typical Application**



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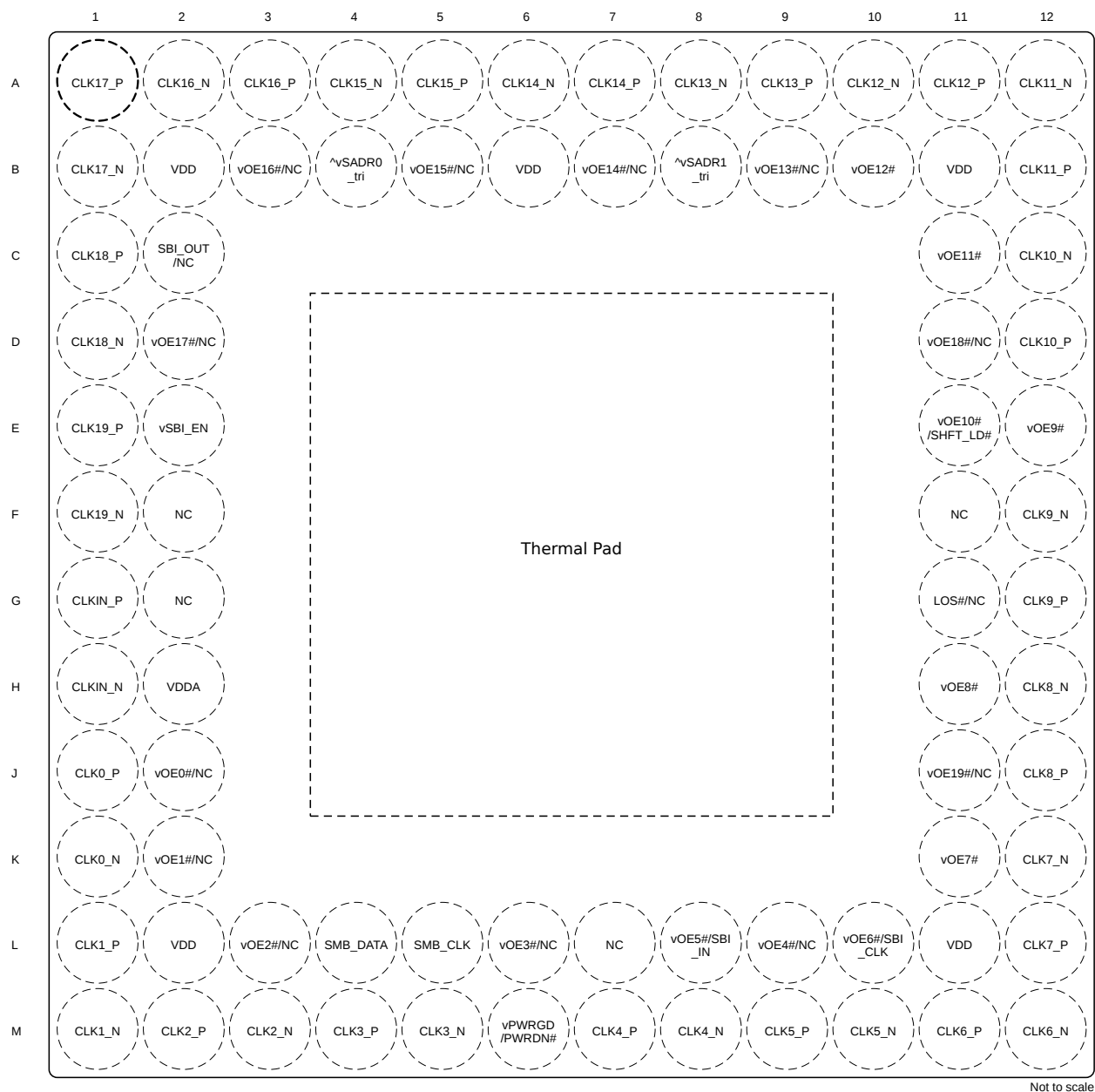
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## 4 Device Comparison

**Table 4-1. Device Comparison**

| PART NUMBER   | DESCRIPTION                                       |
|---------------|---------------------------------------------------|
| LMKDB1120Z85  | 1 input, 20 outputs, 85Ω output impedance         |
| LMKDB1120Z100 | 1 input, 20 outputs, 100Ω output impedance        |
| LMKDB1108Z85  | 1 input, 8 outputs, 85Ω output impedance          |
| LMKDB1108Z100 | 1 input, 8 outputs, 100Ω output impedance         |
| LMKDB1104Z85  | 1 input, 4 outputs, 85Ω output impedance          |
| LMKDB1104Z100 | 1 input, 4 outputs, 100Ω output impedance         |
| LMKDB1204     | 2 inputs, 4 outputs, 85Ω or 100Ω output impedance |
| LMKDB1202     | 2 inputs, 2 outputs, 85Ω or 100Ω output impedance |
| LMKDB1102     | 1 input, 2 outputs, 85Ω or 100Ω output impedance  |

## 5 Pin Configuration and Functions



Not to scale

Figure 5-1. LMKDB1120 NPP Package, 80-Pin TLGA (Top View)

Table 5-1. LMKDB1120 Pin Functions

| PIN     |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                |
|---------|-----|---------------------|------------------------------------------------------------|
| NAME    | NO. |                     |                                                            |
| CLKIN_P | G1  | I                   | Differential clock input.                                  |
| CLKIN_N | H1  | I                   |                                                            |
| CLK0_P  | J1  | O                   | LP-HCSL differential clock output 0. No connect if unused. |
| CLK0_N  | K1  | O                   |                                                            |
| CLK1_P  | L1  | O                   | LP-HCSL differential clock output 1. No connect if unused. |
| CLK1_N  | M1  | O                   |                                                            |

**Table 5-1. LMKDB1120 Pin Functions (continued)**

| PIN     |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                         |
|---------|-----|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME    | NO. |                     |                                                                                                                                                                                                                                                                                     |
| CLK2_P  | M2  | O                   | LP-HCSL differential clock output 2. No connect if unused.                                                                                                                                                                                                                          |
| CLK2_N  | M3  | O                   |                                                                                                                                                                                                                                                                                     |
| CLK3_P  | M4  | O                   | LP-HCSL differential clock output 3. No connect if unused.                                                                                                                                                                                                                          |
| CLK3_N  | M5  | O                   |                                                                                                                                                                                                                                                                                     |
| CLK4_P  | M7  | O                   | LP-HCSL differential clock output 4. No connect if unused.                                                                                                                                                                                                                          |
| CLK4_N  | M8  | O                   |                                                                                                                                                                                                                                                                                     |
| CLK5_P  | M9  | O                   | LP-HCSL differential clock output 5. No connect if unused.                                                                                                                                                                                                                          |
| CLK5_N  | M10 | O                   |                                                                                                                                                                                                                                                                                     |
| CLK6_P  | M11 | O                   | LP-HCSL differential clock output 6. No connect if unused.                                                                                                                                                                                                                          |
| CLK6_N  | M12 | O                   |                                                                                                                                                                                                                                                                                     |
| CLK7_P  | L12 | O                   | LP-HCSL differential clock output 7. No connect if unused.                                                                                                                                                                                                                          |
| CLK7_N  | K12 | O                   |                                                                                                                                                                                                                                                                                     |
| CLK8_P  | J12 | O                   | LP-HCSL differential clock output 8. No connect if unused.                                                                                                                                                                                                                          |
| CLK8_N  | H12 | O                   |                                                                                                                                                                                                                                                                                     |
| CLK9_P  | G12 | O                   | LP-HCSL differential clock output 9. No connect if unused.                                                                                                                                                                                                                          |
| CLK9_N  | F12 | O                   |                                                                                                                                                                                                                                                                                     |
| CLK10_P | D12 | O                   | LP-HCSL differential clock output 10. No connect if unused.                                                                                                                                                                                                                         |
| CLK10_N | C12 | O                   |                                                                                                                                                                                                                                                                                     |
| CLK11_P | B12 | O                   | LP-HCSL differential clock output 11. No connect if unused.                                                                                                                                                                                                                         |
| CLK11_N | A12 | O                   |                                                                                                                                                                                                                                                                                     |
| CLK12_P | A11 | O                   | LP-HCSL differential clock output 12. No connect if unused.                                                                                                                                                                                                                         |
| CLK12_N | A10 | O                   |                                                                                                                                                                                                                                                                                     |
| CLK13_P | A9  | O                   | LP-HCSL differential clock output 13. No connect if unused.                                                                                                                                                                                                                         |
| CLK13_N | A8  | O                   |                                                                                                                                                                                                                                                                                     |
| CLK14_P | A7  | O                   | LP-HCSL differential clock output 14. No connect if unused.                                                                                                                                                                                                                         |
| CLK14_N | A6  | O                   |                                                                                                                                                                                                                                                                                     |
| CLK15_P | A5  | O                   | LP-HCSL differential clock output 15. No connect if unused.                                                                                                                                                                                                                         |
| CLK15_N | A4  | O                   |                                                                                                                                                                                                                                                                                     |
| CLK16_P | A3  | O                   | LP-HCSL differential clock output 16. No connect if unused.                                                                                                                                                                                                                         |
| CLK16_N | A2  | O                   |                                                                                                                                                                                                                                                                                     |
| CLK17_P | A1  | O                   | LP-HCSL differential clock output 17. No connect if unused.                                                                                                                                                                                                                         |
| CLK17_N | B1  | O                   |                                                                                                                                                                                                                                                                                     |
| CLK18_P | C1  | O                   | LP-HCSL differential clock output 18. No connect if unused.                                                                                                                                                                                                                         |
| CLK18_N | D1  | O                   |                                                                                                                                                                                                                                                                                     |
| CLK19_P | E1  | O                   | LP-HCSL differential clock output 19. No connect if unused.                                                                                                                                                                                                                         |
| CLK19_N | F1  | O                   |                                                                                                                                                                                                                                                                                     |
| DAP     | GND | G                   | Ground. Thermal Pad                                                                                                                                                                                                                                                                 |
| LOS#/NC | G11 | O                   | Loss of Input Clock Signal Active Low/No Connect. Open drain. Requires external pullup resistor. This pin can be left no connect to match with DB2000QL pinout. <ul style="list-style-type: none"> <li>• Low = Invalid input clock.</li> <li>• High = Valid input clock.</li> </ul> |
| NC      | F2  | NC                  | No Connect                                                                                                                                                                                                                                                                          |
| NC      | F11 | NC                  | No Connect                                                                                                                                                                                                                                                                          |
| NC      | G2  | NC                  | No Connect                                                                                                                                                                                                                                                                          |

**Table 5-1. LMKDB1120 Pin Functions (continued)**

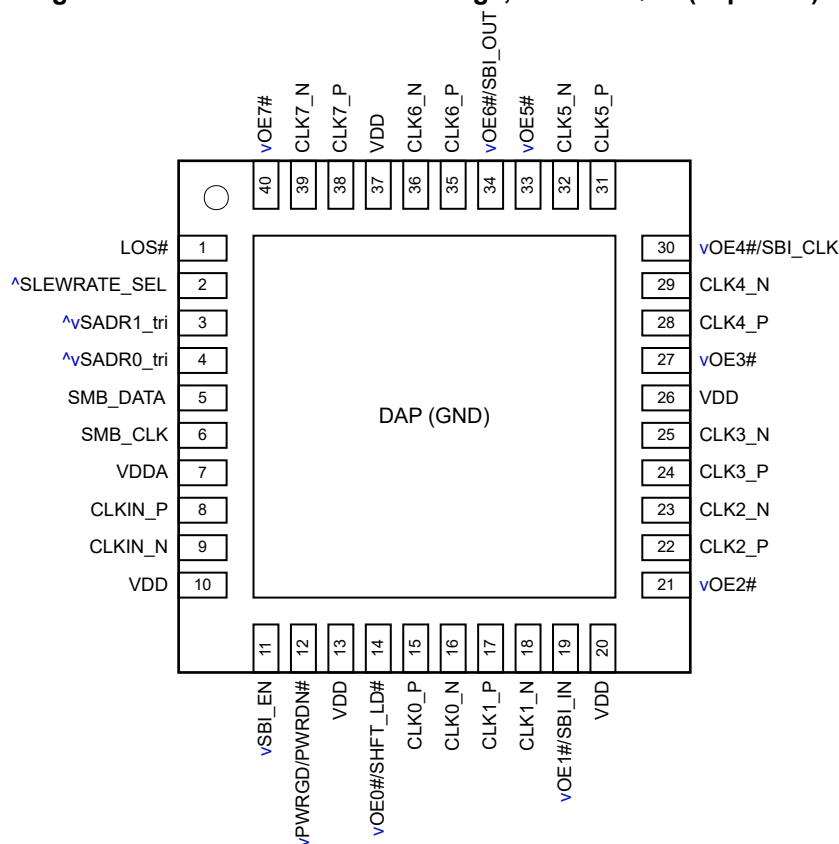
| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                      |
|-----------------|-----|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME            | NO. |                     |                                                                                                                                                                                                  |
| NC              | L7  | NC                  | No Connect                                                                                                                                                                                       |
| SBI_OUT/NC      | C2  | O                   | SBI Data Output/No Connect. This pin can be left no connect to match with DB2000QL pinout.                                                                                                       |
| SMB_DATA        | L4  | I/O                 | SMBus Data. Requires external pullup resistor. No connect if unused.                                                                                                                             |
| SMB_CLK         | L5  | I                   | SMBus Clock. Requires external pullup resistor. No connect if unused.                                                                                                                            |
| VDDA            | H2  | P                   | Analog power supply. Additional power supply filtering is recommended. See <a href="#">Power Supply Recommendations</a> for details.                                                             |
| VDD             | B2  | P                   | Power supply.                                                                                                                                                                                    |
| VDD             | B6  | P                   | Power supply.                                                                                                                                                                                    |
| VDD             | B11 | P                   | Power supply.                                                                                                                                                                                    |
| VDD             | L2  | P                   | Power supply.                                                                                                                                                                                    |
| VDD             | L11 | P                   | Power supply.                                                                                                                                                                                    |
| vOE0#/NC        | J2  | I                   | Output Enable for CLK0 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                         |
| vOE1#/NC        | K2  | I                   | Output Enable for CLK1 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                         |
| vOE2#/NC        | L3  | I                   | Output Enable for CLK2 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                         |
| vOE3#/NC        | L6  | I                   | Output Enable for CLK3 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                         |
| vOE4#/NC        | L9  | I                   | Output Enable for CLK4 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                         |
| vOE5#/SBI_IN    | L8  | I                   | Output Enable for CLK5 Active Low/SBI Data Input. Internal pulldown resistor. Functionality is decided by the state of pin E2 (SBI_EN) at power-up. No connect if unused.                        |
| vOE6#/SBI_CLK   | L10 | I                   | Output Enable for CLK6 Active Low/SBI Clock. Internal pulldown resistor. Functionality is decided by the state of pin E2 (SBI_EN) at power-up. Internal pulldown resistor. No connect if unused. |
| vOE7#           | K11 | I                   | Output Enable for CLK7 Active Low. Internal pulldown resistor. No connect if unused.                                                                                                             |
| vOE8#           | H11 | I                   | Output Enable for CLK8 Active Low. Internal pulldown resistor. No connect if unused.                                                                                                             |
| vOE9#           | E12 | I                   | Output Enable for CLK9 Active Low. Internal pulldown resistor. No connect if unused.                                                                                                             |
| vOE10#/SHFT_LD# | E11 | I                   | Output Enable for CLK10 Active Low/SBI Shift Register Load Active Low. Internal pulldown resistor. Functionality is decided by the state of pin E2 (SBI_EN) at power-up. No connect if unused.   |
| vOE11#          | C11 | I                   | Output Enable for CLK11 Active Low. Internal pulldown resistor. No connect if unused.                                                                                                            |
| vOE12#          | B10 | I                   | Output Enable for CLK12 Active Low. Internal pulldown resistor. No connect if unused.                                                                                                            |
| vOE13#/NC       | B9  | I                   | Output Enable for CLK13 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                        |
| vOE14#/NC       | B7  | I                   | Output Enable for CLK14 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                        |
| vOE15#/NC       | B5  | I                   | Output Enable for CLK15 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                        |
| vOE16#/NC       | B3  | I                   | Output Enable for CLK16 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                        |
| vOE17#/NC       | D2  | I                   | Output Enable for CLK17 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                        |
| vOE18#/NC       | D11 | I                   | Output Enable for CLK18 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                        |
| vOE19#/NC       | J11 | I                   | Output Enable for CLK19 Active Low/No Connect. Internal pulldown resistor. This pin can be left no connect to match with DB2000QL pinout.                                                        |

**Table 5-1. LMKDB1120 Pin Functions (continued)**

| PIN           |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------|-----|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME          | NO. |                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| vPWRGD/PWRDN# | M6  | I                   | <p>Power Good/Power Down Active Low. Multifunctional input pin. Internal pulldown resistor.</p> <ul style="list-style-type: none"> <li>On the first low-to-high transition, functions as Power Good pin which starts up the device</li> <li>On the subsequent low/high transitions, functions as Power Down Active Low pin which controls the device to enter or exit power-down mode. <ul style="list-style-type: none"> <li>Low = power-down mode</li> <li>High = normal operation mode</li> </ul> </li> </ul> |
| vSBI_EN       | E2  | I                   | <p>SBI Enable. Internal pulldown resistor. Do not change the state of this pin after power-up.</p> <ul style="list-style-type: none"> <li>Low at power-up = SBI interface disabled. Pin L8, L10, E11 function as OE pins.</li> <li>High at power-up = SBI interface enabled. Pin L8, L10, E11 function as SBI interface pins. SMBus and other OE pins remain functional.</li> </ul>                                                                                                                              |
| ^vSADR1_tri   | B8  | I                   | SMBus Address 3-level input pin. Internal pullup and pulldown resistors.                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| ^vSADR0_tri   | B4  | I                   | SMBus Address 3-level input pin. Internal pullup and pulldown resistors.                                                                                                                                                                                                                                                                                                                                                                                                                                         |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect

**Figure 5-2. LMKDB1108 RKP Package, 40-Pin VQFN (Top View)**



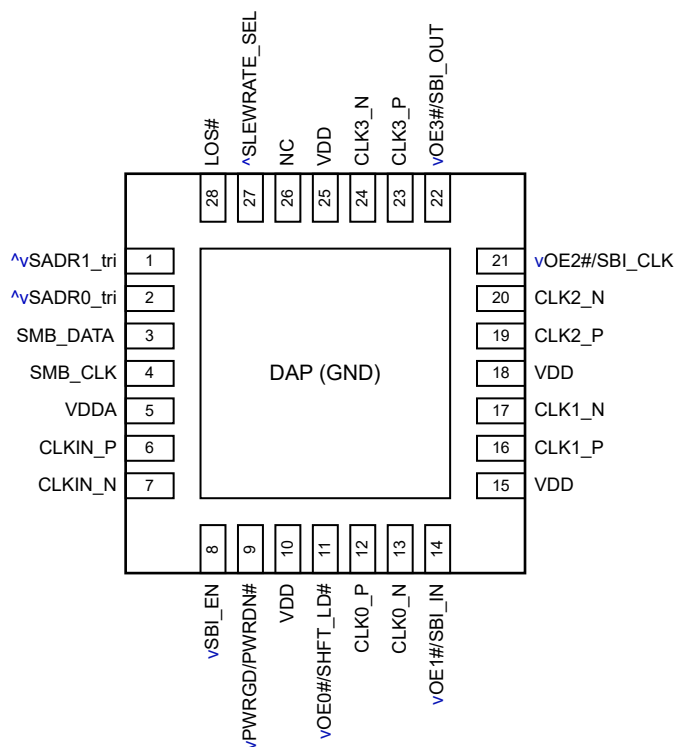
**Table 5-2. LMKDB1108 Pin Functions**

| PIN<br>NAME | NO. | TYPE <sup>(1)</sup> | DESCRIPTION                                                |
|-------------|-----|---------------------|------------------------------------------------------------|
| CLKIN_P     | 8   | I                   | Differential clock input.                                  |
| CLKIN_N     | 9   | I                   |                                                            |
| CLK0_P      | 15  | O                   | LP-HCSL differential clock output 0. No connect if unused. |
| CLK0_N      | 16  | O                   |                                                            |
| CLK1_P      | 17  | O                   | LP-HCSL differential clock output 1. No connect if unused. |
| CLK1_N      | 18  | O                   |                                                            |
| CLK2_P      | 22  | O                   | LP-HCSL differential clock output 2. No connect if unused. |
| CLK2_N      | 23  | O                   |                                                            |
| CLK3_P      | 24  | O                   | LP-HCSL differential clock output 3. No connect if unused. |
| CLK3_N      | 25  | O                   |                                                            |
| CLK4_P      | 28  | O                   | LP-HCSL differential clock output 4. No connect if unused. |
| CLK4_N      | 29  | O                   |                                                            |
| CLK5_P      | 31  | O                   | LP-HCSL differential clock output 5. No connect if unused. |
| CLK5_N      | 32  | O                   |                                                            |
| CLK6_P      | 35  | O                   | LP-HCSL differential clock output 6. No connect if unused. |
| CLK6_N      | 36  | O                   |                                                            |
| CLK7_P      | 38  | O                   | LP-HCSL differential clock output 7. No connect if unused. |
| CLK7_N      | 39  | O                   |                                                            |

**Table 5-2. LMKDB1108 Pin Functions (continued)**

| PIN<br>NAME    | NO. | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------------|-----|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| vPWRGD/PWRDN#  | 12  | I                   | Power Good/Power Down Active Low. Multifunctional input pin. Internal pulldown resistor. <ul style="list-style-type: none"> <li>On the first low-to-high transition, functions as Power Good pin which starts up the device</li> <li>On the subsequent low/high transitions, functions as Power Down Active Low pin which controls the device to enter or exit power-down mode. <ul style="list-style-type: none"> <li>Low = power-down mode</li> <li>High = normal operation mode</li> </ul> </li> </ul> |
| vOE0#/SHFT_LD# | 14  | I                   | Output Enable for CLK0 Active Low/SBI Shift Register Load Active Low. Internal pulldown resistor. Functionality is decided by the state of pin 11 (SBI_EN) at power-up. No connect if unused.                                                                                                                                                                                                                                                                                                             |
| vOE1#/SBI_IN   | 19  | I                   | Output Enable for CLK1 Active Low/SBI Data Input. Internal pulldown resistor. Functionality is decided by the state of pin 11 (SBI_EN) at power-up. No connect if unused.                                                                                                                                                                                                                                                                                                                                 |
| vOE2#          | 21  | I                   | Output Enable for CLK2 Active Low. Internal pulldown resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                      |
| vOE3#          | 27  | I                   | Output Enable for CLK3 Active Low. Internal pulldown resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                      |
| vOE4#/SBI_CLK  | 30  | I                   | Output Enable for CLK4 Active Low/SBI Clock. Internal pulldown resistor. Functionality is decided by the state of pin 11 (SBI_EN) at power-up. Internal pulldown resistor. No connect if unused.                                                                                                                                                                                                                                                                                                          |
| vOE5#          | 33  | I                   | Output Enable for CLK5 Active Low. Internal pulldown resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                      |
| vOE6#/SBI_OUT  | 34  | I or O              | Output Enable for CLK6 Active Low/SBI Data Output. Functionality is decided by the state of pin 11 (SBI_EN) at power-up. Internal pulldown resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                |
| vOE7#          | 40  | I                   | Output Enable for CLK7 Active Low. Internal pulldown resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                      |
| vSBI_EN        | 11  | I                   | SBI Enable. Internal pulldown resistor. Do not change the state of this pin after power-up. <ul style="list-style-type: none"> <li>Low at power-up = SBI interface disabled. Pin 14, 19, 30, 34 function as OE pins.</li> <li>High at power-up = SBI interface enabled. Pin 14, 19, 30, 34 function as SBI interface pins. SMBus and other OE pins remain functional.</li> </ul>                                                                                                                          |
| SMB_DATA       | 5   | I/O                 | SMBus Data. Requires external pullup resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| SMB_CLK        | 6   | I                   | SMBus Clock. Requires external pullup resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| ^vSADR1_tri    | 3   | I                   | SMBus Address 3-level input pins. These two pins select 1 out of 9 SMBus addresses.                                                                                                                                                                                                                                                                                                                                                                                                                       |
| ^vSADR0_tri    | 4   | I                   | SMBus Address 3-level input pins. These two pins select 1 out of 9 SMBus addresses.                                                                                                                                                                                                                                                                                                                                                                                                                       |
| ^SLEWRATE_SEL  | 2   | I                   | Slew Rate Select for output clocks. Internal pullup resistor. <ul style="list-style-type: none"> <li>Low = Slow slew rate</li> <li>High = Fast slew rate</li> </ul>                                                                                                                                                                                                                                                                                                                                       |
| LOS#           | 1   | O                   | Loss of Input Clock Signal Active Low. Open drain. Requires external pullup resistor. <ul style="list-style-type: none"> <li>Low = Invalid input clock.</li> <li>High = Valid input clock.</li> </ul>                                                                                                                                                                                                                                                                                                     |
| VDDA           | 7   | P                   | Analog power supply. Additional power supply filtering is recommended. See <a href="#">Power Supply Recommendations</a> for details.                                                                                                                                                                                                                                                                                                                                                                      |
| VDD            | 13  | P                   | Power supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| VDD            | 20  | P                   | Power supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| VDD            | 26  | P                   | Power supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| VDD            | 37  | P                   | Power supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| VDD            | 10  | P                   | Power supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| DAP            | GND | G                   | Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect



**Figure 5-3. LMKDB1104 4 x 4 mm 28-pin QFN**

**Table 5-3. LMKDB1104 Pin Functions**

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----------------|-----|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME            | NO. |                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| CLKIN_P         | 6   | I                   | Differential clock input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| CLKIN_N         | 7   | I                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| CLK0_P          | 12  | O                   | LP-HCSL differential clock output 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| CLK0_N          | 13  | O                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| CLK1_P          | 16  | O                   | LP-HCSL differential clock output 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| CLK1_N          | 17  | O                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| CLK2_P          | 19  | O                   | LP-HCSL differential clock output 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| CLK2_N          | 20  | O                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| CLK3_P          | 23  | O                   | LP-HCSL differential clock output 3                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| CLK3_N          | 24  | O                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| vPWRGD/PWRDN#   | 9   | I                   | Power Good/Power Down Active Low. Multifunctional input pin. Internal pulldown resistor. <ul style="list-style-type: none"> <li>On the first low-to-high transition, functions as Power Good pin which starts up the device</li> <li>On the subsequent low/high transitions, functions as Power Down Active Low pin which controls the device to enter or exit power-down mode. <ul style="list-style-type: none"> <li>Low = power-down mode</li> <li>High = normal operation mode</li> </ul> </li> </ul> |
| ^VOE0#/SHFT_LD# | 11  | I                   | Output Enable for CLK0 Active Low/SBI Shift Register Load Active Low. Internal pulldown resistor. Functionality is decided by the state of pin 8 (SBI_EN) at power-up. No connect if unused.                                                                                                                                                                                                                                                                                                              |
| ^VOE1#/SBI_IN   | 14  | I                   | Output Enable for CLK1 Active Low/SBI Data Input. Internal pulldown resistor. Functionality is decided by the state of pin 8 (SBI_EN) at power-up. No connect if unused.                                                                                                                                                                                                                                                                                                                                  |

**Table 5-3. LMKDB1104 Pin Functions (continued)**

| PIN           |                | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                      |
|---------------|----------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME          | NO.            |                     |                                                                                                                                                                                                                                                                                                                                                                                  |
| vOE2#/SBI_CLK | 21             | I                   | Output Enable for CLK2 Active Low/SBI Clock. Internal pulldown resistor. Functionality is decided by the state of pin 8 (SBI_EN) at power-up. Internal pulldown resistor. No connect if unused.                                                                                                                                                                                  |
| vOE3#/SBI_OUT | 22             | I or O              | Output Enable for CLK3 Active Low/SBI Data Output. Internal pulldown resistor. Functionality is decided by the state of pin 8 (SBI_EN) at power-up. Internal pulldown resistor. No connect if unused.                                                                                                                                                                            |
| vSBI_EN       | 8              | I                   | SBI Enable. Internal pulldown resistor. Do not change the state of this pin after power-up. <ul style="list-style-type: none"> <li>Low at power-up = SBI interface disabled. Pin 11, 14, 21, 22 function as OE pins.</li> <li>High at power-up = SBI interface enabled. Pin 11, 14, 21, 22 function as SBI interface pins. SMBus and other OE pins remain functional.</li> </ul> |
| SMB_DATA      | 3              | I/O                 | SMBus Data. Requires external pullup resistor. No connect if unused.                                                                                                                                                                                                                                                                                                             |
| SMB_CLK       | 4              | I                   | SMBus Clock. Requires external pullup resistor. No connect if unused.                                                                                                                                                                                                                                                                                                            |
| ^vSADR1_tri   | 1              | I                   | SMBus Address 3-level input pins. These two pins select 1 out of 9 SMBus addresses.                                                                                                                                                                                                                                                                                              |
| ^vSADR0_tri   | 2              | I                   | SMBus Address 3-level input pins. These two pins select 1 out of 9 SMBus addresses.                                                                                                                                                                                                                                                                                              |
| ^SLEWRATE_SEL | 27             | I                   | Slew Rate Select for output clocks. Internal pullup resistor. <ul style="list-style-type: none"> <li>Low = Slow slew rate</li> <li>High = Fast slew rate</li> </ul>                                                                                                                                                                                                              |
| LOS#          | 28             | O                   | Loss of Input Clock Signal Active Low. Open drain. Requires external pullup resistor. <ul style="list-style-type: none"> <li>Low = Invalid input clock.</li> <li>High = Valid input clock.</li> </ul>                                                                                                                                                                            |
| VDDA          | 5              | P                   | Analog power supply. Additional power supply filtering is recommended. See <a href="#">Power Supply Recommendations</a> for details.                                                                                                                                                                                                                                             |
| VDD           | 10, 15, 18, 25 | P                   | Power supply.                                                                                                                                                                                                                                                                                                                                                                    |
| GND           | DAP            | G                   | Ground.                                                                                                                                                                                                                                                                                                                                                                          |
| NC            | 26             | NC                  | No Connect.                                                                                                                                                                                                                                                                                                                                                                      |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect

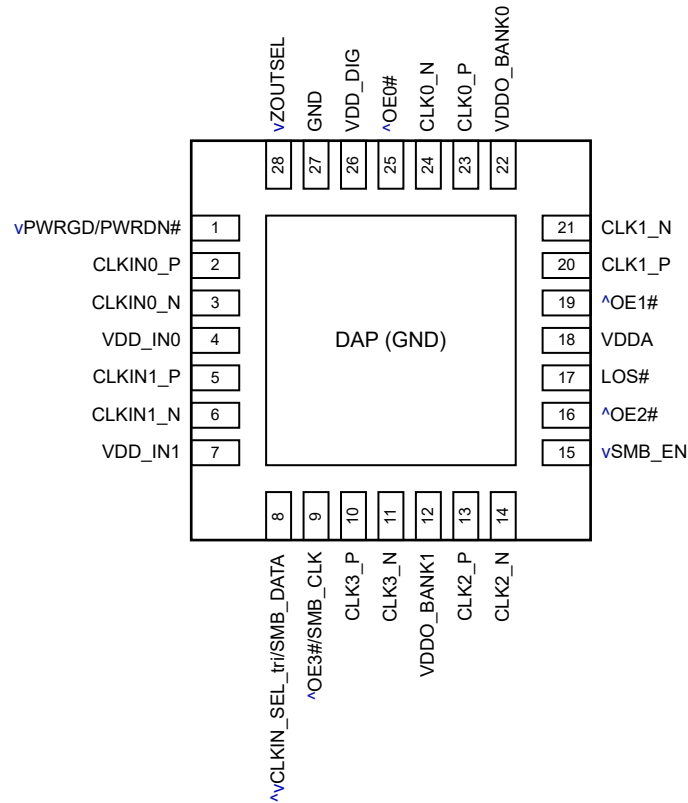


Figure 5-4. LMKDB1204 4 x 4 mm 28-pin QFN

Table 5-4. LMKDB1204 Pin Functions

| PIN           |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|---------------|-----|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME          | NO. |                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| CLKIN0_P      | 2   | I                   | Differential clock input 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| CLKIN0_N      | 3   | I                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| CLKIN1_P      | 5   | I                   | Differential clock input 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| CLKIN1_N      | 6   | I                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| CLK3_P        | 10  | O                   | LP-HCSL differential clock output 3. Output Bank 1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| CLK3_N        | 11  | O                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| CLK2_P        | 13  | O                   | LP-HCSL differential clock output 2. Output Bank 1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| CLK2_N        | 14  | O                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| CLK1_P        | 20  | O                   | LP-HCSL differential clock output 1. Output Bank 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| CLK1_N        | 21  | O                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| CLK0_P        | 23  | O                   | LP-HCSL differential clock output 0. Output Bank 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| CLK0_N        | 24  | O                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| vPWRGD/PWRDN# | 1   | I                   | Power Good/Power Down Active Low. Multifunctional input pin. Internal pulldown resistor. <ul style="list-style-type: none"> <li>On the first low-to-high transition, functions as Power Good pin which starts up the device</li> <li>On the subsequent low/high transitions, functions as Power Down Active Low pin which controls the device to enter or exit power-down mode.               <ul style="list-style-type: none"> <li>Low = power-down mode</li> <li>High = normal operation mode</li> </ul> </li> </ul> |

**Table 5-4. LMKDB1204 Pin Functions (continued)**

| PIN                          |         | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------------------------|---------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                         | NO.     |                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| ^OE3#/SMB_CLK                | 9       | I                   | Output Enable for CLK3 Active Low/SMBus Clock. Internal pullup resistor. Functionality is decided by the state of pin 15 (SMB_EN) at power-up. When used as SMBus Clock pin, external pullup resistor is required. No connect if unused.                                                                                                                                                                                                                                                                     |
| ^OE2#                        | 16      | I                   | Output Enable for CLK2 Active Low. Internal pullup resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| ^OE1#                        | 19      | I                   | Output Enable for CLK1 Active Low. Internal pullup resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| ^OE0#                        | 25      | I                   | Output Enable for CLK0 Active Low. Internal pullup resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| ^vCLKIN_SEL_tri/<br>SMB_DATA | 8       | I or I/O            | 3-Level Clock Input Select/SMBus Data. Internal pullup and pulldown resistor. Functionality is decided by the state of pin 15 (SMB_EN) at power-up. <ul style="list-style-type: none"> <li>When used as CLKIN_SEL_tri pin: <ul style="list-style-type: none"> <li>Low = CLKIN0 goes to all outputs</li> <li>Mid = CLKIN0 goes to Bank 0, CLKIN1 goes to Bank 1</li> <li>High = CLKIN1 goes to all outputs</li> </ul> </li> <li>When used as SMBus Data pin, external pullup resistor is required.</li> </ul> |
| vSMB_EN                      | 15      | I                   | SMBus Enable. Internal pulldown resistor. Do not change the state of this pin after power-up. <ul style="list-style-type: none"> <li>Low at power-up = SMBus disabled. Pin 8 is CLKIN_SEL_tri and Pin 9 is OE3#.</li> <li>High at power-up = SMBus enabled. Pin 8 is SMB_DATA and Pin 9 is SMB_CLK.</li> </ul>                                                                                                                                                                                               |
| vZOUT_SEL                    | 28      | I                   | LP-HCSL Differential Clock Output Impedance Select. Internal pulldown resistor. <ul style="list-style-type: none"> <li>Low = 85Ω</li> <li>High = 100Ω</li> </ul>                                                                                                                                                                                                                                                                                                                                             |
| LOS#                         | 17      | O                   | Loss of Input Clock Signal Active Low. Open drain. Requires external pullup resistor. <ul style="list-style-type: none"> <li>Low = Invalid input clock.</li> <li>High = Valid input clock.</li> </ul>                                                                                                                                                                                                                                                                                                        |
| VDD_IN0                      | 4       | P                   | Power supply for CLKIN0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| VDD_IN1                      | 7       | P                   | Power supply for CLKIN1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| VDDO_BANK1                   | 12      | P                   | Power supply for output bank 1 (OUT2 and OUT3)                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| VDDO_BANK0                   | 22      | P                   | Power supply for output bank 0 (OUT0 and OUT1)                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| VDD_DIG                      | 26      | P                   | Power supply for digital                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| VDDA                         | 18      | P                   | Analog power supply. Additional power supply filtering is recommended. See <a href="#">Power Supply Recommendations</a> for details.                                                                                                                                                                                                                                                                                                                                                                         |
| GND                          | 27, DAP | G                   | Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect

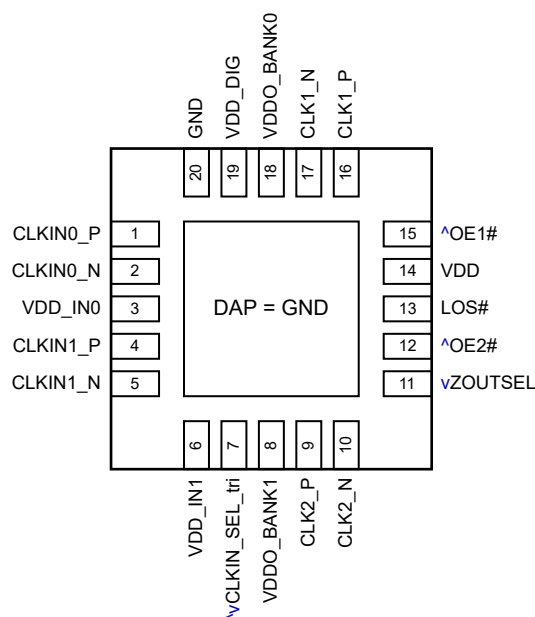


Figure 5-5. LMKDB1202 3 x 3 mm 20-pin QFN

Table 5-5. LMKDB1202 Pin Functions

| PIN                |        | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--------------------|--------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME               | NO.    |                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| CLKIN0_P, CLKIN0_N | 1, 2   | I                   | Differential clock input 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| CLKIN1_P, CLKIN1_N | 4, 5   | I                   | Differential clock input 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| CLK2_P, CLK2_N     | 9, 10  | O                   | LP-HCSL differential clock output 2. Output Bank 1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| CLK1_P, CLK1_N     | 16, 17 | O                   | LP-HCSL differential clock output 1. Output Bank 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| ^OE2#              | 12     | I                   | Output Enable for CLK2 Active Low. Internal pullup resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| ^OE1#              | 15     | I                   | Output Enable for CLK1 Active Low. Internal pullup resistor. No connect if unused. This pin requires either of below conditions to dynamically enable or disable the CLK1 after power-up. If CLK1 stays enabled or disabled after power-up, then below conditions do not need to be met. <ul style="list-style-type: none"> <li>This pin is driven low or high at <math>\geq 0.1</math> V/ns slew rate.</li> <li>The resistance used to drive this pin is <math>\leq 1</math> k<math>\Omega</math>.</li> </ul> The above requirement is only needed for Pin 15. |
| ^vCLKIN_SEL_tri    | 7      | I                   | 3-Level Clock Input Select <ul style="list-style-type: none"> <li>Low = CLKIN0 goes to all outputs</li> <li>Mid = CLKIN0 goes to Bank 0, CLKIN1 goes to Bank 1</li> <li>High = CLKIN1 goes to all outputs</li> </ul>                                                                                                                                                                                                                                                                                                                                            |
| vZOUT_SEL          | 11     | I                   | LP-HCSL Differential Clock Output Impedance Select. Internal pulldown resistor. <ul style="list-style-type: none"> <li>Low = 85<math>\Omega</math></li> <li>High = 100<math>\Omega</math></li> </ul>                                                                                                                                                                                                                                                                                                                                                            |
| LOS#               | 13     | O                   | Loss of Input Clock Signal Active Low. Open drain. Requires external pullup resistor. <ul style="list-style-type: none"> <li>Low = Invalid input clock.</li> <li>High = Valid input clock.</li> </ul>                                                                                                                                                                                                                                                                                                                                                           |
| VDD_IN0            | 3      | P                   | Power supply for CLKIN0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| VDD_IN1            | 6      | P                   | Power supply for CLKIN1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| VDDO_BANK1         | 8      | P                   | Power supply for output bank 1 (CLK2)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Table 5-5. LMKDB1202 Pin Functions (continued)**

| PIN        |         | TYPE <sup>(1)</sup> | DESCRIPTION                           |
|------------|---------|---------------------|---------------------------------------|
| NAME       | NO.     |                     |                                       |
| VDD        | 14      | P                   | Power supply                          |
| VDDO_BANK0 | 18      | P                   | Power supply for output bank 0 (CLK1) |
| VDD_DIG    | 19      | P                   | Power supply for digital              |
| GND        | 20, DAP | G                   | Ground.                               |

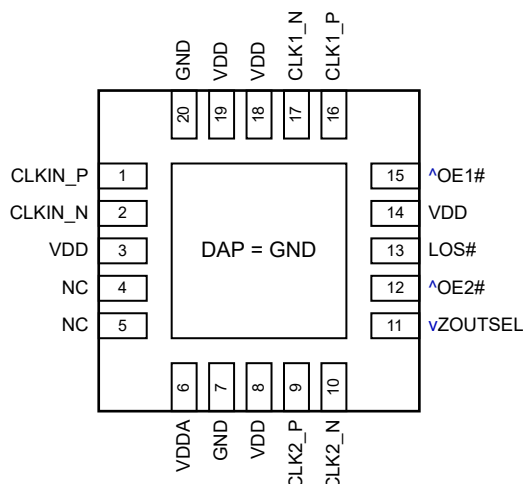


Figure 5-6. LMKDB1102 3 x 3 mm 20-pin QFN

Table 5-6. LMKDB1102 Pin Functions

| PIN       |                  | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------|------------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME      | NO.              |                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| CLKIN_P,  | 1                | I                   | Differential clock input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| CLKIN_N   | 2                | I                   | Differential clock input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| NC        | 4, 5             | I                   | No connect. Leave floating                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| CLK2_P    | 9                | O                   | LP-HCSL differential clock output 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| CLK2_N    | 10               | O                   | LP-HCSL differential clock output 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| CLK1_P    | 16               | O                   | LP-HCSL differential clock output 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| CLK1_N    | 17               | O                   | LP-HCSL differential clock output 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| ^OE2#     | 12               | I                   | Output Enable for CLK2 Active Low. Internal pullup resistor. No connect if unused.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| ^OE1#     | 15               | I                   | Output Enable for CLK1 Active Low. Internal pullup resistor. No connect if unused. This pin requires either of below conditions to dynamically enable or disable the CLK1 after power-up. If CLK1 stays enabled or disabled after power-up, then below conditions do not need to be met. <ul style="list-style-type: none"> <li>This pin is driven low or high at <math>\geq 0.1</math> V/ns slew rate.</li> <li>The resistance used to drive this pin is <math>\leq 1</math> k<math>\Omega</math>.</li> </ul> The above requirement is only needed for Pin 15. |
| GND       | 7                | I or GND            | Digital 0 or GND. Tie to GND through pull down resistor or directly tie to GND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| vZOUT_SEL | 11               | I                   | LP-HCSL Differential Clock Output Impedance Select. Internal pulldown resistor. <ul style="list-style-type: none"> <li>Low = 85 <math>\Omega</math></li> <li>High = 100 <math>\Omega</math></li> </ul>                                                                                                                                                                                                                                                                                                                                                          |
| LOS#      | 13               | O                   | Loss of Input Clock Signal Active Low. Open drain. Requires external pullup resistor. <ul style="list-style-type: none"> <li>Low = Invalid input clock.</li> <li>High = Valid input clock.</li> </ul>                                                                                                                                                                                                                                                                                                                                                           |
| VDDA      | 6                | P                   | Analog power supply. Additional power supply filtering is recommended. See <a href="#">Power Supply Recommendations</a> for details.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| VDD       | 3, 8, 14, 18, 19 | P                   | Power supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| GND       | 20, DAP          | G                   | Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                 | MIN  | MAX  | UNIT |
|------------------|-------------------------------------------------|------|------|------|
| V <sub>DDx</sub> | Supply voltage on any VDD pin                   | −0.3 | 3.63 | V    |
| V <sub>IN</sub>  | Input voltage on CLKIN and digital input pins   | −0.3 | 3.63 | V    |
| I <sub>OUT</sub> | Output current - continuous (CLKOUT)            |      | 30   | mA   |
|                  | Output current - continuous (SMB_DATA, SBI_OUT) |      | 25   | mA   |
|                  | Output current - surge (CLKOUT)                 |      | 60   | mA   |
|                  | Output current - surge (SMB_DATA, SBI_OUT)      |      | 50   | mA   |
| T <sub>S</sub>   | Storage temperature                             | −65  | 150  | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

|                    |                         |                                                                        | VALUE | UNIT |
|--------------------|-------------------------|------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 <sup>(1)</sup>     | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per ANSI/ESDA/ JEDEC JS-002 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                   |                                               | MIN  | NOM | MAX  | UNIT |
|-------------------|-----------------------------------------------|------|-----|------|------|
| T <sub>J</sub>    | Junction temperature                          |      |     | 125  | °C   |
| T <sub>A</sub>    | Ambient temperature                           | −40  |     | 105  | °C   |
| V <sub>DD</sub>   | Power supply voltage                          | 2.97 | 3.3 | 3.6  | V    |
|                   |                                               | 1.71 | 1.8 | 1.89 | V    |
| V <sub>IN</sub>   | Input voltage on CLKIN and digital input pins | −0.3 |     | 3.6  | V    |
| t <sub>ramp</sub> | Power ramping time                            | 0.05 |     | 5    | ms   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | NPP (TLGA) | RKP (VQFN) | REX (VQFN) | REY (VQFN) | UNIT |
|-------------------------------|----------------------------------------------|------------|------------|------------|------------|------|
|                               |                                              | 80 PINS    | 40 PINS    | 28 PINS    | 20 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 33.1       | 33.6       | 44.2       | 46.4       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 31.9       | 24.6       | 36.8       | 50.4       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 16.2       | 13.8       | 20.6       | 20.3       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.5        | 0.4        | 0.9        | 1.1        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 16.0       | 13.7       | 20.6       | 20.3       | °C/W |

| THERMAL METRIC <sup>(1)</sup> |                                              | NPP (TLGA) | RKP (VQFN) | REX (VQFN) | REY (VQFN) | UNIT |
|-------------------------------|----------------------------------------------|------------|------------|------------|------------|------|
|                               |                                              | 80 PINS    | 40 PINS    | 28 PINS    | 20 PINS    |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 1.8        | 4.2        | 5.9        | 6.5        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                               |                                                                             | TEST CONDITIONS                                                                                            | MIN   | TYP | MAX   | UNIT |
|---------------------------------------------------------|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-------|-----|-------|------|
| <b>CLOCK INPUT REQUIREMENTS</b>                         |                                                                             |                                                                                                            |       |     |       |      |
| V <sub>IN, cross</sub>                                  | Clock input crossing point voltage                                          |                                                                                                            | 100   |     | 1400  | mV   |
| DC <sub>IN</sub>                                        | Clock input duty cycle                                                      |                                                                                                            | 45    |     | 55    | %    |
| V <sub>IN</sub>                                         | Differential clock input amplitude (half of differential peak-peak voltage) | f <sub>0</sub> ≤ 300 MHz                                                                                   | 200   |     | 2000  | mV   |
|                                                         |                                                                             | 300 MHz < f <sub>0</sub> ≤ 400 MHz                                                                         | 250   |     | 2000  | mV   |
| dV <sub>IN</sub> /dt                                    | Clock input slew rate                                                       | Measured from –150 mV to +150 mV on the differential waveform                                              | 0.6   |     |       | V/ns |
| <b>CLOCK OUTPUT CHARACTERISTICS - 100 MHz 85 Ω PCIe</b> |                                                                             |                                                                                                            |       |     |       |      |
| V <sub>OH,AC</sub>                                      | Output voltage high                                                         | DB2000QL AC test load <sup>(6)</sup>                                                                       | 670   |     | 820   | mV   |
| V <sub>OL,AC</sub>                                      | Output voltage low                                                          |                                                                                                            | –100  |     | 100   | mV   |
| V <sub>max,AC</sub>                                     | Output max voltage (including overshoot)                                    |                                                                                                            | 670   |     | 920   | mV   |
| V <sub>min,AC</sub>                                     | Output min voltage (including undershoot)                                   |                                                                                                            | –100  |     | 100   | mV   |
| V <sub>OH,DC</sub>                                      | Output voltage high with DC test load                                       | DB2000QL DC test load <sup>(2)</sup>                                                                       | 225   |     | 270   | mV   |
| V <sub>OL,DC</sub>                                      | Output voltage low with DC test load                                        |                                                                                                            | 10    |     | 150   | mV   |
| V <sub>ovs,DC</sub>                                     | Output overshoot voltage with DC test load                                  |                                                                                                            |       |     | 75    | mV   |
| V <sub>uds,DC</sub>                                     | Output undershoot voltage with DC test load                                 |                                                                                                            | –75   |     |       | mV   |
| Z <sub>diff</sub>                                       | Differential output impedance                                               | Measured at V <sub>OL</sub> /V <sub>OH</sub> , V <sub>DD</sub> = 3.3 V                                     | 80.75 | 85  | 89.25 | Ω    |
|                                                         |                                                                             | Measured at V <sub>OL</sub> /V <sub>OH</sub> , V <sub>DD</sub> = 1.8 V                                     | 81    | 85  | 90    | Ω    |
| Z <sub>diff-crossing</sub>                              | Differential output impedance - crossing                                    | Measured during transition                                                                                 | 68    | 85  | 102   | Ω    |
| dV/dt                                                   | Output slew rate                                                            | Measured from –150 mV to +150 mV on the differential waveform. Lowest slew rate <sup>(6) (7)</sup>         | 1.5   |     | 2.2   | V/ns |
|                                                         |                                                                             | Measured from –150 mV to +150 mV on the differential waveform. Low slew rate <sup>(6) (7)</sup>            | 1.8   |     | 2.6   | V/ns |
|                                                         |                                                                             | Measured from –150 mV to +150 mV on the differential waveform. High slew rate (default) <sup>(6) (7)</sup> | 2     |     | 2.9   | V/ns |
|                                                         |                                                                             | Measured from –150 mV to +150 mV on the differential waveform. Highest slew rate <sup>(6) (7)</sup>        | 2.4   |     | 4     | V/ns |
| ΔdV/dt                                                  | Rising edge rate to falling edge rate matching                              | DB2000QL AC test load <sup>(6)</sup>                                                                       |       |     | 10    | %    |
| DCD                                                     | Duty cycle distortion                                                       | Measured on the differential waveform. Input duty cycle = 50% <sup>(6)</sup>                               | –1    |     | 1     | %    |
| V <sub>cross,AC</sub>                                   | Absolute crossing point voltage                                             | DB2000QL AC test load <sup>(6)</sup>                                                                       | 250   |     | 550   | mV   |
| V <sub>cross,DC</sub>                                   | Absolute crossing point voltage                                             | DB2000QL DC test load <sup>(2)</sup>                                                                       | 130   |     | 200   | mV   |
| ΔV <sub>cross,A</sub><br>C                              | Variation of V <sub>cross</sub> over all clock edges                        | DB2000QL AC test load <sup>(6)</sup>                                                                       |       |     | 140   | mV   |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                                  |                                                        | TEST CONDITIONS                                                                                         | MIN  | TYP | MAX | UNIT     |
|----------------------------------------------------------------------------|--------------------------------------------------------|---------------------------------------------------------------------------------------------------------|------|-----|-----|----------|
| $\Delta V_{\text{cross-DC}}$                                               | Variation of $V_{\text{cross}}$ over all clock edges   | DB2000QL DC test load <sup>(2)</sup>                                                                    |      |     | 35  | mV       |
| $ V_{\text{RB}} $                                                          | Absolute value of ring back voltage as defined in PCIe | DB2000QL AC test load <sup>(6)</sup>                                                                    | 100  |     |     | mV       |
| $t_{\text{stable}}$                                                        | Time before $V_{\text{RB}}$ is allowed                 | DB2000QL AC test load <sup>(6)</sup>                                                                    | 500  |     |     | ps       |
| <b>CLOCK OUTPUT CHARACTERISTICS - 100 MHz 100 <math>\Omega</math> PCIe</b> |                                                        |                                                                                                         |      |     |     |          |
| $V_{\text{max}}$                                                           | Output voltage high including overshoot                | PCIe AC test load <sup>(1)</sup>                                                                        | 670  |     | 920 | mV       |
| $V_{\text{min}}$                                                           | Output voltage low including undershoot                | PCIe AC test load <sup>(1)</sup>                                                                        | –100 |     | 100 | mV       |
| $V_{\text{OH}}$                                                            | Output voltage high                                    | PCIe AC test load <sup>(1)</sup>                                                                        | 670  |     | 820 | mV       |
| $V_{\text{OL}}$                                                            | Output voltage low                                     | PCIe AC test load <sup>(1)</sup>                                                                        | –100 |     | 100 | mV       |
| $Z_{\text{diff}}$                                                          | Differential output DC impedance                       | $V_{\text{DD}} = 3.3 \text{ V}$                                                                         | 95   | 100 | 105 | $\Omega$ |
|                                                                            |                                                        | $V_{\text{DD}} = 1.8 \text{ V}$                                                                         | 95   | 100 | 105 | $\Omega$ |
| dV/dt                                                                      | Output slew rate                                       | Measured from –150 mV to +150 mV on the differential waveform. Lowest slew rate <sup>(1) (7)</sup>      | 1.5  |     | 2.2 | V/ns     |
|                                                                            |                                                        | Measured from –150 mV to +150 mV on the differential waveform. Low slew rate <sup>(1) (7)</sup>         | 1.8  |     | 2.6 | V/ns     |
|                                                                            |                                                        | Measured from –150 mV to +150 mV on the differential waveform. High slew rate <sup>(1) (7)</sup>        | 2    |     | 2.9 | V/ns     |
|                                                                            |                                                        | Measured from –150 mV to +150 mV on the differential waveform. Highest slew rate <sup>(1) (7)</sup>     | 2.4  |     | 4   | V/ns     |
| $\Delta dV/dt$                                                             | Rising edge rate to falling edge rate matching         | PCIe AC test load <sup>(1)</sup>                                                                        |      |     | 10  | %        |
| DCD                                                                        | Duty cycle distortion                                  | Measured on the differential waveform. Input duty cycle = 50% <sup>(1)</sup>                            | –1   |     | 1   | %        |
| $V_{\text{cross}}$                                                         | Absolute crossing point voltage                        | PCIe AC test load <sup>(1)</sup>                                                                        | 250  |     | 550 | mV       |
| $\Delta V_{\text{cross}}$                                                  | Variation of $V_{\text{cross}}$ over all clock edges   | PCIe AC test load <sup>(1)</sup>                                                                        |      |     | 140 | mV       |
| $ V_{\text{RB}} $                                                          | Absolute value of ring back voltage as defined in PCIe | PCIe AC test load <sup>(1)</sup>                                                                        | 100  |     |     | mV       |
| $t_{\text{stable}}$                                                        | Time before $V_{\text{RB}}$ is allowed                 | PCIe AC test load <sup>(1)</sup>                                                                        | 500  |     |     | ps       |
| <b>CLOCK OUTPUT CHARACTERISTICS - non-PCIe</b>                             |                                                        |                                                                                                         |      |     |     |          |
| $V_{\text{OH}}$                                                            | Output voltage high                                    | Output swing programmed to 800 mV. $f_0 = 156.25 \text{ MHz}$ or $312.5 \text{ MHz}$                    | 720  |     | 880 | mV       |
| $V_{\text{OL}}$                                                            | Output voltage low                                     |                                                                                                         | –120 |     | 120 | mV       |
| $V_{\text{OH}}$                                                            | Output voltage high                                    | Output swing programmed to 900 mV. $f_0 = 156.25 \text{ MHz}$ or $312.5 \text{ MHz}$                    | 780  |     | 980 | mV       |
| $V_{\text{OL}}$                                                            | Output voltage low                                     |                                                                                                         | –120 |     | 120 | mV       |
| $t_{\text{R}}, t_{\text{F}}$                                               | Rise/fall time on single-ended waveform, 20% to 80%    | Output swing programmed to 800 mV. Fastest slew rate. $f_0 = 156.25 \text{ MHz}$ or $312.5 \text{ MHz}$ |      |     | 340 | ps       |
|                                                                            |                                                        | Output swing programmed to 900 mV. Fastest slew rate. $f_0 = 156.25 \text{ MHz}$ or $312.5 \text{ MHz}$ |      |     | 370 | ps       |
| DCD                                                                        | Duty cycle distortion                                  | Input duty cycle = 50%                                                                                  | –1   |     | 1   | %        |
| <b>SKEW AND DELAY CHARACTERISTICS</b>                                      |                                                        |                                                                                                         |      |     |     |          |
| $t_{\text{skew}}$                                                          | Output-to-output skew                                  | Same bank                                                                                               |      |     | 50  | ps       |
|                                                                            |                                                        | Regardless of banks                                                                                     |      |     | 50  | ps       |
|                                                                            | Part-to-part skew                                      |                                                                                                         |      |     | 330 | ps       |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                   |                                 | TEST CONDITIONS                                                                                                                                                                                 | MIN | TYP | MAX  | UNIT  |
|---------------------------------------------|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|-------|
| $t_{PD}$                                    | Input-to-output delay           |                                                                                                                                                                                                 |     |     | 1    | ns    |
| $\Delta t_{PD}$                             | Input-to-output delay variation | Single device over temperature and voltage                                                                                                                                                      |     |     | 1.7  | ps/°C |
| <b>FREQUENCY AND TIMING CHARACTERISTICS</b> |                                 |                                                                                                                                                                                                 |     |     |      |       |
| $f_0$                                       | Operating frequency             | Automatic Output Disable functionality is disabled                                                                                                                                              | 1   |     | 400  | MHz   |
|                                             |                                 | Automatic Output Disable functionality is enabled                                                                                                                                               | 25  |     | 400  | MHz   |
| $t_{startup}$                               | Startup time                    | Cold start. Measured from VDD valid (90% of final VDD) to output clock stable <sup>(3)</sup> . Input clock is provided before VDD is valid. PWRGD_PWRDN# pin is tied to VDD. $f_0 \geq 100$ MHz |     |     | 0.4  | ms    |
|                                             |                                 | Cold start. Measured from VDD valid (90% of final VDD) to output clock stable <sup>(3)</sup> . Input clock is provided before VDD is valid. PWRGD_PWRDN# pin is tied to VDD. $f_0 < 100$ MHz    |     |     | 0.8  | ms    |
| $t_{stable}$                                | Clock stabilization time        | VDD is stable. Measured from PWRGD assertion <sup>(4)</sup> to output clock stable. $f_0 \geq 100$ MHz <sup>(3)</sup>                                                                           |     |     | 0.4  | ms    |
|                                             |                                 | VDD is stable. Measured from PWRGD assertion <sup>(4)</sup> to output clock stable. $f_0 < 100$ MHz <sup>(3)</sup>                                                                              |     |     | 0.8  | ms    |
| $t_{PD\#}$                                  | Powerdown deassertion time      | Measured from PWRDN# deassertion <sup>(4)</sup> to output clock stable. $f_0 \geq 100$ MHz <sup>(3)</sup>                                                                                       |     |     | 0.15 | ms    |
|                                             |                                 | Measured from PWRDN# deassertion <sup>(4)</sup> to output clock stable. $f_0 < 100$ MHz <sup>(3)</sup>                                                                                          |     |     | 0.5  | ms    |
| $t_{OE}$                                    | Output enable/disable time      | Time elapsed from OE assertion/deassertion <sup>(4)</sup> to output clock starts/stops                                                                                                          | 4   |     | 10   | clk   |
| $t_{LOS-assert}$                            | LOS# assertion time             | Time elapsed from loss of input clock to LOS# assertion. $f_0 < 100$ MHz                                                                                                                        |     |     | 120  | ns    |
|                                             |                                 | Time elapsed from loss of input clock to LOS# assertion. $f_0 \geq 100$ MHz                                                                                                                     |     |     | 120  | ns    |
| $t_{LOS-deassert}$                          | LOS# deassertion time           | Time elapsed from presence of input clock to LOS# deassertion. $f_0 < 100$ MHz                                                                                                                  |     |     | 340  | ns    |
|                                             |                                 | Time elapsed from presence of input clock to LOS# deassertion. $f_0 \geq 100$ MHz                                                                                                               |     |     | 105  | ns    |
| $t_{AOD}$                                   | Automatic output disable time   | Time elapsed from LOS# assertion to output disable (both outputs are low/low). $f_0 < 100$ MHz                                                                                                  |     |     | 0.07 | ns    |
|                                             |                                 | Time elapsed from LOS# assertion to output disable (both outputs are low/low), $f_0 \geq 100$ MHz                                                                                               |     |     | 0.07 | ns    |
| $t_{AOE}$                                   | Automatic output enable time    | Time elapsed from LOS# deassertion to output clock stable. $f_0 < 100$ MHz <sup>(3)</sup>                                                                                                       |     |     | 115  | ns    |
|                                             |                                 | Time elapsed from LOS# deassertion to output clock stable, $f_0 \geq 100$ MHz <sup>(3)</sup>                                                                                                    |     |     | 22   | ns    |
| $t_{switch}$                                | Switch time                     | Switch between two 100MHz input clocks (MUX only)                                                                                                                                               |     |     | 70   | ns    |
| <b>JITTER CHARACTERISTICS</b>               |                                 |                                                                                                                                                                                                 |     |     |      |       |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER             |                      | TEST CONDITIONS                                                                                                                                                                                                                                                                           | MIN   | TYP   | MAX   | UNIT |
|-----------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|------|
| J <sub>PCle1-CC</sub> | PCle Gen 1 CC jitter | Single clock input. Input slew rate $\geq 3.5$ V/ns. Differential input swing $\geq 1600$ mV                                                                                                                                                                                              |       |       | 442.5 | fs   |
| J <sub>PCle2-CC</sub> | PCle Gen 2 CC jitter |                                                                                                                                                                                                                                                                                           |       |       | 39    | fs   |
| J <sub>PCle3-CC</sub> | PCle Gen 3 CC jitter |                                                                                                                                                                                                                                                                                           |       |       | 12.3  | fs   |
| J <sub>PCle4-CC</sub> | PCle Gen 4 CC jitter |                                                                                                                                                                                                                                                                                           |       |       | 12.3  | fs   |
| J <sub>PCle5-CC</sub> | PCle Gen 5 CC jitter |                                                                                                                                                                                                                                                                                           |       |       | 4.9   | fs   |
| J <sub>PCle6-CC</sub> | PCle Gen 6 CC jitter |                                                                                                                                                                                                                                                                                           |       |       | 3     | fs   |
| J <sub>PCle2-IR</sub> | PCle Gen 2 IR jitter |                                                                                                                                                                                                                                                                                           |       |       | 33.8  | fs   |
| J <sub>PCle3-IR</sub> | PCle Gen 3 IR jitter |                                                                                                                                                                                                                                                                                           |       |       | 14.1  | fs   |
| J <sub>PCle4-IR</sub> | PCle Gen 4 IR jitter |                                                                                                                                                                                                                                                                                           |       |       | 14.5  | fs   |
| J <sub>PCle5-IR</sub> | PCle Gen 5 IR jitter |                                                                                                                                                                                                                                                                                           |       |       | 3.9   | fs   |
| J <sub>PCle6-IR</sub> | PCle Gen 6 IR jitter |                                                                                                                                                                                                                                                                                           |       |       | 3     | fs   |
| J <sub>PCle1-CC</sub> | PCle Gen 1 CC jitter | Single clock input. Input slew rate $\geq 1.5$ V/ns. Differential input swing $\geq 800$ mV                                                                                                                                                                                               |       |       | 583.2 | fs   |
| J <sub>PCle2-CC</sub> | PCle Gen 2 CC jitter |                                                                                                                                                                                                                                                                                           |       |       | 51.3  | fs   |
| J <sub>PCle3-CC</sub> | PCle Gen 3 CC jitter |                                                                                                                                                                                                                                                                                           |       |       | 16    | fs   |
| J <sub>PCle4-CC</sub> | PCle Gen 4 CC jitter |                                                                                                                                                                                                                                                                                           |       |       | 16    | fs   |
| J <sub>PCle5-CC</sub> | PCle Gen 5 CC jitter |                                                                                                                                                                                                                                                                                           |       |       | 6.4   | fs   |
| J <sub>PCle6-CC</sub> | PCle Gen 6 CC jitter |                                                                                                                                                                                                                                                                                           |       |       | 3.9   | fs   |
| J <sub>PCle2-IR</sub> | PCle Gen 2 IR jitter |                                                                                                                                                                                                                                                                                           |       |       | 41.9  | fs   |
| J <sub>PCle3-IR</sub> | PCle Gen 3 IR jitter |                                                                                                                                                                                                                                                                                           |       |       | 18.3  | fs   |
| J <sub>PCle4-IR</sub> | PCle Gen 4 IR jitter |                                                                                                                                                                                                                                                                                           |       |       | 18.9  | fs   |
| J <sub>PCle5-IR</sub> | PCle Gen 5 IR jitter |                                                                                                                                                                                                                                                                                           |       |       | 5.1   | fs   |
| J <sub>PCle6-IR</sub> | PCle Gen 6 IR jitter |                                                                                                                                                                                                                                                                                           |       |       | 3.8   | fs   |
| J <sub>PCle1-CC</sub> | PCle Gen 1 CC jitter | Both inputs (for MUX only) have running clocks. CLK_SEL pin = low (CLKIN0 = 100MHz, CLKIN1 = 99.75MHz), mid (CLKIN0 = 100MHz, CLKIN1 = 99.75MHz) or high (CLKIN0 = 99.7MHz, CLKIN1 = 100MHz). Input slew rate $\geq 3.5$ V/ns. Differential input swing $\geq 1600$ mV                    | 255.3 | 517.5 |       | fs   |
| J <sub>PCle2-CC</sub> | PCle Gen 2 CC jitter |                                                                                                                                                                                                                                                                                           | 30    | 45.3  |       | fs   |
| J <sub>PCle3-CC</sub> | PCle Gen 3 CC jitter |                                                                                                                                                                                                                                                                                           | 8.3   | 13.7  |       | fs   |
| J <sub>PCle4-CC</sub> | PCle Gen 4 CC jitter |                                                                                                                                                                                                                                                                                           | 8.3   | 13.7  |       | fs   |
| J <sub>PCle5-CC</sub> | PCle Gen 5 CC jitter |                                                                                                                                                                                                                                                                                           | 2.9   | 5.5   |       | fs   |
| J <sub>PCle6-CC</sub> | PCle Gen 6 CC jitter |                                                                                                                                                                                                                                                                                           | 2     | 3.5   |       | fs   |
| J <sub>PCle2-IR</sub> | PCle Gen 2 IR jitter |                                                                                                                                                                                                                                                                                           | 31.9  | 48.5  |       | fs   |
| J <sub>PCle3-IR</sub> | PCle Gen 3 IR jitter |                                                                                                                                                                                                                                                                                           | 8.8   | 21.7  |       | fs   |
| J <sub>PCle4-IR</sub> | PCle Gen 4 IR jitter |                                                                                                                                                                                                                                                                                           | 8.8   | 21.7  |       | fs   |
| J <sub>PCle5-IR</sub> | PCle Gen 5 IR jitter |                                                                                                                                                                                                                                                                                           | 3.4   | 6.7   |       | fs   |
| J <sub>PCle6-IR</sub> | PCle Gen 6 IR jitter |                                                                                                                                                                                                                                                                                           | 2.8   | 4.7   |       | fs   |
| J <sub>PCle1-CC</sub> | PCle Gen 1 CC jitter | Both inputs (for MUX only) have running clocks. CLK_SEL pin = low (CLKIN0 = 100MHz, CLKIN1 = 99.75MHz), mid (CLKIN0 = 100MHz, CLKIN1 = 99.75MHz) or high (CLKIN0 = 99.7MHz, CLKIN1 = 100MHz). Crosstalk included. Input slew rate $\geq 1.5$ V/ns. Differential input swing $\geq 800$ mV | 388.6 | 669.5 |       | fs   |
| J <sub>PCle2-CC</sub> | PCle Gen 2 CC jitter |                                                                                                                                                                                                                                                                                           | 35.4  | 57    |       | fs   |
| J <sub>PCle3-CC</sub> | PCle Gen 3 CC jitter |                                                                                                                                                                                                                                                                                           | 10.1  | 17.1  |       | fs   |
| J <sub>PCle4-CC</sub> | PCle Gen 4 CC jitter |                                                                                                                                                                                                                                                                                           | 10.1  | 17.1  |       | fs   |
| J <sub>PCle5-CC</sub> | PCle Gen 5 CC jitter |                                                                                                                                                                                                                                                                                           | 3.7   | 7.4   |       | fs   |
| J <sub>PCle6-CC</sub> | PCle Gen 6 CC jitter |                                                                                                                                                                                                                                                                                           | 2.4   | 4.4   |       | fs   |
| J <sub>PCle2-IR</sub> | PCle Gen 2 IR jitter |                                                                                                                                                                                                                                                                                           | 35.4  | 57    |       | fs   |
| J <sub>PCle3-IR</sub> | PCle Gen 3 IR jitter |                                                                                                                                                                                                                                                                                           | 9.8   | 24    |       | fs   |
| J <sub>PCle4-IR</sub> | PCle Gen 4 IR jitter |                                                                                                                                                                                                                                                                                           | 9.9   | 24    |       | fs   |
| J <sub>PCle5-IR</sub> | PCle Gen 5 IR jitter |                                                                                                                                                                                                                                                                                           | 4.3   | 8.6   |       | fs   |
| J <sub>PCle6-IR</sub> | PCle Gen 6 IR jitter |                                                                                                                                                                                                                                                                                           | 3.3   | 6     |       | fs   |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                      |                                                                                        | TEST CONDITIONS                                                               | MIN | TYP  | MAX  | UNIT |
|--------------------------------|----------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-----|------|------|------|
| J <sub>DB2000QL</sub>          | DB2000QL filter                                                                        | Input slew rate ≥ 1.5 V/ns. Differential input swing ≥ 800 mV <sup>(6)</sup>  |     | 8.7  | 11.5 | fs   |
|                                |                                                                                        | Input slew rate ≥ 3.5 V/ns. Differential input swing ≥ 1600 mV <sup>(6)</sup> |     | 6.5  | 9    | fs   |
| J <sub>RMS-additive</sub>      | Additive 12 kHz to 20 MHz RMS jitter                                                   | f = 100 MHz, slew rate ≥ 3.5 V/ns                                             |     | 27.3 | 37.5 | fs   |
|                                |                                                                                        | f = 100 MHz, slew rate ≥ 1.5 V/ns                                             |     | 37.4 | 48.5 | fs   |
|                                | Additive 12 kHz to 20 MHz RMS jitter                                                   | f = 156.25 MHz, slew rate ≥ 3.5 V/ns                                          |     | 21.9 | 31   | fs   |
|                                |                                                                                        | f = 156.25 MHz, slew rate ≥ 1.5 V/ns                                          |     | 29.4 | 38.5 | fs   |
|                                | Additive 12 kHz to 70 MHz RMS jitter                                                   | f = 156.25 MHz, slew rate ≥ 3.5 V/ns                                          |     | 35.1 | 48.5 | fs   |
|                                |                                                                                        | f = 156.25 MHz, slew rate ≥ 1.5 V/ns                                          |     | 47.1 | 60.5 | fs   |
|                                | Additive 12 kHz to 20 MHz RMS jitter                                                   | f = 312.5 MHz, slew rate ≥ 3.5 V/ns                                           |     | 19.3 | 28   | fs   |
|                                |                                                                                        | f = 312.5 MHz, slew rate ≥ 1.5 V/ns                                           |     | 27.4 | 39.5 | fs   |
|                                | Additive 12 kHz to 70 MHz RMS jitter                                                   | f = 312.5 MHz, slew rate ≥ 3.5 V/ns                                           |     | 29.5 | 41.5 | fs   |
|                                |                                                                                        | f = 312.5 MHz, slew rate ≥ 1.5 V/ns                                           |     | 40.7 | 58   | fs   |
| SUPPLY CURRENT CHARACTERISTICS |                                                                                        |                                                                               |     |      |      |      |
| I <sub>DD,total</sub>          | LMKDB1102 total supply current                                                         | All outputs running, f <sub>0</sub> = 100 MHz                                 |     |      | 41   | mA   |
| I <sub>DD,total</sub>          | LMKDB1202 total supply current                                                         | All outputs running, f <sub>0</sub> = 100 MHz                                 |     |      | 41   | mA   |
| I <sub>DD,total</sub>          | LMKDB1104 total supply current                                                         | All outputs running, f <sub>0</sub> = 100 MHz                                 |     |      | 54   | mA   |
| I <sub>DD,total</sub>          | LMKDB1204 total supply current                                                         | All outputs running, f <sub>0</sub> = 100 MHz                                 |     |      | 54   | mA   |
| I <sub>DD,total</sub>          | LMKDB1108 total supply current                                                         | All outputs running, f <sub>0</sub> = 100 MHz                                 |     |      | 85.7 | mA   |
| I <sub>DD,total</sub>          | LMKDB1120 total supply current                                                         | All outputs running, f <sub>0</sub> = 100 MHz                                 |     |      | 162  | mA   |
| I <sub>DD,core</sub>           | LMKDB1102 core supply current                                                          | Pin PWRGD/PWRDN# = high, all outputs disabled                                 |     |      | 25.5 | mA   |
| I <sub>DD,core</sub>           | LMKDB1202 core supply current                                                          | Pin PWRGD/PWRDN# = high, all outputs disabled                                 |     |      | 25.5 | mA   |
| I <sub>DD,core</sub>           | LMKDB1104 core supply current                                                          | Pin PWRGD/PWRDN# = high, all outputs disabled                                 |     |      | 25.5 | mA   |
| I <sub>DD,core</sub>           | LMKDB1204 core supply current                                                          | Pin PWRGD/PWRDN# = high, all outputs disabled                                 |     |      | 25.5 | mA   |
| I <sub>DD,core</sub>           | LMKDB1108 core supply current                                                          | Pin PWRGD/PWRDN# = high, all outputs disabled                                 |     |      | 36.3 | mA   |
| I <sub>DD,core</sub>           | LMKDB1120 core supply current                                                          | Pin PWRGD/PWRDN# = high, all outputs disabled                                 |     |      | 37.9 | mA   |
| I <sub>DDO</sub>               | Output supply current per output                                                       | f <sub>0</sub> = 100 MHz                                                      |     |      | 6.4  | mA   |
|                                |                                                                                        | f <sub>0</sub> = 400 MHz                                                      |     |      | 9.2  | mA   |
| I <sub>PD</sub>                | LMKDB1102, LMKDB1202, LMKDB1104, LMKDB1204, LMKDB1108 and LMKDB1120 power down current | Pin PWRGD/PWRDN# = low                                                        |     |      | 5.6  | mA   |
| PSNR CHARACTERISTICS           |                                                                                        |                                                                               |     |      |      |      |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                        |                                                                      | TEST CONDITIONS                                    | MIN                    | TYP                   | MAX  | UNIT |
|----------------------------------|----------------------------------------------------------------------|----------------------------------------------------|------------------------|-----------------------|------|------|
| PSNR                             | Power Supply Noise Rejection, V <sub>DD</sub> = 3.3 V <sup>(5)</sup> | 10 kHz noise ripple                                |                        |                       | −93  | dBc  |
|                                  |                                                                      | 50 kHz noise ripple                                |                        |                       | −91  | dBc  |
|                                  |                                                                      | 100 kHz noise ripple                               |                        |                       | −91  | dBc  |
|                                  |                                                                      | 500 kHz noise ripple                               |                        |                       | −95  | dBc  |
|                                  |                                                                      | 1 MHz noise ripple                                 |                        |                       | −96  | dBc  |
|                                  |                                                                      | 5 MHz noise ripple                                 |                        |                       | −111 | dBc  |
|                                  |                                                                      | 10 MHz noise ripple                                |                        |                       | −99  | dBc  |
|                                  | Power Supply Noise Rejection, V <sub>DD</sub> = 1.8 V <sup>(5)</sup> | 10 kHz noise ripple                                |                        |                       | −85  | dBc  |
|                                  |                                                                      | 50 kHz noise ripple                                |                        |                       | −89  | dBc  |
|                                  |                                                                      | 100 kHz noise ripple                               |                        |                       | −91  | dBc  |
|                                  |                                                                      | 500 kHz noise ripple                               |                        |                       | −93  | dBc  |
|                                  |                                                                      | 1 MHz noise ripple                                 |                        |                       | −94  | dBc  |
|                                  |                                                                      | 5 MHz noise ripple                                 |                        |                       | −109 | dBc  |
|                                  |                                                                      | 10 MHz noise ripple                                |                        |                       | −97  | dBc  |
| I/O CHARACTERISTICS              |                                                                      |                                                    |                        |                       |      |      |
| V <sub>IH</sub>                  | Input voltage high                                                   | 2-level logic input, V <sub>DD</sub> = 3.3 V ± 10% | 2                      | V <sub>DD</sub> + 0.3 | V    |      |
| V <sub>IL</sub>                  | Input voltage low                                                    |                                                    | −0.3                   | 0.8                   | V    |      |
| V <sub>IH</sub>                  | Input voltage high                                                   | 3-level logic input, V <sub>DD</sub> = 3.3 V ± 10% | 2.4                    | V <sub>DD</sub> + 0.3 | V    |      |
| V <sub>IM</sub>                  | Input voltage mid                                                    |                                                    | 1.2                    | 1.8                   | V    |      |
| V <sub>IL</sub>                  | Input voltage low                                                    |                                                    | −0.3                   | 0.8                   | V    |      |
| V <sub>IH</sub>                  | Input voltage high                                                   | 2-level logic input, V <sub>DD</sub> = 1.8 V ± 5%  | 1.3                    | V <sub>DD</sub> + 0.3 | V    |      |
| V <sub>IL</sub>                  | Input voltage low                                                    |                                                    | −0.3                   | 0.4                   | V    |      |
| V <sub>IH</sub>                  | Input voltage high                                                   | 3-level logic input, V <sub>DD</sub> = 1.8 V ± 5%  | 1.3                    | V <sub>DD</sub> + 0.3 | V    |      |
| V <sub>IM</sub>                  | Input voltage mid                                                    |                                                    | 0.65                   | 0.95                  | V    |      |
| V <sub>IL</sub>                  | Input voltage low                                                    |                                                    | −0.3                   | 0.4                   | V    |      |
| V <sub>OH</sub>                  | Output high voltage                                                  | SBI_OUT, I <sub>OH</sub> = -2 mA                   | 2.4                    | V <sub>DD</sub> + 0.3 | V    |      |
| V <sub>OL</sub>                  | Output low voltage                                                   | SBI_OUT, I <sub>OL</sub> = 2 mA                    |                        | 0.4                   | V    |      |
| I <sub>IN</sub>                  | Input leakage current                                                | CLKINx_P                                           | −40                    | 40                    | μA   |      |
|                                  |                                                                      | CLKINx_N                                           | −40                    | 40                    | μA   |      |
|                                  |                                                                      | single-ended inputs with internal pulldown         | −30                    | 30                    | μA   |      |
|                                  |                                                                      | single-ended inputs without internal pulldown      | −5                     | 5                     | μA   |      |
|                                  |                                                                      | 3-level logic input                                | −30                    | 30                    | μA   |      |
| R <sub>PU,PD</sub>               | Internal pullup/pulldown resistor for single-ended inputs            |                                                    |                        | 120                   | kΩ   |      |
| SMBUS ELECTRICAL CHARACTERISTICS |                                                                      |                                                    |                        |                       |      |      |
| V <sub>IH</sub>                  | SMB_CLK, SMB_DATA input high voltage                                 |                                                    | 0.8 × V <sub>DD</sub>  |                       | V    |      |
| V <sub>IL</sub>                  | SMB_CLK, SMB_DATA input low voltage                                  |                                                    |                        | 0.3 × V <sub>DD</sub> | V    |      |
| V <sub>HYS</sub>                 | Hysteresis of Schmitt Trigger Inputs                                 |                                                    | 0.05 × V <sub>DD</sub> |                       | V    |      |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER         |                                   | TEST CONDITIONS        | MIN | TYP | MAX | UNIT |
|-------------------|-----------------------------------|------------------------|-----|-----|-----|------|
| V <sub>OL</sub>   | SMB_DATA output low voltage       | I <sub>OL</sub> = 4 mA |     |     | 0.4 | V    |
| I <sub>LEAK</sub> | SMB_CLK, SMB_DATA input leakage   |                        | –10 |     | 10  | μA   |
| C <sub>PIN</sub>  | SMB_CLK, SMB_DATA pin capacitance |                        |     |     | 10  | pF   |

- (1) PCIe AC test load
- (2) DB2000QL DC test load
- (3) First clock edge is used for timing measurements. Clock outputs are muted until stabilized.
- (4) For input pins, assertion or deassertion starts when the input voltage reaches the minimum voltage required for a "high" level, or the maximum voltage required for a "low" level
- (5) All power supply pins are tied together. A 0.1μF capacitor is placed close to each power supply pin. 50 mVpp ripple is applied before the decoupling capacitors. Measure the spur level at the clock output
- (6) DB2000QL AC test load
- (7) Slew rate is highly dependent on PCB trace characteristics

## 6.6 SMBus Timing Requirements

|                       |                                                                 | 100-kHz CLASS |      | 400-kHz CLASS |     | UNIT |
|-----------------------|-----------------------------------------------------------------|---------------|------|---------------|-----|------|
|                       |                                                                 | MIN           | MAX  | MIN           | MAX |      |
| f <sub>SMB</sub>      | SMBus Operating Frequency                                       | 10            | 100  | 10            | 400 | kHz  |
| f <sub>BUF</sub>      | Bus free time between STOP and START condition                  | 4.7           | –    | 1.3           | –   | μs   |
| t <sub>HD_STA</sub>   | Hold time after (REPEATED) START condition                      | 4.0           | –    | 0.6           | –   | μs   |
| t <sub>SU_STA</sub>   | REPEATED START condition setup time                             | 4.7           | –    | 0.6           | –   | μs   |
| t <sub>SU_STO</sub>   | STOP condition setup time                                       | 4.0           | –    | 0.6           | –   | μs   |
| t <sub>HD_DAT</sub>   | Data hold time                                                  | 0             | –    | 0             | –   | ns   |
| t <sub>SU_DAT</sub>   | Data setup time                                                 | 250           | –    | 100           | –   | ns   |
| t <sub>TIMEOUT</sub>  | Detect clock low timeout                                        | 25            | 35   | 25            | 35  | ms   |
| t <sub>LOW</sub>      | Clock low period                                                | 4.7           | –    | 1.3           | –   | μs   |
| t <sub>HIGH</sub>     | Clock high period                                               | 4.0           | 50   | 0.6           | 50  | μs   |
| t <sub>LOW_SEXT</sub> | Cumulative clock low extend time (secondary device)             | –             | 25   | –             | 25  | ms   |
| t <sub>LOW_PEXT</sub> | Cumulative clock low extend time (primary device)               | –             | 10   | –             | 10  | ms   |
| t <sub>F</sub>        | Clock/Data Fall Time                                            | –             | 300  | –             | 300 | ns   |
| t <sub>R</sub>        | Clock/Data Rise Time                                            | –             | 1000 | –             | 300 | ns   |
| t <sub>SPIKE</sub>    | Noise spike suppression time                                    | –             | –    | 0             | 50  | ns   |
| t <sub>POR</sub>      | Time in which a device must be operational after power-on reset |               | 500  |               | 500 | ms   |

## 6.7 SBI Timing Requirements

|                     |                                                                    | MIN | MAX | UNIT   |
|---------------------|--------------------------------------------------------------------|-----|-----|--------|
| t <sub>PERIOD</sub> | Clock period                                                       | 40  | –   | ns     |
| t <sub>SETUP</sub>  | SHFT setup to SBI_CLK rising edge                                  | 10  | –   | ns     |
| t <sub>DSU</sub>    | SBI_IN data setup to SBI_CLK rising edge                           | 5   | –   | ns     |
| t <sub>DHOLD</sub>  | SBI_IN data hold after SBI_CLK rising edge                         | 2   | –   | ns     |
| t <sub>DOUT</sub>   | SBI_CLK rising edge to SBI_OUT data valid                          | 2   | –   | ns     |
| t <sub>LD</sub>     | CLK rising edge to LD# falling edge                                | 10  | –   | ns     |
| t <sub>OE</sub>     | Delay from LD# falling edge to output enable/disable taking effect | 4   | 10  | clocks |

|                   |                              | MIN | MAX | UNIT |
|-------------------|------------------------------|-----|-----|------|
| $t_{\text{SLEW}}$ | SBI_CLK 20% to 80% slew rate | 0.7 | 4   | V/ns |

## 6.8 Timing Diagrams

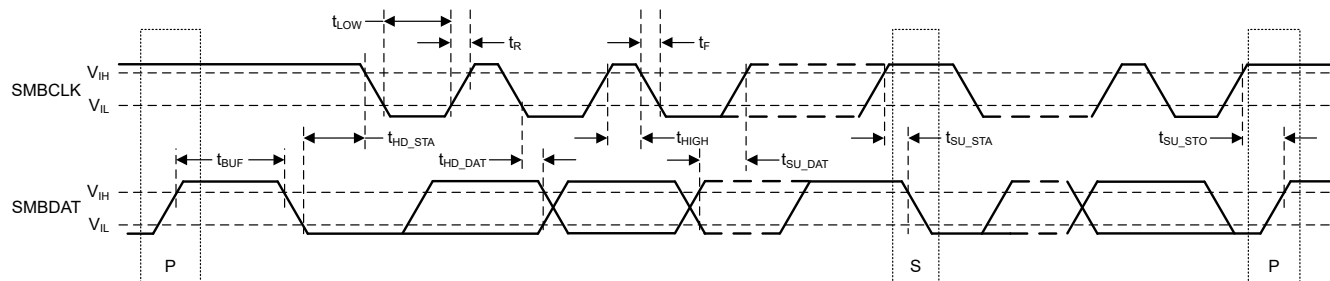


Figure 6-1. SMBus Timing Diagram

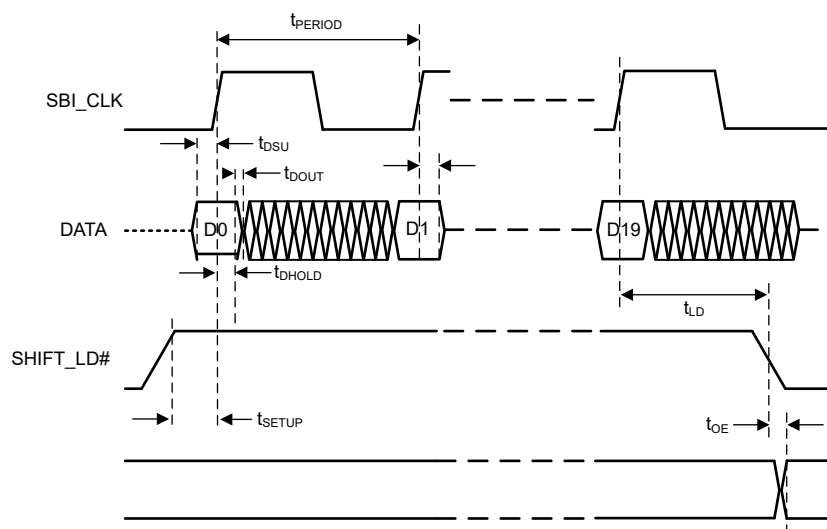


Figure 6-2. SBI Timing Diagram

## 6.9 Typical Characteristics

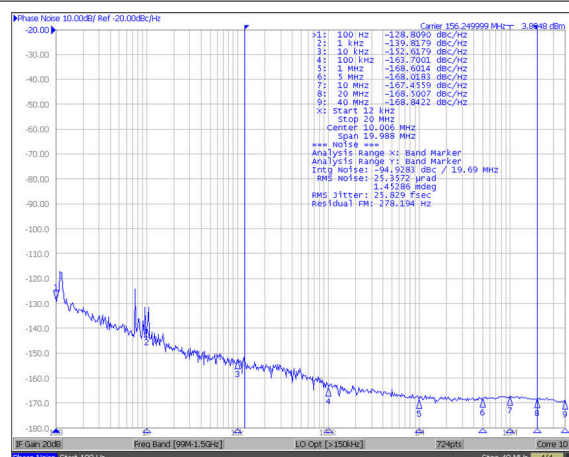
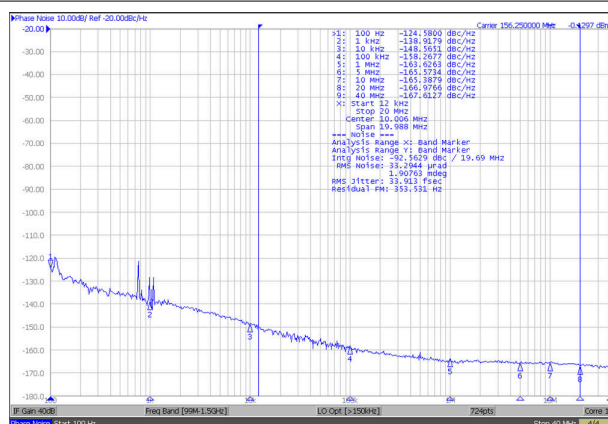


Figure 6-3. Input Source at 156.25MHz (12kHz - 20MHz)



See Note 1 and 2 in Graph Notes table

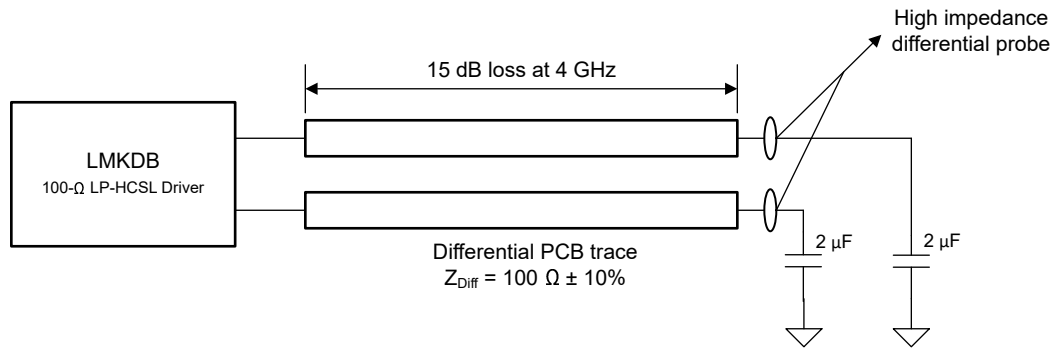
Figure 6-4. LMKDB11xx/120x Phase Noise / Output Jitter at 156.25MHz (12kHz - 20MHz)

## 6.9 Typical Characteristics (continued)

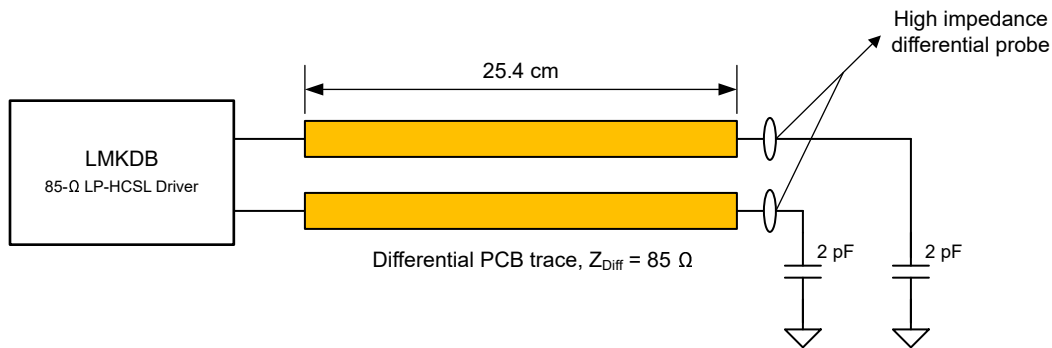
**Table 6-1. Graph Notes**

| NOTE |                                                                                                                                                                                                                                                                                     |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| (1)  | The typical RMS jitter values in the plots show the total output RMS jitter ( $J_{OUT}$ ) for each frequency and the source clock RMS jitter ( $J_{SOURCE}$ ). From these values, the Additive RMS Jitter can be calculated as: $J_{ADD} = \text{SQRT}(J_{OUT}^2 - J_{SOURCE}^2)$ . |
| (2)  | $J_{ADD}$ at 156.25MHz = $\text{SQRT}(33.9^2 - 25.8^2) = 22.0\text{fs}$                                                                                                                                                                                                             |

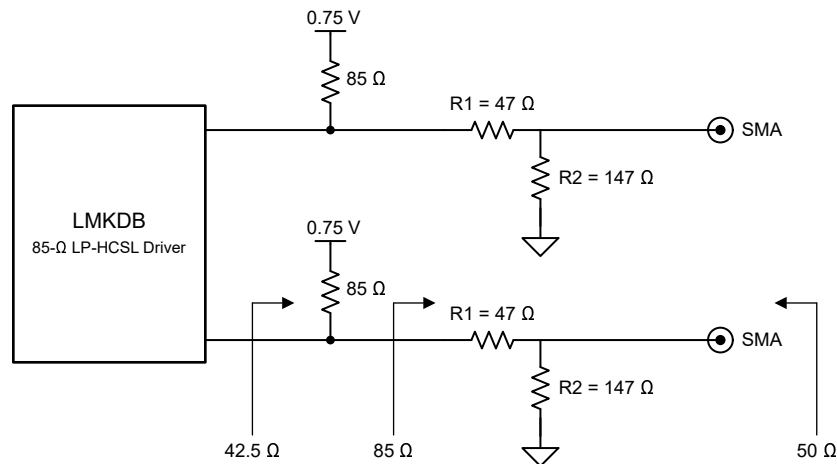
## 7 Parameter Measurement Information



**Figure 7-1. PCIe AC Test Load**



**Figure 7-2. DB2000QL AC Test Load**



**Figure 7-3. DB2000QL DC Test Load**

## 8 Detailed Description

### 8.1 Overview

LMKDB11xx are DB2000QL compliant clock buffers that distribute either 20 (LMKDB1120), or 8 (LMKDB1108) LP-HCSL clocks (respectively) designed for PCIe Gen 1 through 6 applications. LMKDB12xx are DB2000QL compliant clock muxes that can distribute 4 (LMKDB1204) and 2 (LMKDB1202) LP-HCSL clock outputs from two clock input sources.

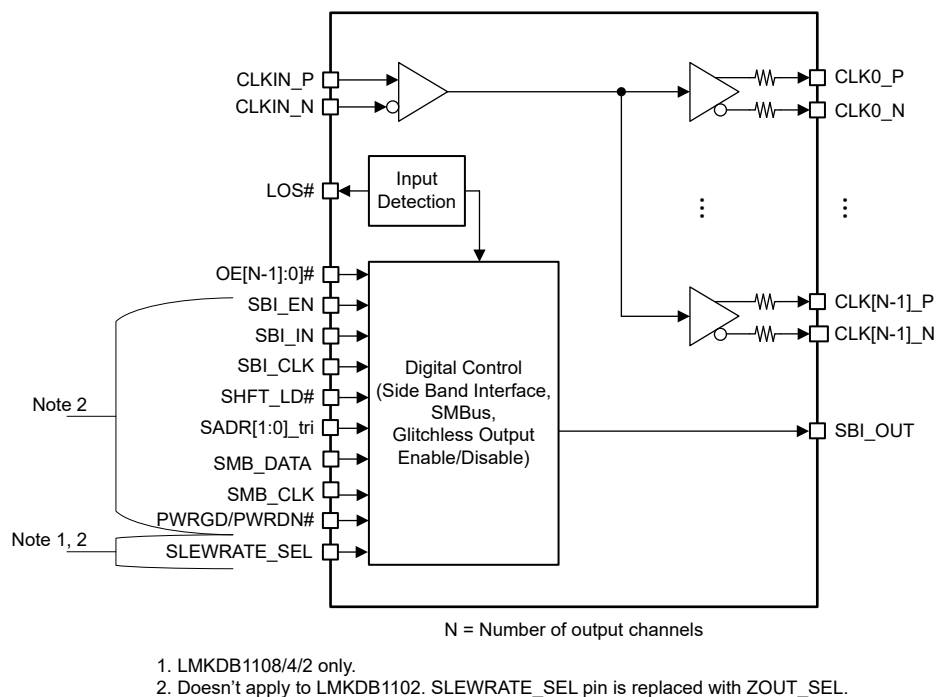
With ultra-low additive jitter and ultra-low propagation delay, both devices allow for enough jitter margin for the entire clock path mainly required for PCIe Gen 5 and Gen 6 buffer cascading and Ethernet fan-out applications. The LMKDB11xx and LMKDB12xx also support both 1.8 V and 3.3 V supply voltages for better design flexibility.

LMKDB11xx and LMKDB12xx have individual OE controls for all outputs, which provides more design flexibility. Each output of each device also has programmable slew rate, programmable output amplitude swing, and automatic output disable. The devices support 100-Ω or 85-Ω LP-HCSL, denoted by the part number as shown in [Section 4](#), with output frequencies of up to 400 MHz. LMKDB12xx devices have ZOUT\_SEL pin to select 100-Ω or 85-Ω LP-HCSL output impedance.

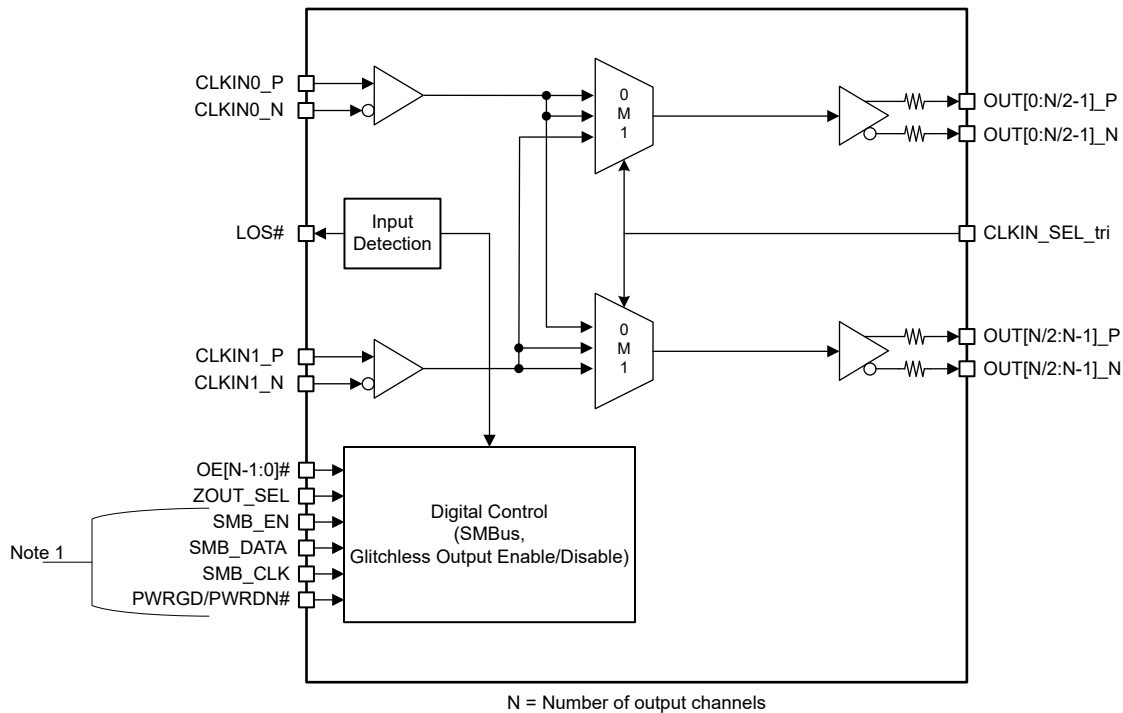
LMKDB11xx have pin mode, SMBus mode, and Side Band Interface (SBI) mode, which can all be used at the same time. While LMKDB12xx only offers pin mode and SMBus mode. The vSMB\_EN pin on LMKDB12xx can be used to select pin mode or SMBus mode. SBI enables or disables output clocks at a much faster speeds (up to 25 MHz) as compared to SMBus. Furthermore, because both SBI and SMBus can operate at the same time, SMBus can still be used to take over device control and readback status after power-up. For more details please refer to [Section 8.4](#)

Refer to [Section 8](#) for the detailed descriptions of the devices pins and the *Register Map* for more details on the device registers.

### 8.2 Functional Block Diagram



**Figure 8-1. LMKDB11xx Functional Block Diagram**



1. LMKDB1204 Only.

Figure 8-2. LMKDB12xx Functional Block Diagram

## 8.3 Feature Description

### 8.3.1 Input Features

#### 8.3.1.1 Running Input Clocks When Device is Powered Off

The device supports running input clocks when power is off. This is different than the fail-safe feature where the input can be pulled to static VDD when device power is off. This is useful if clock inputs are available before power is provided to the clock buffer.

#### 8.3.1.2 Fail-Safe Inputs

All clock input pins and digital input pins support fail-safe. Fail-safe means a pin can be driven to VDD when device power is off, without causing any leakage or reliability problem. For example, an OE# pin can be driven to VDD before device power is up so that the output stays muted until the OE# pin goes low, sometime after power-up.

#### 8.3.1.3 Input Configurations

LMKDB11xx and LMKDB12xx devices input buffer stage supports four different configurations:

- DC coupled HCSL inputs.
- DC coupled LVDS input signal with external 100Ω termination resistor.
- AC coupled inputs with internal self-bias. See [AC-Coupled or DC-Coupled Clock Inputs](#) for more details.
- Internal 50Ω to ground terminations. See [Internal Termination for Clock Inputs](#) for more details.

All the devices with two inputs have individual AC coupling and input termination option. To configure each input, refer to register map for configuration bits.

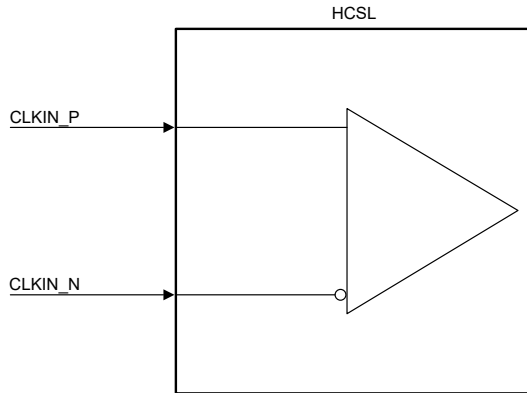


Figure 8-3. HCSL Input Interface (PCIe Standard)

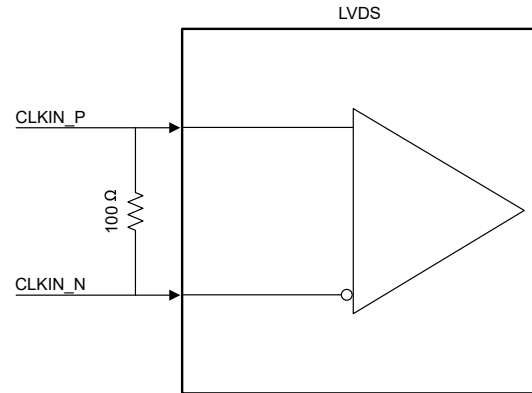


Figure 8-4. LVDS Input Interface

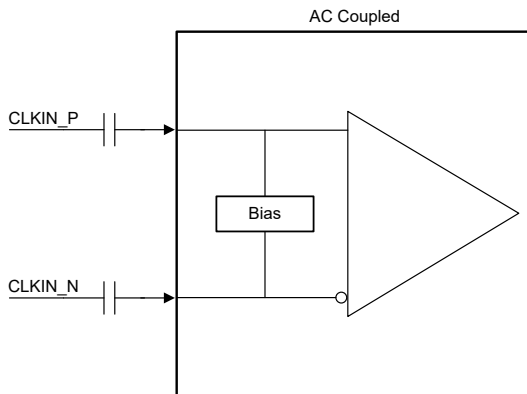


Figure 8-5. External AC-Coupled Input

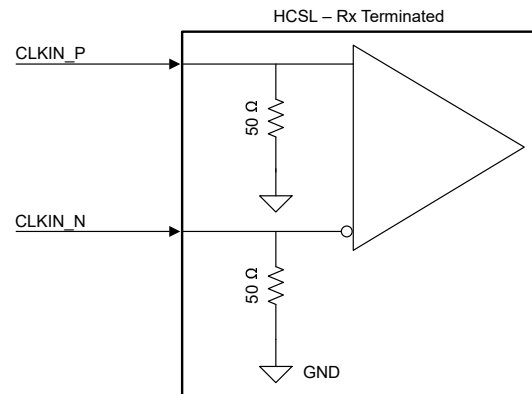


Figure 8-6. Receiver Internal Terminations

#### 8.3.1.3.1 Internal Termination for Clock Inputs

There is an option to enable 50-Ω internal termination for differential clock input. For LP-HCSL input, disable the internal termination. For HCSL input, enable internal termination if external termination is not provided. The internal termination is disabled by default.

#### 8.3.1.3.2 AC-Coupled or DC-Coupled Clock Inputs

Input clocks can be either AC coupled or DC coupled. If the inputs are DC coupled, the input signal swing levels must match those in [Specifications](#) under the *CLOCK INPUT REQUIREMENTS*. Also, register RX\_EN\_AC\_INPUT must be set to 0 for DC-coupled inputs or set to 1 for AC-coupled inputs. Refer to the *Register Map* for more information about RX\_EN\_AC\_INPUT.

### 8.3.2 Flexible Power Sequence

#### 8.3.2.1 PWRDN# Assertion and Deassertion

In the recommended power down sequence, PWRDN# is asserted while input clocks are valid. Make sure to hold the PWRDN# pin at low level for two consecutive rising edges of the input clock cycle. As a result, all clock outputs are muted to low/low (OUTx\_P = Low, OUTx\_N = Low) without a glitch. Following any other sequence brings the device to an undefined mode and can cause glitches or invalid outputs.

#### 8.3.2.2 OE# Assertion and Deassertion

OE# pins can be asserted and deasserted at anytime, whether:

- Device power supply is on or off
- PWRGD/PWRDN# pin is pulled high or low
- Clock input is valid or invalid

The OE# pins only take effect if all below conditions are met:

1. The clock input is valid
2. The PWRGD/PWRDN# pin is high
3. The device power is up

Otherwise outputs are always muted and OE# assertion and deassertion has no impact.

If OE# pins become low in any of the below conditions:

1. Input clock is invalid
2. PWRGD/PWRDN# pin is low
3. Device power is off

Then when all below conditions are met:

1. The clock input is valid
2. The PWRGD/PWRDN# pin is high
3. The device power is up

Outputs are enabled without any glitch (assuming register OE and SBI OE are active).

### 8.3.2.3 PWRGD Assertion

The first low-to-high transition of the PWRGD pin after device power is on can occur while input clock is running, floating, low/low or pulled to VDD. The power-up sequence only starts if the PWRGD pin is pulled from low to high while input clock is valid.

If the PWRGD pin is pulled from low to high while input clock is invalid, then the power-up sequence is not initiated and the outputs stay low/low. When this happens, pulling the PWRGD pin back from high to low has no impact and this low-to-high transition on PWRGD pin is not considered a valid Power Good signal. The device is powered up next time when the PWRGD pin is pulled high while input clock is valid. In other words, there is only one valid Power Good signal for every power cycle.

### 8.3.2.4 Clock Input and PWRGD/PWRDN# Behaviors When Device Power is Off

Input clocks can be running, floating, low/low or pulled to VDD when device power is off, regardless of PWRGD/PWRDN# pin states (low, high, low-to-high transition and high-to-low transition). [Table 8-1](#) shows all the supported sequences; where clock input can be applied before or after VDD is applied.

**Table 8-1. Flexible Power-up Sequences**

| VDD         | PWRGD/PWRDN# | CLKIN_P/CLKIN_N |
|-------------|--------------|-----------------|
| Not Present | X            | Running         |
|             |              | Floating        |
|             |              | Low / Low       |
| Present     | 0 or 1       | Running         |
|             |              | Floating        |
|             |              | Low / Low       |

## 8.3.3 LOS and OE

### 8.3.3.1 Additional OE# Pins for LMKDB1120 and Backward Compatibility

The DB2000QL specification only defines 8 OE# pins. In the LMKDB1120, 12 additional OE# pins are added so that each of the 20 outputs has a dedicated OE# pin. This provides additional design flexibility. The LMKDB1120 is backward pin-compatible with DB2000QL because all OE# pins have internal pulldown resistor. When left floating, these additional OE# pins have no impact (OE# pins are active low), because the three types of OE controls follow the AND logic.

### 8.3.3.2 Synchronous OE

Outputs are enabled and disabled synchronously. Synchronous OE means when an output is enabled or disabled, there is no glitch or runt pulse at the output.

### 8.3.3.3 OE Control

OE (Output Enable) can enable or disable a certain output. Three types of OE controls are supported: OE pin, OE register bit through SMBus, and OE control through SBI. The three controls follow the AND logic. An output is enabled only if all three controls enable that output. If any control disables that output, that output is disabled.

LMKDB12xx offer only SMBus and pin control OE controls.

### 8.3.3.4 Automatic Output Disable

Automatic Output Disable (AOD) is enabled by default, and can be disabled through SMBus. When input clock becomes invalid and LOS# is active, output clocks are muted to low/low (OUTx\_P = Low, OUTx\_N = Low). Before LOS# is active and after input clock becomes invalid (because LOS detection takes time), output clocks stay at a steady state following the last input state. For example, if the input clock stopped at low/high, then output clocks first stay at low/high, then muted to low/low once LOS# is active.

### 8.3.3.5 LOS Detection

LOS (Loss Of input Signal) detects whether the clock input is valid or not. When input clock is valid, LOS# register bit = 1 and LOS# pin = high. When input clock is invalid, LOS register bit = 0 and LOS# pin = low.

At power-up, the LOS# pin is kept low until input is detected valid. Therefore, the LOS# pin can be used for the timing of OE# insertion and other operations.

The LOS# signal is only effective if PWRGD/PWRDN# pin is high. If this pin is low, then LOS# is low regardless of input validity.

## 8.3.4 Output Features

### 8.3.4.1 Output Banks

LMKDB12xx muxes have two output banks that can be used as dual bank buffer mode. Each bank has a dedicated supply pin to avoid cross talk when operating at different frequencies. Refer to [Figure 10-5](#) to minimize noise on the output banks. Below

**Table 8-2. LMKDB12xx Output Banks**

| Output Bank | Outputs (P/N) |
|-------------|---------------|
| 0           | [0:N/2-1]     |
| 1           | [N/2:N-1]     |

### 8.3.4.2 Double Termination

For regular PCIe applications, LP-HCSL outputs do not require external termination, but the LMKDB family does support double termination (this is uncommon). In that case, an external 50-Ω termination is placed and the swing is halved. This results additional power consumption as well due to 50-Ω termination to ground on the output.

### 8.3.4.3 Programmable Output Slew Rate

The LMKDB family offers slew rate control options through SMBus and pin modes. The pin mode option is global slew rate control for all the outputs. SMBus slew rate control supports programmable output slew rate for each individual output. The slew rate is heavily dependent on trace characteristics including trace width, copper thickness, substrate height, dielectric constant, and loss tangent.

LMKDB slew rate control settings are tested with PCIe test load shown in [Figure 7-1](#).

#### 8.3.4.3.1 Slew Rate Control through Pin

The LMKDB1104 and LMKDB1108 offer a global slew rate control pin. The pin can be set to low for slow slew rate setting and high for high slew rate. [Table 8-3](#) provides more information on the slew rate control option through pin mode.

**Table 8-3. Pin Mode Slew Rate Control**

| Pin Status | Slew Rate Setting | Slew Rate Range (V/ns) |
|------------|-------------------|------------------------|
| Low        | Low               | 1.8 - 2.6              |
| High       | High              | 2 - 2.9                |

#### 8.3.4.3.2 Slew Rate Control through SMBus

In SMBus mode, the slew rate can be selected from 16 different values. There are four register field options, named SLEWRATE\_OPT\_#, each storing a slew rate value (chosen out of the 16 available slew rate values). A register field assignment of 0x0 is the fastest slew rate setting and a register field assignment of 0xF is the slowest slew rate setting. The SLEWRATE\_OPT\_# default values are found in [Table 8-4](#). The corresponding ranges for the four default slew rates can be found in [Section 6](#) under *CLOCK OUTPUT CHARACTERISTICS - 100MHz 85Ω PCIe* or *CLOCK OUTPUT CHARACTERISTICS - 100MHz 100Ω PCIe* for the specification *Output slew rate*.

**Table 8-4. LMKDB Default SLEWRATE\_OPT\_# Values**

| Register Field Name | Default Value | Default Slew Rate              |
|---------------------|---------------|--------------------------------|
| SLEWRATE_OPT_1      | 0x0           | Highest                        |
| SLEWRATE_OPT_2      | 0x6           | High (default for all outputs) |
| SLEWRATE_OPT_3      | 0xA           | Low                            |
| SLEWRATE_OPT_4      | 0xF           | Lowest                         |

Each of these slew rates can be assigned to each output separately using the register bits SLEWRATE\_SEL\_CLKX\_LSB and SLEWRATE\_SEL\_CLKX\_MSB. Setting these two bits assigns the slew rate for a specific output X, as shown in [Table 8-4](#). By default, all outputs are assigned to SLEWRATE\_OPT\_2.

**Table 8-5. SLEWRATE\_SEL\_CLKX\_LSB & SLEWRATE\_SEL\_CLKX\_MSB Slew Rate Selection**

| SLEWRATE_SEL_CLKX_LSB | SLEWRATE_SEL_CLKX_MSB | Slew Rate Option Selection |
|-----------------------|-----------------------|----------------------------|
| 0                     | 0                     | SLEWRATE_OPT_4             |
| 1                     | 0                     | SLEWRATE_OPT_3             |
| 0                     | 1                     | SLEWRATE_OPT_2             |
| 1                     | 1                     | SLEWRATE_OPT_1             |

To program the slew rate to the desired slew rate, the following sequence needs to be followed:

- [Optional]: if the default assignments shown in [Table 8-4](#) for each slew rate speed is not as desired, one of the slew rate options value can be changed to another slew rate.
- [LMKDB1108 and 1104 only]: Program SLEWRATE\_CTRL\_MODE register to 1 to select SMBus programming mode for slew rate control. Refer to [Section 9](#) section for LMKDB1108 and LMKDB1104 register bits information.
- Program SLEWRATE\_SEL\_CLKX\_MSB and SLEWRATE\_SEL\_CLKX\_LSB to assign clock output X to desired slew rate speed option, as shown in [Table 8-5](#). The default assignments for each option can be found in [Table 8-4](#).

#### 8.3.4.4 Programmable Output Swing

The LMKDB family supports programmable LP-HCSL swings between a range of 600 mV to 975 mV. All outputs are programmed to the same output swing via register AMP and AMP\_BANKX for both buffer and mux respectively. To program the outputs to the desired swing refer to the [Register Maps](#).

### 8.3.4.5 Accurate Output Impedance

The LMKDB family supports both 100-Ω LP-HCSL and 85-Ω LP-HCSL. The output impedance is accurately trimmed to ±5%. This helps improve impedance matching and clock signal integrity.

### 8.3.4.6 Programmable Output Impedance

The LMKDB12xx pin mode option to select 100-Ω or 85-Ω LP-HCSL output impedance provides flexibility in design. Output impedance can be selected using ZOUT\_SEL pin on the device as shown in Table 8-6. If left floating, 85-Ω output impedance is selected by default through an internal pulldown resistor.

**Table 8-6. Programmable Output Impedance**

| ZOUT_SEL | Output Impedance |
|----------|------------------|
| Low      | 85Ω              |
| High     | 100Ω             |

## 8.4 Device Functional Modes

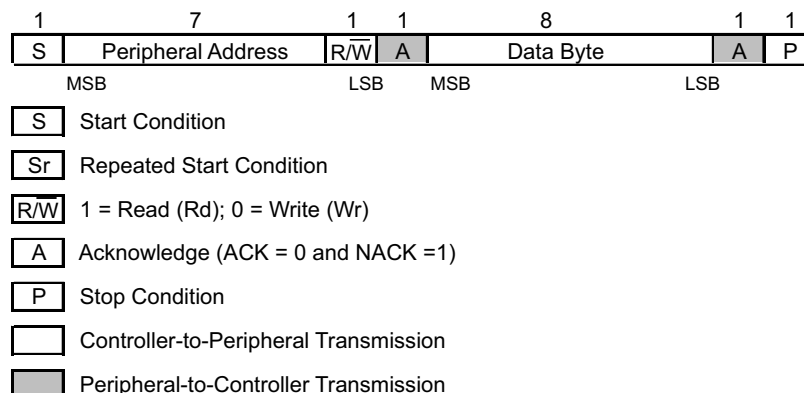
### 8.4.1 SMBus Mode

In SMBus mode, LMKDB11xx device SMBus registers can be written and read through SMBus pins. Pin SADR1 and SADR0 set the SMBus address.

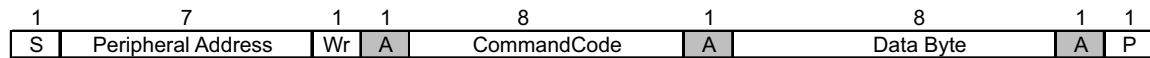
| SADR1 | SADR0 | 8-Bit SMBus Address (R/W Bit = 0) |
|-------|-------|-----------------------------------|
| Low   | Low   | 0xD8                              |
| Low   | Float | 0xDA                              |
| Low   | High  | 0xDE                              |
| Float | Low   | 0xC2                              |
| Float | Float | 0xC4                              |
| Float | High  | 0xC6                              |
| High  | Low   | 0xCA                              |
| High  | Float | 0xCC                              |
| High  | High  | 0xCE                              |

**Table 8-7. Command Code Definition**

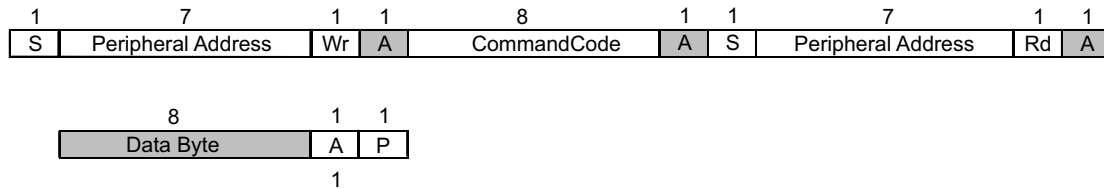
| BIT   | DESCRIPTION                                                                                                  |
|-------|--------------------------------------------------------------------------------------------------------------|
| 7     | 0 = <i>Block Read</i> or <i>Block Write</i> operation<br>1 = <i>Byte Read</i> or <i>Byte Write</i> operation |
| (6:0) | Register address for <i>Byte</i> operations, or starting register address for <i>Block</i> , operations      |



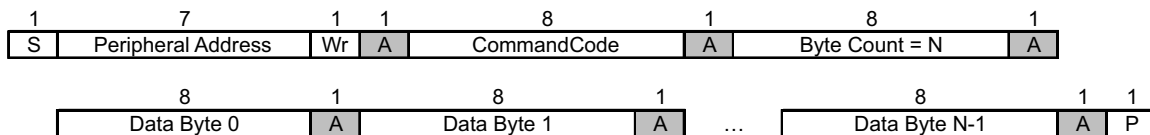
**Figure 8-7. Generic Programming Sequence**



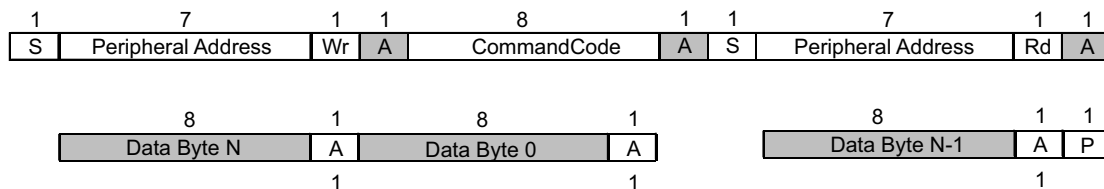
**Figure 8-8. Byte Write Protocol**



**Figure 8-9. Byte Read Protocol**



**Figure 8-10. Block Write Protocol**



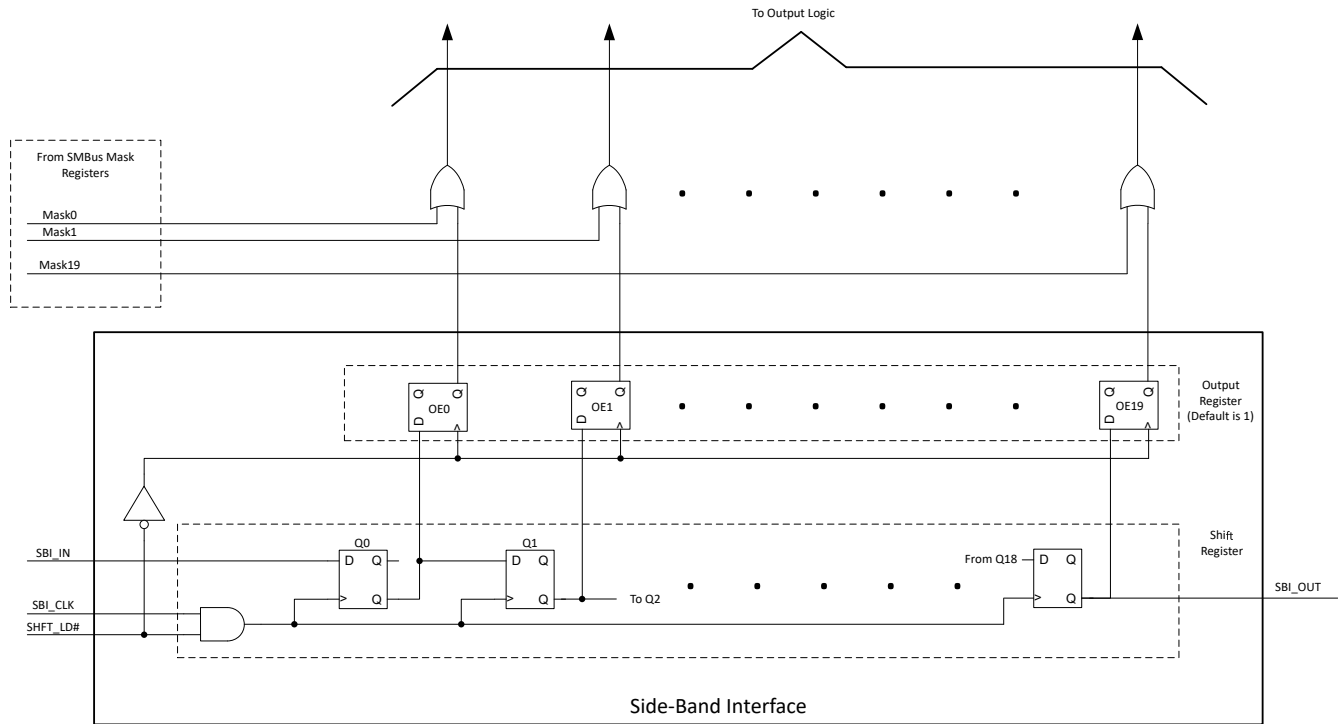
**Figure 8-11. Block Read Protocol**

### 8.4.2 SBI Mode

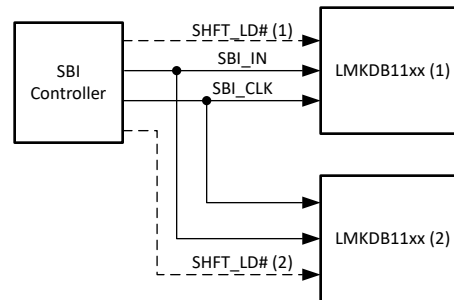
Side-Band Interface (SBI) is a simple 3-wire or 4-wire serial interface which consists of SHFT\_LD#, SBI\_IN, SBI\_CLK and SBI\_OUT (optional) pins. When the SHFT\_LD# pin is high, the rising edge of SBI\_CLK clocks SBI\_IN into a shift register. After shifting data, the falling edge of SHFT\_LD# loads the shift register contents into the output register. SBI registers can be shifted out through SBI\_OUT pin to form daisy chain topology.

Enabling SBI mode does not disable SMBus. SBI registers can be accessed while PWRGD/PWRDN# pin is low.

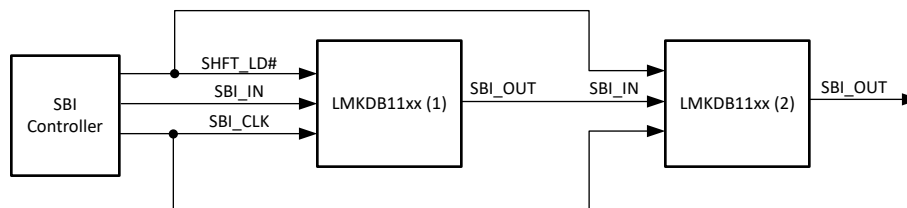
LMKDB12xx only supports pin mode and SMBus mode.



**Figure 8-12. SBI Control Logic**



**Figure 8-13. SBI Star Topology**



**Figure 8-14. SBI Daisy Chain Topology**

SBI register sequence:

- LMKDB1120: SBI\_IN – CLK0, CLK1, CLK2, CLK3, CLK4, CLK5, CLK6, CLK7, CLK8, CLK9, CLK10, CLK11, CLK12, CLK13, CLK14, CLK15, CLK16, CLK17, CLK18, CLK19 – SBI\_OUT
- LMKDB1108: SBI\_IN – CLK7, CLK6, CLK5, CLK4, CLK3, CLK2, CLK1, CLK0 – SBI\_OUT
- LMKDB1104: SBI\_IN – CLK3, CLK2, CLK1, CLK0 – SBI\_OUT

### 8.4.3 Pin Mode

If the SMBus or SBI interface is not needed, the SMBus pins or SBI pins can be left floating. The device can operate in pin mode and the outputs can be enabled or disabled by OE# pins.

## 9 Register Maps

### 9.1 LMKDB1120 Registers

Table 9-1 lists the memory-mapped registers for the LMKDB1120 registers. All register offset addresses not listed in Table 9-1 must be considered as reserved locations and the register contents must not be modified.

**Table 9-1. LMKDB1120 Registers**

| Offset | Acronym | Register Name                                                                  | Section                        |
|--------|---------|--------------------------------------------------------------------------------|--------------------------------|
| 0h     | R0      | Output Enable Control for CLK16 through CLK19                                  | <a href="#">Section 9.1.1</a>  |
| 1h     | R1      | Output Enable Control for CLK0 through CLK7                                    | <a href="#">Section 9.1.2</a>  |
| 2h     | R2      | Output Enable Control for CLK8 through CLK15                                   | <a href="#">Section 9.1.3</a>  |
| 3h     | R3      | OE Pin Readback for CLK5 through CLK12                                         | <a href="#">Section 9.1.4</a>  |
| 4h     | R4      | AOD Enable Control and SBI_EN Readback                                         | <a href="#">Section 9.1.5</a>  |
| 5h     | R5      | Device Info                                                                    | <a href="#">Section 9.1.6</a>  |
| 6h     | R6      | Device Info (cont.)                                                            | <a href="#">Section 9.1.7</a>  |
| 7h     | R7      | SMBus Byte Counter                                                             | <a href="#">Section 9.1.8</a>  |
| 8h     | R8      | SBI Mask for CLK0 through CLK7                                                 | <a href="#">Section 9.1.9</a>  |
| 9h     | R9      | SBI Mask for CLK8 and CLK15                                                    | <a href="#">Section 9.1.10</a> |
| Ah     | R10     | SBI Mask for CLK16 and CLK19                                                   | <a href="#">Section 9.1.11</a> |
| Bh     | R11     | Output Slew Rate Select MSB for CLK0 through CLK7                              | <a href="#">Section 9.1.12</a> |
| Ch     | R12     | Output Slew Rate Select MSB for CLK8 through CLK15                             | <a href="#">Section 9.1.13</a> |
| Dh     | R13     | Output Slew Rate Select MSB for CLK16 through CLK19                            | <a href="#">Section 9.1.14</a> |
| 14h    | R20     | Output Amplitude                                                               | <a href="#">Section 9.1.15</a> |
| 15h    | R21     | Input Configuration, Save Config in PD, SMB SDATA Monitoring, and LOS Readback | <a href="#">Section 9.1.16</a> |
| 21h    | R33     | SBI Mask Readback for CLK0 through CLK7                                        | <a href="#">Section 9.1.17</a> |
| 22h    | R34     | SBI Mask Readback for CLK8 through CLK15                                       | <a href="#">Section 9.1.18</a> |
| 23h    | R35     | SBI Mask Readback for CLK16 through CLK19                                      | <a href="#">Section 9.1.19</a> |
| 26h    | R38     | Non-clearable SMBUS Write Lock                                                 | <a href="#">Section 9.1.20</a> |
| 27h    | R39     | LOS Event Status and Clearable SMBus Write Lock                                | <a href="#">Section 9.1.21</a> |
| 5Bh    | R91     | Slew Rate Speed Options 1 and 2 Assignments                                    | <a href="#">Section 9.1.22</a> |
| 5Ch    | R92     | Slew Rate Speed Options 3 and 4 Assignments                                    | <a href="#">Section 9.1.23</a> |
| 62h    | R98     | Output Slew Rate Select LSB for CLK0 through CLK7                              | <a href="#">Section 9.1.24</a> |
| 63h    | R99     | Output Slew Rate Select LSB for CLK8 through CLK15                             | <a href="#">Section 9.1.25</a> |
| 64h    | R100    | Output Slew Rate Select LSB for CLK16 through CLK19                            | <a href="#">Section 9.1.26</a> |

Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

**Table 9-2. LMKDB1120 Access Type Codes**

| Access Type | Code    | Description         |
|-------------|---------|---------------------|
| Read Type   |         |                     |
| R           | R       | Read                |
| RC          | R<br>C  | Read<br>to Clear    |
| Write Type  |         |                     |
| W           | W       | Write               |
| W1C         | W<br>1C | Write<br>1 to clear |
| WSC         | W       | Write               |

**Table 9-2. LMKDB1120 Access Type Codes  
(continued)**

| Access Type            | Code | Description                            |
|------------------------|------|----------------------------------------|
| Reset or Default Value |      |                                        |
| -n                     |      | Value after reset or the default value |

### 9.1.1 R0 Register (Offset = 0h) [Reset = 78h]

R0 is shown in [Table 9-3](#).

Return to the [Table 9-1](#).

**Table 9-3. R0 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                      |
|-----|-----------|------|-------|----------------------------------------------------------------------------------|
| 7   | RESERVED  | R    | 0h    | Reserved                                                                         |
| 6   | CLK_EN_19 | R/W  | 1h    | Output Enable for CLK19<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 5   | CLK_EN_18 | R/W  | 1h    | Output Enable for CLK18<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 4   | CLK_EN_17 | R/W  | 1h    | Output Enable for CLK17<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 3   | CLK_EN_16 | R/W  | 1h    | Output Enable for CLK16<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 2:0 | RESERVED  | R    | 0h    | Reserved                                                                         |

### 9.1.2 R1 Register (Offset = 1h) [Reset = FFh]

R1 is shown in [Table 9-4](#).

Return to the [Table 9-1](#).

**Table 9-4. R1 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                     |
|-----|----------|------|-------|---------------------------------------------------------------------------------|
| 7   | CLK_EN_7 | R/W  | 1h    | Output Enable for CLK7<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 6   | CLK_EN_6 | R/W  | 1h    | Output Enable for CLK6<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 5   | CLK_EN_5 | R/W  | 1h    | Output Enable for CLK5<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 4   | CLK_EN_4 | R/W  | 1h    | Output Enable for CLK4<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 3   | CLK_EN_3 | R/W  | 1h    | Output Enable for CLK3<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 2   | CLK_EN_2 | R/W  | 1h    | Output Enable for CLK2<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |

**Table 9-4. R1 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                     |
|-----|----------|------|-------|---------------------------------------------------------------------------------|
| 1   | CLK_EN_1 | R/W  | 1h    | Output Enable for CLK1<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 0   | CLK_EN_0 | R/W  | 1h    | Output Enable for CLK0<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |

**9.1.3 R2 Register (Offset = 2h) [Reset = FFh]**

R2 is shown in [Table 9-5](#).

Return to the [Table 9-1](#).

**Table 9-5. R2 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                      |
|-----|-----------|------|-------|----------------------------------------------------------------------------------|
| 7   | CLK_EN_15 | R/W  | 1h    | Output Enable for CLK15<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 6   | CLK_EN_14 | R/W  | 1h    | Output Enable for CLK14<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 5   | CLK_EN_13 | R/W  | 1h    | Output Enable for CLK13<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 4   | CLK_EN_12 | R/W  | 1h    | Output Enable for CLK12<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 3   | CLK_EN_11 | R/W  | 1h    | Output Enable for CLK11<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 2   | CLK_EN_10 | R/W  | 1h    | Output Enable for CLK10<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 1   | CLK_EN_9  | R/W  | 1h    | Output Enable for CLK9<br>0h = Output Disabled (low/low)<br>1h = Output Enabled  |
| 0   | CLK_EN_8  | R/W  | 1h    | Output Enable for CLK8<br>0h = Output Disabled (low/low)<br>1h = Output Enabled  |

**9.1.4 R3 Register (Offset = 3h) [Reset = 00h]**

R3 is shown in [Table 9-6](#).

Return to the [Table 9-1](#).

**Table 9-6. R3 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description     |
|-----|-----------|------|-------|-----------------|
| 7   | RB_OEb_12 | R    | 0h    | Status of OEB12 |
| 6   | RB_OEb_11 | R    | 0h    | Status of OEB11 |
| 5   | RB_OEb_10 | R    | 0h    | Status of OEB10 |
| 4   | RB_OEb_9  | R    | 0h    | Status of OEB9  |
| 3   | RB_OEb_8  | R    | 0h    | Status of OEB8  |
| 2   | RB_OEb_7  | R    | 0h    | Status of OEB7  |

**Table 9-6. R3 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description    |
|-----|----------|------|-------|----------------|
| 1   | RB_OEb_6 | R    | 0h    | Status of OEb6 |
| 0   | RB_OEb_5 | R    | 0h    | Status of OEb5 |

### 9.1.5 R4 Register (Offset = 4h) [Reset = 10h]

R4 is shown in [Table 9-7](#).

Return to the [Table 9-1](#).

**Table 9-7. R4 Register Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                                                                                                                               |
|-----|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | RESERVED         | R    | 0h    | Reserved                                                                                                                                                                  |
| 4   | BANK1_AOD_ENABLE | R/W  | 1h    | Enable automatic output disable to low/low when LOS event is detected. Refer to section "Automatic Output Disable" for more information.<br>0h = Disabled<br>1h = Enabled |
| 3:1 | RESERVED         | R    | 0h    | Reserved                                                                                                                                                                  |
| 0   | RB_SBI_ENQ       | R    | 0h    | Status of SBI_ENQ                                                                                                                                                         |

### 9.1.6 R5 Register (Offset = 5h) [Reset = 0Ah]

R5 is shown in [Table 9-8](#).

Return to the [Table 9-1](#).

**Table 9-8. R5 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description      |
|-----|-----------|------|-------|------------------|
| 7:4 | REV_ID    | R    | 0h    | Silicon revision |
| 3:0 | VENDOR_ID | R    | Ah    | Vendor ID        |

### 9.1.7 R6 Register (Offset = 6h) [Reset = C9h]

R6 is shown in [Table 9-9](#).

Return to the [Table 9-1](#).

**Table 9-9. R6 Register Field Descriptions**

| Bit | Field  | Type | Reset | Description |
|-----|--------|------|-------|-------------|
| 7:0 | DEV_ID | R    | C9h   | Device ID   |

### 9.1.8 R7 Register (Offset = 7h) [Reset = 07h]

R7 is shown in [Table 9-10](#).

Return to the [Table 9-1](#).

**Table 9-10. R7 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                 |
|-----|----------|------|-------|-----------------------------|
| 7:5 | RESERVED | R    | 0h    | Reserved                    |
| 4:0 | SMBUS_BC | R/W  | 7h    | SMBus Block Read Byte Count |

### 9.1.9 R8 Register (Offset = 8h) [Reset = 00h]

R8 is shown in [Table 9-11](#).

Return to the [Table 9-1](#).

**Table 9-11. R8 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                         |
|-----|------------|------|-------|-------------------------------------|
| 7   | SBI_MASK_7 | R/W  | 0h    | Mask off Side-Band Disable for CLK7 |
| 6   | SBI_MASK_6 | R/W  | 0h    | Mask off Side-Band Disable for CLK6 |
| 5   | SBI_MASK_5 | R/W  | 0h    | Mask off Side-Band Disable for CLK5 |
| 4   | SBI_MASK_4 | R/W  | 0h    | Mask off Side-Band Disable for CLK4 |
| 3   | SBI_MASK_3 | R/W  | 0h    | Mask off Side-Band Disable for CLK3 |
| 2   | SBI_MASK_2 | R/W  | 0h    | Mask off Side-Band Disable for CLK2 |
| 1   | SBI_MASK_1 | R/W  | 0h    | Mask off Side-Band Disable for CLK1 |
| 0   | SBI_MASK_0 | R/W  | 0h    | Mask off Side-Band Disable for CLK0 |

### 9.1.10 R9 Register (Offset = 9h) [Reset = 00h]

R9 is shown in [Table 9-12](#).

Return to the [Table 9-1](#).

**Table 9-12. R9 Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                          |
|-----|-------------|------|-------|--------------------------------------|
| 7   | SBI_MASK_15 | R/W  | 0h    | Mask off Side-Band Disable for CLK15 |
| 6   | SBI_MASK_14 | R/W  | 0h    | Mask off Side-Band Disable for CLK14 |
| 5   | SBI_MASK_13 | R/W  | 0h    | Mask off Side-Band Disable for CLK13 |
| 4   | SBI_MASK_12 | R/W  | 0h    | Mask off Side-Band Disable for CLK12 |
| 3   | SBI_MASK_11 | R/W  | 0h    | Mask off Side-Band Disable for CLK11 |
| 2   | SBI_MASK_10 | R/W  | 0h    | Mask off Side-Band Disable for CLK10 |
| 1   | SBI_MASK_9  | R/W  | 0h    | Mask off Side-Band Disable for CLK9  |
| 0   | SBI_MASK_8  | R/W  | 0h    | Mask off Side-Band Disable for CLK8  |

### 9.1.11 R10 Register (Offset = Ah) [Reset = 00h]

R10 is shown in [Table 9-13](#).

Return to the [Table 9-1](#).

**Table 9-13. R10 Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                          |
|-----|-------------|------|-------|--------------------------------------|
| 7:4 | RESERVED    | R    | 0h    | Reserved                             |
| 3   | SBI_MASK_19 | R/W  | 0h    | Mask off Side-Band Disable for CLK19 |
| 2   | SBI_MASK_18 | R/W  | 0h    | Mask off Side-Band Disable for CLK18 |
| 1   | SBI_MASK_17 | R/W  | 0h    | Mask off Side-Band Disable for CLK17 |
| 0   | SBI_MASK_16 | R/W  | 0h    | Mask off Side-Band Disable for CLK16 |

### 9.1.12 R11 Register (Offset = Bh) [Reset = FFh]

R11 is shown in [Table 9-14](#).

Return to the [Table 9-1](#).

**Table 9-14. R11 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description               |
|-----|-----------------------|------|-------|---------------------------|
| 7   | SLEWRATE_SEL_CLK7_MSB | R/W  | 1h    | MSB CLK7 slew rate select |
| 6   | SLEWRATE_SEL_CLK6_MSB | R/W  | 1h    | MSB CLK6 slew rate select |
| 5   | SLEWRATE_SEL_CLK5_MSB | R/W  | 1h    | MSB CLK5 slew rate select |
| 4   | SLEWRATE_SEL_CLK4_MSB | R/W  | 1h    | MSB CLK4 slew rate select |
| 3   | SLEWRATE_SEL_CLK3_MSB | R/W  | 1h    | MSB CLK3 slew rate select |
| 2   | SLEWRATE_SEL_CLK2_MSB | R/W  | 1h    | MSB CLK2 slew rate select |
| 1   | SLEWRATE_SEL_CLK1_MSB | R/W  | 1h    | MSB CLK1 slew rate select |
| 0   | SLEWRATE_SEL_CLK0_MSB | R/W  | 1h    | MSB CLK0 slew rate select |

### 9.1.13 R12 Register (Offset = Ch) [Reset = FFh]

R12 is shown in [Table 9-15](#).

Return to the [Table 9-1](#).

**Table 9-15. R12 Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description                |
|-----|------------------------|------|-------|----------------------------|
| 7   | SLEWRATE_SEL_CLK15_MSB | R/W  | 1h    | MSB CLK15 slew rate select |
| 6   | SLEWRATE_SEL_CLK14_MSB | R/W  | 1h    | MSB CLK14 slew rate select |
| 5   | SLEWRATE_SEL_CLK13_MSB | R/W  | 1h    | MSB CLK13 slew rate select |
| 4   | SLEWRATE_SEL_CLK12_MSB | R/W  | 1h    | MSB CLK12 slew rate select |
| 3   | SLEWRATE_SEL_CLK11_MSB | R/W  | 1h    | MSB CLK11 slew rate select |
| 2   | SLEWRATE_SEL_CLK10_MSB | R/W  | 1h    | MSB CLK10 slew rate select |
| 1   | SLEWRATE_SEL_CLK9_MSB  | R/W  | 1h    | MSB CLK9 slew rate select  |
| 0   | SLEWRATE_SEL_CLK8_MSB  | R/W  | 1h    | MSB CLK8 slew rate select  |

### 9.1.14 R13 Register (Offset = Dh) [Reset = 0Fh]

R13 is shown in [Table 9-16](#).

Return to the [Table 9-1](#).

**Table 9-16. R13 Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description                |
|-----|------------------------|------|-------|----------------------------|
| 7:4 | RESERVED               | R    | 0h    | Reserved                   |
| 3   | SLEWRATE_SEL_CLK19_MSB | R/W  | 1h    | MSB CLK19 slew rate select |

**Table 9-16. R13 Register Field Descriptions (continued)**

| Bit | Field                  | Type | Reset | Description                |
|-----|------------------------|------|-------|----------------------------|
| 2   | SLEWRATE_SEL_CLK18_MSB | R/W  | 1h    | MSB CLK18 slew rate select |
| 1   | SLEWRATE_SEL_CLK17_MSB | R/W  | 1h    | MSB CLK17 slew rate select |
| 0   | SLEWRATE_SEL_CLK16_MSB | R/W  | 1h    | MSB CLK16 slew rate select |

### 9.1.15 R20 Register (Offset = 14h) [Reset = 66h]

R20 is shown in [Table 9-17](#).

Return to the [Table 9-1](#).

**Table 9-17. R20 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                |
|-----|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | AMP      | R/W  | 6h    | Global Differential output Control = 0.6V to approximately 1V<br>25mV/step Default = 0.75V<br>0h = 600mV<br>1h = 625mV<br>2h = 650mV<br>3h = 675mV<br>4h = 700mV<br>5h = 725mV<br>6h = 750mV<br>7h = 775mV<br>8h = 800mV<br>9h = 825mV<br>Ah = 850mV<br>Bh = 875mV<br>Ch = 900mV<br>Dh = 925mV<br>Eh = 950mV<br>Fh = 975mV |
| 3:0 | RESERVED | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                   |

### 9.1.16 R21 Register (Offset = 15h) [Reset = 0Ch]

R21 is shown in [Table 9-18](#).

Return to the [Table 9-1](#).

**Table 9-18. R21 Register Field Descriptions**

| Bit | Field            | Type | Reset | Description                                                                                                     |
|-----|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 7   | RX1_EN_AC_INPUT  | R/W  | 0h    | Enable receiver bias when CLKIN is AC coupled<br>0h = DC Coupled Input<br>1h = AC Coupled Input                 |
| 6   | RX1_EN_RTERM_LSB | R/W  | 0h    | Enable termination resistors on CLKIN1<br>0h = Input Termination R Disabled<br>1h = Input Termination R Enabled |
| 5   | RESERVED         | R    | 0h    | Reserved                                                                                                        |
| 4   | RESERVED         | R    | 0h    | Reserved                                                                                                        |
| 3   | PD_RESTOREB      | R/W  | 1h    | Save Configuration in Power Down 1'b0 : config cleared 1'b1: config saved                                       |
| 2   | SDATA_TIMEOUT_EN | R/W  | 1h    | Enable SMB SDATA time out monitoring<br>0h = Disable SDATA Time Out<br>1h = Enable SDATA Time Out               |
| 1   | RESERVED         | R    | 0h    | Reserved                                                                                                        |

**Table 9-18. R21 Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                               |
|-----|---------|------|-------|-----------------------------------------------------------------------------------------------------------|
| 0   | LOSb_RB | R    | 0h    | Real time read back of loss detect block output<br>0h = LOS Event Detected<br>1h = LOS Event Not-Detected |

### 9.1.17 R33 Register (Offset = 21h) [Reset = FFh]

R33 is shown in [Table 9-19](#).

Return to the [Table 9-1](#).

**Table 9-19. R33 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                            |
|-----|-----------|------|-------|----------------------------------------|
| 7   | SBI_CLK_7 | R    | 1h    | Readback of Side-Band Disable for CLK7 |
| 6   | SBI_CLK_6 | R    | 1h    | Readback of Side-Band Disable for CLK6 |
| 5   | SBI_CLK_5 | R    | 1h    | Readback of Side-Band Disable for CLK5 |
| 4   | SBI_CLK_4 | R    | 1h    | Readback of Side-Band Disable for CLK4 |
| 3   | SBI_CLK_3 | R    | 1h    | Readback of Side-Band Disable for CLK3 |
| 2   | SBI_CLK_2 | R    | 1h    | Readback of Side-Band Disable for CLK2 |
| 1   | SBI_CLK_1 | R    | 1h    | Readback of Side-Band Disable for CLK1 |
| 0   | SBI_CLK_0 | R    | 1h    | Readback of Side-Band Disable for CLK0 |

### 9.1.18 R34 Register (Offset = 22h) [Reset = FFh]

R34 is shown in [Table 9-20](#).

Return to the [Table 9-1](#).

**Table 9-20. R34 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                             |
|-----|------------|------|-------|-----------------------------------------|
| 7   | SBI_CLK_15 | R    | 1h    | Readback of Side-Band Disable for CLK15 |
| 6   | SBI_CLK_14 | R    | 1h    | Readback of Side-Band Disable for CLK14 |
| 5   | SBI_CLK_13 | R    | 1h    | Readback of Side-Band Disable for CLK13 |
| 4   | SBI_CLK_12 | R    | 1h    | Readback of Side-Band Disable for CLK12 |
| 3   | SBI_CLK_11 | R    | 1h    | Readback of Side-Band Disable for CLK11 |
| 2   | SBI_CLK_10 | R    | 1h    | Readback of Side-Band Disable for CLK10 |
| 1   | SBI_CLK_9  | R    | 1h    | Readback of Side-Band Disable for CLK9  |
| 0   | SBI_CLK_8  | R    | 1h    | Readback of Side-Band Disable for CLK8  |

### 9.1.19 R35 Register (Offset = 23h) [Reset = 0Fh]

R35 is shown in [Table 9-21](#).

Return to the [Table 9-1](#).

**Table 9-21. R35 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                             |
|-----|------------|------|-------|-----------------------------------------|
| 7:4 | RESERVED   | R    | 0h    | Reserved                                |
| 3   | SBI_CLK_19 | R    | 1h    | Readback of Side-Band Disable for CLK19 |
| 2   | SBI_CLK_18 | R    | 1h    | Readback of Side-Band Disable for CLK18 |
| 1   | SBI_CLK_17 | R    | 1h    | Readback of Side-Band Disable for CLK17 |

**Table 9-21. R35 Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                             |
|-----|------------|------|-------|-----------------------------------------|
| 0   | SBI_CLK_16 | R    | 1h    | Readback of Side-Band Disable for CLK16 |

#### 9.1.20 R38 Register (Offset = 26h) [Reset = 00h]

R38 is shown in [Table 9-22](#).

Return to the [Table 9-1](#).

**Table 9-22. R38 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                       |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | RESERVED   | R    | 0h    | Reserved                                                                                                                                                                                                                          |
| 0   | WRITE_LOCK | W1C  | 0h    | Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by recycling power.<br>0h = SMBus Not locked for Writing<br>1h = SMBus Locked for Writing |

#### 9.1.21 R39 Register (Offset = 27h) [Reset = 00h]

R39 is shown in [Table 9-23](#).

Return to the [Table 9-1](#).

**Table 9-23. R39 Register Field Descriptions**

| Bit | Field           | Type  | Reset | Description                                                                                                                                                                                                                     |
|-----|-----------------|-------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | RESERVED        | R     | 0h    | Reserved                                                                                                                                                                                                                        |
| 1   | LOS_EVT         | R/WSC | 0h    | LOS Event Status When high, indicates that a LOS event is detected. Can be cleared by writing a 1 to the bit.<br>0h = LOS Event Not-Detected<br>1h = LOS Event Detected                                                         |
| 0   | WRITE_LOCK_RW1C | R/W   | 0h    | Clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can be cleared by writing a 1 to the bit.<br>0h = SMBus Not Locked for Writing<br>1h = SMBus locked for writing |

#### 9.1.22 R91 Register (Offset = 5Bh) [Reset = 00h]

R91 is shown in [Table 9-24](#).

Return to the [Table 9-1](#).

**Table 9-24. R91 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | SLEWRATE_OPT_2 | R/W  | 0h    | <p>There are four register assignments each storing a slew rate value (chosen out of 16 available slew rate values). This register bits relate to the 2nd option. Go to Programmable Output Slew Rate section for more information.</p> <p>0h = 0<br/>1h = 1<br/>2h = 2<br/>3h = 3<br/>4h = 4<br/>5h = 5<br/>6h = 6<br/>7h = 7<br/>8h = 8<br/>9h = 9<br/>Ah = 10<br/>Bh = 11<br/>Ch = 12<br/>Dh = 13<br/>Eh = 14<br/>Fh = 15</p> |
| 3:0 | SLEWRATE_OPT_1 | R/W  | 0h    | <p>There are four register assignments each storing a slew rate value (chosen out of 16 available slew rate values). This register bits relate to the 1st option. Go to Programmable Output Slew Rate section for more information.</p> <p>0h = 0<br/>1h = 1<br/>2h = 2<br/>3h = 3<br/>4h = 4<br/>5h = 5<br/>6h = 6<br/>7h = 7<br/>8h = 8<br/>9h = 9<br/>Ah = 10<br/>Bh = 11<br/>Ch = 12<br/>Dh = 13<br/>Eh = 14<br/>Fh = 15</p> |

### 9.1.23 R92 Register (Offset = 5Ch) [Reset = 00h]

R92 is shown in [Table 9-25](#).

Return to the [Table 9-1](#).

**Table 9-25. R92 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | SLEWRATE_OPT_4 | R/W  | 0h    | There are four register assignments each storing a slew rate value (chosen out of 16 available slew rate values). This register bits relate to the 4th option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 |
| 3:0 | SLEWRATE_OPT_3 | R/W  | 0h    | There are four register assignments each storing a slew rate value (chosen out of 16 available slew rate values). This register bits relate to the 3rd option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 |

#### 9.1.24 R98 Register (Offset = 62h) [Reset = 00h]

R98 is shown in [Table 9-26](#).

Return to the [Table 9-1](#).

**Table 9-26. R98 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description               |
|-----|-----------------------|------|-------|---------------------------|
| 7   | SLEWRATE_SEL_CLK7_LSB | R/W  | 0h    | LSB CLK7 slew rate select |
| 6   | SLEWRATE_SEL_CLK6_LSB | R/W  | 0h    | LSB CLK6 slew rate select |
| 5   | SLEWRATE_SEL_CLK5_LSB | R/W  | 0h    | LSB CLK5 slew rate select |
| 4   | SLEWRATE_SEL_CLK4_LSB | R/W  | 0h    | LSB CLK4 slew rate select |
| 3   | SLEWRATE_SEL_CLK3_LSB | R/W  | 0h    | LSB CLK3 slew rate select |

**Table 9-26. R98 Register Field Descriptions (continued)**

| Bit | Field                 | Type | Reset | Description               |
|-----|-----------------------|------|-------|---------------------------|
| 2   | SLEWRATE_SEL_CLK2_LSB | R/W  | 0h    | LSB CLK2 slew rate select |
| 1   | SLEWRATE_SEL_CLK1_LSB | R/W  | 0h    | LSB CLK1 slew rate select |
| 0   | SLEWRATE_SEL_CLK0_LSB | R/W  | 0h    | LSB CLK0 slew rate select |

### 9.1.25 R99 Register (Offset = 63h) [Reset = 00h]

R99 is shown in [Table 9-27](#).

Return to the [Table 9-1](#).

**Table 9-27. R99 Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description                |
|-----|------------------------|------|-------|----------------------------|
| 7   | SLEWRATE_SEL_CLK15_LSB | R/W  | 0h    | LSB CLK15 slew rate select |
| 6   | SLEWRATE_SEL_CLK14_LSB | R/W  | 0h    | LSB CLK14 slew rate select |
| 5   | SLEWRATE_SEL_CLK13_LSB | R/W  | 0h    | LSB CLK13 slew rate select |
| 4   | SLEWRATE_SEL_CLK12_LSB | R/W  | 0h    | LSB CLK12 slew rate select |
| 3   | SLEWRATE_SEL_CLK11_LSB | R/W  | 0h    | LSB CLK11 slew rate select |
| 2   | SLEWRATE_SEL_CLK10_LSB | R/W  | 0h    | LSB CLK10 slew rate select |
| 1   | SLEWRATE_SEL_CLK9_LSB  | R/W  | 0h    | LSB CLK9 slew rate select  |
| 0   | SLEWRATE_SEL_CLK8_LSB  | R/W  | 0h    | LSB CLK8 slew rate select  |

### 9.1.26 R100 Register (Offset = 64h) [Reset = 00h]

R100 is shown in [Table 9-28](#).

Return to the [Table 9-1](#).

**Table 9-28. R100 Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description                |
|-----|------------------------|------|-------|----------------------------|
| 7:4 | RESERVED               | R    | 0h    | Reserved                   |
| 3   | SLEWRATE_SEL_CLK19_LSB | R/W  | 0h    | LSB CLK19 slew rate select |
| 2   | SLEWRATE_SEL_CLK18_LSB | R/W  | 0h    | LSB CLK18 slew rate select |
| 1   | SLEWRATE_SEL_CLK17_LSB | R/W  | 0h    | LSB CLK17 slew rate select |
| 0   | SLEWRATE_SEL_CLK16_LSB | R/W  | 0h    | LSB CLK16 slew rate select |

## 9.2 LMKDB1108 Registers

Table 9-29 lists the memory-mapped registers for the LMKDB1108 registers. All register offset addresses not listed in Table 9-29 must be considered as reserved locations and the register contents must not be modified.

**Table 9-29. LMKDB1108 Registers**

| Offset | Acronym | Register Name                                                                  | Section                        |
|--------|---------|--------------------------------------------------------------------------------|--------------------------------|
| 0h     | R0      | Output Enable Control for CLK2 through CLK7                                    | <a href="#">Section 9.2.1</a>  |
| 1h     | R1      | Output Enable Control for CLK0 and CLK1                                        | <a href="#">Section 9.2.2</a>  |
| 2h     | R2      | OE Pin Readback for CLK2 through CLK7                                          | <a href="#">Section 9.2.3</a>  |
| 3h     | R3      | OE Pin Readback for CLK0 and CLK1                                              | <a href="#">Section 9.2.4</a>  |
| 4h     | R4      | AOD Enable Control and SBI_EN Readback                                         | <a href="#">Section 9.2.5</a>  |
| 5h     | R5      | Device Info                                                                    | <a href="#">Section 9.2.6</a>  |
| 6h     | R6      | Device Info (cont.)                                                            | <a href="#">Section 9.2.7</a>  |
| 7h     | R7      | SMBus Byte Counter                                                             | <a href="#">Section 9.2.8</a>  |
| 8h     | R8      | SBI Mask for CLK2 through CLK7                                                 | <a href="#">Section 9.2.9</a>  |
| 9h     | R9      | SBI Mask for CLK0 and CLK1                                                     | <a href="#">Section 9.2.10</a> |
| Bh     | R11     | SBI Mask Readback for CLK0 through CLK5                                        | <a href="#">Section 9.2.11</a> |
| Ch     | R12     | SBI Mask Readback for CLK6 and CLK7                                            | <a href="#">Section 9.2.12</a> |
| 11h    | R17     | Output Amplitude                                                               | <a href="#">Section 9.2.13</a> |
| 12h    | R18     | Input Configuration, Save Config in PD, SMB SDATA Monitoring, and LOS Readback | <a href="#">Section 9.2.14</a> |
| 14h    | R20     | Output Slew Rate Select MSB for CLK2 through CLK7                              | <a href="#">Section 9.2.15</a> |
| 15h    | R21     | Output Slew Rate Select MSB for CLK0 and CLK1                                  | <a href="#">Section 9.2.16</a> |
| 26h    | R38     | Non-clearable SMBUS Write Lock                                                 | <a href="#">Section 9.2.17</a> |
| 27h    | R39     | LOS Event Status and Clearable SMBus Write Lock                                | <a href="#">Section 9.2.18</a> |
| 35h    | R53     | Slew Rate Mode Control Selection                                               | <a href="#">Section 9.2.19</a> |
| 5Bh    | R91     | Slew Rate Speed Options 1 and 2 Assignments                                    | <a href="#">Section 9.2.20</a> |
| 5Ch    | R92     | Slew Rate Speed Options 3 and 4 Assignments                                    | <a href="#">Section 9.2.21</a> |
| 62h    | R98     | Output Slew Rate Select LSB for CLK0 through CLK7                              | <a href="#">Section 9.2.22</a> |

Complex bit access types are encoded to fit into small table cells. Table 9-30 shows the codes that are used for access types in this section.

**Table 9-30. LMKDB1108 Access Type Codes**

| Access Type            | Code    | Description                               |
|------------------------|---------|-------------------------------------------|
| Read Type              |         |                                           |
| R                      | R       | Read                                      |
| RC                     | R<br>C  | Read<br>to Clear                          |
| Write Type             |         |                                           |
| W                      | W       | Write                                     |
| W1C                    | W<br>1C | Write<br>1 to clear                       |
| WSC                    | W       | Write                                     |
| Reset or Default Value |         |                                           |
| -n                     |         | Value after reset or the default<br>value |

### 9.2.1 R0 Register (Offset = 0h) [Reset = EEh]

R0 is shown in [Table 9-31](#).

Return to the [Table 9-29](#).

**Table 9-31. R0 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                     |
|-----|----------|------|-------|---------------------------------------------------------------------------------|
| 7   | CLK_EN_2 | R/W  | 1h    | Output Enable for CLK2<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 6   | CLK_EN_3 | R/W  | 1h    | Output Enable for CLK3<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 5   | CLK_EN_4 | R/W  | 1h    | Output Enable for CLK4<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 4   | RESERVED | R    | 0h    | Reserved                                                                        |
| 3   | CLK_EN_5 | R/W  | 1h    | Output Enable for CLK5<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 2   | CLK_EN_6 | R/W  | 1h    | Output Enable for CLK6<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 1   | CLK_EN_7 | R/W  | 1h    | Output Enable for CLK7<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 0   | RESERVED | R    | 0h    | Reserved                                                                        |

### 9.2.2 R1 Register (Offset = 1h) [Reset = 24h]

R1 is shown in [Table 9-32](#).

Return to the [Table 9-29](#).

**Table 9-32. R1 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                     |
|-----|----------|------|-------|---------------------------------------------------------------------------------|
| 7:6 | RESERVED | R    | 0h    | Reserved                                                                        |
| 5   | CLK_EN_0 | R/W  | 1h    | Output Enable for CLK0<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 4:3 | RESERVED | R    | 0h    | Reserved                                                                        |
| 2   | CLK_EN_1 | R/W  | 1h    | Output Enable for CLK1<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 1:0 | RESERVED | R    | 0h    | Reserved                                                                        |

### 9.2.3 R2 Register (Offset = 2h) [Reset = 00h]

R2 is shown in [Table 9-33](#).

Return to the [Table 9-29](#).

**Table 9-33. R2 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description    |
|-----|----------|------|-------|----------------|
| 7   | RB_OEb_2 | R    | 0h    | Status of OEb2 |
| 6   | RB_OEb_3 | R    | 0h    | Status of OEb3 |

**Table 9-33. R2 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description    |
|-----|----------|------|-------|----------------|
| 5   | RB_OEb_4 | R    | 0h    | Status of OEb4 |
| 4   | RESERVED | R    | 0h    | Reserved       |
| 3   | RB_OEb_5 | R    | 0h    | Status of OEb5 |
| 2   | RB_OEb_6 | R    | 0h    | Status of OEb6 |
| 1   | RB_OEb_7 | R    | 0h    | Status of OEb7 |
| 0   | RESERVED | R    | 0h    | Reserved       |

**9.2.4 R3 Register (Offset = 3h) [Reset = 00h]**

R3 is shown in [Table 9-34](#).

Return to the [Table 9-29](#).

**Table 9-34. R3 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description    |
|-----|----------|------|-------|----------------|
| 7:6 | RESERVED | R    | 0h    | Reserved       |
| 5   | RB_OEb_0 | R    | 0h    | Status of OEb0 |
| 4:3 | RESERVED | R    | 0h    | Reserved       |
| 2   | RB_OEb_1 | R    | 0h    | Status of OEb1 |
| 1:0 | RESERVED | R    | 0h    | Reserved       |

**9.2.5 R4 Register (Offset = 4h) [Reset = 10h]**

R4 is shown in [Table 9-35](#).

Return to the [Table 9-29](#).

**Table 9-35. R4 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                               |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | RESERVED   | R    | 0h    | Reserved                                                                                                                                                                                                  |
| 4   | AOD_ENABLE | R/W  | 1h    | Enable automatic output disable (AOD) to low/low when LOS event is detected. Refer to section "Automatic Output Disable" for more information.<br>0h = Disabled (DC Coupled)<br>1h = Enabled (AC Coupled) |
| 3:1 | RESERVED   | R    | 0h    | Reserved                                                                                                                                                                                                  |
| 0   | RB_SBI_ENQ | R    | 0h    | Status of SBI_ENQ                                                                                                                                                                                         |

**9.2.6 R5 Register (Offset = 5h) [Reset = 0Ah]**

R5 is shown in [Table 9-36](#).

Return to the [Table 9-29](#).

**Table 9-36. R5 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description |
|-----|-----------|------|-------|-------------|
| 7:4 | REV_ID    | R    | 0h    | Revision ID |
| 3:0 | VENDOR_ID | R    | Ah    | Vendor ID   |

### 9.2.7 R6 Register (Offset = 6h) [Reset = 08h]

R6 is shown in [Table 9-37](#).

Return to the [Table 9-29](#).

**Table 9-37. R6 Register Field Descriptions**

| Bit | Field  | Type | Reset | Description |
|-----|--------|------|-------|-------------|
| 7:0 | DEV_ID | R    | 8h    | Device ID   |

### 9.2.8 R7 Register (Offset = 7h) [Reset = 07h]

R7 is shown in [Table 9-38](#).

Return to the [Table 9-29](#).

**Table 9-38. R7 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                 |
|-----|----------|------|-------|-----------------------------|
| 7:5 | RESERVED | R    | 0h    | Reserved                    |
| 4:0 | SMBUS_BC | R/W  | 7h    | SMBUS Block Read Byte Count |

### 9.2.9 R8 Register (Offset = 8h) [Reset = 00h]

R8 is shown in [Table 9-39](#).

Return to the [Table 9-29](#).

**Table 9-39. R8 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                         |
|-----|------------|------|-------|-------------------------------------|
| 7   | SBI_MASK_2 | R/W  | 0h    | Mask off Side-Band Disable for CLK2 |
| 6   | SBI_MASK_3 | R/W  | 0h    | Mask off Side-Band Disable for CLK3 |
| 5   | SBI_MASK_4 | R/W  | 0h    | Mask off Side-Band Disable for CLK4 |
| 4   | RESERVED   | R    | 0h    | Reserved                            |
| 3   | SBI_MASK_5 | R/W  | 0h    | Mask off Side-Band Disable for CLK5 |
| 2   | SBI_MASK_6 | R/W  | 0h    | Mask off Side-Band Disable for CLK6 |
| 1   | SBI_MASK_7 | R/W  | 0h    | Mask off Side-Band Disable for CLK7 |
| 0   | RESERVED   | R    | 0h    | Reserved                            |

### 9.2.10 R9 Register (Offset = 9h) [Reset = 00h]

R9 is shown in [Table 9-40](#).

Return to the [Table 9-29](#).

**Table 9-40. R9 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                         |
|-----|------------|------|-------|-------------------------------------|
| 7:6 | RESERVED   | R    | 0h    | Reserved                            |
| 5   | SBI_MASK_0 | R/W  | 0h    | Mask off Side-Band Disable for CLK0 |
| 4:3 | RESERVED   | R    | 0h    | Reserved                            |
| 2   | SBI_MASK_1 | R/W  | 0h    | Mask off Side-Band Disable for CLK1 |
| 1:0 | RESERVED   | R    | 0h    | Reserved                            |

### 9.2.11 R11 Register (Offset = Bh) [Reset = EEh]

R11 is shown in [Table 9-41](#).

Return to the [Table 9-29](#).

**Table 9-41. R11 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                            |
|-----|-----------|------|-------|----------------------------------------|
| 7   | SBI_CLK_2 | R    | 1h    | Readback of Side-Band Disable for CLK5 |
| 6   | SBI_CLK_3 | R    | 1h    | Readback of Side-Band Disable for CLK4 |
| 5   | SBI_CLK_4 | R    | 1h    | Readback of Side-Band Disable for CLK3 |
| 4   | RESERVED  | R    | 0h    | Reserved                               |
| 3   | SBI_CLK_5 | R    | 1h    | Readback of Side-Band Disable for CLK2 |
| 2   | SBI_CLK_6 | R    | 1h    | Readback of Side-Band Disable for CLK1 |
| 1   | SBI_CLK_7 | R    | 1h    | Readback of Side-Band Disable for CLK0 |
| 0   | RESERVED  | R    | 0h    | Reserved                               |

### 9.2.12 R12 Register (Offset = Ch) [Reset = 24h]

R12 is shown in [Table 9-42](#).

Return to the [Table 9-29](#).

**Table 9-42. R12 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                            |
|-----|-----------|------|-------|----------------------------------------|
| 7:6 | RESERVED  | R    | 0h    | Reserved                               |
| 5   | SBI_CLK_0 | R    | 1h    | Readback of Side-Band Disable for CLK7 |
| 4:3 | RESERVED  | R    | 0h    | Reserved                               |
| 2   | SBI_CLK_1 | R    | 1h    | Readback of Side-Band Disable for CLK6 |
| 1:0 | RESERVED  | R    | 0h    | Reserved                               |

### 9.2.13 R17 Register (Offset = 11h) [Reset = 66h]

R17 is shown in [Table 9-43](#).

Return to the [Table 9-29](#).

**Table 9-43. R17 Register Field Descriptions**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                            |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | AMP   | R/W  | 6h    | Global Differential output Control 0.6V to 1V 25mV/step Default = 0.8V<br>0h = 600mV<br>1h = 625mV<br>2h = 650mV<br>3h = 675mV<br>4h = 700mV<br>5h = 725mV<br>6h = 750mV<br>7h = 775mV<br>8h = 800mV<br>9h = 825mV<br>Ah = 850mV<br>Bh = 875mV<br>Ch = 900mV<br>Dh = 925mV<br>Eh = 950mV<br>Fh = 975mV |

**Table 9-43. R17 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 3:0 | RESERVED | R    | 0h    | Reserved    |

#### 9.2.14 R18 Register (Offset = 12h) [Reset = 08h]

R18 is shown in [Table 9-44](#).

Return to the [Table 9-29](#).

**Table 9-44. R18 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                                               |
|-----|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------|
| 7   | RX_EN_AC_INPUT  | R/W  | 0h    | Enable receiver bias when CLKIN is AC coupled<br>0h = DC Coupled Input<br>1h = AC Coupled Input           |
| 6   | RX_EN_RTERM_LSB | R/W  | 0h    | Enable/Disables termination resistors on CLKIN1<br>0h = Disabled<br>1h = Enabled                          |
| 5:4 | RESERVED        | R    | 0h    | Reserved                                                                                                  |
| 3   | PD_RESTOREB     | R/W  | 1h    | Save Configuration in Power Down<br>0h = Config Cleared<br>1h = Config Saved                              |
| 2:1 | RESERVED        | R    | 0h    | Reserved                                                                                                  |
| 0   | LOSb_RB         | R    | 0h    | Real time read back of loss detect block output<br>0h = LOS Event Detected<br>1h = LOS Event Not-Detected |

#### 9.2.15 R20 Register (Offset = 14h) [Reset = EEh]

R20 is shown in [Table 9-45](#).

Return to the [Table 9-29](#).

**Table 9-45. R20 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description               |
|-----|-----------------------|------|-------|---------------------------|
| 7   | SLEWRATE_SEL_CLK2_MSB | R/W  | 1h    | MSB CLK2 slew rate select |
| 6   | SLEWRATE_SEL_CLK3_MSB | R/W  | 1h    | MSB CLK3 slew rate select |
| 5   | SLEWRATE_SEL_CLK4_MSB | R/W  | 1h    | MSB CLK4 slew rate select |
| 4   | RESERVED              | R    | 0h    | Reserved                  |
| 3   | SLEWRATE_SEL_CLK5_MSB | R/W  | 1h    | MSB CLK5 slew rate select |
| 2   | SLEWRATE_SEL_CLK6_MSB | R/W  | 1h    | MSB CLK6 slew rate select |
| 1   | SLEWRATE_SEL_CLK7_MSB | R/W  | 1h    | MSB CLK7 slew rate select |
| 0   | RESERVED              | R    | 0h    | Reserved                  |

#### 9.2.16 R21 Register (Offset = 15h) [Reset = 24h]

R21 is shown in [Table 9-46](#).

Return to the [Table 9-29](#).

**Table 9-46. R21 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description               |
|-----|-----------------------|------|-------|---------------------------|
| 7:6 | RESERVED              | R    | 0h    | Reserved                  |
| 5   | SLEWRATE_SEL_CLK0_MSB | R/W  | 1h    | MSB CLK0 slew rate select |
| 4:3 | RESERVED              | R    | 0h    | Reserved                  |
| 2   | SLEWRATE_SEL_CLK1_MSB | R/W  | 1h    | MSB CLK1 slew rate select |
| 1:0 | RESERVED              | R    | 0h    | Reserved                  |

**9.2.17 R38 Register (Offset = 26h) [Reset = 00h]**

R38 is shown in [Table 9-47](#).

Return to the [Table 9-29](#).

**Table 9-47. R38 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                       |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | RESERVED   | R    | 0h    | Reserved                                                                                                                                                                                                                          |
| 0   | WRITE_LOCK | R    | 0h    | Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by recycling power.<br>0h = SMBus Not Locked for Writing<br>1h = SMBus Locked for Writing |

**9.2.18 R39 Register (Offset = 27h) [Reset = 00h]**

R39 is shown in [Table 9-48](#).

Return to the [Table 9-29](#).

**Table 9-48. R39 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                           |
|-----|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | RESERVED        | R    | 0h    | Reserved                                                                                                                                                                                                              |
| 1   | LOS_EVT         | R/W  | 0h    | LOS Event Status. When high, indicates that a LOS event is detected. Can be cleared by writing a 1.<br>0h = Not LOS Event Detected<br>1h = LOS Event Detected                                                         |
| 0   | WRITE_LOCK_RW1C | R    | 0h    | Clearable SMBus Write Lock bit. When written to one, the SMBus control registers can not be written to. This bit can be cleared by writing a 1.<br>0h = SMBus Not Locked for Writing<br>1h = SMBus Locked for Writing |

**9.2.19 R53 Register (Offset = 35h) [Reset = 00h]**

R53 is shown in [Table 9-49](#).

Return to the [Table 9-29](#).

**Table 9-49. R53 Register Field Descriptions**

| Bit | Field              | Type  | Reset | Description                                                                                  |
|-----|--------------------|-------|-------|----------------------------------------------------------------------------------------------|
| 7:6 | RESERVED           | R     | 0h    | Reserved                                                                                     |
| 5   | SLEWRATE_CTRL_MODE | R/WSC | 0h    | Sets which mode is used to change the outputs slew rates<br>0h = Pin mode<br>1h = SMBus mode |

**Table 9-49. R53 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 4:0 | RESERVED | R    | 0h    | Reserved    |

### 9.2.20 R91 Register (Offset = 5Bh) [Reset = 60h]

R91 is shown in [Table 9-50](#).

Return to the [Table 9-29](#).

**Table 9-50. R91 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | SLEWRATE_OPT_2 | R/W  | 6h    | There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 2nd option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 |
| 3:0 | SLEWRATE_OPT_1 | R/W  | 0h    | There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 1st option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 |

### 9.2.21 R92 Register (Offset = 5Ch) [Reset = FAh]

R92 is shown in [Table 9-51](#).

Return to the [Table 9-29](#).

**Table 9-51. R92 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | SLEWRATE_OPT_4 | R/W  | Fh    | There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 4th option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 |
| 3:0 | SLEWRATE_OPT_3 | R/W  | Ah    | There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 3rd option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 |

### 9.2.22 R98 Register (Offset = 62h) [Reset = 00h]

R98 is shown in [Table 9-52](#).

Return to the [Table 9-29](#).

**Table 9-52. R98 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description                |
|-----|-----------------------|------|-------|----------------------------|
| 7   | SLEWRATE_SEL_CLK7_LSB | R/W  | 0h    | LSB CLK7 Slew Rate Control |
| 6   | SLEWRATE_SEL_CLK6_LSB | R/W  | 0h    | LSB CLK6 Slew Rate Control |
| 5   | SLEWRATE_SEL_CLK5_LSB | R/W  | 0h    | LSB CLK5 Slew Rate Control |
| 4   | SLEWRATE_SEL_CLK4_LSB | R/W  | 0h    | LSB CLK4 Slew Rate Control |
| 3   | SLEWRATE_SEL_CLK3_LSB | R/W  | 0h    | LSB CLK3 Slew Rate Control |

**Table 9-52. R98 Register Field Descriptions (continued)**

| Bit | Field                 | Type | Reset | Description                |
|-----|-----------------------|------|-------|----------------------------|
| 2   | SLEWRATE_SEL_CLK2_LSB | R/W  | 0h    | LSB CLK2 Slew Rate Control |
| 1   | SLEWRATE_SEL_CLK1_LSB | R/W  | 0h    | LSB CLK1 Slew Rate Control |
| 0   | SLEWRATE_SEL_CLK0_LSB | R/W  | 0h    | LSB CLK0 Slew Rate Control |

### 9.3 LMKDB1104 Registers

Table 9-53 lists the memory-mapped registers for the LMKDB1104 registers. All register offset addresses not listed in Table 9-53 must be considered as reserved locations and the register contents must not be modified.

**Table 9-53. LMKDB1104 Registers**

| Offset | Acronym | Register Name                                                                                         | Section                        |
|--------|---------|-------------------------------------------------------------------------------------------------------|--------------------------------|
| 0h     | R0      | Output Enable Control for CLK2 and CLK3                                                               | <a href="#">Section 9.3.1</a>  |
| 1h     | R1      | Output Enable Control for CLK0 and CLK1                                                               | <a href="#">Section 9.3.2</a>  |
| 2h     | R2      | OE Pin Readback for CLK2 and CLK3                                                                     | <a href="#">Section 9.3.3</a>  |
| 3h     | R3      | OE Pin Readback for CLK0 and CLK1                                                                     | <a href="#">Section 9.3.4</a>  |
| 4h     | R4      | Readback status of SBI_EN and CLKIN AOD Enable Control                                                | <a href="#">Section 9.3.5</a>  |
| 5h     | R5      | Device Info                                                                                           | <a href="#">Section 9.3.6</a>  |
| 6h     | R6      | Device Info (cont.)                                                                                   | <a href="#">Section 9.3.7</a>  |
| 7h     | R7      | SMBus Byte Counter                                                                                    | <a href="#">Section 9.3.8</a>  |
| 8h     | R8      | Mask off Side-Band Disable for CLK3 and CLK2                                                          | <a href="#">Section 9.3.9</a>  |
| 9h     | R9      | Mask off Side-Band Disable for CLK1 and CLK0                                                          | <a href="#">Section 9.3.10</a> |
| Bh     | R11     | Readback of Side-Band Disable for CLK3 and CLK2                                                       | <a href="#">Section 9.3.11</a> |
| Ch     | R12     | Readback of Side-Band Disable for CLK1 and CLK0                                                       | <a href="#">Section 9.3.12</a> |
| 11h    | R17     | Output Amplitude                                                                                      | <a href="#">Section 9.3.13</a> |
| 12h    | R18     | Input Configuration, Save Config in PD, Slew Rate select mode, SMB SDATA Monitoring, and LOS Readback | <a href="#">Section 9.3.14</a> |
| 14h    | R20     | Output Slew Rate Select MSB for CLK2 and CLK3                                                         | <a href="#">Section 9.3.15</a> |
| 15h    | R21     | Output Slew Rate Select MSB for CLK0 and CLK1                                                         | <a href="#">Section 9.3.16</a> |
| 26h    | R38     | Non-clearable SMBUS Write Lock                                                                        | <a href="#">Section 9.3.17</a> |
| 27h    | R39     | LOS Event Status and Clearable SMBus Write Lock                                                       | <a href="#">Section 9.3.18</a> |
| 5Bh    | R91     | Slew Rate Speed Options 1 and 2 Assignments                                                           | <a href="#">Section 9.3.19</a> |
| 5Ch    | R92     | Slew Rate Speed Options 3 and 4 Assignments                                                           | <a href="#">Section 9.3.20</a> |
| 62h    | R98     | Output Slew Rate Select LSB for CLK0 and CLK1                                                         | <a href="#">Section 9.3.21</a> |
| 63h    | R99     | Output Slew Rate Select LSB for CLK2 and CLK3                                                         | <a href="#">Section 9.3.22</a> |

Complex bit access types are encoded to fit into small table cells. Table 9-54 shows the codes that are used for access types in this section.

**Table 9-54. LMKDB1104 Access Type Codes**

| Access Type            | Code    | Description                            |
|------------------------|---------|----------------------------------------|
| Read Type              |         |                                        |
| R                      | R       | Read                                   |
| Write Type             |         |                                        |
| W                      | W       | Write                                  |
| W1C                    | W<br>1C | Write<br>1 to clear                    |
| Reset or Default Value |         |                                        |
| -n                     |         | Value after reset or the default value |

#### 9.3.1 R0 Register (Offset = 0h) [Reset = 24h]

R0 is shown in Table 9-55.

Return to the [Table 9-53](#).

**Table 9-55. R0 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                     |
|-----|----------|------|-------|---------------------------------------------------------------------------------|
| 7:6 | RESERVED | R    | 0h    | Reserved                                                                        |
| 5   | CLK_EN_2 | R/W  | 1h    | Output Enable for CLK2<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 4:3 | RESERVED | R    | 0h    | Reserved                                                                        |
| 2   | CLK_EN_3 | R/W  | 1h    | Output Enable for CLK3<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 1:0 | RESERVED | R    | 0h    | Reserved                                                                        |

### 9.3.2 R1 Register (Offset = 1h) [Reset = 22h]

R1 is shown in [Table 9-56](#).

Return to the [Table 9-53](#).

**Table 9-56. R1 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                     |
|-----|----------|------|-------|---------------------------------------------------------------------------------|
| 7:6 | RESERVED | R    | 0h    | Reserved                                                                        |
| 5   | CLK_EN_0 | R/W  | 1h    | Output Enable for CLK0<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 4:2 | RESERVED | R    | 0h    | Reserved                                                                        |
| 1   | CLK_EN_1 | R/W  | 1h    | Output Enable for CLK1<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 0   | RESERVED | R    | 0h    | Reserved                                                                        |

### 9.3.3 R2 Register (Offset = 2h) [Reset = 00h]

R2 is shown in [Table 9-57](#).

Return to the [Table 9-53](#).

**Table 9-57. R2 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description    |
|-----|----------|------|-------|----------------|
| 7:6 | RESERVED | R    | 0h    | Reserved       |
| 5   | RB_OEb_2 | R    | 0h    | Status of OEB2 |
| 4:3 | RESERVED | R    | 0h    | Reserved       |
| 2   | RB_OEb_3 | R    | 0h    | Status of OEB3 |
| 1:0 | RESERVED | R    | 0h    | Reserved       |

### 9.3.4 R3 Register (Offset = 3h) [Reset = 00h]

R3 is shown in [Table 9-58](#).

Return to the [Table 9-53](#).

**Table 9-58. R3 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7:6 | RESERVED | R    | 0h    | Reserved    |

**Table 9-58. R3 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description    |
|-----|----------|------|-------|----------------|
| 5   | RB_OEb_0 | R    | 0h    | Status of OEb0 |
| 4:2 | RESERVED | R    | 0h    | Reserved       |
| 1   | RB_OEb_1 | R    | 0h    | Status of OEb1 |
| 0   | RESERVED | R    | 0h    | Reserved       |

**9.3.5 R4 Register (Offset = 4h) [Reset = 10h]**

R4 is shown in [Table 9-59](#).

Return to the [Table 9-53](#).

**Table 9-59. R4 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                              |
|-----|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | RESERVED   | R    | 0h    | Reserved                                                                                                                                                                                 |
| 4   | AOD_ENABLE | R/W  | 1h    | Enable automatic output disable (AOD) for CLKIN to low/low when LOS event is detected. Refer to section "Automatic Output Disable" for more information.<br>0h = Inactive<br>1h = Active |
| 3:1 | RESERVED   | R    | 0h    | Reserved                                                                                                                                                                                 |
| 0   | RB_SBI_ENQ | R    | 0h    | Status of SBI_ENQ                                                                                                                                                                        |

**9.3.6 R5 Register (Offset = 5h) [Reset = 0Ah]**

R5 is shown in [Table 9-60](#).

Return to the [Table 9-53](#).

**Table 9-60. R5 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description |
|-----|-----------|------|-------|-------------|
| 7:4 | REV_ID    | R    | 0h    | Revision ID |
| 3:0 | VENDOR_ID | R    | Ah    | Vendor ID   |

**9.3.7 R6 Register (Offset = 6h) [Reset = 04h]**

R6 is shown in [Table 9-61](#).

Return to the [Table 9-53](#).

**Table 9-61. R6 Register Field Descriptions**

| Bit | Field  | Type | Reset | Description |
|-----|--------|------|-------|-------------|
| 7:0 | DEV_ID | R    | 4h    | Device ID   |

**9.3.8 R7 Register (Offset = 7h) [Reset = 07h]**

R7 is shown in [Table 9-62](#).

Return to the [Table 9-53](#).

**Table 9-62. R7 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7:5 | RESERVED | R    | 0h    | Reserved    |

**Table 9-62. R7 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                 |
|-----|----------|------|-------|-----------------------------|
| 4:0 | SMBUS_BC | R/W  | 7h    | SMBUS Block Read Byte Count |

### 9.3.9 R8 Register (Offset = 8h) [Reset = 00h]

R8 is shown in [Table 9-63](#).

Return to the [Table 9-53](#).

**Table 9-63. R8 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                         |
|-----|------------|------|-------|-------------------------------------|
| 7:6 | RESERVED   | R    | 0h    | Reserved                            |
| 5   | SBI_MASK_2 | R/W  | 0h    | Mask off Side-Band Disable for CLK2 |
| 4:3 | RESERVED   | R    | 0h    | Reserved                            |
| 2   | SBI_MASK_3 | R/W  | 0h    | Mask off Side-Band Disable for CLK3 |
| 1:0 | RESERVED   | R    | 0h    | Reserved                            |

### 9.3.10 R9 Register (Offset = 9h) [Reset = 00h]

R9 is shown in [Table 9-64](#).

Return to the [Table 9-53](#).

**Table 9-64. R9 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                         |
|-----|------------|------|-------|-------------------------------------|
| 7:6 | RESERVED   | R    | 0h    | Reserved                            |
| 5   | SBI_MASK_0 | R/W  | 0h    | Mask off Side-Band Disable for CLK0 |
| 4:2 | RESERVED   | R    | 0h    | Reserved                            |
| 1   | SBI_MASK_1 | R/W  | 0h    | Mask off Side-Band Disable for CLK1 |
| 0   | RESERVED   | R    | 0h    | Reserved                            |

### 9.3.11 R11 Register (Offset = Bh) [Reset = 24h]

R11 is shown in [Table 9-65](#).

Return to the [Table 9-53](#).

**Table 9-65. R11 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                            |
|-----|-----------|------|-------|----------------------------------------|
| 7:6 | RESERVED  | R    | 0h    | Reserved                               |
| 5   | SBI_CLK_2 | R    | 1h    | Readback of Side-Band Disable for CLK2 |
| 4:3 | RESERVED  | R    | 0h    | Reserved                               |
| 2   | SBI_CLK_3 | R    | 1h    | Readback of Side-Band Disable for CLK3 |
| 1:0 | RESERVED  | R    | 0h    | Reserved                               |

### 9.3.12 R12 Register (Offset = Ch) [Reset = 22h]

R12 is shown in [Table 9-66](#).

Return to the [Table 9-53](#).

**Table 9-66. R12 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                            |
|-----|-----------|------|-------|----------------------------------------|
| 7:6 | RESERVED  | R    | 0h    | Reserved                               |
| 5   | SBI_CLK_0 | R    | 1h    | Readback of Side-Band Disable for CLK0 |
| 4:2 | RESERVED  | R    | 0h    | Reserved                               |
| 1   | SBI_CLK_1 | R    | 1h    | Readback of Side-Band Disable for CLK1 |
| 0   | RESERVED  | R    | 0h    | Reserved                               |

**9.3.13 R17 Register (Offset = 11h) [Reset = 66h]**

R17 is shown in [Table 9-67](#).

Return to the [Table 9-53](#).

**Table 9-67. R17 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                              |
|-----|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | AMP      | R/W  | 6h    | Global Differential output Control, approximately 0.6V to 1V 25mV/step (default = 0.75V)<br>0h = 600 mV<br>1h = 625 mV<br>2h = 650 mV<br>3h = 675 mV<br>4h = 700 mV<br>5h = 725 mV<br>6h = 750 mV<br>7h = 775 mV<br>8h = 800 mV<br>9h = 825 mV<br>Ah = 850 mV<br>Bh = 875 mV<br>Ch = 900 mV<br>Dh = 925 mV<br>Eh = 950 mV<br>Fh = 975 mV |
| 3:0 | RESERVED | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                 |

**9.3.14 R18 Register (Offset = 12h) [Reset = 0Ah]**

R18 is shown in [Table 9-68](#).

Return to the [Table 9-53](#).

**Table 9-68. R18 Register Field Descriptions**

| Bit | Field                    | Type | Reset | Description                                                                                                  |
|-----|--------------------------|------|-------|--------------------------------------------------------------------------------------------------------------|
| 7   | RX_CLKIN_EN_AC_INPU<br>T | R/W  | 0h    | Enable receiver bias when CLKIN is AC coupled<br>0h = DC Coupled Input<br>1h = AC Coupled Input              |
| 6   | RX_CLKIN_EN_RTERM        | R/W  | 0h    | Enable termination resistors on CLKIN1<br>0h = Input termination inactive<br>1h = Input termination active   |
| 5   | RESERVED                 | R    | 0h    | Reserved                                                                                                     |
| 4   | SLEWRATE_CTRL_MOD<br>E   | R    | 0h    | Slew rate select preference between pin mode and register mode.<br>0h = Pin Control<br>1h = Register Control |
| 3   | PD_RESTOREB              | R    | 1h    | Save configuration in powerdown<br>0h = Config Cleared<br>1h = Config Saved                                  |
| 2   | RESERVED                 | R    | 0h    | Reserved                                                                                                     |

**Table 9-68. R18 Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                               |
|-----|------------------|------|-------|-----------------------------------------------------------------------------------------------------------|
| 1   | SDATA_TIMEOUT_EN | R    | 1h    | Enable SMBus SDATA time out monitoring<br>0h = Disable SDATA timeout<br>1h = Enable SDATA timeout         |
| 0   | LOSb_RB          | R    | 0h    | Real time read back of loss detect block output<br>0h = LOS Event Detected<br>1h = LOS Event Not-Detected |

### 9.3.15 R20 Register (Offset = 14h) [Reset = 24h]

R20 is shown in [Table 9-69](#).

Return to the [Table 9-53](#).

**Table 9-69. R20 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description               |
|-----|-----------------------|------|-------|---------------------------|
| 7:6 | RESERVED              | R    | 0h    | Reserved                  |
| 5   | SLEWRATE_SEL_CLK2_MSB | R/W  | 1h    | MSB CLK2 slew rate select |
| 4:3 | RESERVED              | R    | 0h    | Reserved                  |
| 2   | SLEWRATE_SEL_CLK3_MSB | R/W  | 1h    | MSB CLK3 slew rate select |
| 1:0 | RESERVED              | R    | 0h    | Reserved                  |

### 9.3.16 R21 Register (Offset = 15h) [Reset = 22h]

R21 is shown in [Table 9-70](#).

Return to the [Table 9-53](#).

**Table 9-70. R21 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description               |
|-----|-----------------------|------|-------|---------------------------|
| 7:6 | RESERVED              | R    | 0h    | Reserved                  |
| 5   | SLEWRATE_SEL_CLK0_MSB | R/W  | 1h    | MSB CLK0 slew rate select |
| 4:2 | RESERVED              | R    | 0h    | Reserved                  |
| 1   | SLEWRATE_SEL_CLK1_MSB | R/W  | 1h    | MSB CLK1 slew rate select |
| 0   | RESERVED              | R    | 0h    | Reserved                  |

### 9.3.17 R38 Register (Offset = 26h) [Reset = 00h]

R38 is shown in [Table 9-71](#).

Return to the [Table 9-53](#).

**Table 9-71. R38 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                       |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | RESERVED   | R    | 0h    | Reserved                                                                                                                                                                                                                          |
| 0   | WRITE_LOCK | R    | 0h    | Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by recycling power.<br>0h = SMBus Not Locked for Writing<br>1h = SMBus Locked for Writing |

### 9.3.18 R39 Register (Offset = 27h) [Reset = 00h]

R39 is shown in [Table 9-72](#).

Return to the [Table 9-53](#).

**Table 9-72. R39 Register Field Descriptions**

| Bit | Field           | Type  | Reset | Description                                                                                                                                                                                                           |
|-----|-----------------|-------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | RESERVED        | R     | 0h    | Reserved                                                                                                                                                                                                              |
| 1   | LOS_EVT         | R     | 0h    | LOS Event Status. When high, indicates that a LOS event is detected. Can be cleared by writing a 1.<br>0h = Not LOS Event Detected<br>1h = LOS Event Detected                                                         |
| 0   | WRITE_LOCK_RW1C | R/W1C | 0h    | Clearable SMBus Write Lock bit. When written to one, the SMBus control registers can not be written to. This bit can be cleared by writing a 1.<br>0h = SMBus Not Locked for Writing<br>1h = SMBus Locked for Writing |

### 9.3.19 R91 Register (Offset = 5Bh) [Reset = 60h]

R91 is shown in [Table 9-73](#).

Return to the [Table 9-53](#).

**Table 9-73. R91 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | SLEWRATE_OPT_2 | R/W  | 6h    | There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 2nd option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0 (fastest)<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 (slowest) |

**Table 9-73. R91 Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | SLEWRATE_OPT_1 | R/W  | 0h    | <p>There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 1st option. Go to Programmable Output Slew Rate section for more information.</p> <p>0h = 0 (fastest)<br/> 1h = 1<br/> 2h = 2<br/> 3h = 3<br/> 4h = 4<br/> 5h = 5<br/> 6h = 6<br/> 7h = 7<br/> 8h = 8<br/> 9h = 9<br/> Ah = 10<br/> Bh = 11<br/> Ch = 12<br/> Dh = 13<br/> Eh = 14<br/> Fh = 15 (slowest)</p> |

### 9.3.20 R92 Register (Offset = 5Ch) [Reset = FAh]

R92 is shown in [Table 9-74](#).

Return to the [Table 9-53](#).

**Table 9-74. R92 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | SLEWRATE_OPT_4 | R/W  | Fh    | <p>There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 4th option. Go to Programmable Output Slew Rate section for more information.</p> <p>0h = 0 (fastest)<br/> 1h = 1<br/> 2h = 2<br/> 3h = 3<br/> 4h = 4<br/> 5h = 5<br/> 6h = 6<br/> 7h = 7<br/> 8h = 8<br/> 9h = 9<br/> Ah = 10<br/> Bh = 11<br/> Ch = 12<br/> Dh = 13<br/> Eh = 14<br/> Fh = 15 (slowest)</p> |

**Table 9-74. R92 Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | SLEWRATE_OPT_3 | R/W  | Ah    | <p>There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 3rd option. Go to Programmable Output Slew Rate section for more information.</p> <p>0h = 0 (fastest)<br/> 1h = 1<br/> 2h = 2<br/> 3h = 3<br/> 4h = 4<br/> 5h = 5<br/> 6h = 6<br/> 7h = 7<br/> 8h = 8<br/> 9h = 9<br/> Ah = 10<br/> Bh = 11<br/> Ch = 12<br/> Dh = 13<br/> Eh = 14<br/> Fh = 15 (slowest)</p> |

**9.3.21 R98 Register (Offset = 62h) [Reset = 00h]**

R98 is shown in [Table 9-75](#).

Return to the [Table 9-53](#).

**Table 9-75. R98 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description                |
|-----|-----------------------|------|-------|----------------------------|
| 7   | SLEWRATE_SEL_CLK1_LSB | R/W  | 0h    | LSB CLK1 Slew Rate Control |
| 6:5 | RESERVED              | R    | 0h    | Reserved                   |
| 4   | SLEWRATE_SEL_CLK0_LSB | R/W  | 0h    | LSB CLK0 Slew Rate Control |
| 3:0 | RESERVED              | R    | 0h    | Reserved                   |

**9.3.22 R99 Register (Offset = 63h) [Reset = 00h]**

R99 is shown in [Table 9-76](#).

Return to the [Table 9-53](#).

**Table 9-76. R99 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description                |
|-----|-----------------------|------|-------|----------------------------|
| 7   | RESERVED              | R    | 0h    | Reserved                   |
| 6   | SLEWRATE_SEL_CLK3_LSB | R/W  | 0h    | LSB CLK3 Slew Rate Control |
| 5:3 | RESERVED              | R    | 0h    | Reserved                   |
| 2   | SLEWRATE_SEL_CLK2_LSB | R/W  | 0h    | LSB CLK2 Slew Rate Control |
| 1:0 | RESERVED              | R    | 0h    | Reserved                   |

## 9.4 LMKDB1204 Registers

Table 9-77 lists the memory-mapped registers for the LMKDB1204 registers. All register offset addresses not listed in Table 9-77 must be considered as reserved locations and the register contents must not be modified.

**Table 9-77. LMKDB1204 Registers**

| Offset | Acronym | Register Name                                                                  | Section                        |
|--------|---------|--------------------------------------------------------------------------------|--------------------------------|
| 0h     | R0      | Output Enable Control for CLK2 and CLK3                                        | <a href="#">Section 9.4.1</a>  |
| 1h     | R1      | Output Enable Control for CLK0 and CLK1                                        | <a href="#">Section 9.4.2</a>  |
| 2h     | R2      | OE Pin Readback for CLK2 and CLK3                                              | <a href="#">Section 9.4.3</a>  |
| 3h     | R3      | OE Pin Readback for CLK0 and CLK1                                              | <a href="#">Section 9.4.4</a>  |
| 4h     | R4      | CLKIN1 AOD Enable Control                                                      | <a href="#">Section 9.4.5</a>  |
| 5h     | R5      | Device Info                                                                    | <a href="#">Section 9.4.6</a>  |
| 6h     | R6      | Device Info (cont.)                                                            | <a href="#">Section 9.4.7</a>  |
| 7h     | R7      | SMBus Byte Counter                                                             | <a href="#">Section 9.4.8</a>  |
| 11h    | R17     | Output Amplitude                                                               | <a href="#">Section 9.4.9</a>  |
| 12h    | R18     | Input Configuration, Save Config in PD, SMB SDATA Monitoring, and LOS Readback | <a href="#">Section 9.4.10</a> |
| 14h    | R20     | Output Slew Rate Select MSB for CLK2 and CLK3                                  | <a href="#">Section 9.4.11</a> |
| 15h    | R21     | Output Slew Rate Select MSB for CLK0 and CLK1                                  | <a href="#">Section 9.4.12</a> |
| 24h    | R36     | CLKIN0 AOD Enable Control                                                      | <a href="#">Section 9.4.13</a> |
| 26h    | R38     | Non-clearable SMBUS Write Lock                                                 | <a href="#">Section 9.4.14</a> |
| 27h    | R39     | LOS Event Status and Clearable SMBus Write Lock                                | <a href="#">Section 9.4.15</a> |
| 2Bh    | R43     | CLKIN Source Select                                                            | <a href="#">Section 9.4.16</a> |
| 5Bh    | R91     | Slew Rate Speed Options 1 and 2 Assignments                                    | <a href="#">Section 9.4.17</a> |
| 5Ch    | R92     | Slew Rate Speed Options 3 and 4 Assignments                                    | <a href="#">Section 9.4.18</a> |
| 5Dh    | R93     | CLKIN0 AC/DC coupled Selection                                                 | <a href="#">Section 9.4.19</a> |
| 62h    | R98     | Output Slew Rate Select LSB for CLK0 and CLK1                                  | <a href="#">Section 9.4.20</a> |
| 63h    | R99     | Output Slew Rate Select LSB for CLK2 and CLK3                                  | <a href="#">Section 9.4.21</a> |

Complex bit access types are encoded to fit into small table cells. Table 9-78 shows the codes that are used for access types in this section.

**Table 9-78. LMKDB1204 Access Type Codes**

| Access Type            | Code    | Description                            |
|------------------------|---------|----------------------------------------|
| Read Type              |         |                                        |
| R                      | R       | Read                                   |
| Write Type             |         |                                        |
| W                      | W       | Write                                  |
| W1C                    | W<br>1C | Write<br>1 to clear                    |
| Reset or Default Value |         |                                        |
| -n                     |         | Value after reset or the default value |

### 9.4.1 R0 Register (Offset = 0h) [Reset = 28h]

R0 is shown in Table 9-79.

Return to the Table 9-77.

**Table 9-79. R0 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                     |
|-----|----------|------|-------|---------------------------------------------------------------------------------|
| 7:6 | RESERVED | R    | 0h    | Reserved                                                                        |
| 5   | CLK_EN_1 | R/W  | 1h    | Output Enable for CLK1<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 4   | RESERVED | R    | 0h    | Reserved                                                                        |
| 3   | CLK_EN_0 | R/W  | 1h    | Output Enable for CLK0<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 2:0 | RESERVED | R    | 0h    | Reserved                                                                        |

**9.4.2 R1 Register (Offset = 1h) [Reset = 14h]**

R1 is shown in [Table 9-80](#).

Return to the [Table 9-77](#).

**Table 9-80. R1 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                     |
|-----|----------|------|-------|---------------------------------------------------------------------------------|
| 7:5 | RESERVED | R    | 0h    | Reserved                                                                        |
| 4   | CLK_EN_3 | R/W  | 1h    | Output Enable for CLK3<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 3   | RESERVED | R    | 0h    | Reserved                                                                        |
| 2   | CLK_EN_2 | R/W  | 1h    | Output Enable for CLK2<br>0h = Output Disabled (low/low)<br>1h = Output Enabled |
| 1:0 | RESERVED | R    | 0h    | Reserved                                                                        |

**9.4.3 R2 Register (Offset = 2h) [Reset = 00h]**

R2 is shown in [Table 9-81](#).

Return to the [Table 9-77](#).

**Table 9-81. R2 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description    |
|-----|----------|------|-------|----------------|
| 7:6 | RESERVED | R    | 0h    | Reserved       |
| 5   | RB_OEb_1 | R    | 0h    | Status of OEb1 |
| 4   | RESERVED | R    | 0h    | Reserved       |
| 3   | RB_OEb_0 | R    | 0h    | Status of OEb0 |
| 2:0 | RESERVED | R    | 0h    | Reserved       |

**9.4.4 R3 Register (Offset = 3h) [Reset = 00h]**

R3 is shown in [Table 9-82](#).

Return to the [Table 9-77](#).

**Table 9-82. R3 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description    |
|-----|----------|------|-------|----------------|
| 7:5 | RESERVED | R    | 0h    | Reserved       |
| 4   | RB_OEb_3 | R    | 0h    | Status of OEb3 |

**Table 9-82. R3 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description    |
|-----|----------|------|-------|----------------|
| 3   | RESERVED | R    | 0h    | Reserved       |
| 2   | RB_OEb_2 | R    | 0h    | Status of OEB2 |
| 1:0 | RESERVED | R    | 0h    | Reserved       |

#### 9.4.5 R4 Register (Offset = 4h) [Reset = 10h]

R4 is shown in [Table 9-83](#).

Return to the [Table 9-77](#).

**Table 9-83. R4 Register Field Descriptions**

| Bit | Field             | Type | Reset | Description                                                                                                                                                                               |
|-----|-------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | RESERVED          | R    | 0h    | Reserved                                                                                                                                                                                  |
| 4   | CLKIN1_AOD_ENABLE | R/W  | 1h    | Enable automatic output disable (AOD) for CLKIN1 to low/low when LOS event is detected. Refer to section "Automatic Output Disable" for more information.<br>0h = Inactive<br>1h = Active |
| 3:0 | RESERVED          | R    | 0h    | Reserved                                                                                                                                                                                  |

#### 9.4.6 R5 Register (Offset = 5h) [Reset = 0Ah]

R5 is shown in [Table 9-84](#).

Return to the [Table 9-77](#).

**Table 9-84. R5 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description |
|-----|-----------|------|-------|-------------|
| 7:4 | REV_ID    | R    | 0h    | Revision ID |
| 3:0 | VENDOR_ID | R    | Ah    | Vendor ID   |

#### 9.4.7 R6 Register (Offset = 6h) [Reset = 24h]

R6 is shown in [Table 9-85](#).

Return to the [Table 9-77](#).

**Table 9-85. R6 Register Field Descriptions**

| Bit | Field  | Type | Reset | Description |
|-----|--------|------|-------|-------------|
| 7:0 | DEV_ID | R    | 24h   | Device ID   |

#### 9.4.8 R7 Register (Offset = 7h) [Reset = 07h]

R7 is shown in [Table 9-86](#).

Return to the [Table 9-77](#).

**Table 9-86. R7 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                 |
|-----|----------|------|-------|-----------------------------|
| 7:5 | RESERVED | R    | 0h    | Reserved                    |
| 4:0 | SMBUS_BC | R/W  | 7h    | SMBUS Block Read Byte Count |

#### 9.4.9 R17 Register (Offset = 11h) [Reset = 66h]

R17 is shown in [Table 9-87](#).

Return to the [Table 9-77](#).

**Table 9-87. R17 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                              |
|-----|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | AMP_BANK1 | R/W  | 6h    | Global Differential output Control, approximately 0.6V to 1V 25mV/step (default = 0.75V)<br>0h = 600 mV<br>1h = 625 mV<br>2h = 650 mV<br>3h = 675 mV<br>4h = 700 mV<br>5h = 725 mV<br>6h = 750 mV<br>7h = 775 mV<br>8h = 800 mV<br>9h = 825 mV<br>Ah = 850 mV<br>Bh = 875 mV<br>Ch = 900 mV<br>Dh = 925 mV<br>Eh = 950 mV<br>Fh = 975 mV |
| 3:0 | AMP_BANK0 | R/W  | 6h    | Global Differential output Control, approximately 0.6V to 1V 25mV/step (default = 0.75V)<br>0h = 600 mV<br>1h = 625 mV<br>2h = 650 mV<br>3h = 675 mV<br>4h = 700 mV<br>5h = 725 mV<br>6h = 750 mV<br>7h = 775 mV<br>8h = 800 mV<br>9h = 825 mV<br>Ah = 850 mV<br>Bh = 875 mV<br>Ch = 900 mV<br>Dh = 925 mV<br>Eh = 950 mV<br>Fh = 975 mV |

#### 9.4.10 R18 Register (Offset = 12h) [Reset = 0Ah]

R18 is shown in [Table 9-88](#).

Return to the [Table 9-77](#).

**Table 9-88. R18 Register Field Descriptions**

| Bit | Field                     | Type | Reset | Description                                                                                                |
|-----|---------------------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 7   | RX_CLKIN1_EN_AC_INP<br>UT | R/W  | 0h    | Enable receiver bias when CLKIN1 is AC coupled<br>0h = DC Coupled Input<br>1h = AC Coupled Input           |
| 6   | RX_CLKIN1_EN_RTERM        | R/W  | 0h    | Enable termination resistors on CLKIN1<br>0h = Input termination inactive<br>1h = Input termination active |
| 5   | RX_CLKIN0_EN_RTERM        | R/W  | 0h    | Enable termination resistors on CLKIN0<br>0h = Input termination inactive<br>1h = Input termination active |
| 4   | RESERVED                  | R    | 0h    | Reserved                                                                                                   |

**Table 9-88. R18 Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                               |
|-----|------------------|------|-------|-----------------------------------------------------------------------------------------------------------|
| 3   | PD_RESTOREB      | R    | 1h    | Save configuration in powerdown<br>0h = Config Cleared<br>1h = Config Saved                               |
| 2   | RESERVED         | R    | 0h    | Reserved                                                                                                  |
| 1   | SDATA_TIMEOUT_EN | R    | 1h    | Enable SMBus SDATA time out monitoring<br>0h = Disable SDATA timeout<br>1h = Enable SDATA timeout         |
| 0   | LOSb_RB          | R    | 0h    | Real time read back of loss detect block output<br>0h = LOS Event Detected<br>1h = LOS Event Not-Detected |

#### 9.4.11 R20 Register (Offset = 14h) [Reset = 28h]

R20 is shown in [Table 9-89](#).

Return to the [Table 9-77](#).

**Table 9-89. R20 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description               |
|-----|-----------------------|------|-------|---------------------------|
| 7:6 | RESERVED              | R    | 0h    | Reserved                  |
| 5   | SLEWRATE_SEL_CLK1_MSB | R/W  | 1h    | MSB CLK1 slew rate select |
| 4   | RESERVED              | R    | 0h    | Reserved                  |
| 3   | SLEWRATE_SEL_CLK0_MSB | R/W  | 1h    | MSB CLK0 slew rate select |
| 2:0 | RESERVED              | R    | 0h    | Reserved                  |

#### 9.4.12 R21 Register (Offset = 15h) [Reset = 14h]

R21 is shown in [Table 9-90](#).

Return to the [Table 9-77](#).

**Table 9-90. R21 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description               |
|-----|-----------------------|------|-------|---------------------------|
| 7:5 | RESERVED              | R    | 0h    | Reserved                  |
| 4   | SLEWRATE_SEL_CLK3_MSB | R/W  | 1h    | MSB CLK3 slew rate select |
| 3   | RESERVED              | R    | 0h    | Reserved                  |
| 2   | SLEWRATE_SEL_CLK2_MSB | R/W  | 1h    | MSB CLK2 slew rate select |
| 1:0 | RESERVED              | R    | 0h    | Reserved                  |

#### 9.4.13 R36 Register (Offset = 24h) [Reset = 09h]

R36 is shown in [Table 9-91](#).

Return to the [Table 9-77](#).

**Table 9-91. R36 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7:4 | RESERVED | R    | 0h    | Reserved    |

**Table 9-91. R36 Register Field Descriptions (continued)**

| Bit | Field             | Type | Reset | Description                                                                                                                                                                               |
|-----|-------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | CLKIN0_AOD_ENABLE | R/W  | 1h    | Enable automatic output disable (AOD) for CLKIN0 to low/low when LOS event is detected. Refer to section "Automatic Output Disable" for more information.<br>0h = Inactive<br>1h = Active |
| 2:0 | RESERVED          | R    | 0h    | Reserved                                                                                                                                                                                  |

#### 9.4.14 R38 Register (Offset = 26h) [Reset = 00h]

R38 is shown in [Table 9-92](#).

Return to the [Table 9-77](#).

**Table 9-92. R38 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                       |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | RESERVED   | R    | 0h    | Reserved                                                                                                                                                                                                                          |
| 0   | WRITE_LOCK | R    | 0h    | Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by recycling power.<br>0h = SMBus Not Locked for Writing<br>1h = SMBus Locked for Writing |

#### 9.4.15 R39 Register (Offset = 27h) [Reset = 00h]

R39 is shown in [Table 9-93](#).

Return to the [Table 9-77](#).

**Table 9-93. R39 Register Field Descriptions**

| Bit | Field           | Type  | Reset | Description                                                                                                                                                                                                           |
|-----|-----------------|-------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | RESERVED        | R     | 0h    | Reserved                                                                                                                                                                                                              |
| 1   | LOS_EVT         | R     | 0h    | LOS Event Status. When high, indicates that a LOS event is detected. Can be cleared by writing a 1.<br>0h = Not LOS Event Detected<br>1h = LOS Event Detected                                                         |
| 0   | WRITE_LOCK_RW1C | R/W1C | 0h    | Clearable SMBus Write Lock bit. When written to one, the SMBus control registers can not be written to. This bit can be cleared by writing a 1.<br>0h = SMBus Not Locked for Writing<br>1h = SMBus Locked for Writing |

#### 9.4.16 R43 Register (Offset = 2Bh) [Reset = 00h]

R43 is shown in [Table 9-94](#).

Return to the [Table 9-77](#).

**Table 9-94. R43 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                   |
|-----|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | RESERVED  | R    | 0h    | Reserved                                                                                                                                                                      |
| 5:4 | CLKIN_SEL | R/W  | 0h    | CLKIN Source Select<br>0h = All outputs come from CLKIN0<br>1h = CLKIN0 inputs go to BANK0 and CLKIN1 inputs go to BANK1<br>2h = Invalid<br>3h = All outputs come from CLKIN1 |

**Table 9-94. R43 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 3:0 | RESERVED | R    | 0h    | Reserved    |

#### 9.4.17 R91 Register (Offset = 5Bh) [Reset = 60h]

R91 is shown in [Table 9-95](#).

Return to the [Table 9-77](#).

**Table 9-95. R91 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | SLEWRATE_OPT_2 | R/W  | 6h    | There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 2nd option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0 (fastest)<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 (slowest) |
| 3:0 | SLEWRATE_OPT_1 | R/W  | 0h    | There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 1st option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0 (fastest)<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 (slowest) |

#### 9.4.18 R92 Register (Offset = 5Ch) [Reset = FAh]

R92 is shown in [Table 9-96](#).

Return to the [Table 9-77](#).

**Table 9-96. R92 Register Field Descriptions**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | SLEWRATE_OPT_4 | R/W  | Fh    | There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 4th option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0 (fastest)<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 (slowest) |
| 3:0 | SLEWRATE_OPT_3 | R/W  | Ah    | There are four register assignments each storing a slew rate value (chosen out of the 16 available slew rate values). This register bits relate to the 3rd option. Go to Programmable Output Slew Rate section for more information.<br>0h = 0 (fastest)<br>1h = 1<br>2h = 2<br>3h = 3<br>4h = 4<br>5h = 5<br>6h = 6<br>7h = 7<br>8h = 8<br>9h = 9<br>Ah = 10<br>Bh = 11<br>Ch = 12<br>Dh = 13<br>Eh = 14<br>Fh = 15 (slowest) |

#### 9.4.19 R93 Register (Offset = 5Dh) [Reset = 00h]

R93 is shown in [Table 9-97](#).

Return to the [Table 9-77](#).

**Table 9-97. R93 Register Field Descriptions**

| Bit | Field                     | Type | Reset | Description                                                                                      |
|-----|---------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 7:1 | RESERVED                  | R    | 0h    | Reserved                                                                                         |
| 0   | RX_CLKIN0_EN_AC_INP<br>UT | R/W  | 0h    | Enable receiver bias when CLKIN0 is AC coupled<br>0h = DC Coupled Input<br>1h = AC Coupled Input |

#### 9.4.20 R98 Register (Offset = 62h) [Reset = 00h]

R98 is shown in [Table 9-98](#).

Return to the [Table 9-77](#).

**Table 9-98. R98 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description                |
|-----|-----------------------|------|-------|----------------------------|
| 7:6 | RESERVED              | R    | 0h    | Reserved                   |
| 5   | SLEWRATE_SEL_CLK2_LSB | R/W  | 0h    | LSB CLK2 Slew Rate Control |
| 4   | SLEWRATE_SEL_CLK3_LSB | R/W  | 0h    | LSB CLK3 Slew Rate Control |
| 3:0 | RESERVED              | R    | 0h    | Reserved                   |

#### 9.4.21 R99 Register (Offset = 63h) [Reset = 00h]

R99 is shown in [Table 9-99](#).

Return to the [Table 9-77](#).

**Table 9-99. R99 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description                |
|-----|-----------------------|------|-------|----------------------------|
| 7   | RESERVED              | R    | 0h    | Reserved                   |
| 6   | SLEWRATE_SEL_CLK0_LSB | R/W  | 0h    | LSB CLK0 Slew Rate Control |
| 5:3 | RESERVED              | R    | 0h    | Reserved                   |
| 2   | SLEWRATE_SEL_CLK1_LSB | R/W  | 0h    | LSB CLK1 Slew Rate Control |
| 1:0 | RESERVED              | R    | 0h    | Reserved                   |

## 10 Application and Implementation

### Note

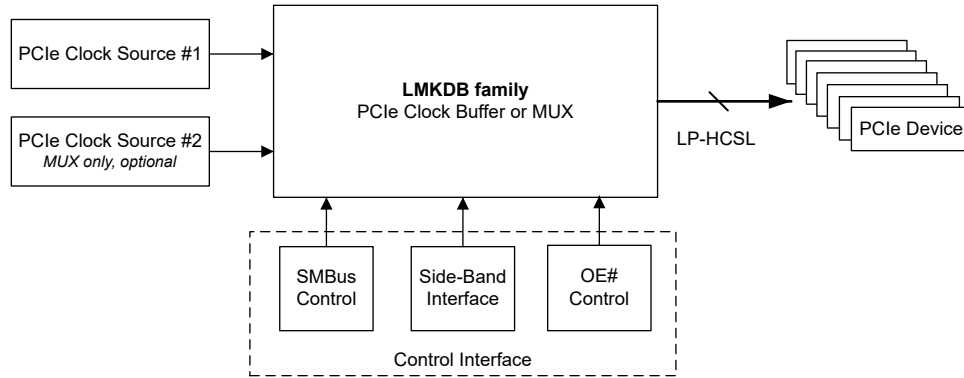
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 10.1 Application Information

The LMKDB devices are a family of ultra-low additive jitter LP-HCSL clock buffers and clock MUX. The device can be controlled through SMBus registers, Side Band Interface, and OE# pins.

### 10.2 Typical Application

This example shows PCIe and Ethernet clock distribution. Provide multiple copies of PCIe clocks (100 MHz) or Ethernet clocks (156.25 MHz) based on the given source.



**Figure 10-1. Typical Application**

### 10.2.1 Design Requirements

Find two buffers for PCIe clock fan-out and Ethernet clock fan-out separately. Jitter requirements must be met and space must be minimized.

**Table 10-1. Design Parameters**

| PARAMETER                                            | VALUE             |
|------------------------------------------------------|-------------------|
| Number of PCIe clocks                                | 15                |
| Number of 156.25 MHz Ethernet clocks                 | 7                 |
| PCIe architecture                                    | CC (Common Clock) |
| PCIe reference clock slew rate                       | $\geq 3.5$ V/ns   |
| PCIe Gen 5 reference clock jitter                    | 45 fs maximum     |
| PCIe Gen 5 total jitter                              | 50 fs maximum     |
| 156.25-MHz reference clock slew rate                 | $\geq 3.5$ V/ns   |
| 156.25-MHz reference clock jitter (12 kHz to 20 MHz) | 90 fs maximum     |
| 156.25-MHz total jitter (12 kHz to 20 MHz)           | 100 fs maximum    |

### 10.2.2 Detailed Design Procedure

First of all, calculate the jitter budget for the clock buffer using RMS addition. The maximum allowed additive jitter for the clock buffer is square root of the difference between square of reference clock jitter and square of total clock jitter.

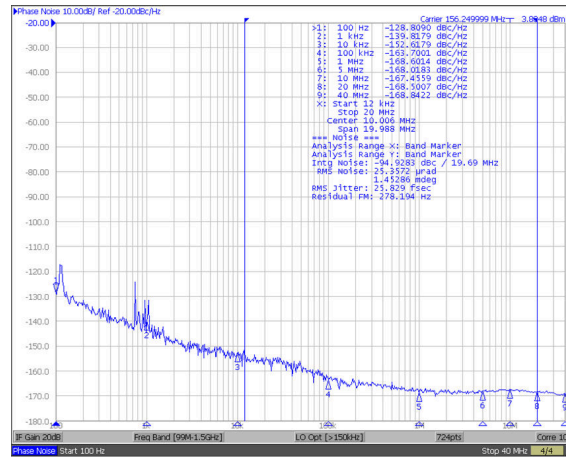
The maximum PCIe Gen 5 additive jitter allowed for the buffer is  $\sqrt{50^2 - 45^2} = 21$  fs. According to the [Specifications](#) under the *Electrical Characteristics* table, the additive PCIe Gen 5 jitter under Common Clock and  $\geq 3.5$  V/ns input slew rate test condition is 13 fs maximum, well below 21 fs requirement. Therefore, the LMKDB1120 (20 outputs) can be used for PCIe Gen 5 clock distribution.

Similarly, the maximum 12 kHz to 20 MHz additive jitter allowed at 156.25 MHz is  $\sqrt{100^2 - 90^2} = 43$  fs. According to the [Specifications](#) under the *Electrical Characteristics* table, the 12 kHz to 20 MHz additive jitter at 156.25 MHz is 31 fs maximum, well below the 43 fs requirement. Therefore, the LMKDB1108 (8 outputs) can be used for Ethernet clock distribution.

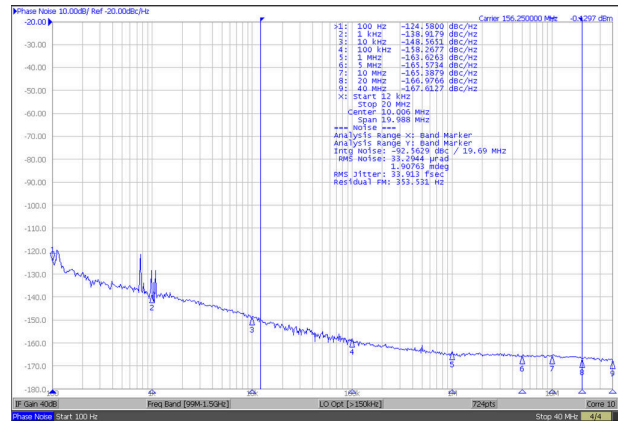
### 10.2.3 Application Curves

The following plots are example phase noise plots before and after using the LMKDB at 156.25 MHz, respectively. The LMKDB clock buffer adds a 22-fs (typical) jitter from 12 kHz to 20 MHz. All LMKDB devices have very similar performance.

To better understand jitter and how the additive jitter of the LMKDB resulted in 22-fs refer to [Timing is Everything: How to measure additive jitter](#) TI blog post.



**Figure 10-2. Input Source at 156.25MHz (12kHz - 20MHz)**



See Note 1 and 2 in Graph Notes table

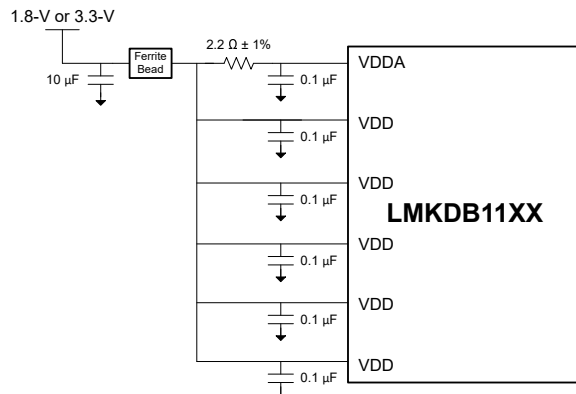
**Figure 10-3. LMKDB11xx/120x Phase Noise / Output Jitter at 156.25MHz (12kHz - 20MHz)**

**Table 10-2. Graph Notes**

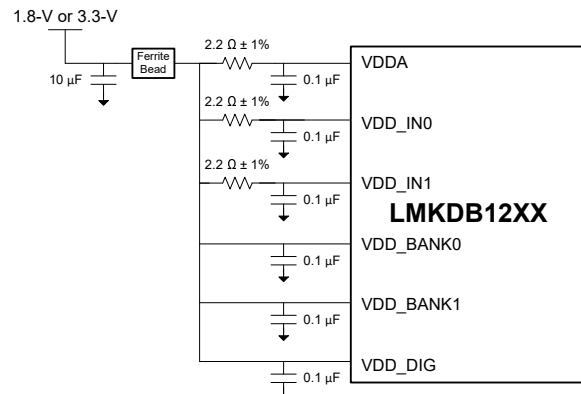
| NOTE |                                                                                                                                                                                                                                                                                     |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| (1)  | The typical RMS jitter values in the plots show the total output RMS jitter ( $J_{OUT}$ ) for each frequency and the source clock RMS jitter ( $J_{SOURCE}$ ). From these values, the Additive RMS Jitter can be calculated as: $J_{ADD} = \text{SQRT}(J_{OUT}^2 - J_{SOURCE}^2)$ . |
| (2)  | $J_{ADD}$ at 156.25MHz = $\text{SQRT}(33.9^2 - 25.8^2) = 22.0$ fs                                                                                                                                                                                                                   |

### 10.3 Power Supply Recommendations

Place a 0.1-μF capacitor close to every power supply pin. To minimize noise on VDDA, VDD\_IN0 and VDD\_IN1, place a 2.2-Ω resistor next to the pins. All supply pins can be grouped onto one power rail. TI recommends a Ferrite Bead and a 10-μF capacitor to GND for the entire chip. Figure 10-4 and Figure 10-5 shows an example power schematic.



**Figure 10-4. Power Supply Recommendation for LMKDB11XX Buffer**



**Figure 10-5. Power Supply Recommendation for LMKDB12XX MUX**

If both inputs are used for a MUX device and the two inputs have different frequencies (including PCIe SSC and PCIe No SSC), then isolate the inputs and corresponding output banks by adding more Ferrite Beads.

## 10.4 Layout

### 10.4.1 Layout Guidelines

Use a low-inductance ground connection between the device DAP and the PCB.

Match PCB trace impedance with device output impedance (85- $\Omega$  or 100- $\Omega$  differential impedance). Eliminate stubs and reduce discontinuity on the transmission lines.

### 10.4.2 Layout Example

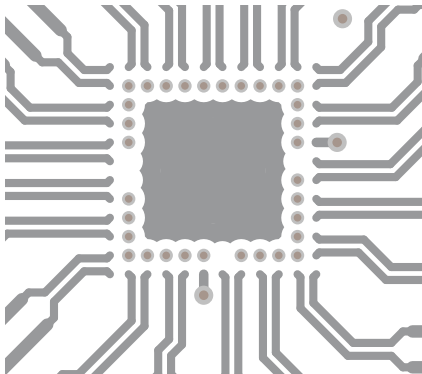


Figure 10-6. LMKDB1120 Layout Example - Top Layer

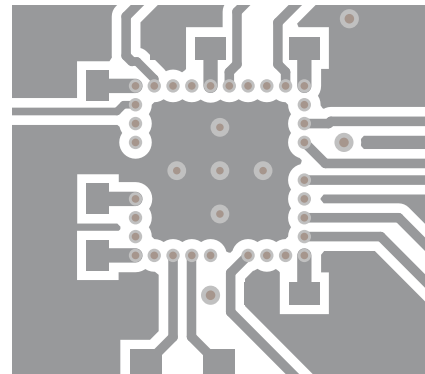


Figure 10-7. LMKDB1120 Layout Example - Bottom Layer

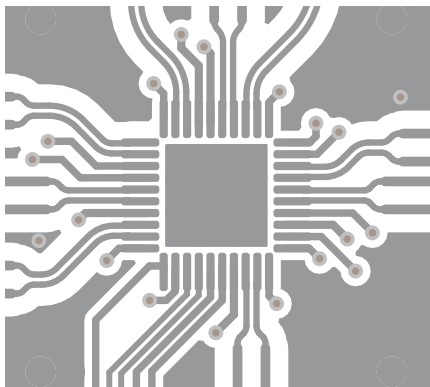


Figure 10-8. LMKDB1108 Layout Example - Top Layer

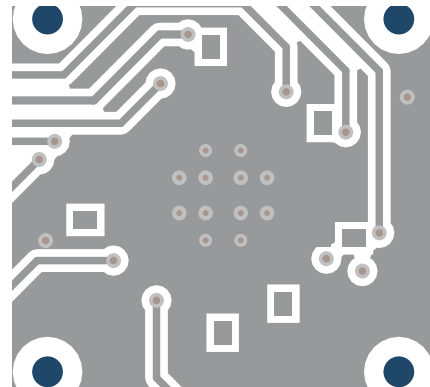


Figure 10-9. LMKDB1108 Layout Example - Bottom Layer

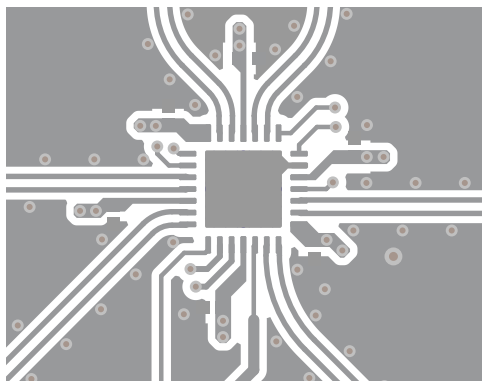


Figure 10-10. LMKDB1204 Layout Example - Top Layer

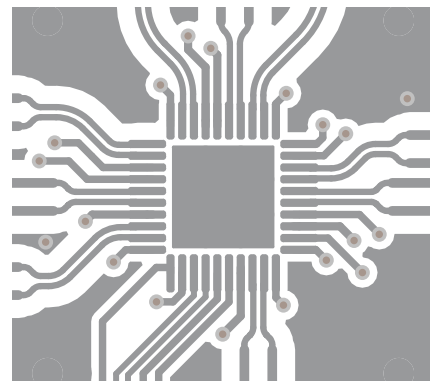
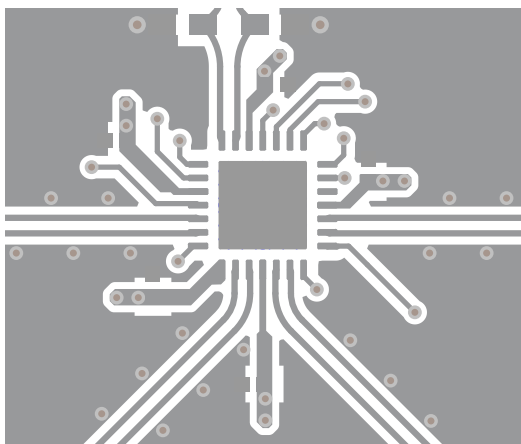
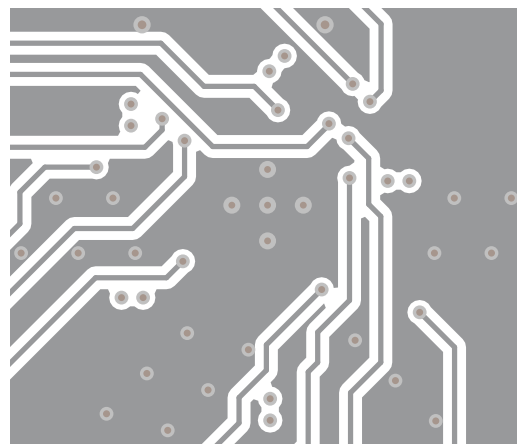


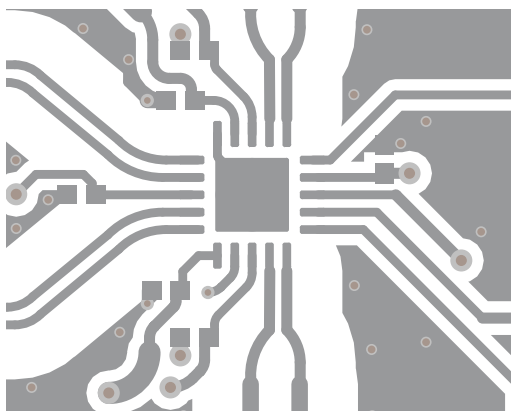
Figure 10-11. LMKDB1204 Layout Example - Bottom Layer



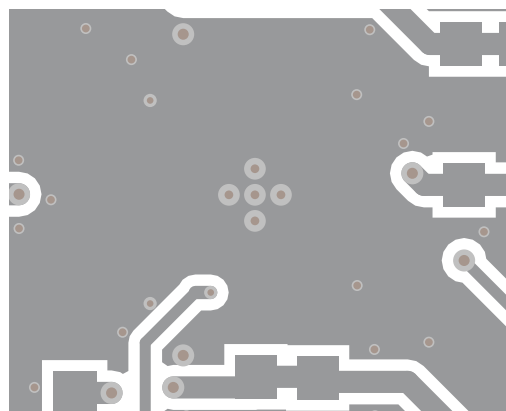
**Figure 10-12. LMKDB1104 Layout Example - Top Layer**



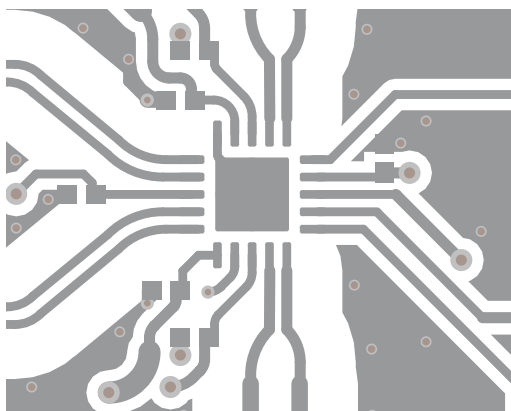
**Figure 10-13. LMKDB1104 Layout Example - Bottom Layer**



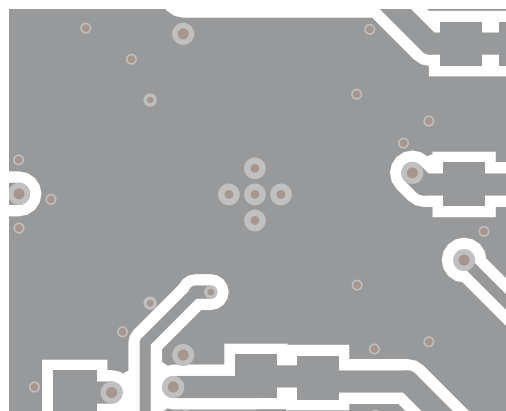
**Figure 10-14. LMKDB1202 Layout Example - Top Layer**



**Figure 10-15. LMKDB1202 Layout Example - Bottom Layer**



**Figure 10-16. LMKDB1102 Layout Example - Top Layer**



**Figure 10-17. LMKDB1102 Layout Example - Bottom Layer**

## 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [LMKDB1120 Evaluation Module](#), user's guide
- Texas Instruments, [LMKDB1108 Evaluation Module](#), user's guide
- Texas Instruments, [LMKDB1104 Evaluation Module](#), user's guide
- Texas Instruments, [LMKDB1204 Evaluation Module](#), user's guide
- Texas Instruments, [LMKDB1102/1202 Evaluation Module](#), user's guide
- Texas Instruments, [Timing is Everything: How to measure additive jitter](#), blog post

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (May 2024) to Revision D (June 2024)                                                 | Page |
|--------------------------------------------------------------------------------------------------------------|------|
| • Updated the number format for tables, figures, and cross-references throughout the document.....           | 1    |
| • Updated R17 register 7:4 name to "AMP" to match GUI name for LMKDB1108:.....                               | 1    |
| • Updated R18 table to stack Reserved bits 5:4 in one row for LMKDB1108.....                                 | 1    |
| • Exposed registers R5 to change REV_ID for LMKDB1108.....                                                   | 1    |
| • Exposed R91 and R92 to show output slew rate control for LMKDB1108.....                                    | 1    |
| • Corrected register names that control correct outputs of chip (R0, R1, R2, R3, R20, R21) for LMKDB1204.... | 1    |
| • Updated ^vSADR1_tri to ^vSADR0_tri for pin 4 in <a href="#">Figure 5-2</a> .....                           | 3    |

|                                                                                                                                                              |    |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| • Updated pin 7 name and description from "VDD" to "VDDA" in <a href="#">Figure 5-2</a> .....                                                                | 3  |
| • Updated pin 10 name and description from "VDDA" to "VDD" in <a href="#">Figure 5-2</a> .....                                                               | 3  |
| • Updated functional block diagram <a href="#">Figure 8-2</a> to fix HW_SW_CTRL pin naming to SMB_EN. Changed the structure of functional block diagram..... | 26 |
| • Updated functional block diagram <a href="#">Figure 8-2</a> to fix HW_SW_CTRL pin naming to SMB_EN.....                                                    | 26 |
| • Changed the structure of functional block diagram.....                                                                                                     | 26 |
| • Added pin mode description in the <a href="#">Section 8.3.4.3</a> section.....                                                                             | 30 |
| • Added layout examples for LMKDB1102, LMKDB1202, LMKDB1104, LMKDB1204 and LMKDB1108.....                                                                    | 78 |

| <b>Changes from Revision B (February 2024) to Revision C (May 2024)</b>                            | <b>Page</b> |
|----------------------------------------------------------------------------------------------------|-------------|
| • Updated the number format for tables, figures, and cross-references throughout the document..... | 1           |
| • Deleted preview information from LMKDB1204 rows in the <i>Device Comparison</i> table.....       | 2           |
| • Updated ^vSADR1_tri to ^vSADR0_tri for pin 4 in <a href="#">LMKDB1108 Pin Functions</a> .....    | 3           |
| • Added <a href="#">Input Configurations</a> section. ....                                         | 27          |
| • Added <a href="#">Table 8-1</a> .....                                                            | 29          |

| <b>Changes from Revision A (December 2023) to Revision B (February 2024)</b>                                                                                                              | <b>Page</b> |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Updated the number format for tables, figures, and cross-references throughout the document.....                                                                                        | 1           |
| • Added additional explanations for recommended PWRDN# assertion/deassertion sequences and effects when not followed properly in the <i>PWRDN# Assertion and Deassertion</i> section..... | 28          |

| <b>Changes from Revision * (November 2023) to Revision A (December 2023)</b>                       | <b>Page</b> |
|----------------------------------------------------------------------------------------------------|-------------|
| • Updated the number format for tables, figures, and cross-references throughout the document..... | 1           |

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMKDB1102REYR     | ACTIVE        | VQFN         | REY             | 20   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | DB1102                  | <a href="#">Samples</a> |
| LMKDB1102REYT     | ACTIVE        | VQFN         | REY             | 20   | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | DB1102                  | <a href="#">Samples</a> |
| LMKDB1104Z85REXR  | ACTIVE        | VQFN         | REX             | 28   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | LMKDB<br>1104Z85        | <a href="#">Samples</a> |
| LMKDB1104Z85REXT  | ACTIVE        | VQFN         | REX             | 28   | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | LMKDB<br>1104Z85        | <a href="#">Samples</a> |
| LMKDB1108Z100RKPR | ACTIVE        | VQFN         | RKP             | 40   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | LMKDB<br>108Z100        | <a href="#">Samples</a> |
| LMKDB1108Z100RKPT | ACTIVE        | VQFN         | RKP             | 40   | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | LMKDB<br>108Z100        | <a href="#">Samples</a> |
| LMKDB1108Z85RKPR  | ACTIVE        | VQFN         | RKP             | 40   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | LMKDB<br>1108Z85        | <a href="#">Samples</a> |
| LMKDB1108Z85RKPT  | ACTIVE        | VQFN         | RKP             | 40   | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | LMKDB<br>1108Z85        | <a href="#">Samples</a> |
| LMKDB1120Z100NPPR | ACTIVE        | TLGA         | NPP             | 80   | 2500        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 105   | LMKDB<br>1120Z100       | <a href="#">Samples</a> |
| LMKDB1120Z100NPPT | ACTIVE        | TLGA         | NPP             | 80   | 250         | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 105   | LMKDB<br>1120Z100       | <a href="#">Samples</a> |
| LMKDB1120Z85NPPR  | ACTIVE        | TLGA         | NPP             | 80   | 2500        | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 105   | LMKDB<br>1120Z85        | <a href="#">Samples</a> |
| LMKDB1120Z85NPPT  | ACTIVE        | TLGA         | NPP             | 80   | 250         | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 105   | LMKDB<br>1120Z85        | <a href="#">Samples</a> |
| LMKDB1202REYR     | ACTIVE        | VQFN         | REY             | 20   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | DB1202                  | <a href="#">Samples</a> |
| LMKDB1202REYT     | ACTIVE        | VQFN         | REY             | 20   | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | DB1202                  | <a href="#">Samples</a> |
| LMKDB1204REXR     | ACTIVE        | VQFN         | REX             | 28   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | LMKDB<br>1204           | <a href="#">Samples</a> |
| LMKDB1204REXT     | ACTIVE        | VQFN         | REX             | 28   | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | LMKDB<br>1204           | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

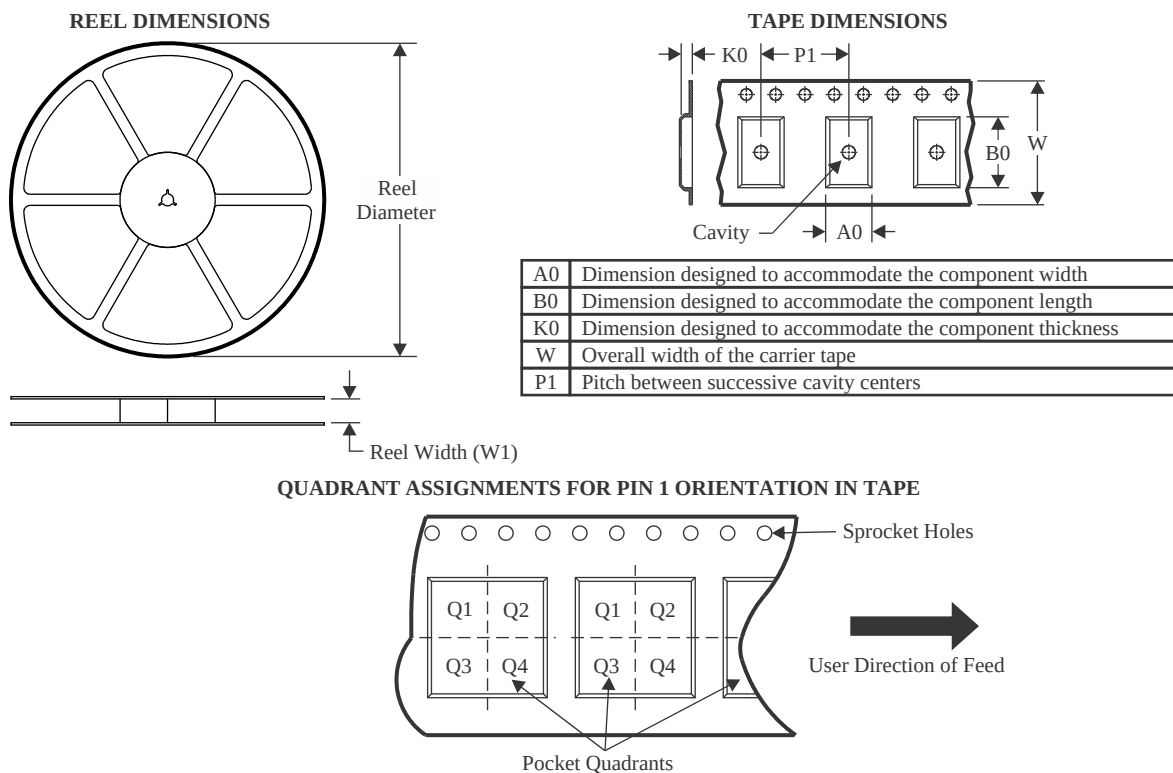
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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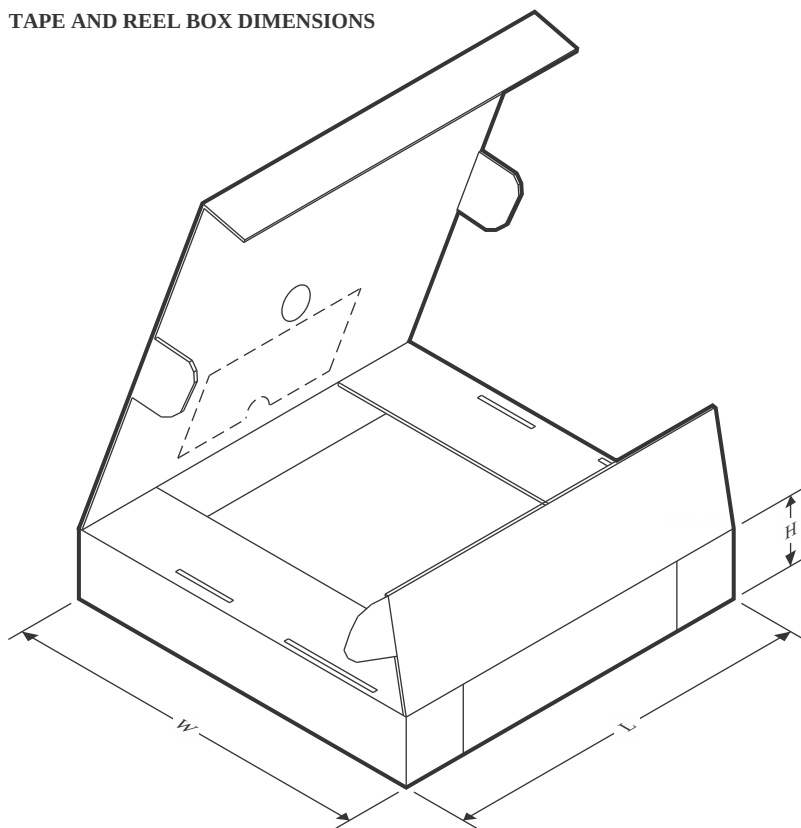
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMKDB1108Z100RKPR | VQFN         | RKP             | 40   | 2500 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| LMKDB1108Z100RKPT | VQFN         | RKP             | 40   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| LMKDB1108Z85RKPR  | VQFN         | RKP             | 40   | 2500 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| LMKDB1108Z85RKPT  | VQFN         | RKP             | 40   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| LMKDB1120Z100NPPR | TLGA         | NPP             | 80   | 2500 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| LMKDB1120Z100NPPT | TLGA         | NPP             | 80   | 250  | 180.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| LMKDB1120Z85NPPR  | TLGA         | NPP             | 80   | 2500 | 180.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| LMKDB1120Z85NPPT  | TLGA         | NPP             | 80   | 250  | 180.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| LMKDB1204REXR     | VQFN         | REX             | 28   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| LMKDB1204REXT     | VQFN         | REX             | 28   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

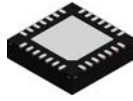
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMKDB1108Z100RKPR | VQFN         | RKP             | 40   | 2500 | 367.0       | 367.0      | 35.0        |
| LMKDB1108Z100RKPT | VQFN         | RKP             | 40   | 250  | 210.0       | 185.0      | 35.0        |
| LMKDB1108Z85RKPR  | VQFN         | RKP             | 40   | 2500 | 367.0       | 367.0      | 35.0        |
| LMKDB1108Z85RKPT  | VQFN         | RKP             | 40   | 250  | 210.0       | 185.0      | 35.0        |
| LMKDB1120Z100NPPR | TLGA         | NPP             | 80   | 2500 | 367.0       | 367.0      | 38.0        |
| LMKDB1120Z100NPPT | TLGA         | NPP             | 80   | 250  | 210.0       | 185.0      | 35.0        |
| LMKDB1120Z85NPPR  | TLGA         | NPP             | 80   | 2500 | 210.0       | 185.0      | 35.0        |
| LMKDB1120Z85NPPT  | TLGA         | NPP             | 80   | 250  | 210.0       | 185.0      | 35.0        |
| LMKDB1204REXR     | VQFN         | REX             | 28   | 3000 | 367.0       | 367.0      | 35.0        |
| LMKDB1204REXT     | VQFN         | REX             | 28   | 250  | 210.0       | 185.0      | 35.0        |

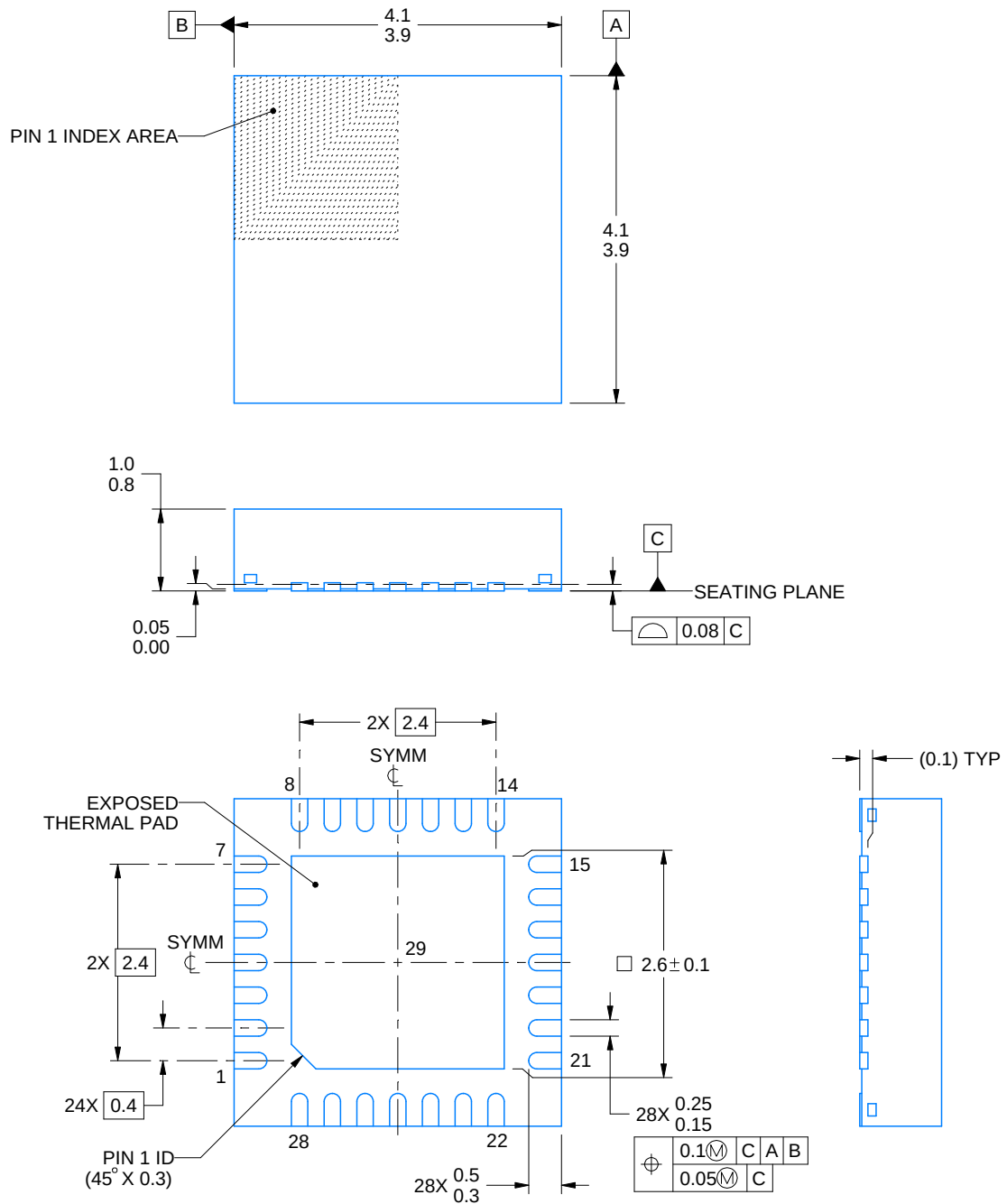
REX0028A



## PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4229744/A 06/2023

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

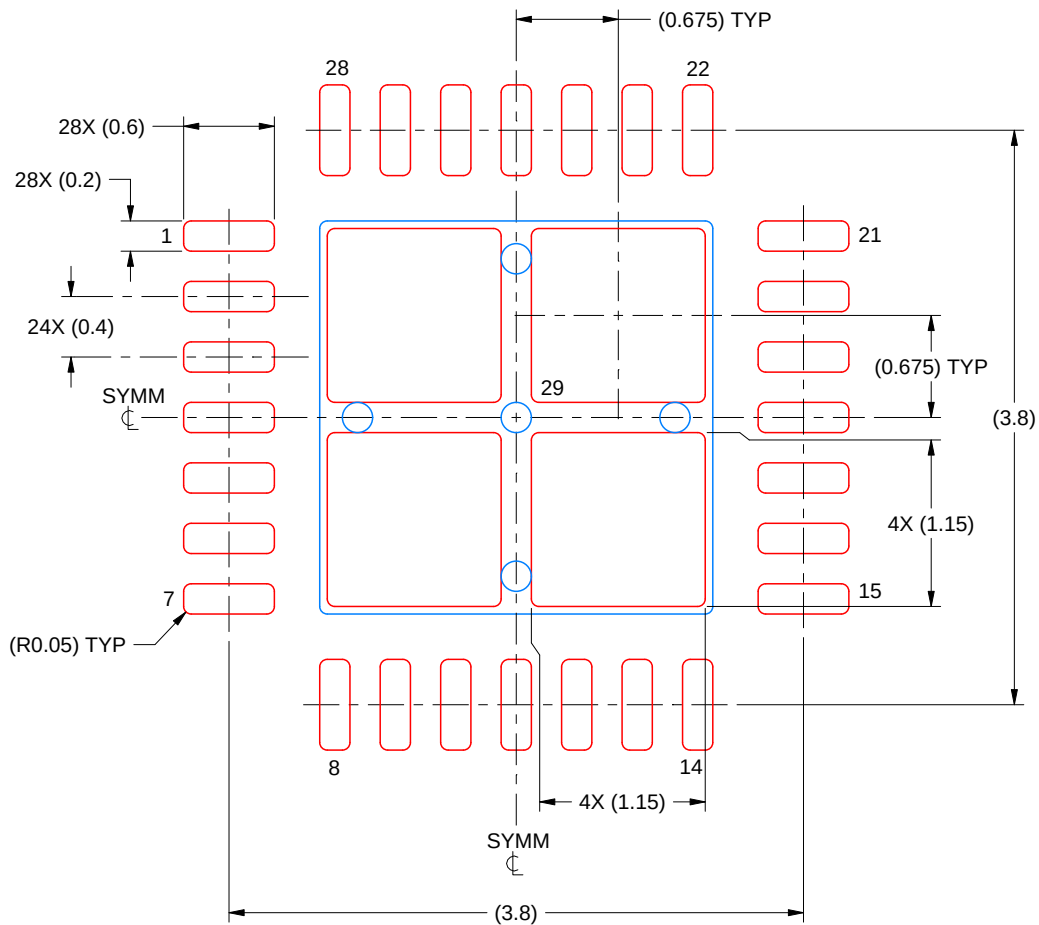


# EXAMPLE STENCIL DESIGN

REX0028A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



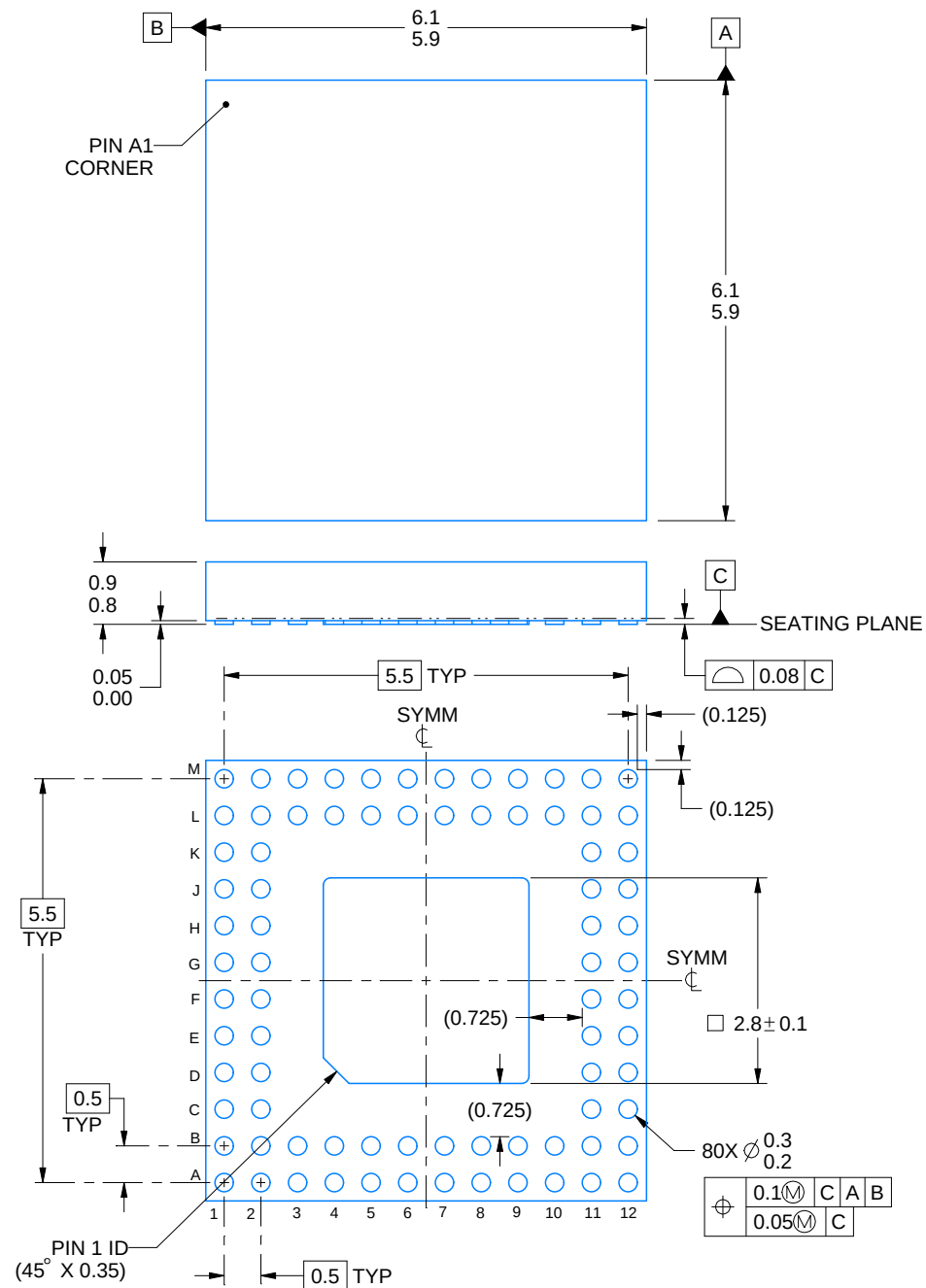
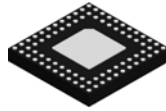
SOLDER PASTE EXAMPLE  
BASED ON 0.1 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 29  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229744/A 06/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4224877/A 03/2019

## NOTES:

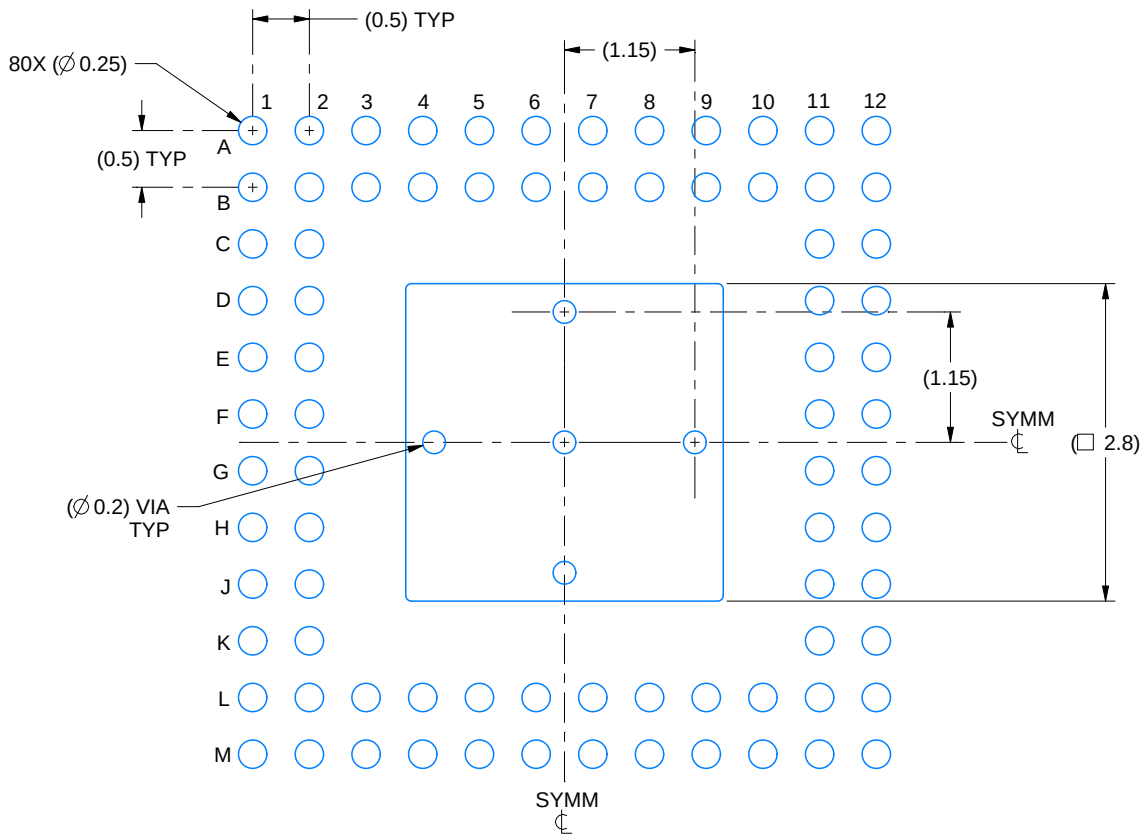
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

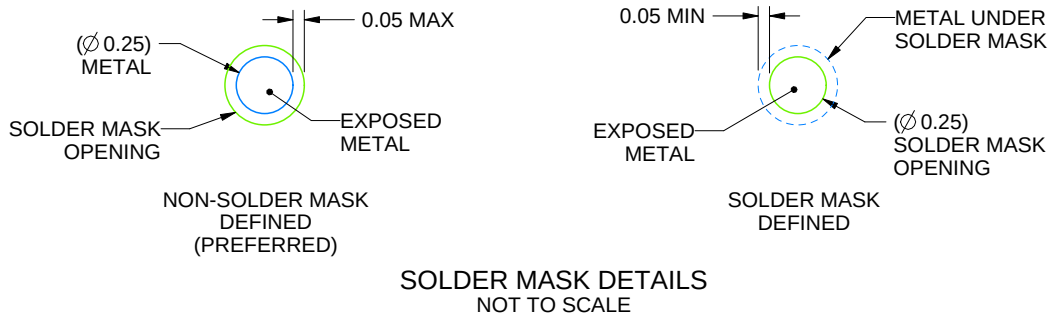
NPP0080A

TLGA - 0.9 mm max height

THIN LAND GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS  
NOT TO SCALE

4224877/A 03/2019

NOTES: (continued)

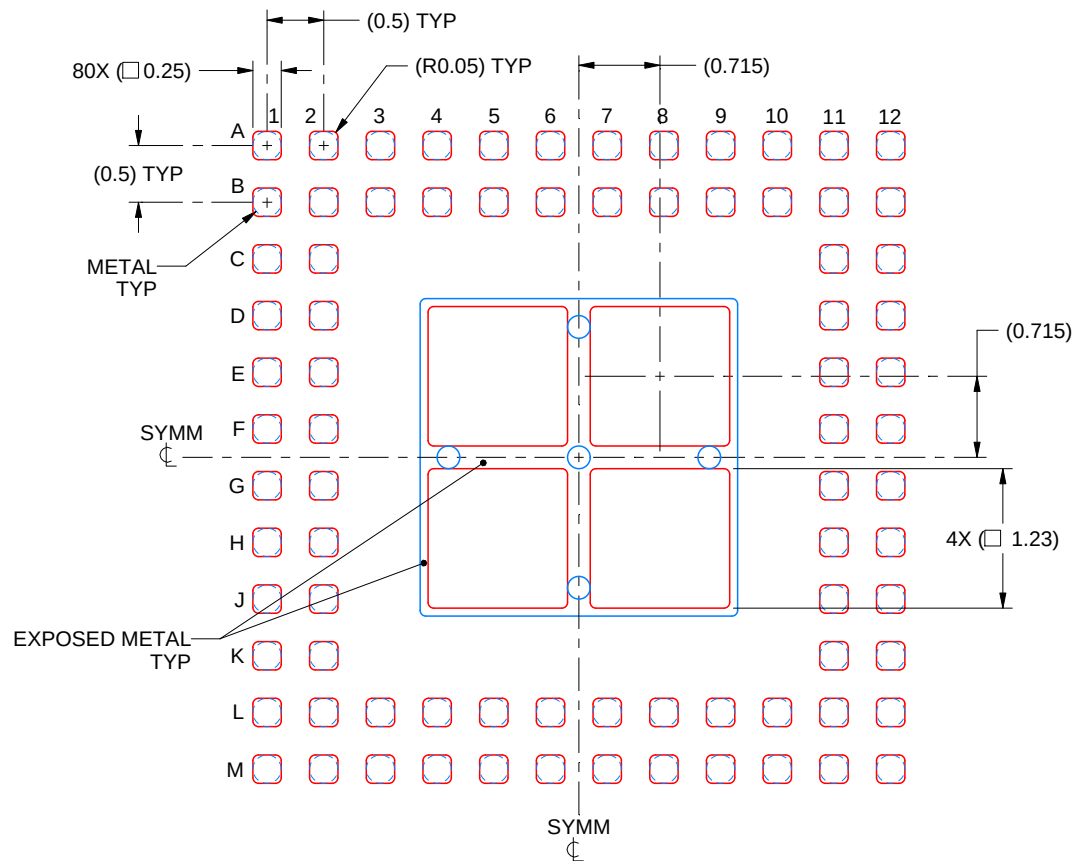
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

NPP0080A

TLGA - 0.9 mm max height

THIN LAND GRID ARRAY

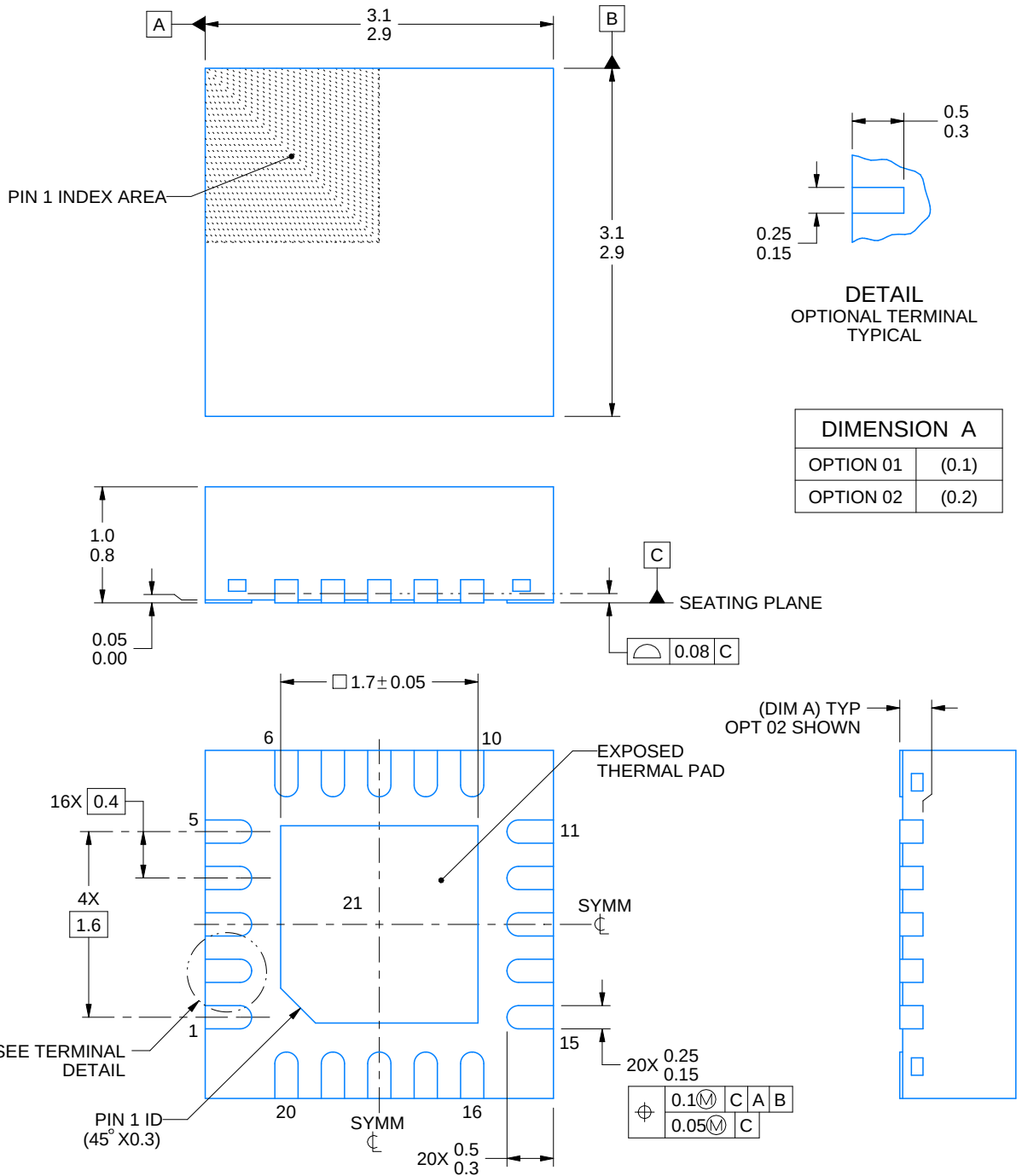
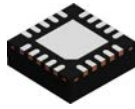


SOLDER PASTE EXAMPLE  
 BASED ON 0.1 mm THICK STENCIL  
 SCALE: 15X

4224877/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4229745/A 06/2023

NOTES:

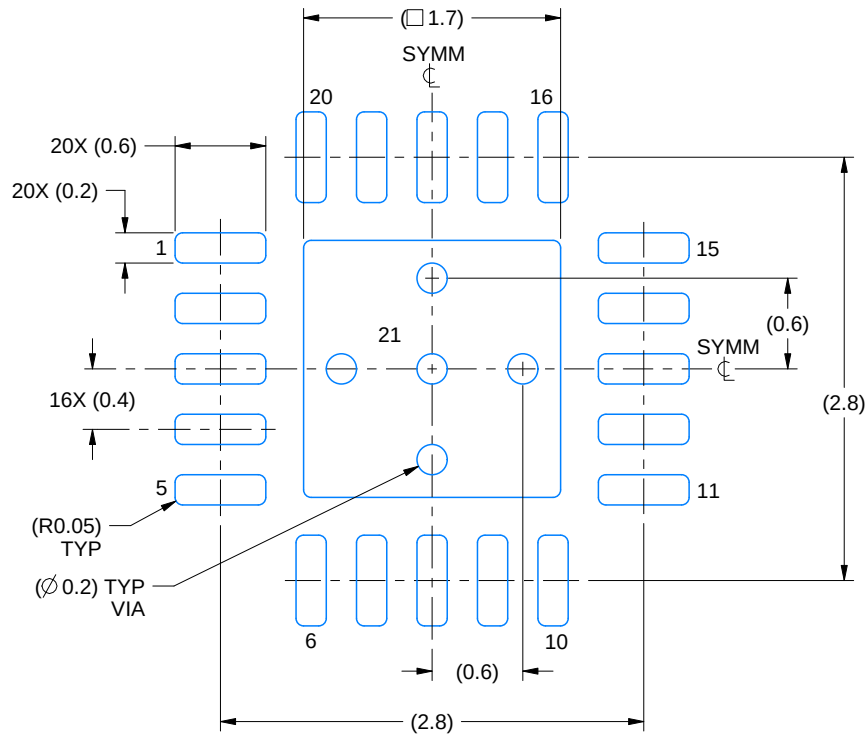
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

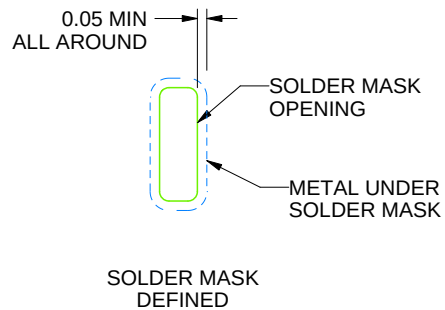
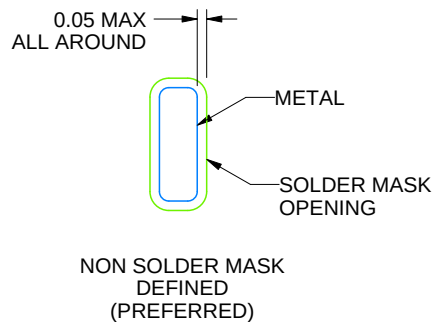
REY0020B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4229745/A 06/2023

NOTES: (continued)

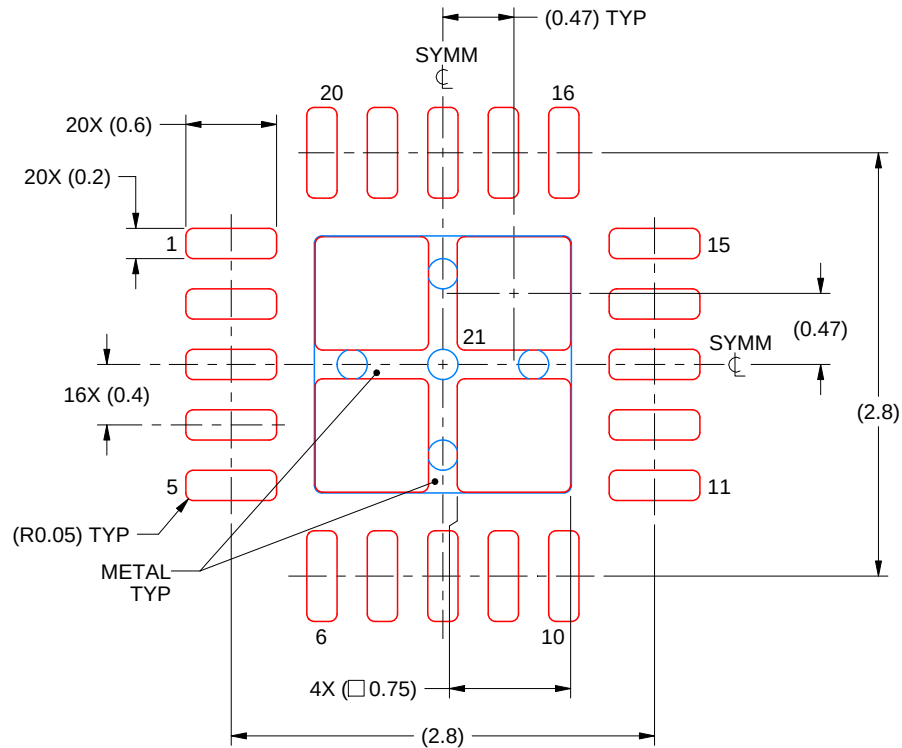
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

REY0020B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4229745/A 06/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

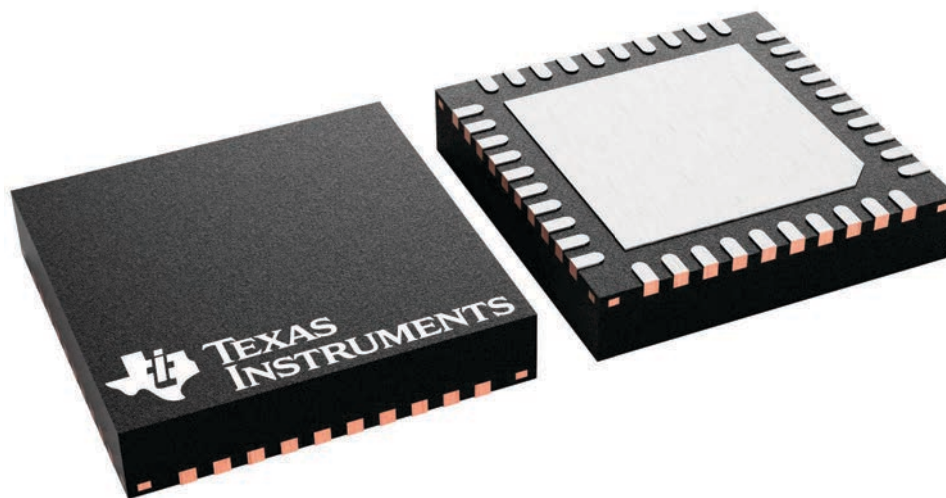
**RKP 40**

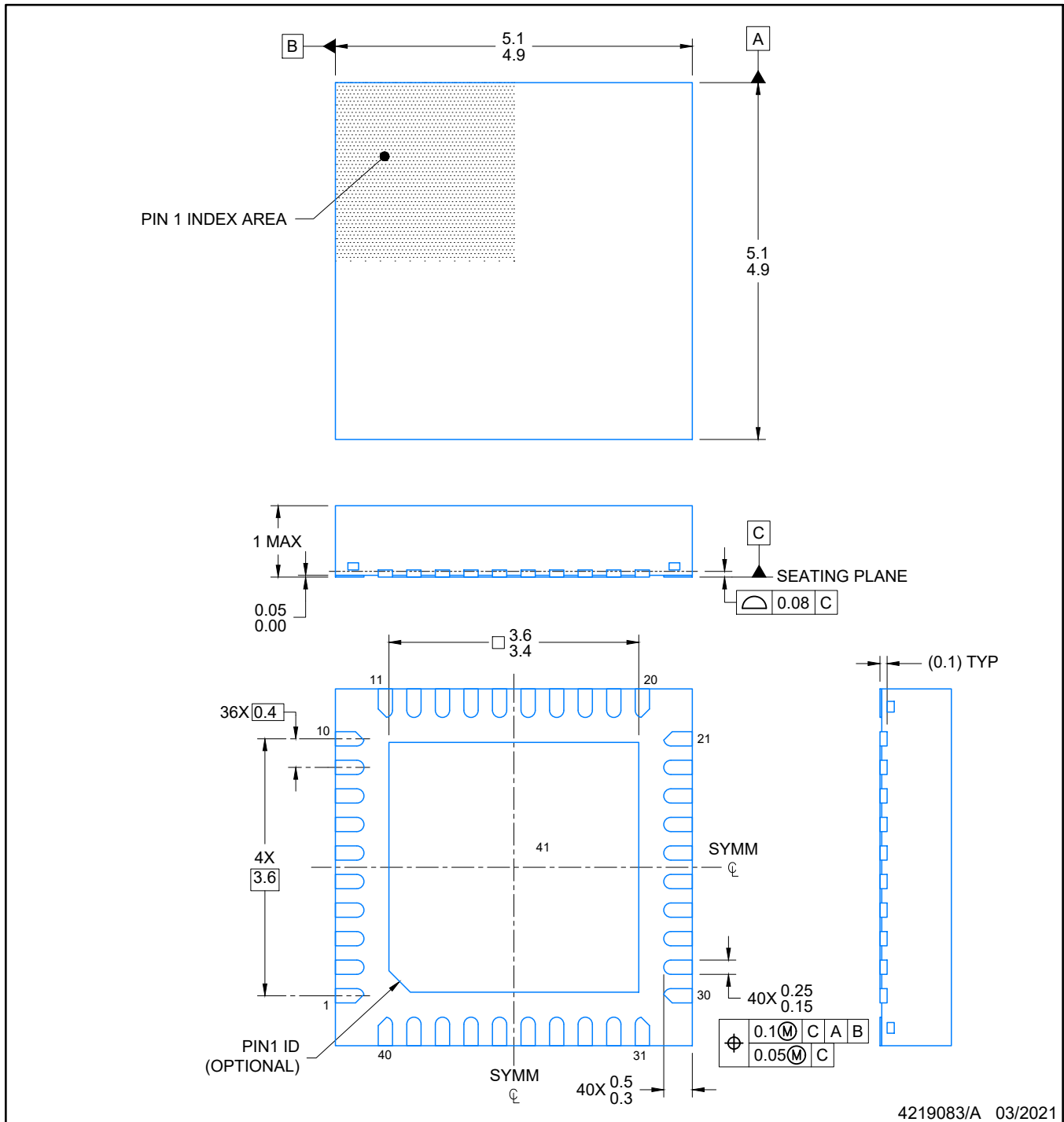
**VQFN - 1 mm max height**

5 x 5, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





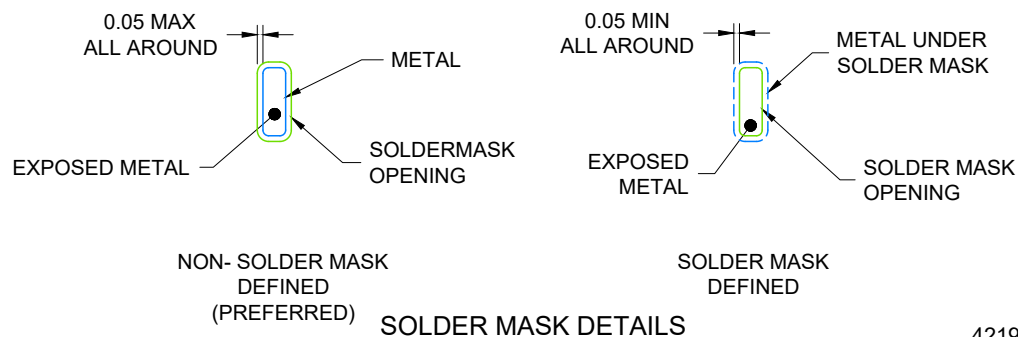
4219083/A 03/2021

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

## VQFN - 1 mm max height

SCALE: 15X

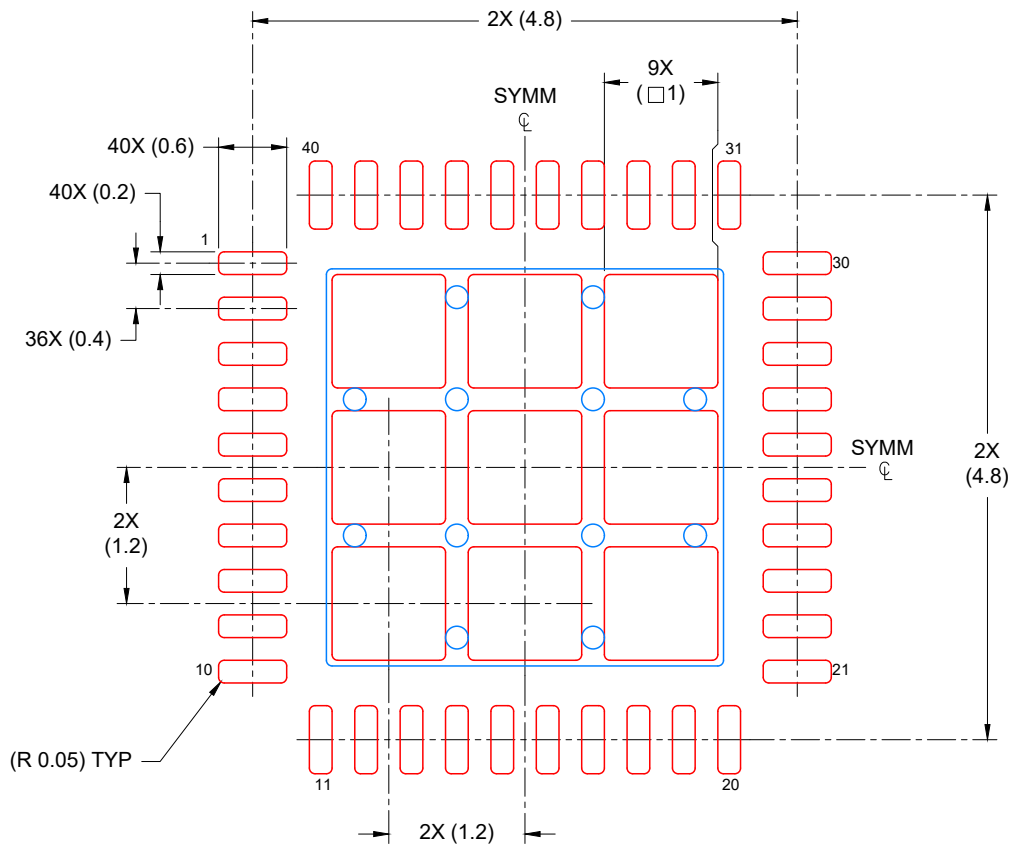


# EXAMPLE STENCIL DESIGN

RKP0040B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
74% PRINTED COVERAGE BY AREA  
SCALE: 15X

4219083/A 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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