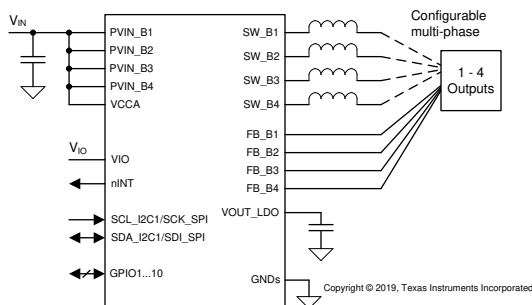


LP8769-Q1 高频四路直流/直流降压转换器

1 特性

- 具有符合 AEC-Q100 标准的下列特性：
 - 输入电压：2.8 V 至 5.5V
 - 器件温度等级 1：-40°C 至 +125°C 环境温度范围
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C4B
- 符合功能安全标准
 - 专为功能安全应用开发
 - 有助于使 ISO 26262 系统设计符合 ASIL-D 要求的文档
 - 有助于使 IEC 61508 系统设计符合 SIL-3 要求的文档
 - 系统可满足 ASIL D 级要求
 - 硬件完整性高达 ASIL-D 级
 - 窗口式电压和过流监控器
 - 具有可选触发/Q&A 模式的看门狗
 - 电平或 PWM 错误信号监控 (ESM)
 - 具有高温警告和热关断功能的温度监测
 - 对配置寄存器和非易失性存储器的位完整性 (CRC) 错误检测
- 4 个高效直流/直流降压转换器：
 - 输出电压：0.3V 至 3.34V (多相位输出的电压为 0.3V 至 1.9V)
 - 最大输出电流：每相位 5A，四相配置最高可达 20A
 - 可编程输出电压压摆率：0.5 mV/μs 至 33 mV/μs
 - 开关频率：2.2 MHz 或 4.4 MHz
- 10 个可配置通用 I/O (GPIO)
- SPMI 接口支持多个 PMIC 同步
- 输入过压监控 (OVP) 和欠压锁定 (UVLO)



简化版原理图

2 应用

- 高级驾驶辅助系统 (ADAS)
- 前置摄像头
- 环视系统 ECU
- 远距离雷达
- 传感器融合
- 域控制器

3 说明

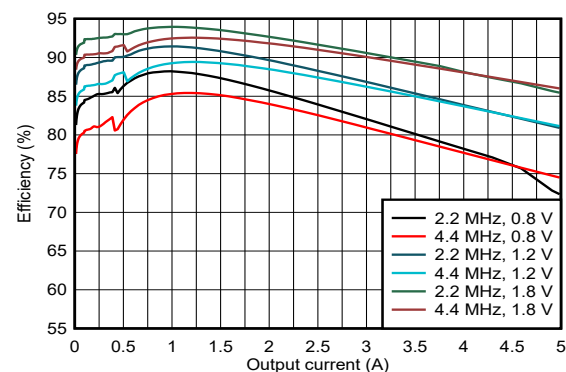
LP8769x-Q1 器件旨在满足各种安全相关的汽车和工业应用中新型处理器和平台的电源管理要求。该器件具有 4 个直流/直流降压转换器内核，可配置为从 1 个四相输出到 4 个单相输出的五种不同相位配置。该器件设置可通过兼容 I²C 的串行接口或 SPI 串行接口进行更改。

自动 PFM/PWM (AUTO 模式) 操作与自动相位增加和相位减少相结合，可在较宽输出电流范围内最大限度地提高效率。LP8769x-Q1 器件支持对多相位输出的远程差分电压检测，可补偿稳压器输出与负载点 (POL) 之间的 IR 压降，从而提高输出电压的精度。开关时钟可以强制进入 PWM 模式，并且相位会交错。可以将开关与外部时钟同步并启用展频模式，以最大限度地降低干扰。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
LP8769-Q1	VQFN-HR (32)	5.50 mm × 5.00 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



效率与输出电流间的关系 (单相)



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2022	*	Initial release

5 Pin Configuration and Functions

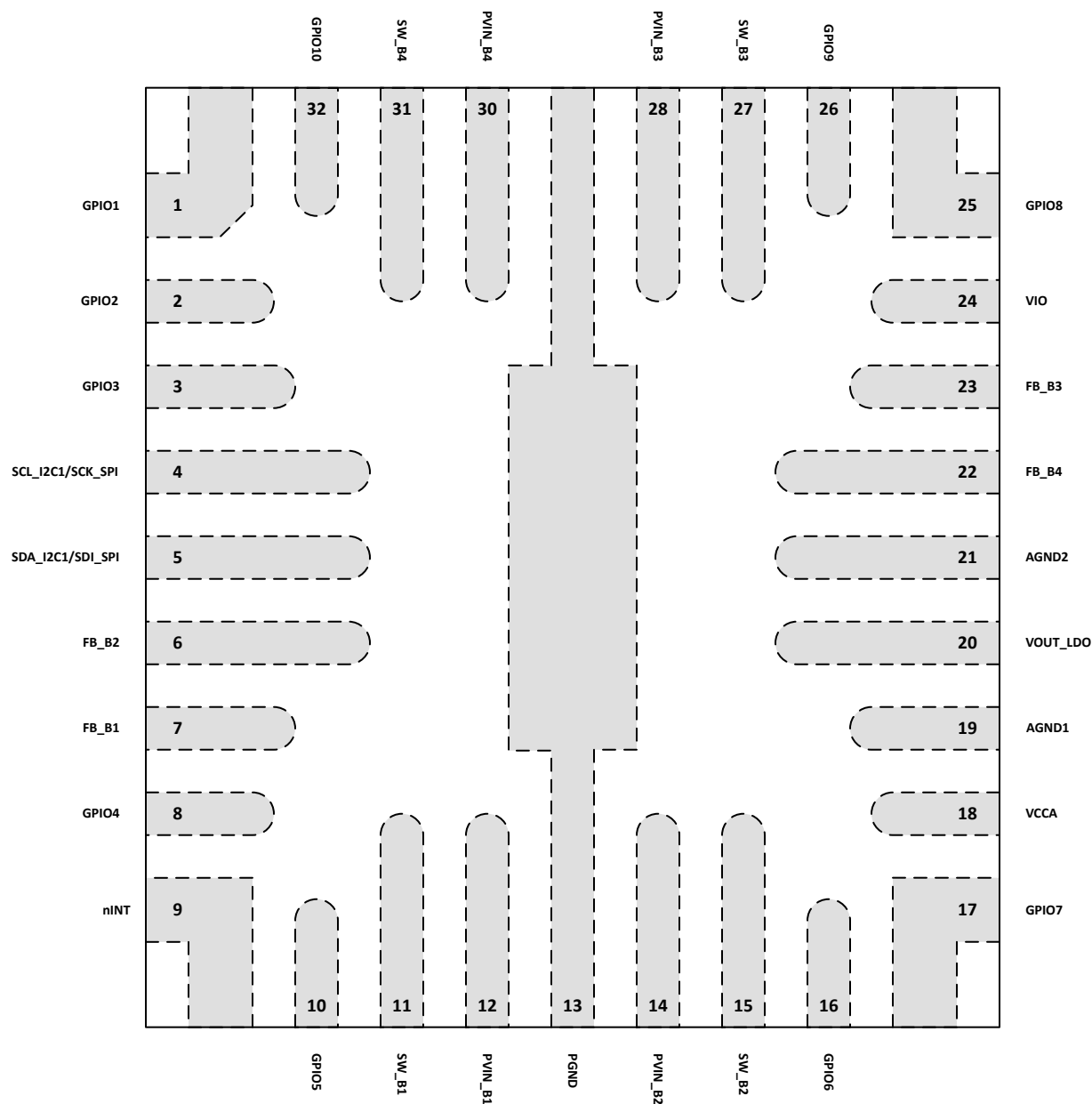


图 5-1. RQK Package 32-Pin VQFN-HR Top View

表 5-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
1	GPIO1	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		O	Digital	Alternative programmable function: EN_DRV - Enable Drive output pin to indicate the device entering safe state (set low when ENABLE_DRV bit is '0').	Floating
		O	Digital	Alternative programmable function: nRSTOUT_SOC - System reset or power on reset output (low = reset).	Floating
		O	Digital	Alternative programmable function: PGOOD - Programmable Power Good indication pin.	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
2	GPIO2	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: SCL_I2C2 - Serial interface clock input for I2C access.	Ground
		I	Digital	Alternative programmable function: CS_SPI - Serial interface Chip Select signal for SPI access.	Ground
		I	Digital	Alternative programmable function: TRIG_WDOG - Trigger signal for trigger mode watchdog.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
3	GPIO3	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I/O	Digital	Alternative programmable function: SDA_I2C2 - Serial interface data input and output for I2C access.	Ground
		O	Digital	Alternative programmable function: SDO_SPI - Serial interface data output signal for SPI access.	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
4	SCL_I2C1/ SCK_SPI	I	Digital	If SPI is not used: SCL_I2C1 - Serial interface clock input for I2C access.	Ground
		I	Digital	If SPI is used: SCK_SPI - Serial interface clock input for SPI access.	Ground
5	SDA_I2C1/ SDI_SPI	I/O	Digital	If SPI is not used: SDA_I2C1 - Serial interface data input and output for I2C access.	Ground
		I	Digital	If SPI is used: SDI_SPI - Serial interface data input signal for SPI access.	Ground
6	FB_B2	—	Analog	Output voltage feedback (positive) for BUCK2. Alternatively ground feedback for BUCK1 in multiphase configuration.	Ground
7	FB_B1	—	Analog	Output voltage feedback (positive) for BUCK1.	Ground

表 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
8	GPIO4	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: ENABLE - External power-on control.	Ground
		I	Digital	Alternative programmable function: TRIG_WDOG - Trigger signal for trigger mode watchdog.	Ground
		—	Analog	Alternative programmable function: BUCK1_VMON - Voltage monitoring input for BUCK1 regulator.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
9	nINT	O	Digital	Open-drain interrupt output, active LOW.	Floating
10	GPIO5	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: SYNCCLKIN - External switching clock input for Buck regulators.	Ground
		O	Digital	Alternative programmable function: SYNCCLKOUT - Switching clock output for external regulators.	Floating
		O	Digital	Alternative programmable function: nRSTOUT_SOC - System reset or power on reset output (low = reset).	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
11	SW_B1	—	Analog	BUCK1 switch node.	Floating
12	PVIN_B1	—	Power	Power input for BUCK1. The separate power pins PVIN_Bx are not connected together internally - PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
13	PGND	—	Ground	Power ground for Buck regulators.	Ground
14	PVIN_B2	—	Power	Power input for BUCK2. The separate power pins PVIN_Bx are not connected together internally - PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
15	SW_B2	—	Analog	BUCK2 switch node.	Floating
16	GPIO6	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: nERR_MCU - System error count down input signal from the MCU.	Floating
		O	Digital	Alternative programmable function: SYNCCLKOUT - Switching clock output for external regulators.	Floating
		O	Digital	Alternative programmable function: PGOOD - Programmable Power Good indication pin.	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground

表 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
17	GPIO7	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I	Digital	Alternative programmable function: nERR_MCU - System error count down input signal from the MCU.	Floating
		O	Analog	Alternative programmable function: REFOUT - Buffered bandgap output.	Floating
		I	Analog	Alternative programmable function: VMON1 - External voltage monitoring input.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
18	VCCA	—	Power	Supply voltage for internal LDO. VCCA and PVIN_Bx pins must be connected together in the application and be locally bypassed.	System supply
19	AGND1	—	Ground	Ground	Ground
20	VOUT_LDO	—	Power	LDO regulator filter node. LDO is used for internal purposes.	—
21	AGND2	—	Ground	Ground	Ground
22	FB_B4	—	Analog	Output voltage feedback (positive) for BUCK4. Alternatively ground feedback for BUCK3 in dualphase configuration.	Ground
23	FB_B3	—	Analog	Output voltage feedback (positive) for BUCK3.	Ground
24	VIO	—	Power	Supply voltage for selected digital outputs.	Ground
25	GPIO8	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I/O	Digital	Alternative programmable function: SCLK_SPMI - Multi-PMIC SPMI serial interface clock signal. This pin is an output pin for the master SPMI device, and an input pin for the slave SPMI device.	Ground
		I	Analog	Alternative programmable function: VMON2 - External voltage monitoring input.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
26	GPIO9	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		I/O	Digital	Alternative programmable function: SDATA_SPMI - Multi-PMIC SPMI serial interface bidirectional data signal	Floating
		O	Digital	Alternative programmable function: PGOOD - Programmable Power Good indication pin.	Floating
		I	Digital	Alternative programmable function: SYNCCLKIN - External switching clock input for Buck regulators.	Ground
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground
27	SW_B3	—	Analog	BUCK3 switch node.	Floating
28	PVIN_B3	—	Power	Power input for BUCK3. The separate power pins PVIN_Bx are not connected together internally - PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply

表 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
30	PVIN_B4	—	Power	Power input for BUCK4. The separate power pins PVIN_Bx are not connected together internally - PVIN_Bx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
31	SW_B4	—	Analog	BUCK4 switch node.	Floating
32	GPIO10	I/O	Digital	Primary function: General Purpose Input/Output signal. When configured as an output pin, it can be included as part of the power sequencer output signal to enable an external regulator.	Input: Ground, Output: Floating
		O	Digital	Alternative programmable function: nRSTOUT - System reset or power on reset output (low = reset).	Floating
		O	Digital	Alternative programmable function: nRSTOUT_SOC - System reset or power on reset output (low = reset).	Floating
		I	Digital	Alternative programmable function: nSLEEP1 or nSLEEP2, which are the sleep request signals for the device to go to lower power states (Active Low).	Ground
		I	Digital	Alternative programmable function: WKUP1 or WKUP2, which are the wake-up request signals for the device to go to higher power states.	Ground

6 Device and Documentation Support

6.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

6.3 Trademarks

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6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP876924C3RQKRQ1	ACTIVE	VQFN-HR	RQK	32	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LP8769 24C3-Q1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

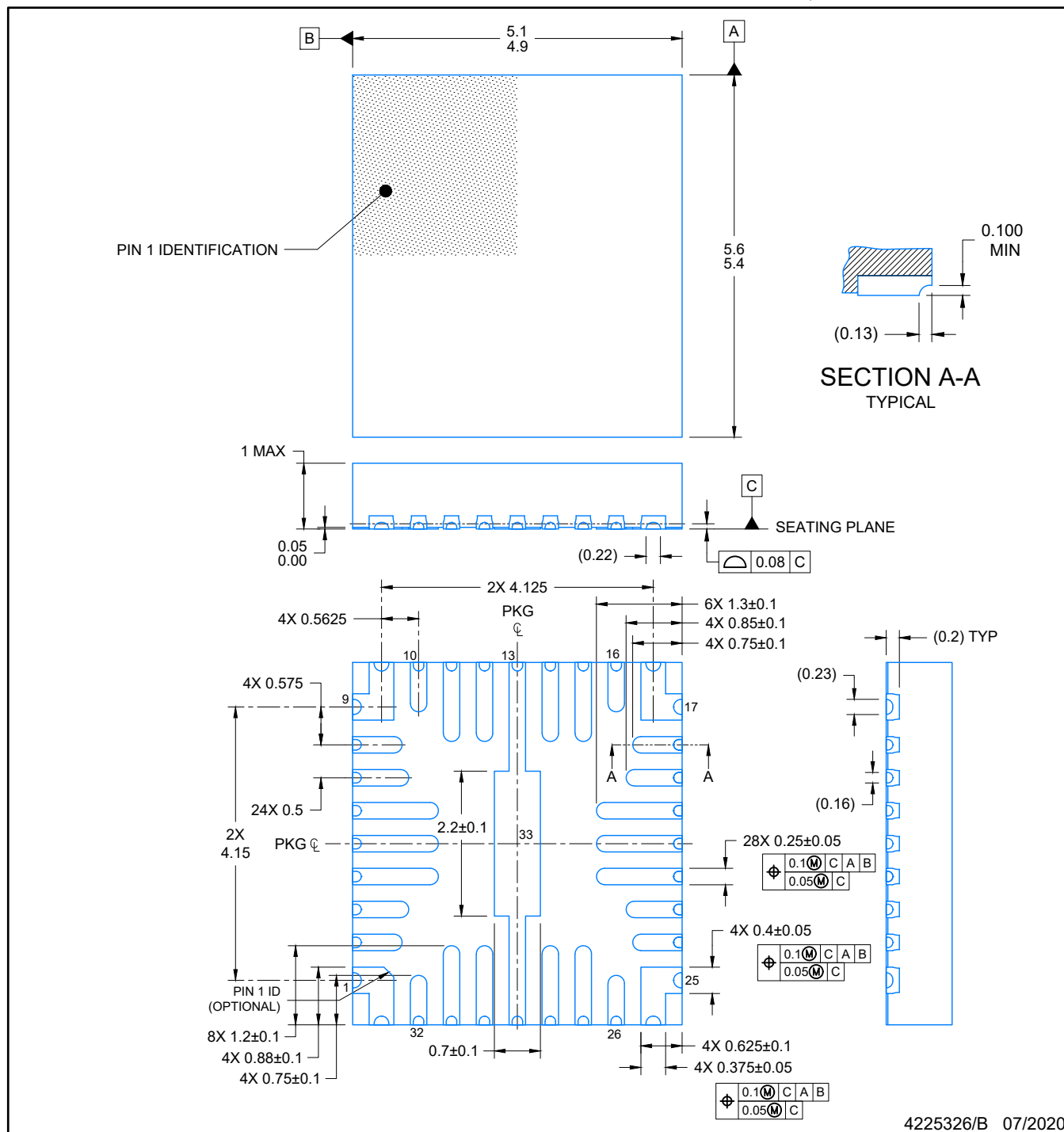
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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