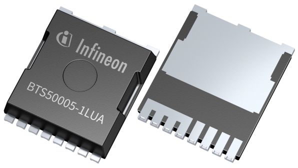
BTS50005-1LUA

Datasheet

Power PROFET™ + 12V smart high-side power switch



AEC Qualified

RoHS

ISO 26262 ready

Halogen-free

Features

- PRO-SIL™ ISO 26262-ready for supporting the integrator in evaluation of hardware element according to ISO 26262:2018 Clause 8-13
- One channel device
- Low stand-by current
- Reverse ON protection for low power dissipation in reverse battery condition
- Ground loss protection
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility (EMC)
- Compatible to cranking pulses
- Integrated diagnostic functions
- Integrated protection functions
- Green product (RoHS compliant)

Potential applications

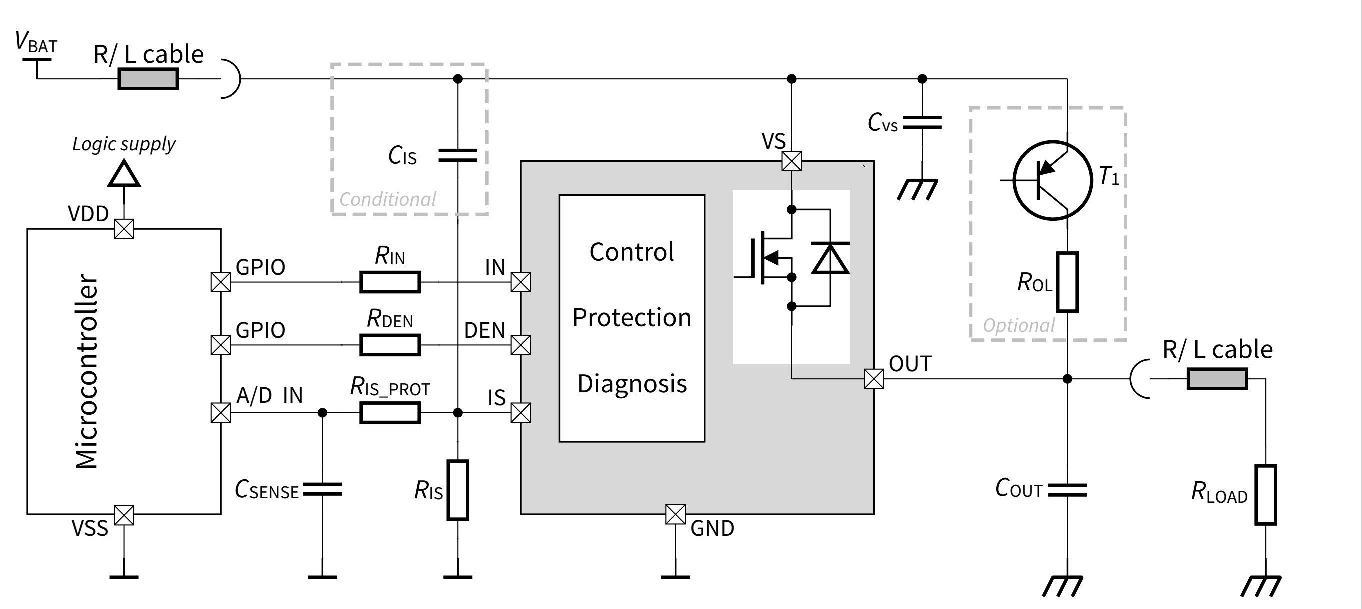
- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for application with high current loads, such as heating system, fan and pump
- PWM applications with low frequency

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100 grade 1.

Description

The device is a 0.6 mΩ single channel smart high-side power switch, available in a PG-HSOF-8 package, providing protective functions and diagnosis. It contains Reverse ON functionality. It is especially designed to drive high current loads, for applications like heaters, glow plugs, fans and pumps.



Application diagram

Product type	Package	Marking
BTS50005-1LUA	PG-HSOF-8	S50005A

Please read the sections "Important notice" and "Warnings" at the end of this document

Table of contents

1 Product description

1.1 Product summary

Table 1 **Product summary**

Parameter	Symbol	Values
Operating voltage	$V_{S(NOM)}$	5.8 V … 18 V
Extended supply voltage range	$V_{S(EXT)}$	3.1 V...28 V
Maximum on-state resistance (T_J = 150°C)	$R_{DS(ON)}$	1.1 mΩ
Minimum nominal load current (T_A = 85°C)	$I_{L(NOM)}$	57 A
Typical current sense ratio	dk_{ILIS}	50000
Minimum short circuit current threshold	$I_{CL(0)}$	150 A
Maximum reverse battery voltage	$-V_{S(REV)}$	-18 V
Maximum stand-by current at T_J = 25 °C	$I_{VS(OFF)}$	3 µA

1.2 Integrated diagnosis and protection functions

Integrated diagnosis functions

- Proportional load current sense
- Open load detection in on and off state
- Diagnosis enable pin
- Latched status signal after short circuit or overtemperature detection

Integrated protection functions

- Reverse ON: Reverse battery protection by self turn on of power MOSFET
- Short circuit protection with latch
- Overtemperature protection with latch
- Enhanced short circuit operation
- Smart clamping for inductive loads demagnetization

2 Block diagram

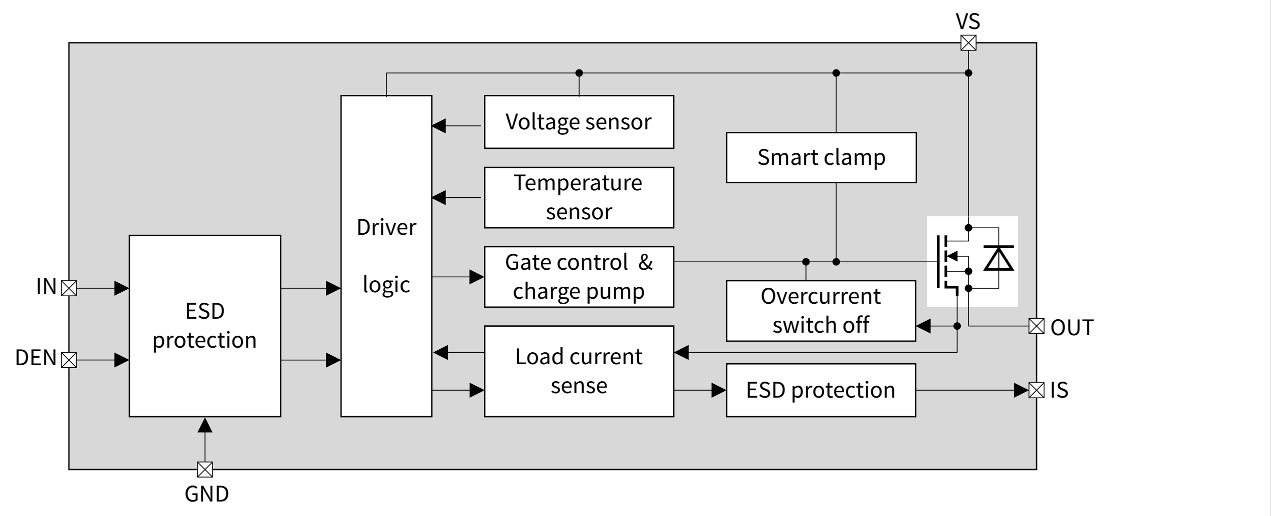


Figure 2 **Block diagram**

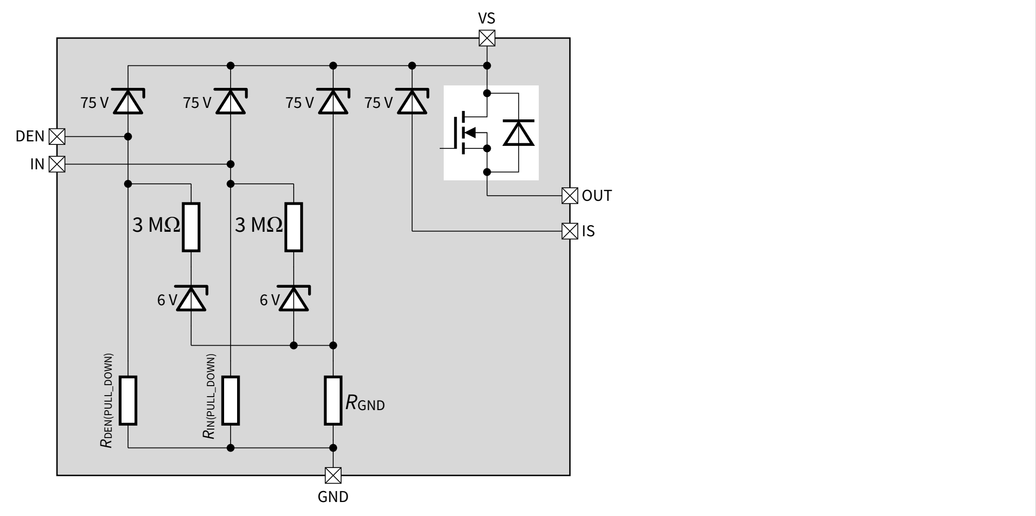


Figure 3 **Internal diode diagram**

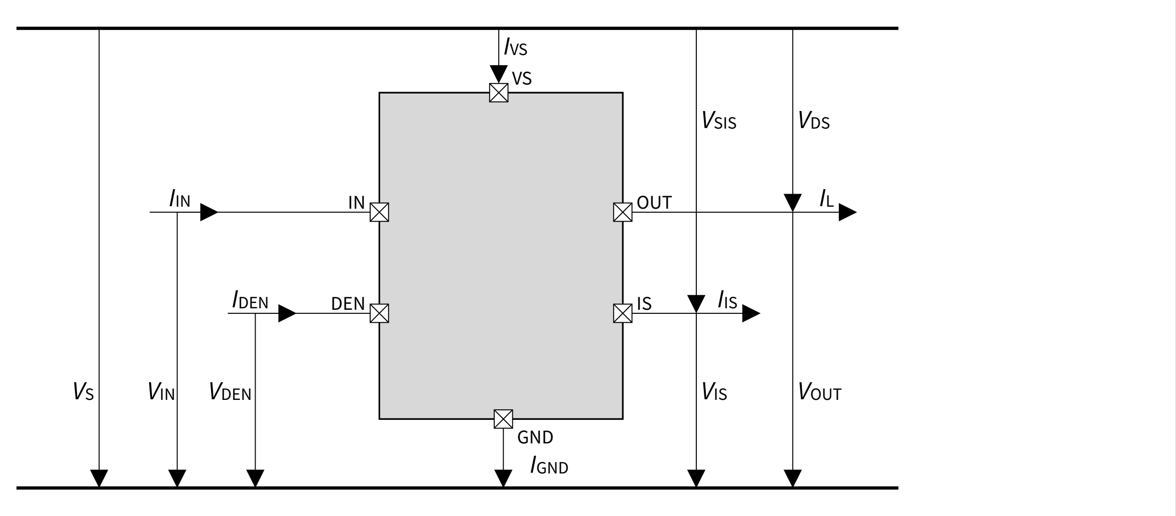


Figure 4 **Voltage and current definition**

3 Pin configuration

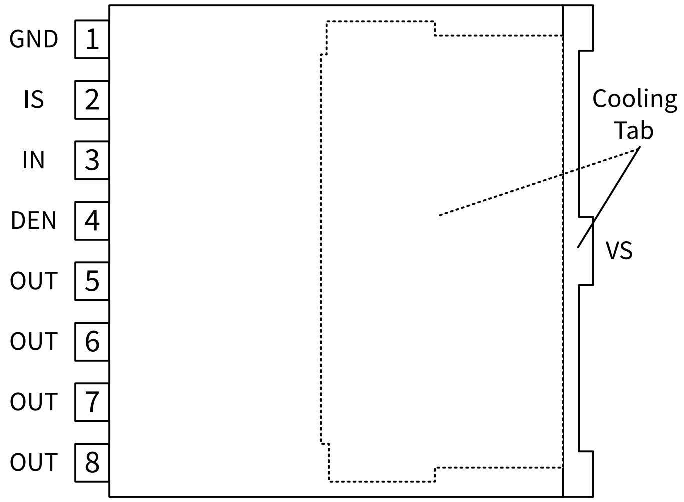


Figure 5 **Pin assignment**

Table 2 **Pin definitions and function**

Pin	Symbol	Function
1	GND	Ground pin
2	IS	Sense pin: analog/digital signal for diagnosis, if not used: left open
3	IN	Input pin: digital signal to switch on channel (active high)
4	DEN	Diagnosis enable: digital signal to enable the diagnosis (active high)
5, 6, 7, 8	OUT	Output pin: protected high side power output channel
Cooling tab	VS	Supply voltage: battery voltage

4 General product characteristics

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltages							
Supply voltage	V_S	-0.3	–	35	V	1)	PRQ-50
Reverse polarity voltage	$V_{S(REV)}$	-18	–	–	V	2) 1) $T_A = 25°C$ $t \leq 5$ min. $R_L \geq 0.32\ \Omega$	PRQ-51
Load dump voltage	$V_{S(LD)}$	–	–	43	V	1) Suppressed Load Dump acc. to ISO16750-2 $R_I = 2\ \Omega$ td = 200 ms Us = 100 V $R_L = 0.32\ \Omega$ $R_{IS} = 1\ k\Omega$ $V_{S(LD)} = U_S^*$	PRQ-52
Short circuit capability							
Supply voltage for short circuit protection	$V_{S(SC)}$	3.1	–	18	V	1) According to the test circuit defined in figure 1 of AEC-Q100-012 with $L_{SUPPLY} = 0.5..5\ \mu H$ $L_{SHORT} = 0..5\ \mu H$ $R_{MIN} = 10\ m\Omega$	PRQ-53
Input pin (IN)							
Voltage at IN pin	V_{IN}	V_S - 75	–	V_S + 0.3	V	1)	PRQ-54
Current through IN pin	I_{IN}	-50	–	50	mA	1)	PRQ-55
Maximum input frequency	f_{IN}	–	–	200	Hz	1) 5.8 V < V_S < 28 V	PRQ-56
Maximum retry cycle rate in fault condition	f_{FAULT}	–	–	200	Hz	1)	PRQ-57
Diagnosis enable pin (DEN)							
Voltage at DEN pin	V_{DEN}	V_S - 75	–	V_S + 0.3	V	1)	PRQ-162
Current through DEN pin	I_{DEN}	-50	–	50	mA	1)	PRQ-163
Sense and diagnosis pin (IS)							
Voltage at IS pin	V_{IS}	V_S - 75	–	V_S + 0.3	V	1)	PRQ-58

(table continues...)

Table 3 (continued) Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current through IS pin	I_{IS}	-50	–	50	mA	[1]	PRQ-59
Power stage							
Maximum energy dissipation by switching off inductive load single pulse over lifetime	E_{AS}	–	–	450	mJ	[1] V_S = 13.5 V I_L = 42 A $T_{J(0)} \leq$ 150°C See Figure 6	PRQ-60
Maximum energy dissipation repetitive pulse	E_{AR}	–	–	160	mJ	[1] V_S = 13.5 V, I_L = 42A, $T_{J(0)} \leq$ 105°C See Figure 6 1M cycles	PRQ-61
Voltage at OUT pin	V_S - V_{OUT}	-0.3	–	35	V	[1]	PRQ-62
Temperatures							
Junction temperature	T_J	-40	–	150	°C	[1]	PRQ-63
Dynamic temperature increase while switching	ΔT_J	–	–	60	K	[1]	PRQ-64
Storage temperature	T_{STG}	-55	–	150	°C	[1]	PRQ-65
ESD susceptibility							
ESD susceptibility (all pins)	$V_{ESD(HBM)}$	-2	–	2	kV	[1] Human body model "HBM" according to AEC Q100-002	PRQ-66
ESD susceptibility OUT pin vs. VS	$V_{ESD(HBM)}$	-4	–	4	kV	[1] Human body model "HBM" according to AEC Q100-002	PRQ-67
ESD susceptibility (all pins)	$V_{ESD(CDM)}$	-500	–	500	V	[1] Charge device model "CDM" according to AEC Q100-011	PRQ-175
ESD susceptibility (corner pins)	$V_{ESD(CDM)}$	-750	–	750	V	[1] Charge device model "CDM" according to AEC Q100-011	PRQ-176

1) Not subject to production test, specified by design.
2) The device is mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection.

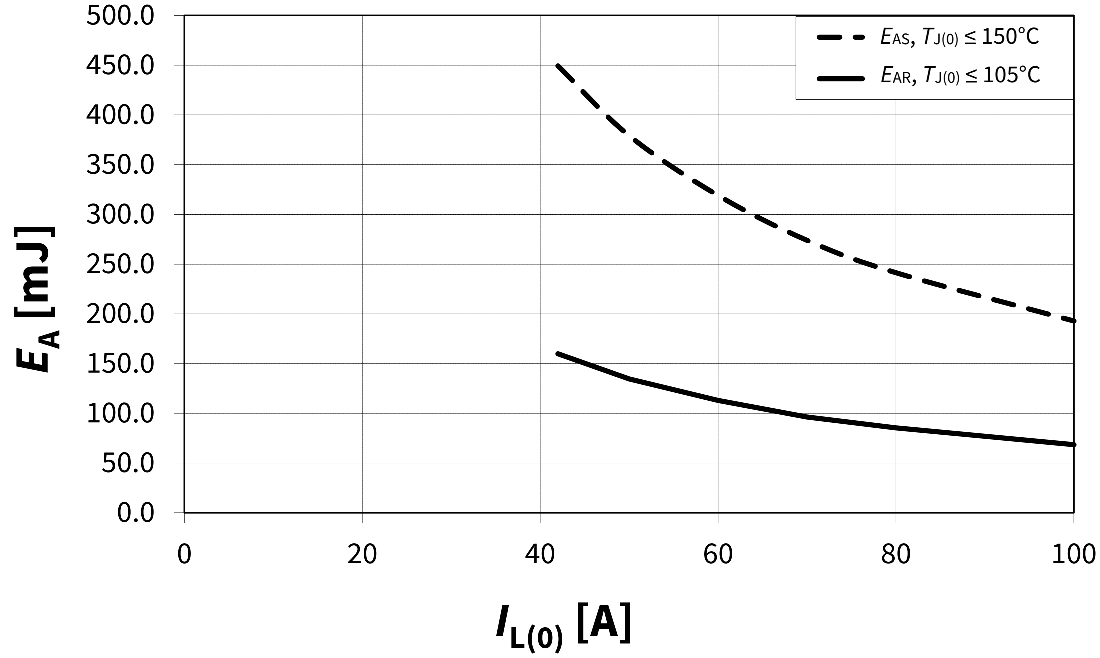


Figure 6 Maximum energy dissipation for inductive switch off, $E_{AS/AR}$ vs. I_L at V_S = 13.5 V

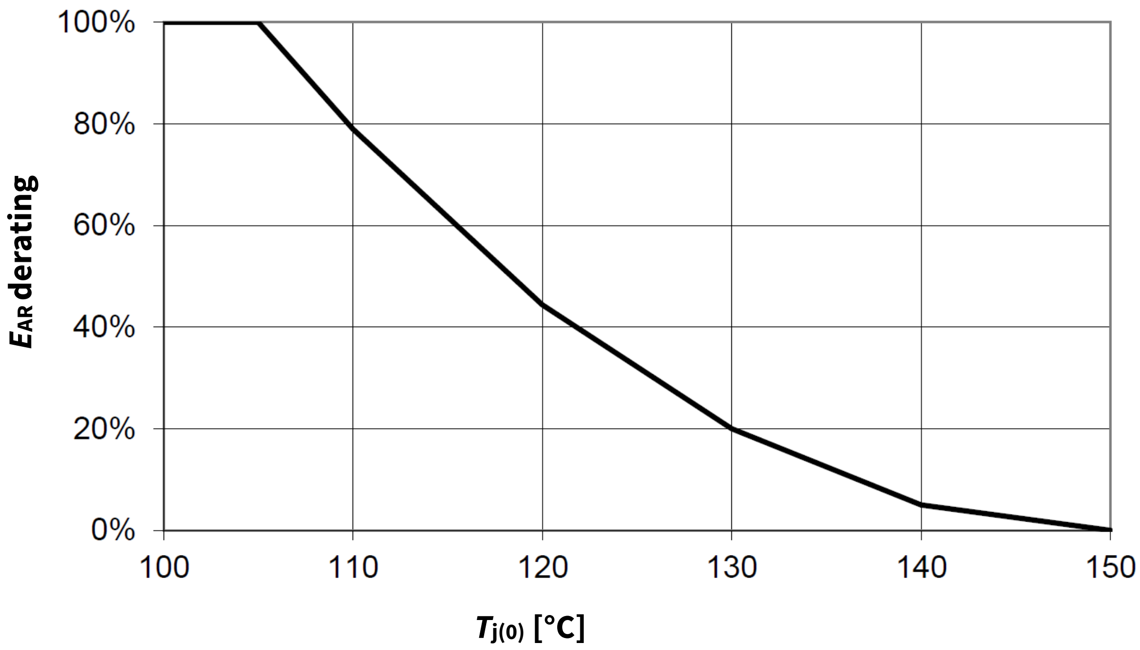


Figure 7 Maximum energy dissipation repetitive pulse temperature derating

Note: *1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional description

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage range for nominal operation	$V_{S(NOM)}$	5.8	–	18	V	[1]	PRQ-68
Supply voltage range for extended operation	$V_{S(EXT)}$	3.1	–	28	V	[2] [1] Parameter deviation possible	PRQ-69

1) Not subject to production test, specified by design.
2) Protection function still operative

Note: *Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*

4.3 Thermal resistance

Note: *This thermal data was generated in accordance to JEDEC JESD51 standards. For more information, go to www.jedec.org.*

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	–	0.4	K/W	[1]	PRQ-70
Junction to ambient	$R_{thJA(2s2p)}$	–	18	–	K/W	[1] [2]	PRQ-71
Junction to ambient	$R_{thJA(1s0p)}$ /600mm^2	–	32	–	K/W	[1] [3]	PRQ-72

1) Not subject to production test, specified by design.
2) The specified RthJA value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at TA = 105°C, $P_{DISSIPATION}$ = 2W.
3) The specified RthJA value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board. The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm board with only one top copper layer 1 × 70 µm. Simulation done at TA = 105°C, $P_{DISSIPATION}$ = 2W.

The figure below shows the typical thermal impedance of BTS50005-1LUA mounted according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 1s0p and 2s2p boards.

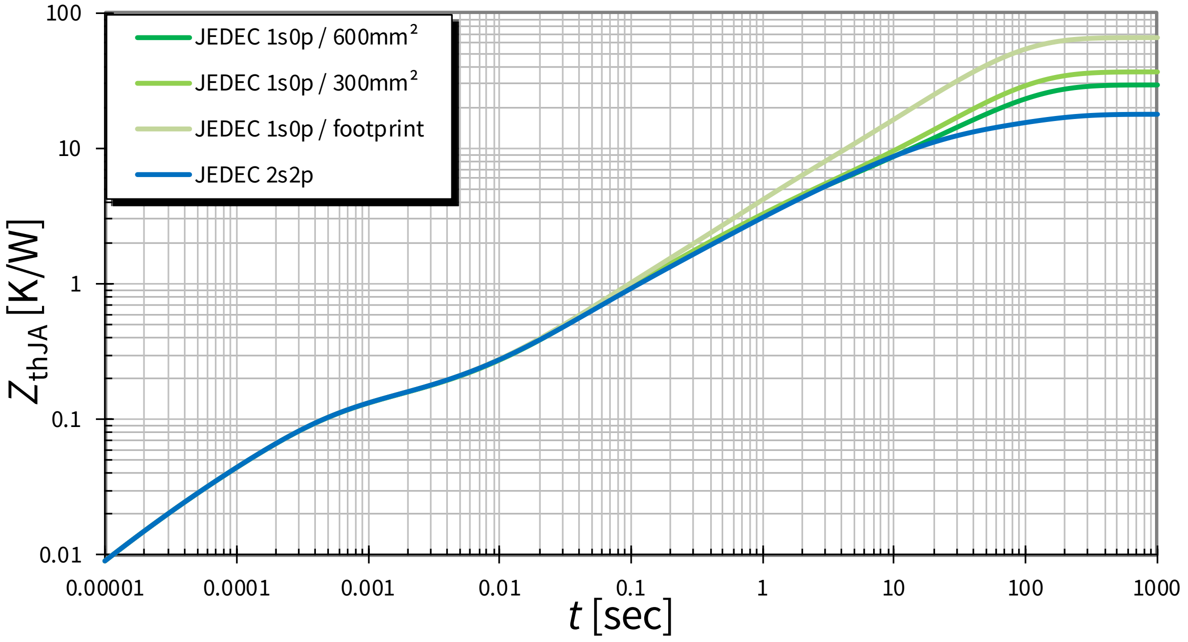


Figure 8 **Typical transient thermal impedance $Z_{th(JA)}$ = f(time) for different PCB conditions**

5 Functional description

5.1 Power stage

The power stage is built by an N-channel power MOSFET with a charge pump.

5.1.1 Output on-state resistance

The on-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as on the junction temperature T_J. Chapter 6 shows the dependencies in terms of temperature and supply voltage, for the typical on-state resistance. The behavior in reverse polarity is described in Chapter 5.3.3.

5.1.2 Switching resistive loads

The figure below shows the typical timing when switching a resistive load. The power stage has a defined switching behavior.

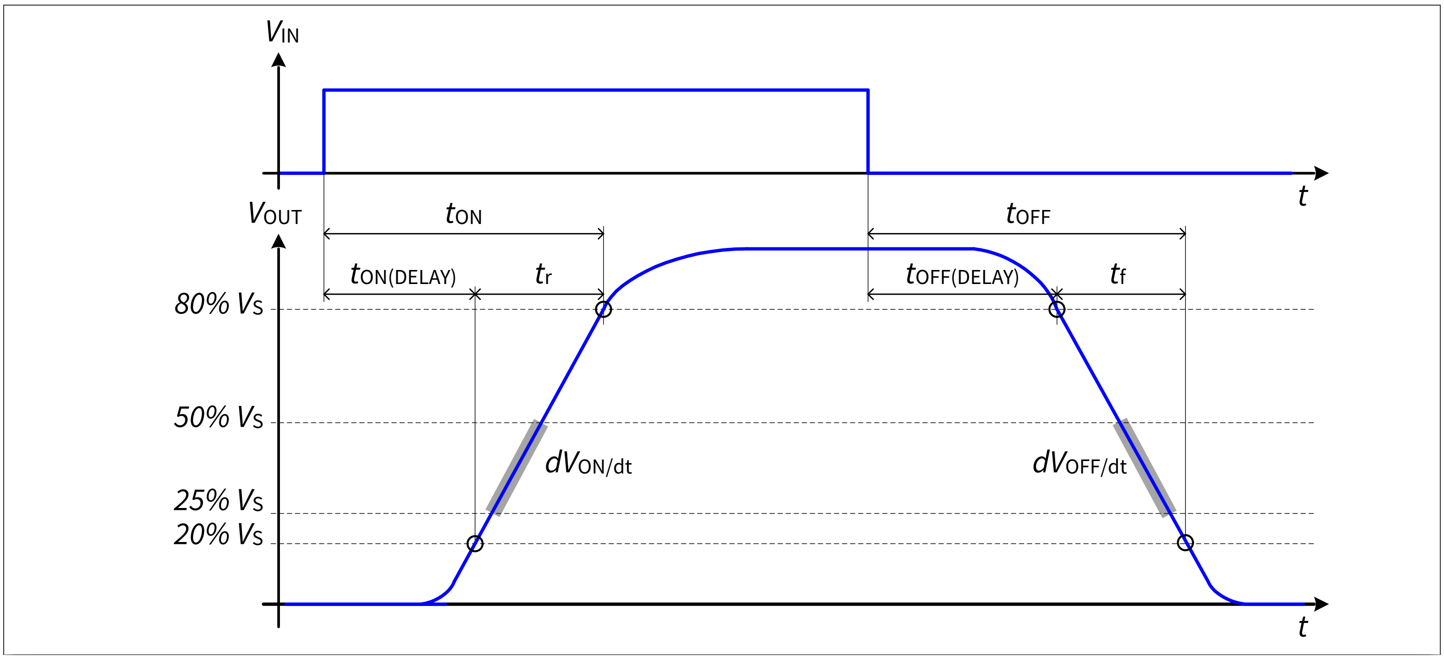


Figure 9 **Switching a resistive load: timing**

5.1.3 PWM switching

Consider the switching losses properly during this operation (see following equation):

$$P_{\mathrm{TOTAL}} = \frac{switch\_on\_energy + switch\_off\_energy + \left(I_{\mathrm{L}}{}^{2} \times R_{\mathrm{DS(ON)}} \times t_{\mathrm{DC}}\right)}{Period} \tag{1}$$

If a fault condition occurs, ensure that the PWM frequency does not exceed a maximum retry frequency of f_{FAULT}.

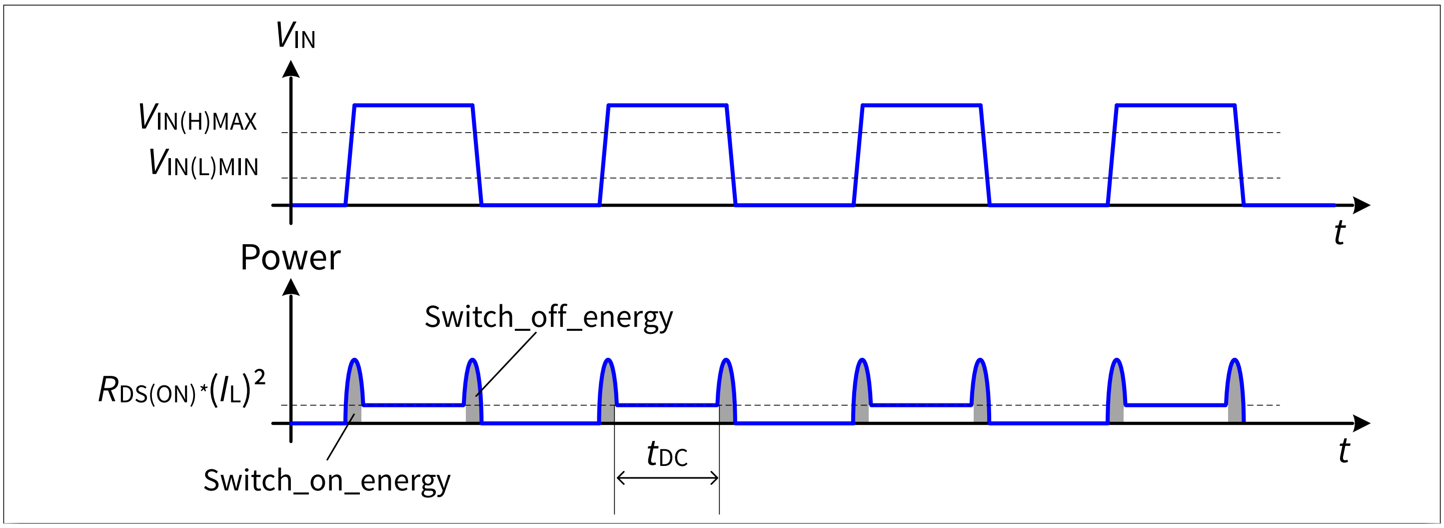


Figure 10 Switching in PWM

5.1.4 Switching inductive loads

5.1.4.1 Output clamping

When switching off inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current.

To prevent the destruction of the device due to high voltages, there is a smart clamping mechanism implemented that keeps negative output voltage to a certain level (V_S - $V_{DS(CL)}$). Please refer to Figure 11 and Figure 12 for details. Nevertheless, the maximum allowed load inductance remains limited.

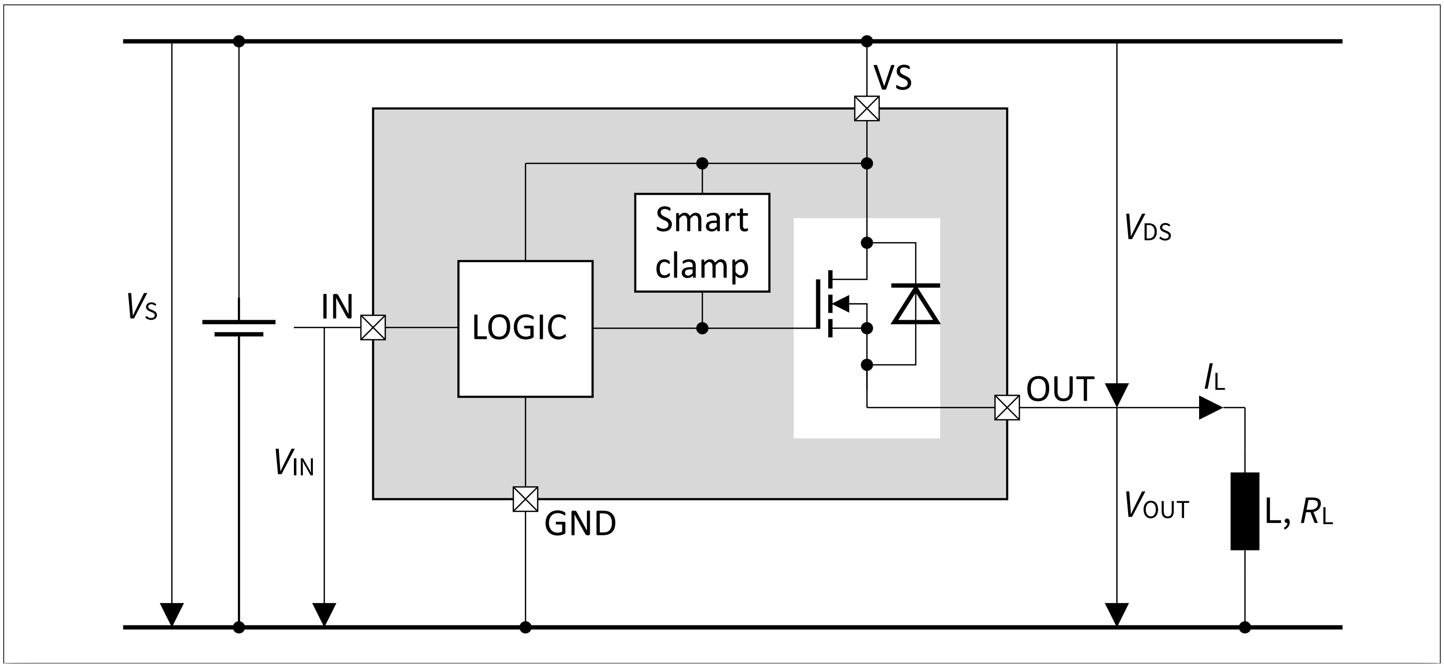


Figure 11 Output clamp

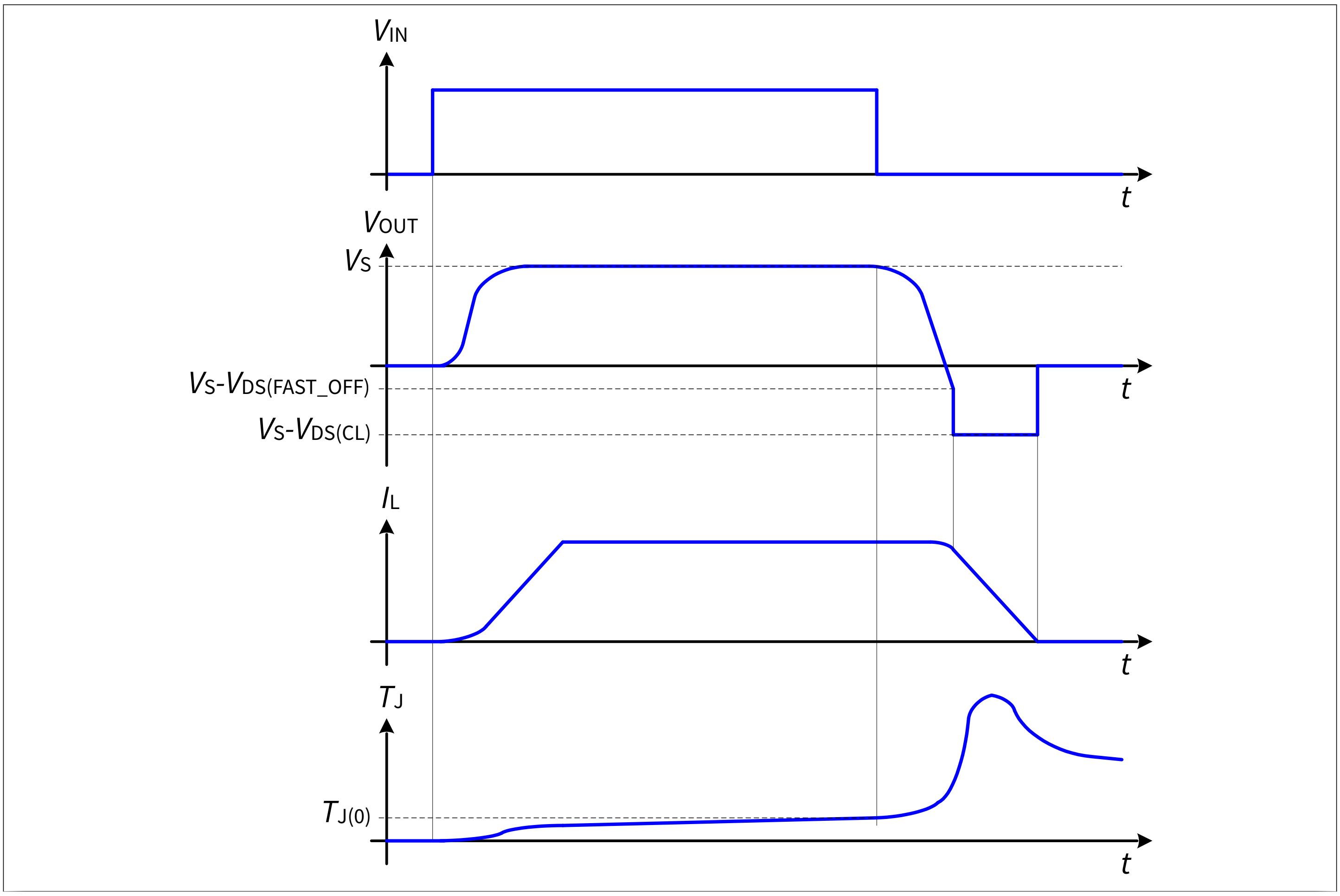


Figure 12 **Switching an inductance**

The device features a fast switch off when driving an inductive load in order to increase the energy capability. The fast turn off is triggered when V_{DS} is higher than $V_{DS(FAST\_OFF)}$.

The device must not be reactivated (V_{IN} goes from low to high) before $t_{IN(RESETDELAY)}$. Otherwise the device may not turn on and can be latched.

5.1.4.2 Maximum load inductance

During the demagnetization of inductive loads, the energy must be dissipated in the device. This energy can be calculated using the following equation:

$$E = V_{DS(CL)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{DS(CL)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(CL)}}\right) + I_L \right] \tag{2}$$

The following equation simplifies under the assumption of $R_L = 0\ \Omega$.

$$E = \frac{1}{2} \times L \times I_L^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(CL)}}\right) \tag{3}$$

The energy, which is converted into heat, is limited by the thermal design of the component. See Figure 6 for the maximum allowed energy dissipation as a function of the load current.

5.1.5 Advanced switch-off behavior

In order to reduce device stress when switching off inductive and critical loads, the device provides an advanced switching off functionality which results in a faster switching off behavior.

The fast switch off functionality is triggered by each of the following conditions:

- The device is turned off by applying $V_{IN(L)}$ at the IN pin. During the switch off operation the OUT pins' voltage in respect to VS pin drops below $V_{DS(FAST\_OFF)}$. See Figure 12.
- The device is turned on or is already in on state. The device then detects a short circuit condition ($I_L \geq I_{CL(0)}$) and initiates a protective switch off. Please refer to Chapter 5.3.1.1 and Chapter 5.3.1.2 for details.
- The device is turned on or is already in on state. The device then detects an overtemperature condition.
- The device is turned on or is already in on state. The device then detects an overpower condition.

5.1.6 Inverse current behavior

When $V_{OUT} > V_S$, a current flows into the power output transistor. This condition is known as "inverse current". If the channel is in off state, the current flows through the intrinsic body diode generating high power losses therefore an increase of overall device temperature. If the channel is in on state, the power dissipation in the output stage is comparable to normal operation in $R_{DS(ON)}$.

During inverse current condition, the channel remains in on or off state and it is possible to switch on as long as $|-I_L| < |-I_{CL(0)}|$.

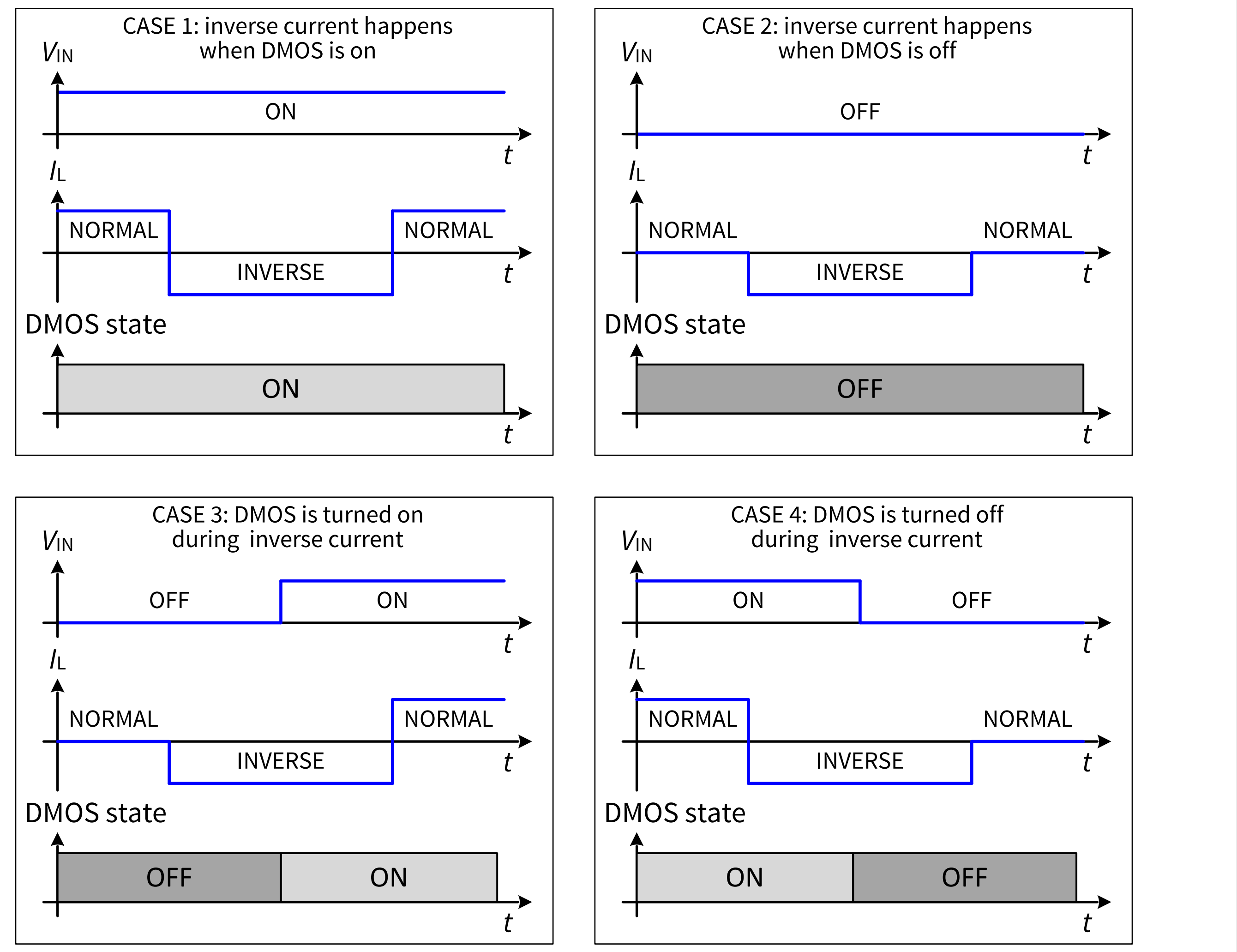


Figure 13 **Channel behavior in case of applied inverse current**

5.2 Input pin

The input circuitry is compatible with 3.3 V and 5 V microcontroller. It can also be connected to V_S directly. The maximum voltage on the input pin is referenced to V_S and can go below the ground. See input pin in Table 3.

The figure below shows the electrical equivalent input circuitry.

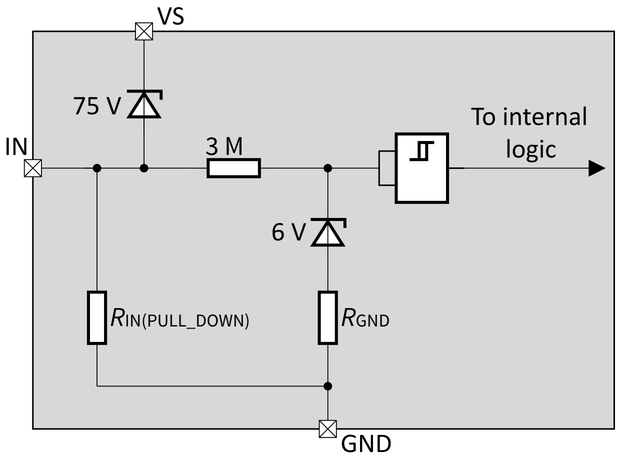


Figure 14 **Simplified schematics of the IN pin circuitry**

5.3 Protection functions

The device provides integrated protection functions. Integrated protection functions are designed to prevent the destruction of the IC from fault conditions described in the datasheet. Fault conditions are considered as outside normal operating range. Protection functions are designed neither for continuous nor for repetitive operation.

The figure below describes the typical functionality of the diagnosis and protection block.

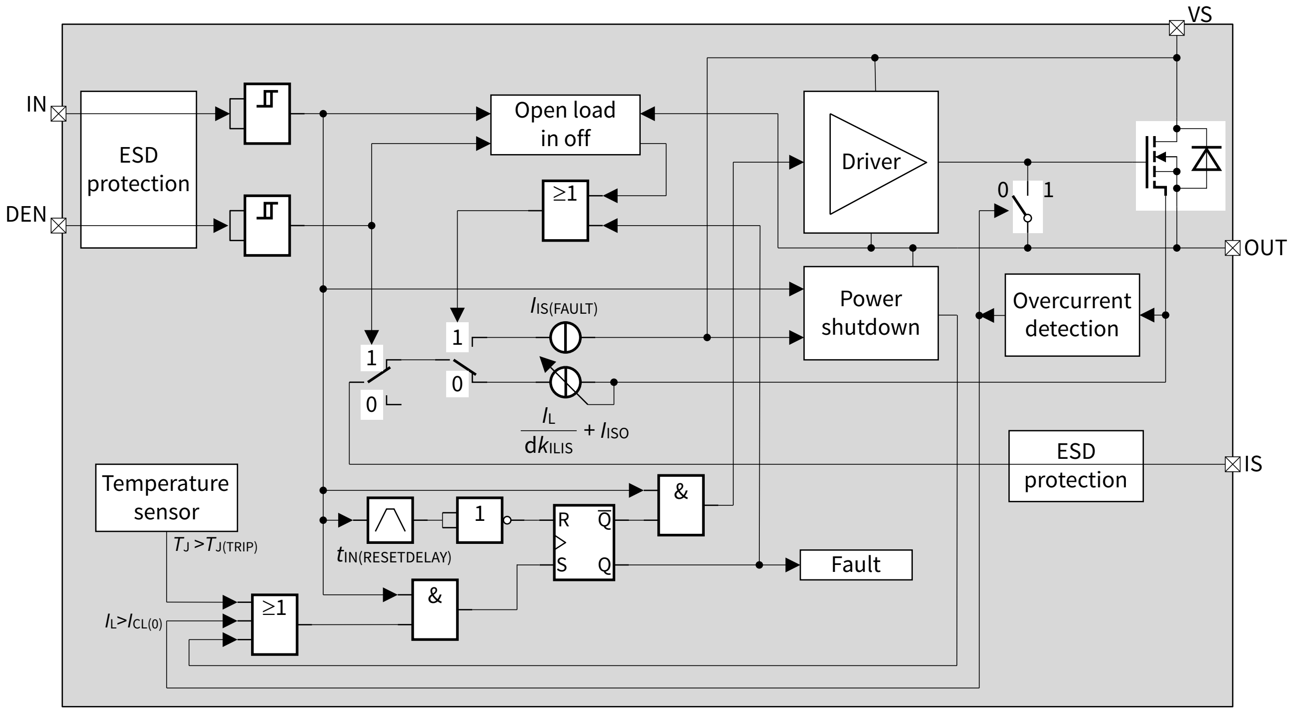


Figure 15 **Diagram of diagnosis and protection blocks**

5.3.1 Overload protection

In case of overload, high inrush current or short circuit to ground, the device offers several protection mechanisms.

An overcurrent, an overtemperature or an overpower shutdown switch off the output and latches the device.

There are two ways to reset the internal latch:

- Set $V_{IN} < V_{IN(L)}$ for t > $t_{IN(RESETDELAY)}$.
- $V_S < V_{S(UVL)}$ for t > $t_{IN(RESETDELAY)}$.

For overload (short circuit or overtemperature), the maximum retry cycle (f_{FAULT}) under fault condition must be considered.

5.3.1.1 Activation of the switch into short circuit (short circuit type 1)

When the switch is activated into short circuit, the current is rising. When the output current reaches the $I_{CL(0)}$ value, the device latches and turns off after $t_{OFF(TRIP)}$ regardless the output current value.

5.3.1.2 Short circuit appearance when the device is already on (short circuit type 2)

When the device is in on state and a short circuit to ground appears at the output with an overcurrent higher than $I_{CL(0)}$, the device automatically turns off and latches.

5.3.1.3 Overpower shutdown (PSD)

The device integrates an overpower shutdown protection in order to limit the power dissipation. This protection intends to limit the maximum junction temperature in case of soft short circuit ($I_L < I_{CL(0)}$), repetitive short circuit or short circuit at low voltage.

If there is a short circuit at low voltage with a high resistor or an inductor in the battery line, V_S can drop below $V_{S(PSD)}$ and the load current does not reach $I_{CL(0)}$. In these conditions, the overpower shutdown protection activates and latches the device after $t_{PSD(UV)}$.

Note: Overpower shutdown also limits the maximum PWM frequency below f_{IN}. See Figure 16 below:

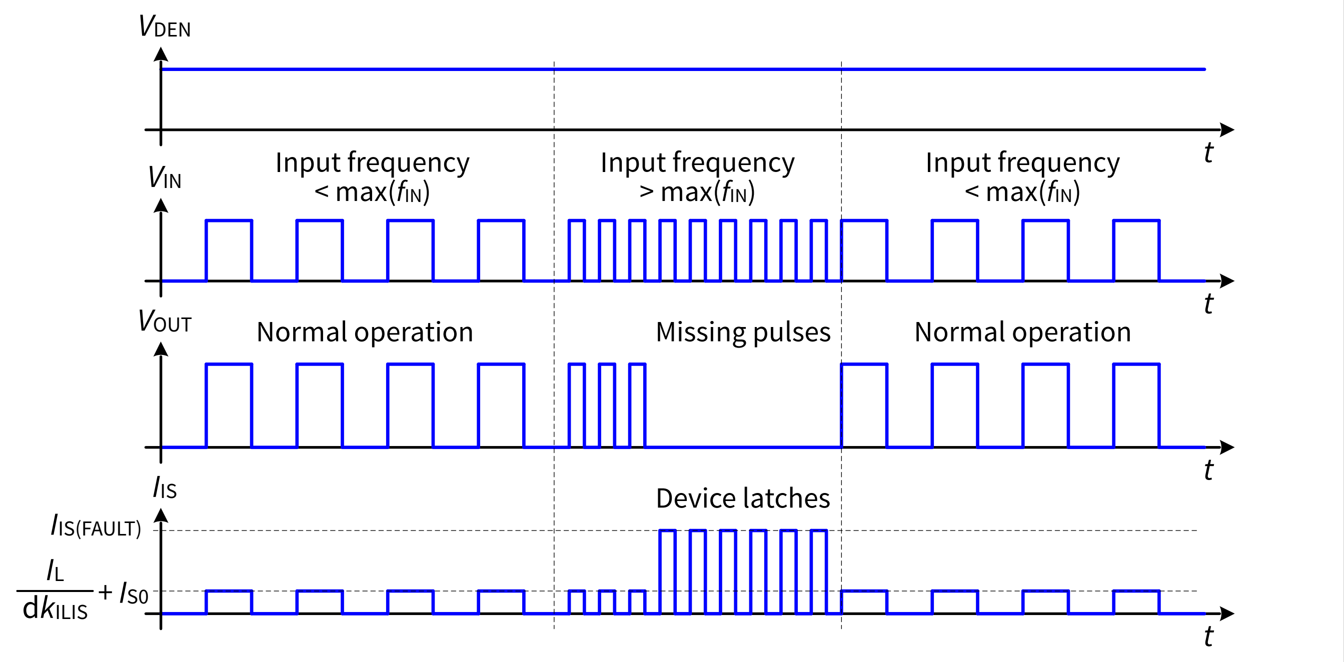


Figure 16 **Behavior during PWM operation above f_{IN} max**

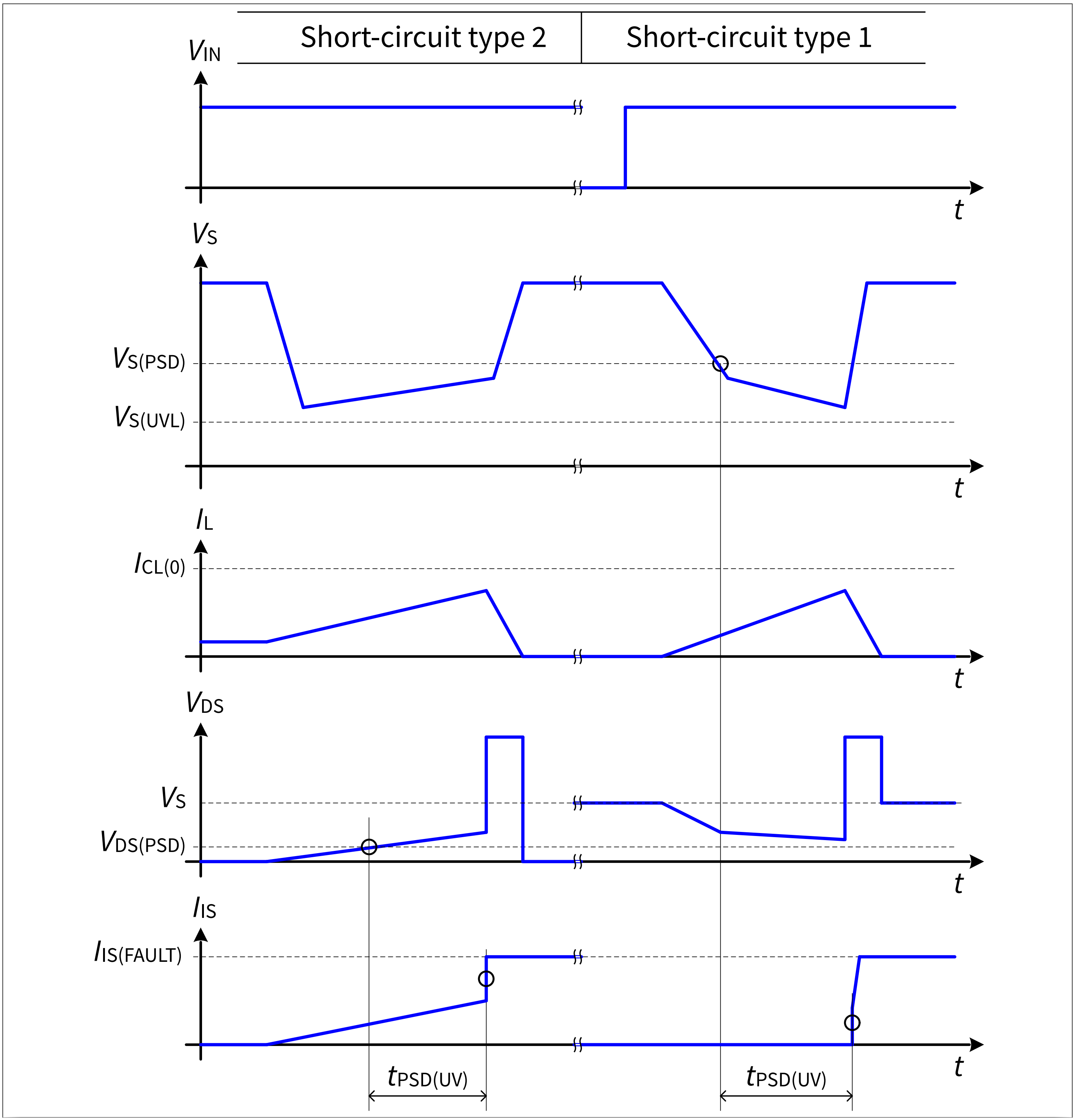


Figure 17 **Overpower shutdown behavior at low voltage**

5.3.1.4 Temperature limitation in the power DMOS

The device incorporates a temperature sensor. Triggering the overtemperature ($T_{J(TRIP)}$) switches off the power MOSFET to prevent destruction and latches the device.

5.3.2 Ground loss protection

In case of loss of module or device ground, while the load remains connected to ground, the device protects itself by automatically turning off (when it was previously on) or remains off, regardless of the voltage applied at IN pin.

5.3.3 Reverse battery protection

In case of reverse polarity, the intrinsic body diode of the power DMOS causes power dissipation. To limit the risk of overtemperature, the device provides Reverse ON functionality. The power in this intrinsic body diode is limited by turning the DMOS on. The DMOS resistance is then equal to $R_{DS(REV)}$. Additionally, the current into the logic has to be limited with R_{IN} and R_{DEN} because there is a current path in the microcontroller.

The device includes a R_{GND} resistor which limits the current without any external resistor. R_{IS} is used to limit the current into IS pin.

See Chapter 7.

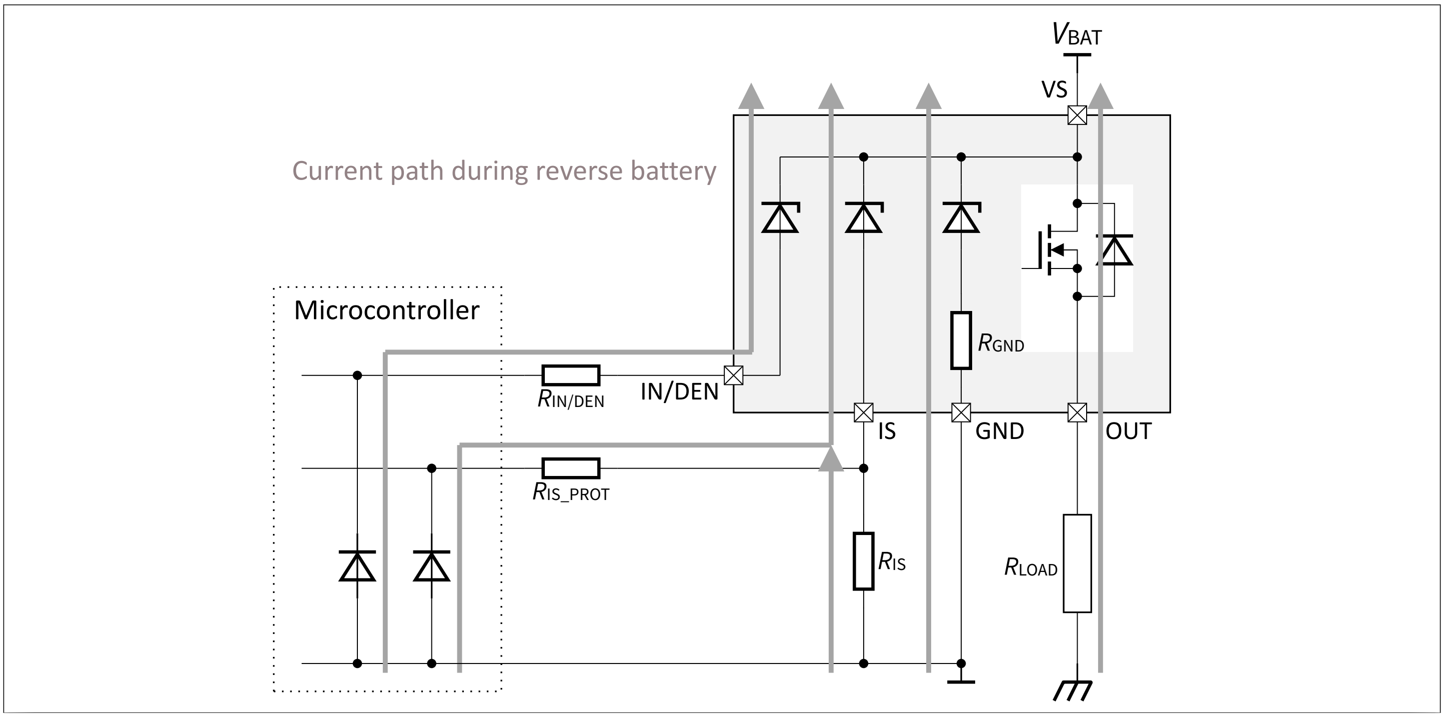


Figure 18 Reverse battery current path

5.4 Diagnosis functions

For diagnosis purposes, the device provides a combination of digital and analog signals at pin IS.

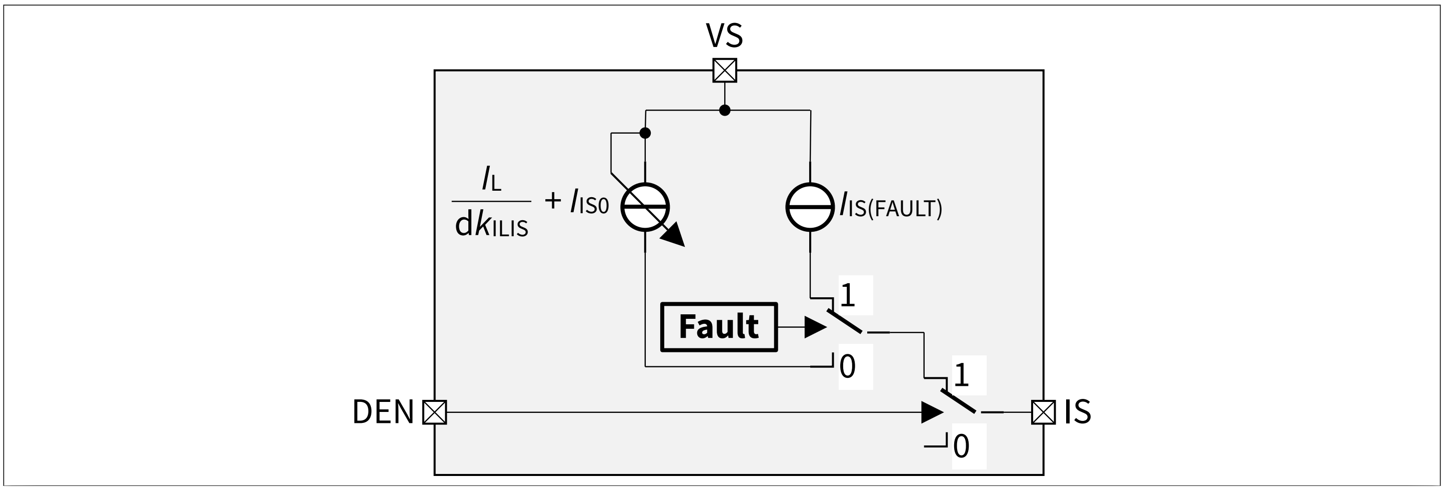


Figure 19 Diagnosis block diagram

5.4.1 DEN pin

The DEN input circuitry is compatible with 3.3 V and 5 V microcontroller or can be directly connected to V_S. The maximum voltage on the DEN pin is referenced to V_S and can go below the ground. See DEN pin in Table 3.

The figure below shows the electrical equivalent DEN input circuitry.

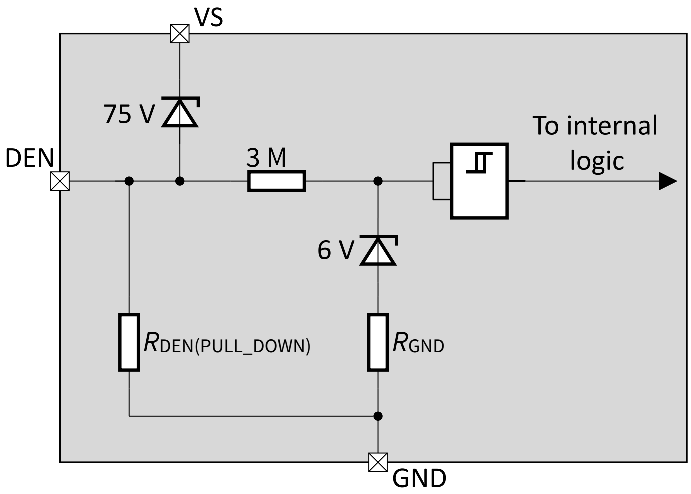


Figure 20 **Simplified schematics of the DEN pin circuitry**

5.4.2 Overview

Operation mode	V_{IN}	V_{DEN}	V_{OUT}	**Diagnosis output**
Normal condition	Low (OFF)	High	GND	$I_{IS(OFF)}$
Short circuit to GND			GND	$I_{IS(OFF)}$
Overtemperature			GND	$I_{IS(OFF)}$
Short circuit to VS			V_S	$I_{IS(FAULT)}$
Open load			$V_{OUT} > V_{OUT(OL\_OFF)}$ 1)	$I_{IS(FAULT)}$
			$V_{OUT} < V_{OUT(OL\_OFF)}$	$I_{IS(OFF)}$
Normal condition	High (ON)		~ V_S	$I_{IS} = I_L / dk_{ILIS} + I_{IS0}$
Short circuit to GND			GND	$I_{IS(FAULT)}$
Overtemperature			GND	$I_{IS(FAULT)}$
Short circuit to VS			V_S	$I_{IS} \leq I_L / dk_{ILIS} + I_{IS0}$
Open load			V_S	I_{IS0} if I_{IS0} positive, $I_{IS(OFF)}$ if I_{IS0} negative
All conditions	n.a.	Low	n.a.	$I_{IS(OFF)}$

1) With additional pull-up resistor

5.4.3 Diagnosis in on state

A current proportional to the load current is provided at IS pin when the following conditions are fulfilled:

- The power output stage is switched on with $V_S - V_{IS} > 3.5V$.
- The diagnosis is enabled.

- No fault is present or was present.
- The R_{IS} recommended value is 1kΩ.

A current $I_{IS(FAULT)}$ is provided at IS pin if:

- If a “hard” failure mode is present or was present.
- The diagnosis is enabled.

Figure 21 and Figure 22 show the current sense as function of the load current in the power DMOS. Usually, a pull-down resistor R_{IS} is connected to the current sense pin IS. The dotted curve represents the typical sense current, assuming a typical dk_{ILIS} factor value. The range between the two solid curves shows the sense accuracy range that the device is able to provide, at a defined current.

$$I_{IS} = \frac{I_L}{dk_{ILIS}} + I_{IS0} \text{ with } (I_{IS} \geq 0) \tag{4}$$

Where the definition of dk_{ILIS} is:

$$dk_{ILIS} = \frac{I_{L2} - I_{L1}}{I_{IS2} - I_{IS1}} \tag{5}$$

the definition I_{IS0} is:

$$I_{IS0} = I_{IS1} - \frac{I_{L1}}{dk_{ILIS}} \tag{6}$$

and the definition of I_{L0} is:

$$I_{L0} = I_{L1} - I_{IS1} \times dk_{ILIS} \tag{7}$$

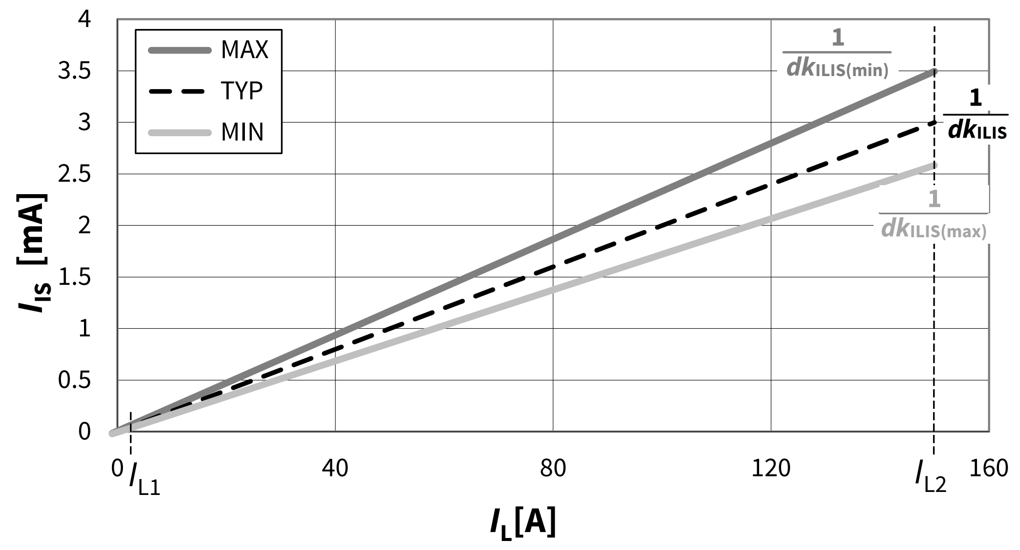


Figure 21 **Current sense at IS pin as a function of load current**

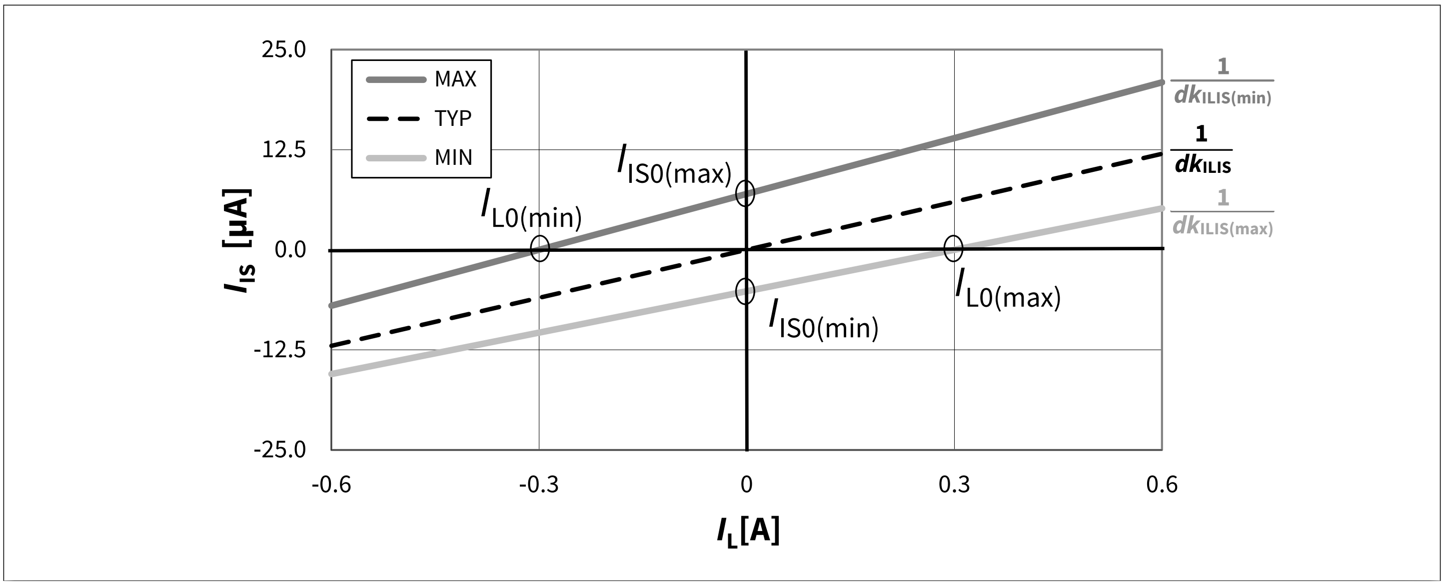


Figure 22 I_{IS0} and I_{L0} definition

5.4.3.1 Sense signal variation and calibration

In some applications, an enhanced accuracy is required around the device's nominal current range $I_{L(NOM)}$. To achieve this accuracy requirement, calibration on the application is possible. After two-point calibration, the device has a limited I_{IS} value spread at different load currents and temperature conditions. The I_{IS} variation can be described with the parameters $\Delta(dk_{ILIS(CAL)})$ and the $\Delta I_{IS0(CAL)}$. The grey solid line in Figure 23 is the current sense ratio after the two-point calibration at a given temperature. The slope of this line is defined as follows:

$$\frac{1}{\mathrm{d}k_{\mathrm{ILIS(CAL)}}} = \frac{I_{\mathrm{IS(CAL)2}} - I_{\mathrm{IS(CAL)1}}}{I_{\mathrm{L(CAL)2}} - I_{\mathrm{L(CAL)1}}} \tag{8}$$

The offset is defined as follows:

$$I_{\mathrm{IS0(CAL)}} = I_{\mathrm{IS(CAL)1}} - \frac{I_{\mathrm{L(CAL)1}}}{\mathrm{d}k_{\mathrm{ILIS(CAL)}}} = I_{\mathrm{IS(CAL)2}} - \frac{I_{\mathrm{L(CAL)2}}}{\mathrm{d}k_{\mathrm{ILIS(CAL)}}} \tag{9}$$

The grey area in Figure 23 is the range where the current sense ratio can vary across temperature and load current after performing the calibration. The accuracy of the load current sensing is improved and, given a sense current value I_{IS} (measured in the application), the load current can be calculated as follows, using the absolute value for $\Delta(dk_{ILIS(CAL)})$ instead of % values:

$$I_{\mathrm{L}} = \mathrm{d}k_{\mathrm{ILIS(CAL)}} \times \left(1 + \Delta\left(\mathrm{d}k_{\mathrm{ILIS(CAL)}}\right)\right) \times \left(I_{\mathrm{IS}} - I_{\mathrm{IS0(CAL)}} - \Delta I_{\mathrm{IS0(CAL)}}\right) \tag{10}$$

where $dk_{ILIS(CAL)}$ is the current sense ratio measured after two-point calibration (defined in Equation Max I_{IS0}, below), $I_{IS0(CAL)}$ is the current sense offset (calculated after two-point calibration, see Equation Min I_{IS0}, below, and $\Delta I_{IS0(CAL)}$ is the additional variation of the individual offset over lifetime and temperature. For calibration at 25°C $\Delta I_{IS0(CAL)}$ varies over temperature and lifetime for all positive $\Delta I_{IS0(CAL)}$ within the differences of the temperature-dependent maximum limits. All negative $\Delta I_{IS0(CAL)}$ vary within the differences of the temperature-dependent minimum limits. For positive $I_{IS0(CAL)}$ values ($I_{IS0(CAL)} > 0$):

$$MaxI_{\mathrm{IS0}}(@T_{\mathrm{J}} = 150°C) - MaxI_{\mathrm{IS0}}(@T_{\mathrm{J}} = 25°C) \le \Delta I_{\mathrm{IS0(CAL)}} \le MaxI_{\mathrm{IS0}}(@T_{\mathrm{J}} = -40°C) - MaxI_{\mathrm{IS0}}(@T_{\mathrm{J}} = 25°C) \tag{11}$$

For negative $I_{\mathrm{IS0(CAL)}}$ values ($I_{\mathrm{IS0(CAL)}} < 0$):

$$MinI_{\mathrm{IS0}}(@T_{\mathrm{J}} = 150°C) - MinI_{\mathrm{IS0}}(@T_{\mathrm{J}} = 25°C) \ge \Delta I_{\mathrm{IS0(CAL)}} \ge MinI_{\mathrm{IS0}}(@T_{\mathrm{J}} = -40°C) - MinI_{IS0}(@T_{\mathrm{J}} = 25°C) \tag{12}$$

There are four solutions for load current, considering that $\Delta(\mathrm{d}k_{\mathrm{ILIS(CAL)}})$ and $\Delta I_{\mathrm{IS0(CAL)}}$ can be both positive and negative. The load current I_{L} for any sense current I_{IS} spreads between a minimum I_{L} value resulting from the combination of lowest $\Delta(\mathrm{d}k_{\mathrm{ILIS(CAL)}})$ value and highest $\Delta I_{\mathrm{IS0(CAL)}}$ and a maximum I_{L} value resulting from the combination of highest $\Delta(\mathrm{d}k_{\mathrm{ILIS(CAL)}})$ value and lowest $\Delta I_{\mathrm{IS0(CAL)}}$.

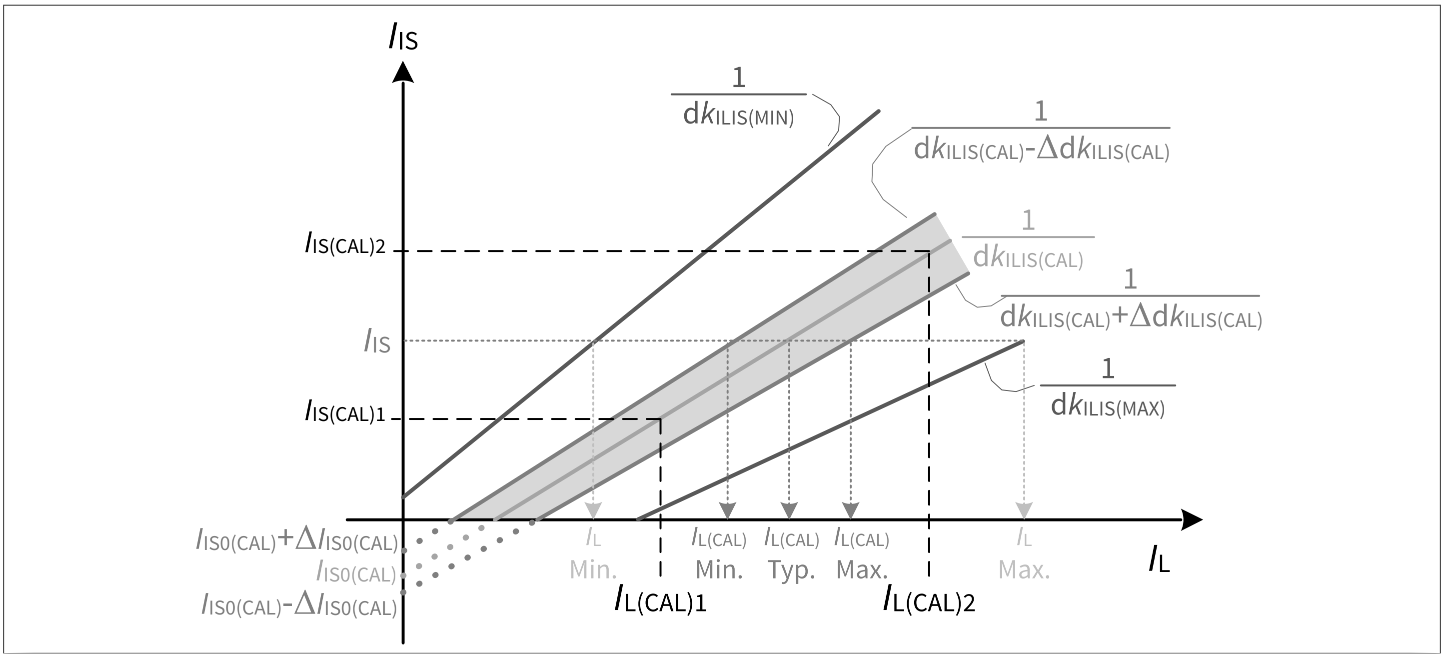


Figure 23 **Improved current sense accuracy after 2 points calibration**

5.4.3.2 Sense signal timing

The figure shows the timing during setting time and disabling of the sense.

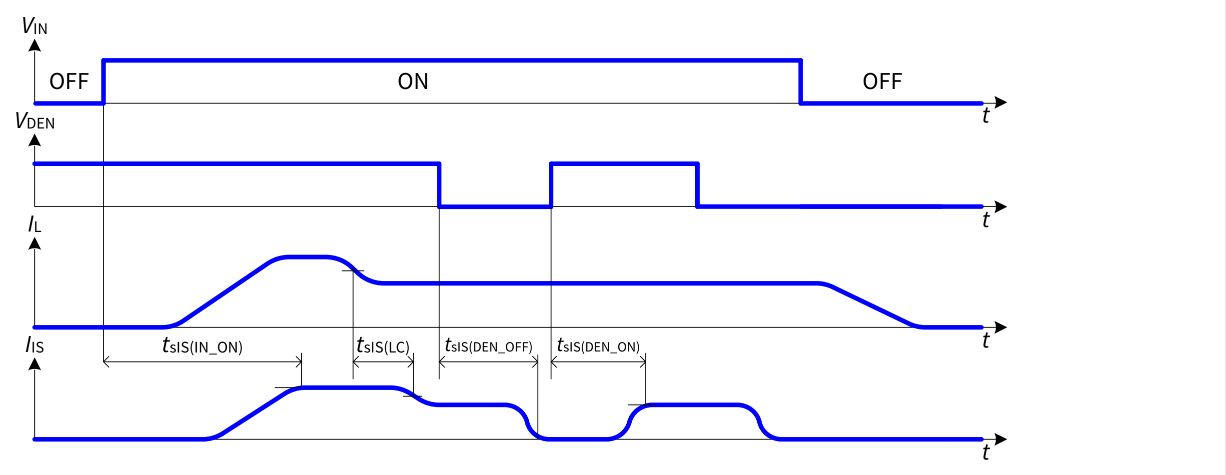


Figure 24 **Current sense timing in normal operation**

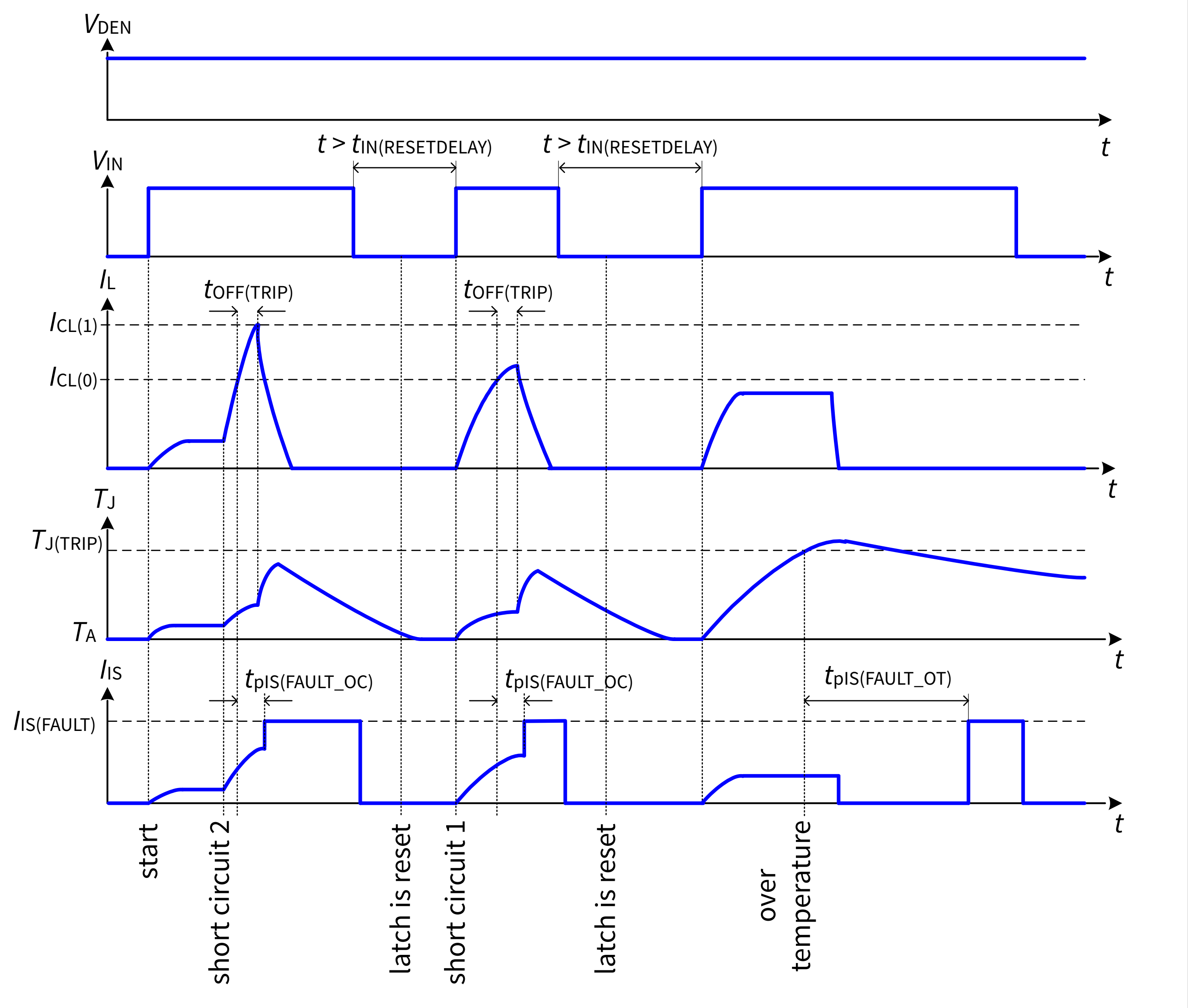


Figure 25 IS pin behavior under protection

5.4.4 Diagnosis in off state

The device features a detection of open load when off. An internal comparator is monitoring the V_{OUT}. If $V_{OUT} > V_{OUT(OL\_OFF)}$ and $V_{DEN} > V_{DEN(H)}$, the curent at IS pin is $I_{IS(FAULT)}$. In order to pull-up OUT in case of open load condition, an external pull-up resistor must be connected between VS and OUT pin. This external resistor must be switchable to keep the quiescent current as low as possible on VS pin.

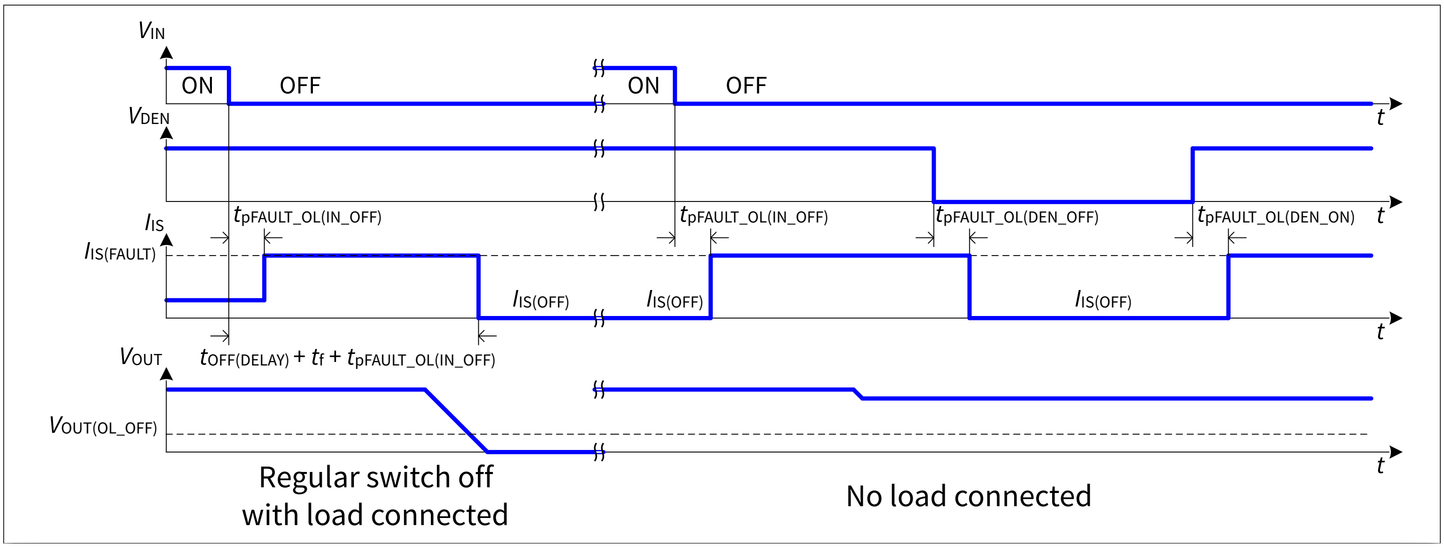


Figure 26 **Behavior of the open load detection in off feature with and without load connected**

5.5 Electrical characteristics

Table 6 **Electrical characteristics table**

V_S =5.8 V to 18 V, T_J = -40°C to +150°C unless otherwise specified. For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Operating and standby currents							
Standby current for whole device with load	$I_{VS(OFF)}$	–	1	3	µA	$V_{OUT} = 0$ V $V_{IN} = 0$V $V_{DEN} = 0$V $T_J \leq 85$°C After 10ms	PRQ-73
Standby current for whole device with load	$I_{VS(OFF\_DEN)}$	–	120	300	µA	$V_{OUT} = 0$ V $V_{IN} = 0$V $V_{DEN} = 5$V $T_J \leq 85$°C After 10ms	PRQ-258
Standby current for whole device with load	$I_{VS(OFF)}$	–	35	100	µA	$V_{OUT} = 0$ V $V_{IN} = 0$ V $V_{DEN} = 0$ V $T_J \leq 150$°C After 10ms	PRQ-74
Supply current on GND pin	$I_{GND(ON)}$	–	2	5	mA	$V_{IN(H)} \leq V_{IN} \leq V_S$ $V_{DEN(H)} \leq V_{DEN} \leq V_S$	PRQ-186
Ground resistor	R_{GND}	130	180	230	Ω	–	PRQ-173

(table continues...)

Table 6 (continued) Electrical characteristics table

V_S =5.8 V to 18 V, T_J = -40°C to +150°C unless otherwise specified. For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power stage							
On-state resistance in forward condition	$R_{DS(ON)}$	–	0.6	–	mΩ	[1] T_J = 25°C $V_S \geq$ 5.8 V	PRQ-76
On-state resistance in forward condition	$R_{DS(ON)}$	–	0.85	1.1	mΩ	T_J = 150°C $V_S \geq$ 5.8 V	PRQ-75
On-state resistance in forward condition, low battery voltage	$R_{DS(ON)}$	–	0.75	–	mΩ	[1] T_J = 25°C $V_S \geq$ 3.1 V	PRQ-78
On-state resistance in forward condition, low battery voltage	$R_{DS(ON)}$	–	1.2	4	mΩ	T_J = 150°C $V_S \geq$ 3.1 V	PRQ-77
On-state resistance in inverse condition	$R_{DS(INV)}$	–	0.6	–	mΩ	[1] T_J = 25°C	PRQ-328
On-state resistance in inverse condition	$R_{DS(INV)}$	–	0.85	1.1	mΩ	T_J = 150°C	PRQ-331
Nominal load current	$I_{L(NOM)}$	57	65	–	A	[1] T_A = 85°C, $T_J \leq$ 150°C, $R_{thJA(2S2P)}$	PRQ-81
Drain to source smart clamp voltage VDS(CL) = VS - VOUT	$V_{DS(CL)}$	35	–	–	V	I_L = 10 mA	PRQ-82
Drain to source smart clamp voltage VDS(CL) = VS - VOUT after short circuit detection	$V_{DS(CL\_SC)}$	28.5	–	–	V	After activation of the short circuit protection ($I_L > I_{CL(0)}$)	PRQ-316
Fast turn off detection voltage	$V_{DS(FAST\_OFF)}$	19	22	25	V	–	PRQ-165
Body diode forward voltage	V_F	–	0.6	0.8	V	I_L = -40 A T_J = 150°C	PRQ-83
Output leakage current	$I_{OUT(OFF)}$	–	1	3	µA	V_S = 18 V V_{OUT} = 0 V V_{IN} = 0 V V_{DEN} = 0 V $T_J \leq$ 85°C (10ms after V_{IN} = 0V)	PRQ-84
Output leakage current	$I_{OUT(OFF)}$	–	35	100	µA	V_S = 18 V V_{OUT} = 0 V V_{IN} = 0 V V_{DEN} = 0 V $T_J \leq$ 150°C (10ms after V_{IN} = 0V)	PRQ-166

(table continues...)

Table 6 (continued) Electrical characteristics table

V_S =5.8 V to 18 V, T_J = -40°C to +150°C unless otherwise specified. For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Turn on slew rate VOUT = 25% to 50% VS	$dV_{ON/dt}$	0.15	0.3	0.6	V/µs	R_L = 0.32 Ω V_S = 13.5 V	PRQ-86
Turn off slew rate VOUT = 50% to 25% VS	$-dV_{OFF/dt}$	0.15	0.3	0.6	V/µs	R_L = 0.32 Ω V_S = 13.5 V	PRQ-87
Rising time during turn on VOUT from 20% to 80% of VS	t_r	15	40	90	µs	R_L = 0.32 Ω V_S = 13.5 V	PRQ-88
Falling time during turn off VOUT from 80% to 20% of VS	t_f	15	30	60	µs	R_L = 0.32 Ω V_S = 13.5 V	PRQ-89
Turn on time to VOUT = 20% of VS	$t_{ON(DELAY)}$	17.5	45	105	µs	R_L = 0.32 Ω V_S = 13.5 V	PRQ-90
Turn off time to VOUT = 80% of VS	$t_{OFF(DELAY)}$	40	100	160	µs	R_L = 0.32 Ω V_S = 13.5 V	PRQ-91
Turn on time to VOUT = 80% of VS	t_{ON}	35	85	190	µs	R_L = 0.32 Ω V_S = 13.5 V	PRQ-339
Turn off time to VOUT = 20% of VS	t_{OFF}	55	130	220	µs	R_L = 0.32 Ω $V_S \leq$ 13.5 V	PRQ-342
Switch on energy	E_{ON}	–	9.5	–	mJ	1) R_L = 0.32 Ω V_S = 13.5 V	PRQ-92
Switch off energy	E_{OFF}	–	5.5	–	mJ	1) R_L = 0.32 Ω V_S = 13.5 V	PRQ-93
VS pin							
Power supply undervoltage shutdown	$V_{S(UVL)}$	2.3	2.7	3.1	V	V_S decreasing	PRQ-184
Power supply undervoltage turn on	$V_{S(UVH)}$	4	4.8	5.8	V	V_S increasing	PRQ-185
Input pin							
High level input voltage	$V_{IN(H)}$	–	–	2.5	V	–	PRQ-171
Low level input voltage	$V_{IN(L)}$	0.5	–	–	V	–	PRQ-170
Input voltage hysteresis	$V_{IN(HYS)}$	–	0.2	–	V	–	PRQ-94
Input pull-down resistor	$R_{IN(PULL\_DOWN)}$	100	200	–	kΩ	–	PRQ-95
DEN pin							
High level DEN voltage	$V_{DEN(H)}$	–	–	2.5	V	–	PRQ-172

(table continues...)

Table 6 (continued) Electrical characteristics table

V_S =5.8 V to 18 V, T_J = -40°C to +150°C unless otherwise specified. For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Low level DEN voltage	$V_{DEN(L)}$	0.5	–	–	V	–	PRQ-304
DEN voltage hysteresis	$V_{DEN(HYS)}$	–	0.2	–	V	–	PRQ-303
DEN pull-down resistor	$R_{DEN(PULL\_DOWN)}$	100	200	–	kΩ	–	PRQ-183
Protection: reverse polarity							
On-state resistance in reverse polarity	$R_{DS(REV)}$	–	0.7	1.4	mΩ	-18 V ≤ V_S ≤ -8 V T_J ≤ 150°C	PRQ-96
Protection: overload							
Current trip detection level	$I_{CL(0)}$	150	215	275	A	T_J = -40°C	PRQ-362
Current trip detection level	$I_{CL(0)}$	150	210	265	A	[1] T_J = 25°C	PRQ-97
Current trip detection level	$I_{CL(0)}$	150	200	250	A	T_J = 150°C	PRQ-370
Current trip detection level at low voltage	$I_{CL(0\_UV)}$	35	200	300	A	3.1 V ≤ V_S ≤ 5.8 V	PRQ-98
Current trip maximum level	$I_{CL(1)}$	150	220	285	A	dI_L/dt = 1 A/µs T_J = -40°C	PRQ-364
Current trip maximum level	$I_{CL(1)}$	150	215	275	A	[1] dI_L/dt = 1 A/µs T_J = 25°C	PRQ-99
Current trip maximum level	$I_{CL(1)}$	150	205	260	A	dI_L/dt = 1 A/µs T_J = 150°C	PRQ-365
Overload shutdown delay time	$t_{OFF(TRIP)}$	–	7	15	µs	–	PRQ-100
Thermal shutdown temperature	$T_{J(TRIP)}$	150	175	200	°C	[1] 3.1 V ≤ V_S ≤ 28 V	PRQ-101
Overpower shutdown detection level	$V_{DS(PSD)}$	700	850	1000	mV	[1]	PRQ-102
Overpower shutdown activation level	$V_{S(PSD)}$	3.5	4.3	5.3	V	[1]	PRQ-103
Overpower shutdown time	$t_{PSD(UV)}$	10	–	300	µs	Time defined from $V_S \le V_{S(PSD)}$ and $V_{DS} \ge V_{DS(PSD)}$ until $I_{IS} = I_{IS(FAULT)}$	PRQ-104
Diagnosis function: sense pin							
Current sense differential ratio	dk_{ILIS}	43000	50000	58000	–	I_{L0} max ≤ I_L ≤ $I_{CL(0)}$ min V_S - V_{IS} ≥ 3.5 V	PRQ-106

(table continues...)

Table 6 (continued) Electrical characteristics table

V_S =5.8 V to 18 V, T_J = -40°C to +150°C unless otherwise specified. For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Calculated sense offset load current IS= 0 A	I_{L0}	-300	0	300	mA	$V_S - V_{IS} \geq 3.5$ V T_J = -40°C	PRQ-107
Calculated sense offset load current IS= 0 A	I_{L0}	-275	0	275	mA	1) $V_S - V_{IS} \geq 3.5$ V T_J = 25°C	PRQ-245
Calculated sense offset load current IS= 0 A	I_{L0}	-250	0	250	mA	$V_S - V_{IS} \geq 3.5$ V T_J = 150°C	PRQ-246
Calculated sense offset current IL = 0 A	I_{IS0}	-5.17	0	6.98	µA	1) $V_S - V_{IS} \geq 3.5$ V T_J = -40°C	PRQ-108
Calculated sense offset current IL = 0 A	I_{IS0}	-4.74	0	6.40	µA	1) $V_S - V_{IS} \geq 3.5$ V T_J = 25°C	PRQ-248
Calculated sense offset current IL = 0 A	I_{IS0}	-4.31	0	5.81	µA	1) $V_S - V_{IS} \geq 3.5$ V T_J = 150°C	PRQ-169
Current sense ratio spread over temperature and repetitive pulse operation	$\Delta(dk_{ILIS(CAL)})$	-5	0	+5	%	1)	PRQ-111
Diagnosis function in normal condition							
Current sense settling time until 90% and 110% of IIS stable after turn on	$t_{sIS(IN\_ON)}$	–	400	700	µs	$V_S - V_{IS} \geq 3.5$ V $R_L = 0.32\ \Omega$	PRQ-112
Current sense settling time to IIS stable after turn on	$t_{sIS(IN\_ON)}$	–	1000	1500	µs	$V_S - V_{IS} \geq 3.5$ V $R_L = 0.32\ \Omega$	PRQ-288
Current sense settling time to IIS stable after activation of DEN	$t_{sIS(DEN\_ON)}$	–	40	85	µs	$V_S - V_{IS} \geq 3.5$ V	PRQ-177
Current sense disable time	$t_{sIS(DEN\_OFF)}$	–	5	25	µs	From DEN falling edge to $I_{IS} = I_{IS(OFF)}$	PRQ-178
Current sense settling time after load change	$t_{sIS(LC)}$	–	40	–	µs	1) $V_S - V_{IS} \geq 3.5$ V $I_L \geq I_{L0(MAX)}$	PRQ-114
IIS leakage current when DEN is disabled	$I_{IS(OFF)}$	–	–	1	µA	$V_{DEN} < V_{DEN(L)}$ $R_{IS} = 1$ kΩ; $T_J \leq 150$°C	PRQ-113
Diagnosis function in overload condition							
Sense signal current in fault condition	$I_{IS(FAULT)}$	4	13	20	mA	$V_S - V_{IS} \geq 3.5$ V Typ value: $V_S - V_{IS} \geq 8$ V	PRQ-105

(table continues...)

Table 6 **(continued) Electrical characteristics table**

V_S =5.8 V to 18 V, T_J = -40°C to +150°C unless otherwise specified. For a given temperature or voltage range, typical values are specified at V_S = 13.5 V, T_J = 25°C.

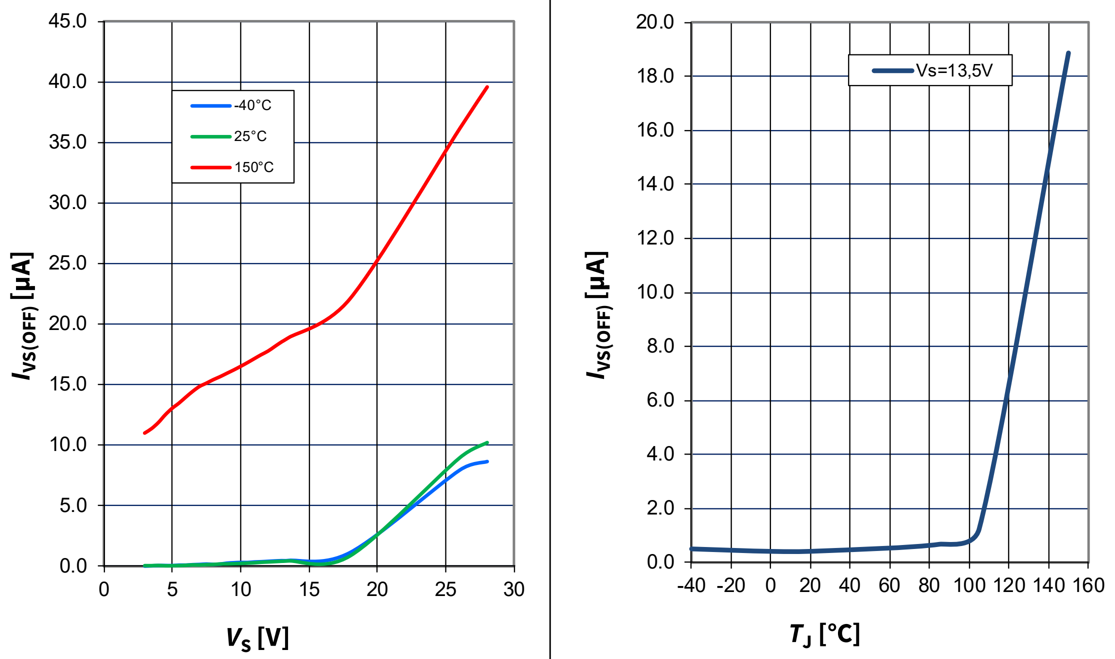
Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Fault propagation time for short circuit detection	$t_{\mathrm{pIS(FAULT\_OC)}}$	–	3	30	µs	–	PRQ-115
Fault propagation time for overtemperature detection	$t_{\mathrm{pIS(FAULT\_OT)}}$	–	1.5	2.5	ms	[1]	PRQ-116
Delay time to reset fault pin after turning off VIN	$t_{\mathrm{IN(RESETDELAY)}}$	6	–	5000	µs	–	PRQ-117
Diagnosis function open load off							
Open load detection threshold in off state voltage control	$V_{\mathrm{OUT(OL\_OFF)}}$	2	3	4	V	V_{IN}<$V_{\mathrm{IN(L)}}$ and V_{DEN} > $V_{\mathrm{DEN(H)}}$	PRQ-174
Fault propagation time for open load detection off during turn off	$t_{\mathrm{pFAULT\_OL(IN\_OFF)}}$	–	10	30	µs	From falling edge on V_{IN} to $I_{\mathrm{S(FAULT)}}$ on IS pin V_{DEN} > $V_{\mathrm{DEN(H)}}$ V_{OUT} > $V_{\mathrm{OUT(OL\_OFF)}}$	PRQ-179
Fault propagation time for open load detection off after activation of DEN	$t_{\mathrm{pFAULT\_OL(DEN\_ON)}}$	–	5	30	µs	From rising edge on V_{DEN} to $I_{\mathrm{IS(FAULT)}}$ on IS pin V_{IN} < $V_{\mathrm{IN(L)}}$ V_{OUT} > $V_{\mathrm{OUT(OL\_OFF)}}$	PRQ-180
Disable time of IIS(FAULT) in off condition after desactivation of DEN	$t_{\mathrm{pFAULT\_OL(DEN\_OFF)}}$	–	5	40	µs	From falling edge on V_{DEN} to $I_{\mathrm{IS(OFF)}}$ on IS pin V_{IN} < $V_{\mathrm{IN(L)}}$	PRQ-181

[1] Not subject to production test, specified by design.

6 Typical performance characteristics

Standby current for whole device with load, $I_{VS(OFF)} = f(V_S, T_J)$

Standby current for whole device with load, $I_{VS(OFF)} = f(T_J)$, at V_S = 13.5 V



GND current when IN and DEN are biased to VS, $I_{GND(ON)} = f(V_S, T_J)$

GND current when IN and DEN are biased to 5.5 V, $I_{GND(ON)} = f(V_S, T_J)$

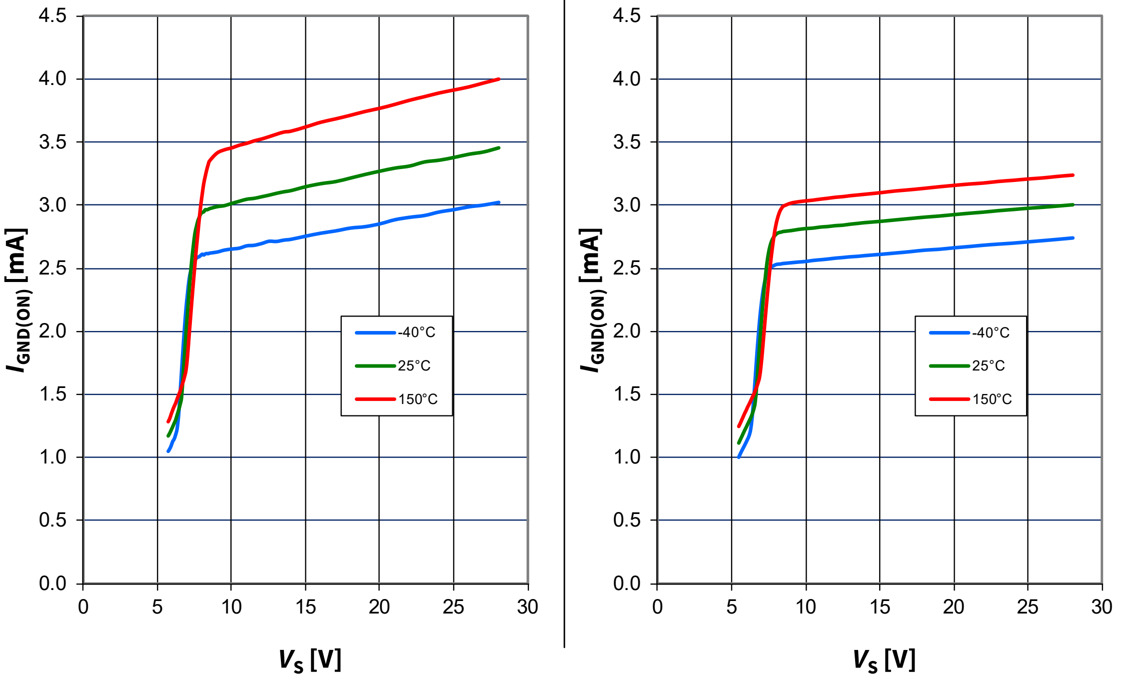
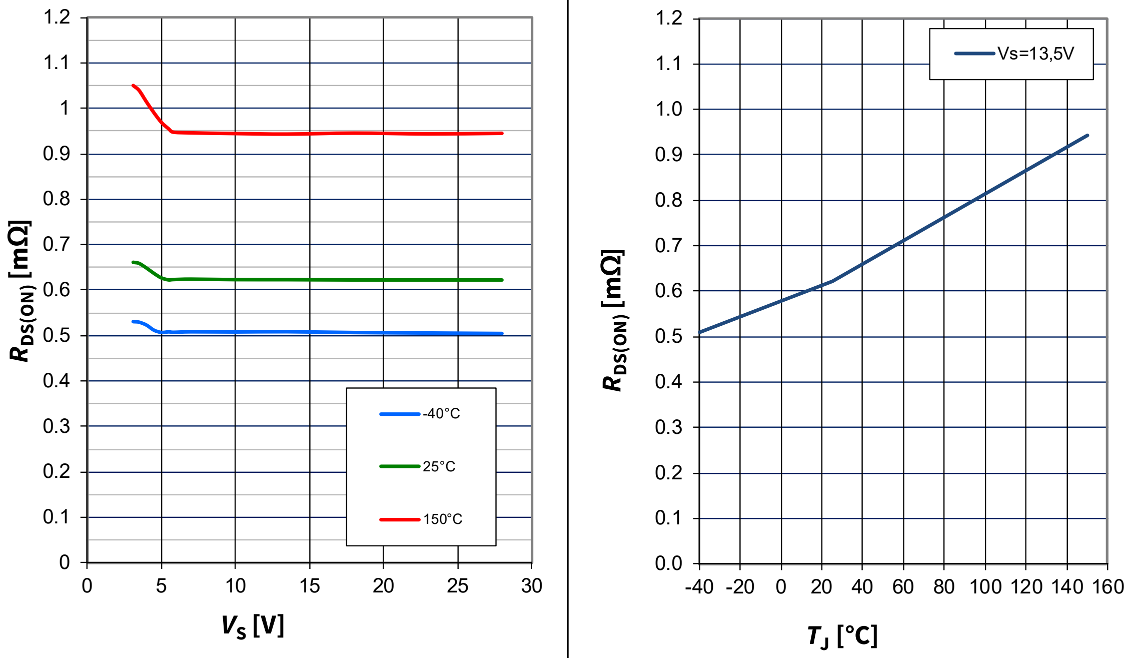


Figure 27 **Typical performance characteristics**



ON state resistance at I_L = 65 A
$R_{DS(ON)} = f(V_S, T_J)$

ON state resistance at I_L = 65 A and V_S = 13.5 V
$R_{DS(ON)} = f(T_J)$

Turn ON time
$t_{ON} = f(V_S, T_J)$, $R_L = 0.32\ \Omega$

Turn OFF time
$t_{ON} = f(V_S, T_J)$, $R_L = 0.32\ \Omega$

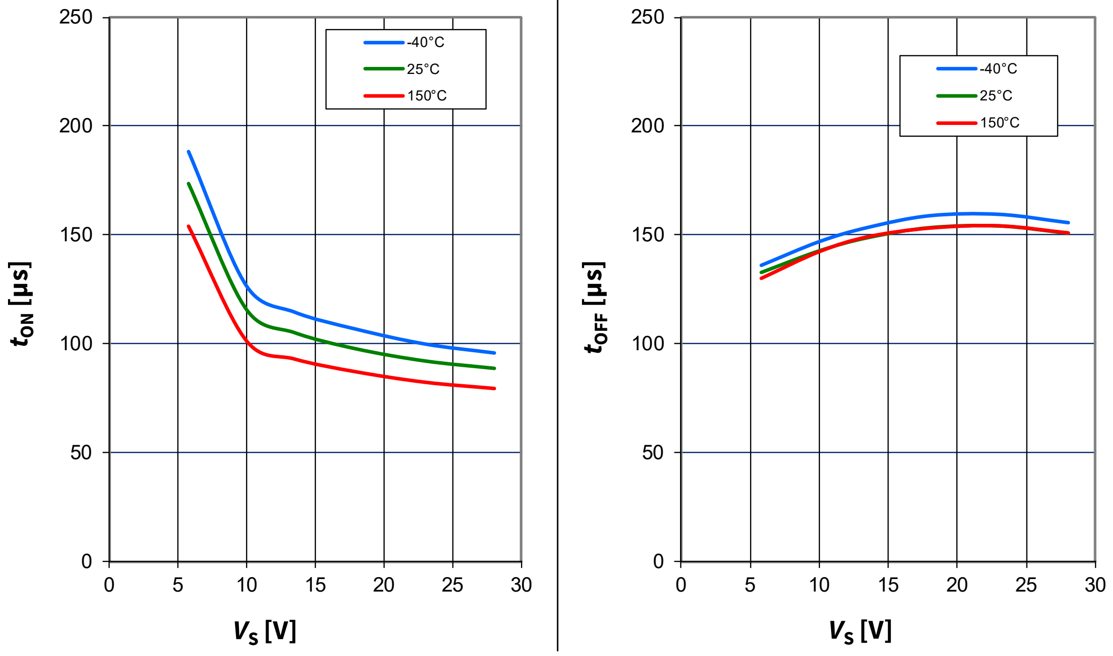
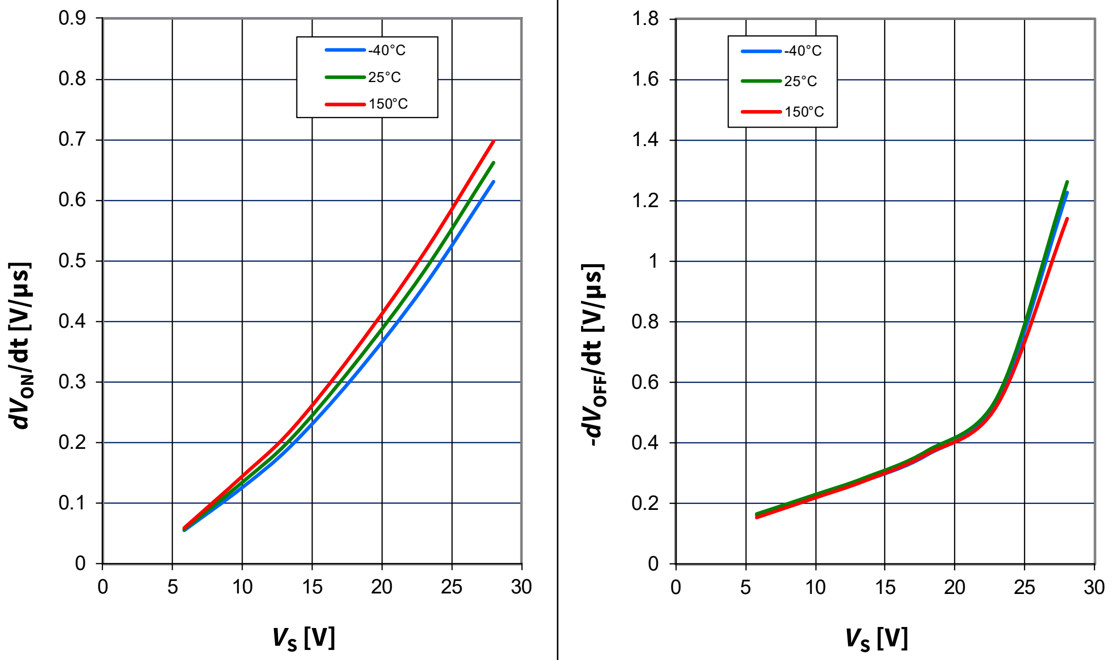
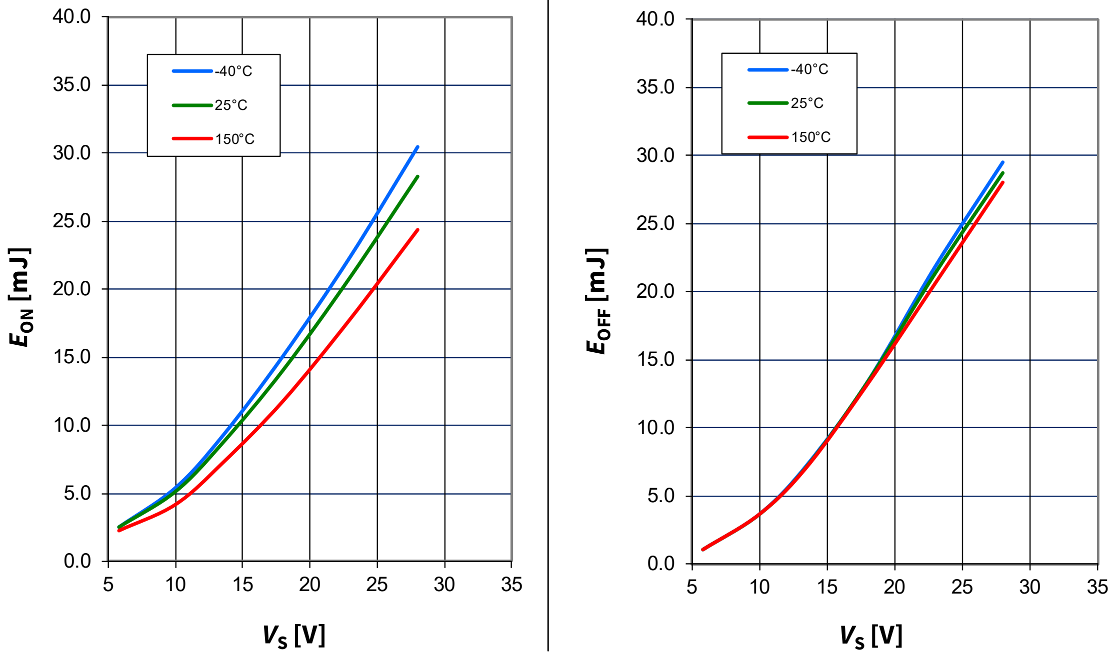


Figure 28 Typical performance characteristics (continued)



Slew rate at turn ON
$dV_{ON/dt}$ = f(V_S, T_J), R_L = 0.32 Ω

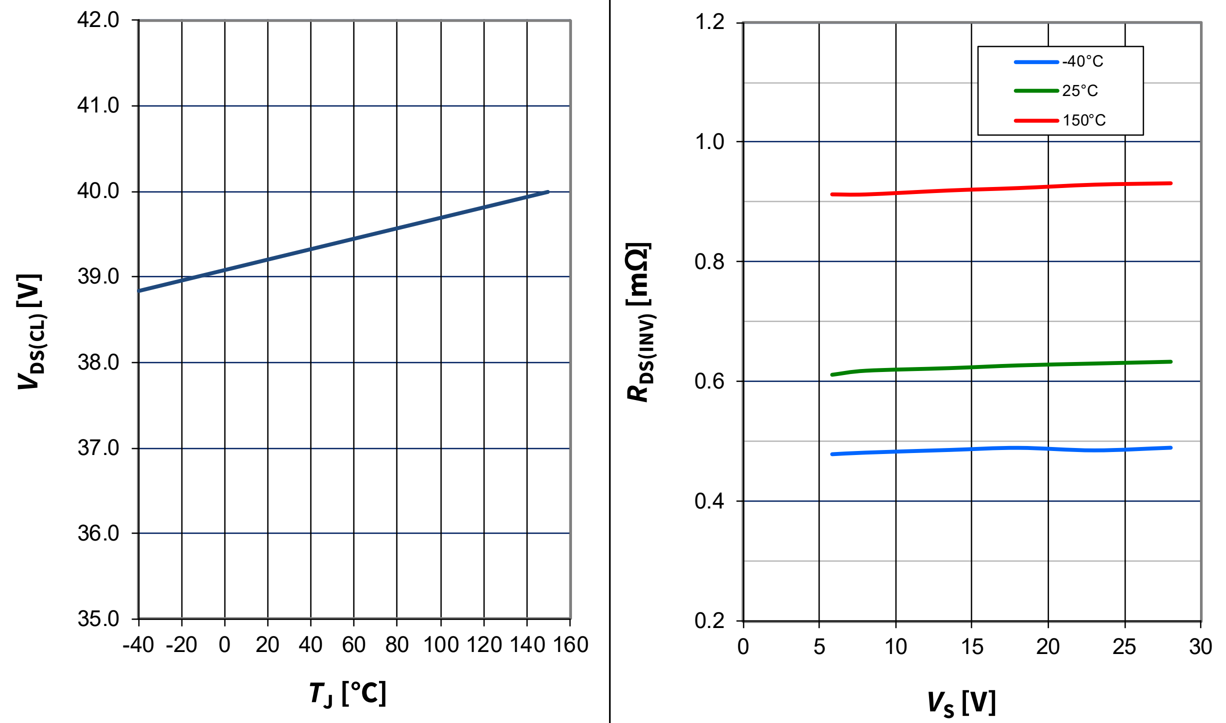
Slew rate at turn OFF
$-dV_{OFF/dt}$ = f(V_S, T_J), R_L = 0.32 Ω



Energy at turn ON
E_{ON} = f(V_S, T_J), R_L = 0.32 Ω

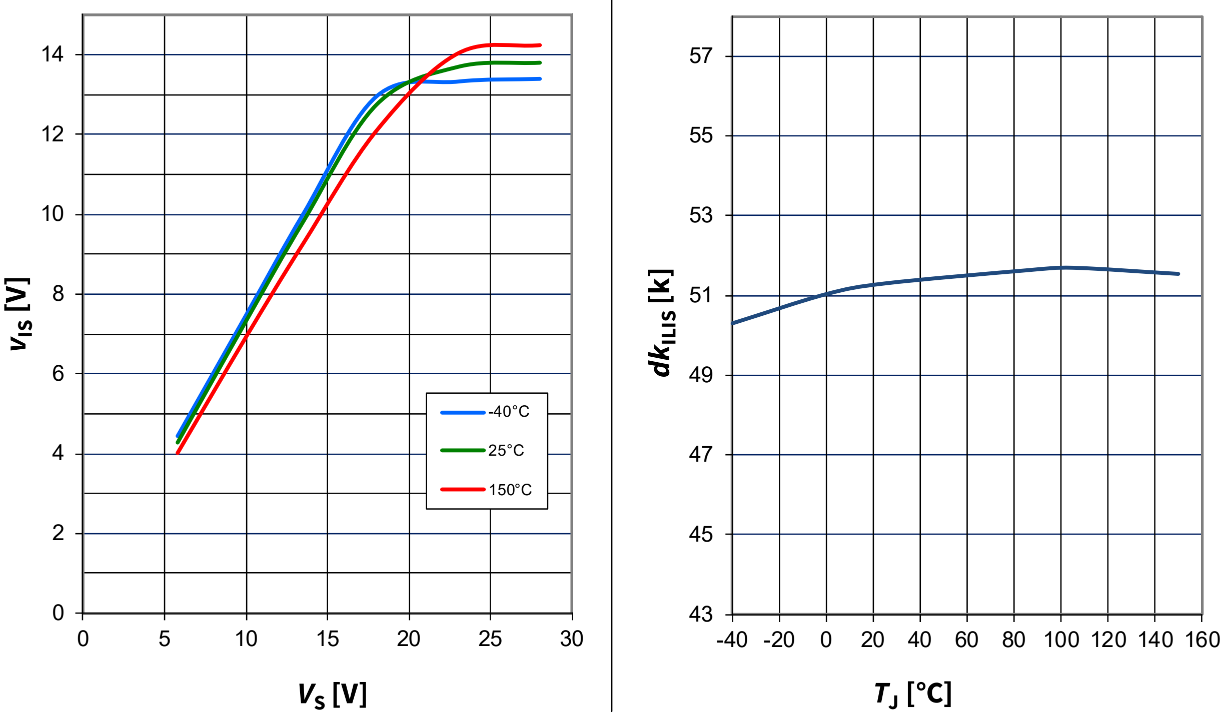
Energy at turn OFF
E_{OFF} = f(V_S, T_J), R_L = 0.32 Ω

Figure 29 **Typical performance characteristics (continued)**



Drain to source smart clamp voltage
$V_{DS(CL)} = f(T_J)$

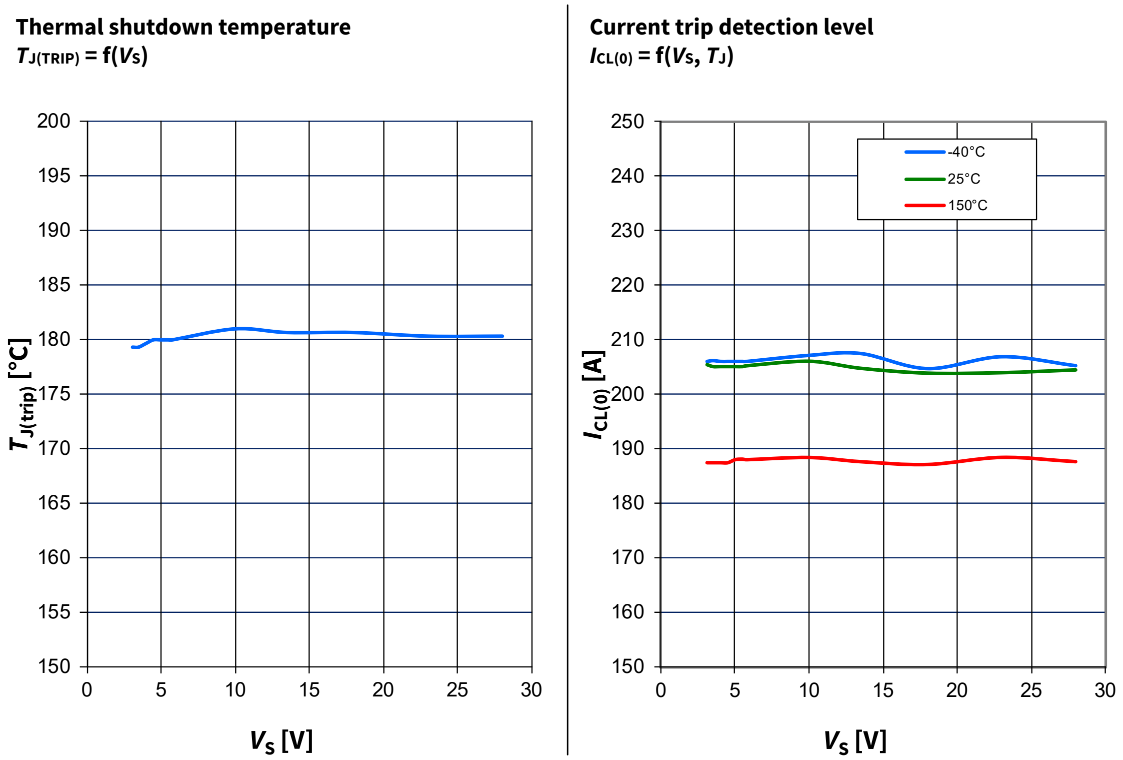
ON resistance in inverse at I_L = -50 A
$R_{DS(INV)} = f(V_S)$



Voltage on IS in fault
$V_{IS} = f(V_S, T_J)$, R_{IS} = 1.0 kΩ

Current sense differential ratio
$dk_{ILIS} = f(T_J)$

Figure 30 Typical performance characteristics (continued)



Thermal shutdown temperature
$T_{J(TRIP)} = f(V_S)$

Current trip detection level
$I_{CL(0)} = f(V_S, T_J)$

Figure 31 Typical performance characteristics (continued)

7 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. This is a very simplified example of an application circuit. The function must be verified in the real application.

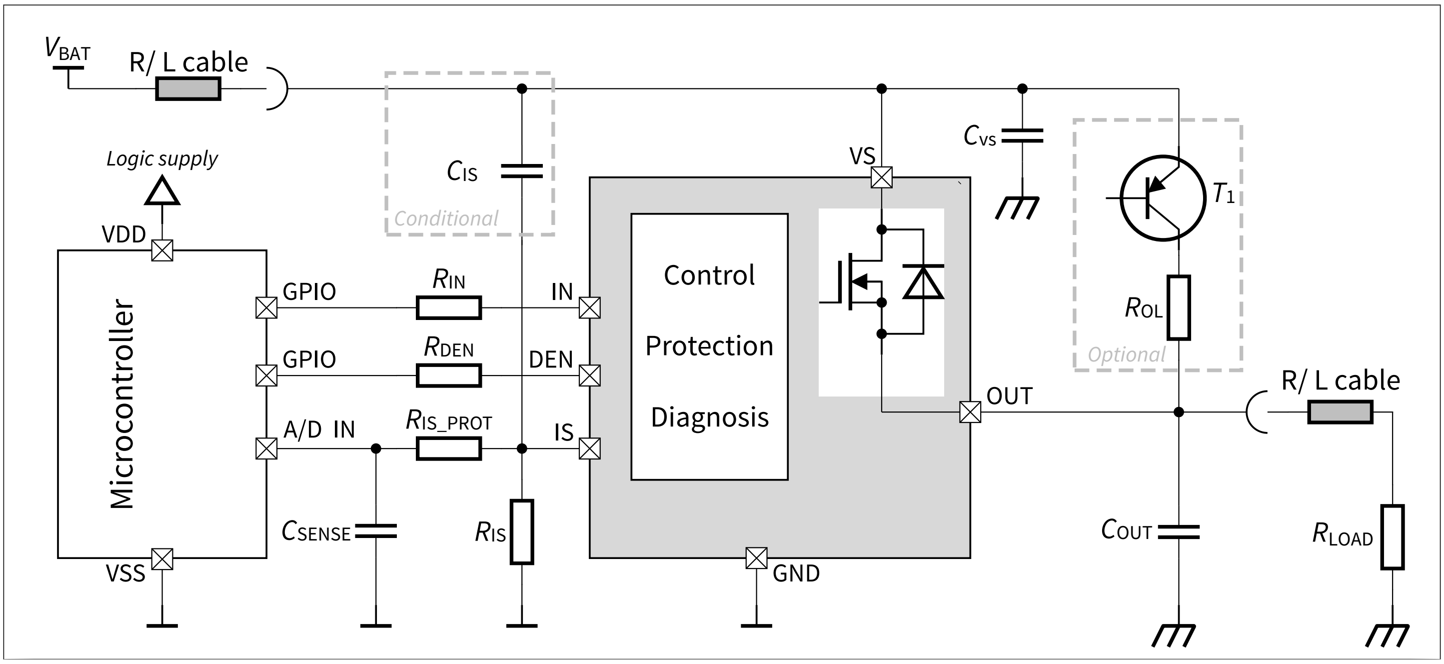


Figure 32 Application diagram: device controlled by a microcontroller

Table 7 Bill of material

Reference	Value	Purpose
R_{IN}	4.7 kΩ	Protection of the microcontroller during reverse polarity
R_{DEN}	4.7 kΩ	Protection of the microcontroller during reverse polarity
R_{IS}	1 kΩ	Sense resistor
R_{IS_PROT}	4.7 kΩ	Protection of the microcontroller during reverse polarity and during loss of ground
C_{SENSE}	10 nF	Sense signal filtering
C_{VS}	100 nF	Improved EMC behavior
C_{OUT}	10 nF	Protection against EMC
R_{OL}	Application specific	Open load detection off state to have V_{OUT} higher than $V_{OUT(OL\_OFF)}$. The value depends on the leakage outside the ECU between OUT and GND
C_{IS}	1 nF	Conditional: connect if R_{IS} is bigger than 2 kΩ

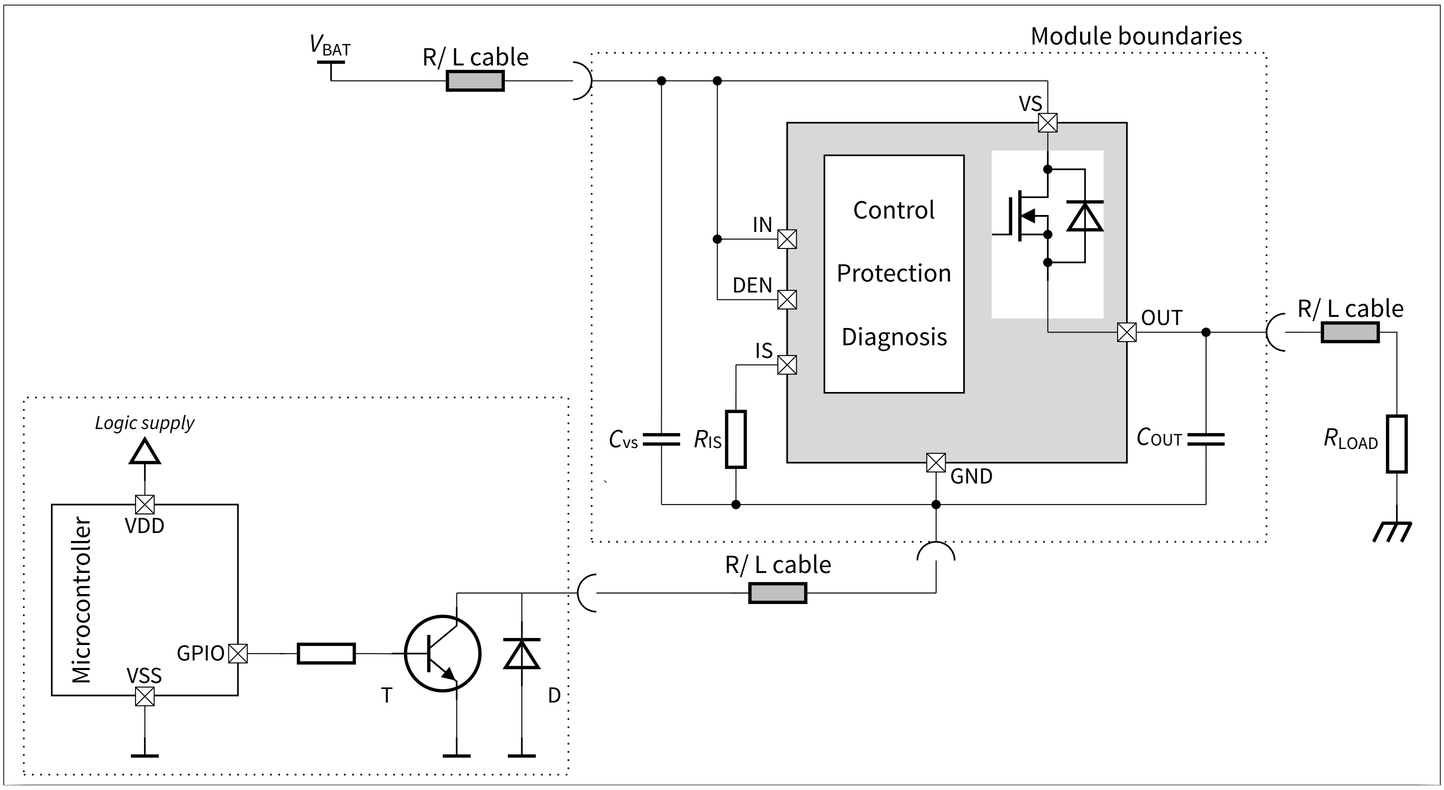


Figure 33 Application diagram: solid state relay for direct relay replacement

Table 8 Bill of material

Reference	Value	Purpose
R_{IS}	1 kΩ	Sense resistor
C_{VS}	100 nF	Improved EMC behavior
C_{OUT}	10 nF	Protection against EMC
T	Bipolar or MOSFET	Switch to turn on and off the device
D	–	Enable Reverse ON protection during reverse battery. Not required if a MOSFET is used for T

8 Package information

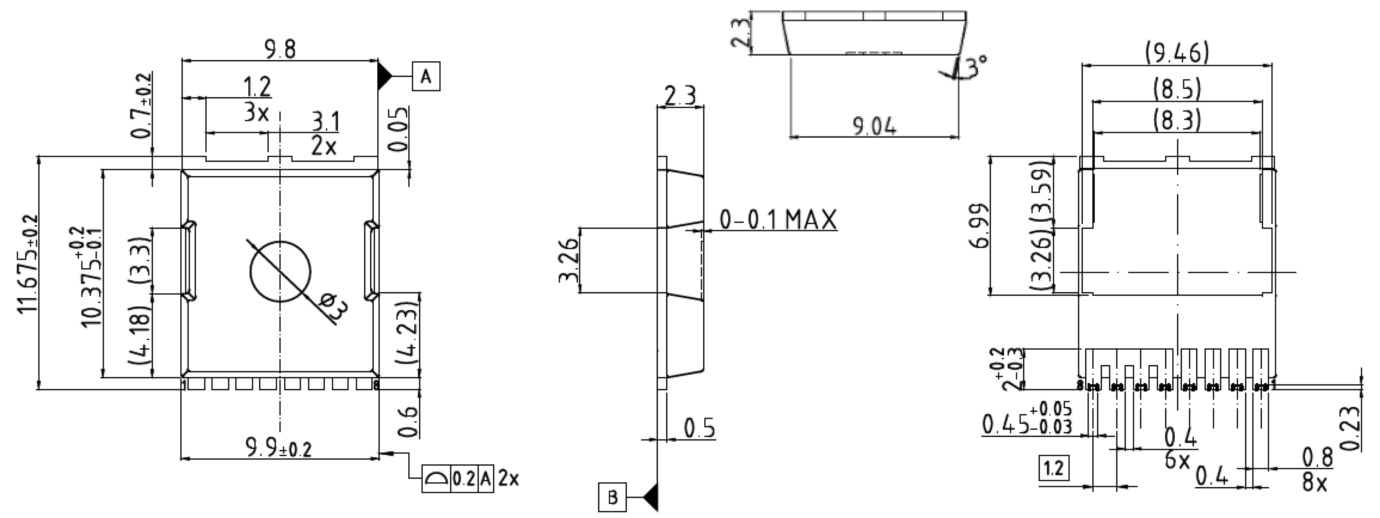


Figure 34 PG-HSOF-8 (8-pin TO-Leadless) package dimensions

Green Product (RoHS compliant) To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

9 Revision history

Revision	Date	Changes
1.00	2022-12-02	Datasheet released
1.01	2023-01-23	Footnote "Not subject to production test, specified by design" added where it was missing.
1.10	2023-04-18	- Footnote "Not subject to production test, specified by design" added to the PRQ-102, PRQ-103, PRQ-116. - I_{OUT}, I_{DS} and I_{LOAD} replaced by I_L as defined in the Figure 4 - Note added at the end of the Chapter 4.1 - Minor editorial changes

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Edition 2023-04-18

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-qom1622555714287

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