OPAx836 极低功耗、轨到轨输出、负轨输入、电压反馈运算放大器

1 特性

- 低功耗：
  - 电源电压：2.5V 至 5.5V
  - 静态电流：1mA（典型值）
  - 断电模式：0.5μA（典型值）
- 带宽：205MHz
- 压摆率：560V/μs
- 上升时间：3ns (2VSTEP)
- 稳定时间 (0.1%)：22ns (2VSTEP)
- 过驱恢复时间：60ns
- SNR：在 1kHz (1VRMS) 时为 0.00013% (-117.6dBc)
- THD：在 1kHz (1VRMS) 时为 0.00003% (-130dBc)
- HD2/HD3：在 1MHz (2VPP) 时为 -85dBc/-105dBc
- 输入电压噪声：4.6nV/√Hz (f = 100kHz)
- 输入失调电压：65μV（最大 ±400μV）
- CMRR：116dB
- 输出电流驱动：50mA
- RRO：轨到轨输出
- 输入电压范围：
  - –0.2V 到 +3.9V（5V 电源）
- 工作温度范围：
  - –40°C 至 +125°C

2 应用

- 低功耗信号调节
- 音频模数转换器 (ADC) 输入缓冲器
- 低功耗逐次逼近寄存器 (SAR) 和三角积分 (ΔΣ) ADC 驱动器
- 便携式系统
- 低功耗系统
- 高密度系统

3 说明

OPA836 和 OPA2836 器件 (OPAx836) 为单通道和双通道超低功耗、轨至轨输出、负电源轨输入、电压反馈 (VFB) 运算放大器，依设计可由 2.5V 至 5.5V 范围内的单电源或者 ±1.25V 至 ±2.75V 范围内的双电源供电运行。这些轨至轨放大器每通道仅消耗 1mA 的电流，单位增益带宽为 205MHz，功耗/性能比处于先进水平。

OPA836 和 OPA2836 器件同时拥有低功耗特性和出色的高频性能，并且可提供其他同类器件所无法达到的性能/功耗比，因此非常适合注重功耗的电池供电类便携式应用。这些器件还具有节能模式，可将电流降至 1.5μA 以下，这对于电池供电类应用中的高频放大器而言是极具吸引力的解决方案。

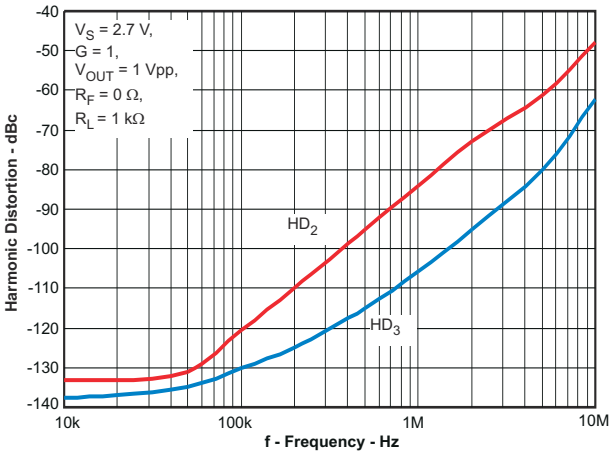
OPA836 RUN 封装选件包含集成的增益设置电阻器，因此可在印刷电路板上实现超小的尺寸（约 2.00mm × 2.00mm）。通过在 PCB 上添加电路迹线，可实现 +1、–1、–1.33、+2、+2.33、–3、+4、–4、+5、–5.33、+6.33、–7、+8 的增益和 –0.1429、–0.1875、–0.25、–0.33、–0.75 的反相衰减。有关详细信息，请参见表 9-1 和表 9-2。

OPA836 和 OPA2836 器件在 –40°C 至 +125°C 的扩展工业温度范围内运行。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA836	SOT-23 (6)	2.90mm × 1.60mm
	WQFN (10)	2.00mm x 2.00mm
OPA2836	SOIC (8)	4.90mm × 3.91mm
	VSSOP (10)	3.00mm × 3.00mm
	UQFN (10)	2.00mm x 2.00mm
	WQFN (10)	2.00mm x 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



谐波失真与频率间的关系

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (October 2016) to Revision J (March 2021) — **Page**

- 更新了整个文档的表、图和交叉参考的编号格式 1
- Changed the input impedance common mode conditions From: = 200 || 1.2 kΩ || pF (Typical) To: 100 || 1.2 MΩ || pF (Typical) 9
- Changed the input impedance differential mode conditions From: = 200 || 1 kΩ || pF (Typical) To: 100 || 1 kΩ || pF (Typical) 9
- Changed the input impedance common mode conditions From: = 200 || 1.2 kΩ || pF (Typical) To: 100 || 1.2 MΩ || pF (Typical) 12
- Changed the input impedance differential mode conditions From: = 200 || 1 kΩ || pF (Typical) To: 100 || 1 kΩ || pF (Typical) 12

Changes from Revision H (September 2016) to Revision I (October 2016) — **Page**

- 更改了整个数据表中各节的文本，使之更加清晰准确 1
- Changed "R_G = ∞ Ω (open)" to "R_G = open" 32
- Changed "gain tracking is superior to using" to "gain drift is superior to the drift with" 35
- Changed "results in degraded harmonic distortion" to "increases the harmonic distortion" 38
- Deleted "A 10-Ω series resistor can be inserted between the capacitor and the noninverting pin to isolate the capacitance." 39

Changes from Revision G (October 2015) to Revision H (September 2016) — **Page**

- Changed "Type" column header to "I/O" on *Pin Functions* table 6
- Reformatted header rows in *Thermal Information: OPA836* and *Thermal Information: OPA2836* tables 8
- Reformatted *Thermal Information* table note 8
- Reformatted *Thermal Information* table note 9
- Deleted the word "linear" from Output section parameters in *Electrical Characteristics V_S = 2.7 V* table 9
- Deleted the word "linear" from Output section parameters in *Electrical Characteristics V_S = 5 V* table 12
- Reformatted *Development Support* subsection 44

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- Reformatted *Related Documentation* section 44

Changes from Revision E (September 2013) to Revision F (June 2015) **Page**

- 更改了特性 部分..... 1
- 添加了 *引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分..... 1
- Changed *Device Comparison Table* 5
- Changed *Pin Functions* table..... 6
- Changed *Open Loop Gain vs Frequency* graph..... 15
- Changed *Input Referred Noise vs Frequency* graph 15
- Changed *Open Loop Gain vs Frequency* graph 20
- Changed *Input Referred Noise vs Frequency* graph..... 20

Changes from Revision D (October 2011) to Revision E (September 2013) **Page**

- 在文档中增加了 OPA2836 RMC 封装..... 1
- Added RMC pin definitions to *Pin Functions* table..... 6
- Deleted Packaging/Ordering Information table, leaving only note to POA..... 8
- Added OPA2836 RMC package to *Thermal Information* table..... 9

Changes from Revision C (September 2011) to Revision D (September 2011) **Page**

- Removed Product Preview from OPA835IRUNT and OPA835IRUNR..... 5
- Removed Product Preview from OPA836IRUNT and OPA836IRUNR..... 8
- Changed typical value for resistor temperature coefficien parameter from TBD to < 10..... 9
- Changed "quiescent operating current" parameter to "quiescent operating current per amplifier"..... 9
- Changed resistor temperature coefficient typical value from TBD to < 10..... 12
- Changed "quiescent operating current" to "quiescent operating current per amplifier"..... 12

Changes from Revision B (May 2011) to Revision C (August 2011) **Page**

- 在“说明”中添加了“OPA836 RUN 封装...”文本..... 1
- Removed Product Preview from all devices except OPA835IRUNT and OPA835IRUNR..... 5
- Removed Product Preview from all devices except OPA836IRUNT and OPA836IRUNR..... 8
- Changed typical value for channel to channel crosstalk (OPA2836) parameter from TBD to –120 dB..... 9
- Changed the common-mode rejection ratio minimum value from 94 dB to 91 dB..... 9
- Added Gain Setting Resistors (OPA836IRUN ONLY) parameter in *Electrical Characteristics* table..... 9
- Changed the quiescent operating current (T_A = 25°C) minimum value from 0.8 mA to 0.7 mA..... 9
- Changed the minimum value for power supply rejection (±PSRR) parameter from 95 dB to 91 dB..... 9
- Changed the power-down pin bias current test condition from $\overline{PD}$ = 0.7 V to $\overline{PD}$ = 0.5 V..... 9
- Changed the power-down quiescent current test condition from $\overline{PD}$ = 0.7 V to $\overline{PD}$ = 0.5 V..... 9
- Changed typical value for channel to channel crosstalk (OPA2836) parameter from TBD to –120 dB..... 12
- Changed the Common-mode rejection ratio Min value From: 97 dB To: 94 dB..... 12
- Added GAIN SETTING RESISTORS (OPA836I RUN ONLY) parameter to *Electrical Characteristics* table..... 12
- Changed the quiescent operating current (T_A = 25°C) minimum value from 0.9 mA to 0.8 mA..... 12
- Changed the power supply rejection (±PSRR) minimum value from: 97 dB to 94 dB..... 12
- Changed the Power-down quiescent current CONDITIONS From: $\overline{PD}$ = 0.7 V To: $\overline{PD}$ = 0.5 V..... 12
- Changed the Power-down quiescent current Conditions From: $\overline{PD}$ = 0.7 V To: $\overline{PD}$ = 0.5 V..... 12
- Added Figure Crosstalk vs Frequency..... 15
- Added *Crosstalk vs Frequency* figure..... 20
- Added section *Single Ended to Differential Amplifier* 32

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Changes from Revision A (March 2011) to Revision B (May 2011) **Page**

- 已将 OPA836 从“产品预发布”更改为“量产数据” 1

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5 Device Comparison Table

DEVICE	BW (A_V = 1) (MHz)	SLEW RATE (V/µs)	Iq (+5 V) (mA)	INPUT NOISE (nV/√Hz)	RAIL-TO-RAIL IN/OUT	DUALS
OPA836	205	560	1	4.6	– VS/Out	OPA2836
OPA835	30	110	0.25	9.3	– VS/Out	OPA2835
OPA365	50	25	5	4.5	In/Out	OPA2365
THS4281	95	35	0.75	12.5	In/Out	
LMH6618	140	45	1.25	10	In/Out	LMH6619
OPA830	310	600	3.9	9.5	– VS/Out	OPA2830

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6 Pin Configuration and Functions

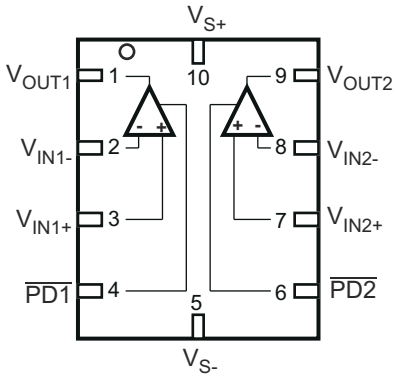

图 6-1. OPA2836 RUN, RMC Packages 10-Pin WQFN, UQFN Top View

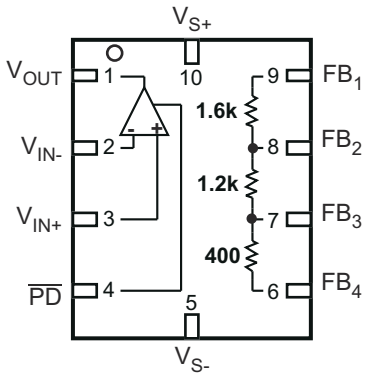

图 6-2. OPA836 RUN Package 10-Pin WQFN Top View

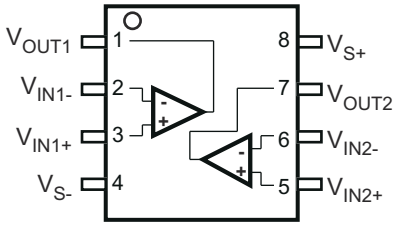

图 6-3. OPA2836 D Package 8-Pin SOIC Top View

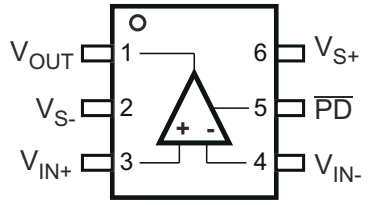

图 6-4. OPA836 DBV Package 6-Pin SOT-23 Top View

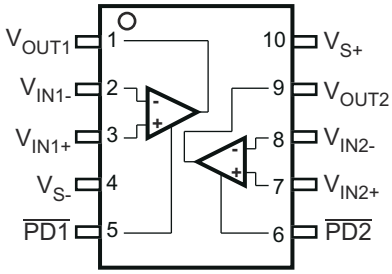

图 6-5. OPA2836 DGS Package 10-Pin VSSOP Top View

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表 6-1. Pin Functions

PIN						I/O	DESCRIPTION
NAME	OPA836		OPA2836				
	SOT-23	WQFN	SOIC	VSSOP	WQFN, UQFN		
FB_1	—	9	—	—	—	I/O	Connection to top of 2.4-kΩ internal gain setting resistors
FB_2		8				I/O	Connection to junction of 1.8-kΩ and 2.4-kΩ internal gain setting resistors
FB_3		7				I/O	Connection to junction of 600-Ω and 1.8-kΩ internal gain setting resistors
FB_4		6				I/O	Connection to bottom of 600-Ω internal gain setting resistors
$\overline{PD}$	5	4	—			I	Amplifier Power Down, low = low-power mode, high = normal operation **(PIN MUST BE DRIVEN)**
$\overline{PD1}$	—	—		5	4	I	Amplifier 1 Power Down, low = low-power mode, high = normal operation **(PIN MUST BE DRIVEN)**
$\overline{PD2}$				6	6	I	Amplifier 2 Power Down, low = low-power mode, high = normal operation **(PIN MUST BE DRIVEN)**
V_{IN+}	3	3		—	—	I	Amplifier noninverting input
V_{IN-}	4	2				I	Amplifier inverting input
V_{IN1+}	—	—	3	3	3	I	Amplifier 1 noninverting input
V_{IN1-}			2	2	2	I	Amplifier 1 inverting input
V_{IN2+}			5	7	7	I	Amplifier 2 noninverting input
V_{IN2-}			6	8	8	I	Amplifier 2 inverting input
V_{OUT}	1	1	—	—	—	O	Amplifier output
V_{OUT1}	—	—	1	1	1	O	Amplifier 1 output
V_{OUT2}			7	9	9	O	Amplifier 2 output
V_{S+}	6	10	8	10	10	POW	Positive power supply input
V_{S-}	2	5	4	4	5	POW	Negative power supply input

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{S-} to V_{S+}	Supply voltage		5.5	V
V_I	Input voltage	V_{S-} – 0.7	V_{S+} + 0.7	V
V_{ID}	Differential input voltage		1	V
I_I	Continuous input current		0.85	mA
I_O	Continuous output current		60	mA
	Continuous power dissipation	See 节 7.4 and 节 7.5		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Single supply voltage	2.5	5	5.5	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information: OPA836

THERMAL METRIC(1)		OPA836		UNIT
		DBV (SOT23-6)	RUN (WQFN-10)	
		6 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	194	145.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	129.2	75.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.4	38.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.6	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.9	104.5	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

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7.5 Thermal Information: OPA2836

THERMAL METRIC[1]		OPA2836				UNIT
		D (SOIC-8)	(DGS) VSSOP, MSOP-10	(RUN) WQFN-10	RMC (UQFN-10)	
		8 PINS	10 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150.1	206	145.8	143.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	83.8	75.3	75.1	49.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.4	96.2	38.9	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	33.0	12.9	13.5	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.9	94.6	104.5	61.9	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

7.6 Electrical Characteristics: V_S = 2.7 V

at V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL[1]
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		200		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		100			
	V_{OUT} = 100 mV_{PP}, G = 5		26			
	V_{OUT} = 100 mV_{PP}, G = 10		11			
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		110		MHz	C
Large-signal bandwidth	V_{OUT} = 1 V_{PP}, G = 2		60		MHz	C
Bandwidth for 0.1-dB flatness	V_{OUT} = 1 V_{PP}, G = 2		25		MHz	C
Slew rate, rise	V_{OUT} = 1 V_{STEP}, G = 2		260		V/µs	C
Slew rate, fall	V_{OUT} = 1 V_{STEP}, G = 2		240		V/µs	C
Rise time	V_{OUT} = 1 V_{STEP}, G = 2		4		ns	C
Fall time	V_{OUT} = 1 V_{STEP}, G = 2		4.5		ns	C
Settling time to 1%, rise	V_{OUT} = 1 V_{STEP}, G = 2		15		ns	C
Settling time to 1%, fall	V_{OUT} = 1 V_{STEP}, G = 2		15		ns	C
Settling time to 0.1%, rise	V_{OUT} = 1 V_{STEP}, G = 2		30		ns	C
Settling time to 0.1%, fall	V_{OUT} = 1 V_{STEP}, G = 2		25		ns	C
Settling time to 0.01%, rise	V_{OUT} = 1 V_{STEP}, G = 2		50		ns	C
Settling time to 0.01%, fall	V_{OUT} = 1 V_{STEP}, G = 2		45		ns	C
Overshoot/Undershoot	V_{OUT} = 1 V_{STEP}, G = 2		5%/3%			C
Second-order harmonic distortion	f = 10 kHz, V_{IN_CM} = mid-supply – 0.5 V		–133		dBc	C
	f = 100 kHz, V_{IN_CM} = mid-supply – 0.5 V		–120			C
	f = 1 MHz, V_{IN_CM} = mid-supply – 0.5 V		–84			C
Third-order harmonic distortion	f = 10 kHz, V_{IN_CM} = mid-supply – 0.5 V		–137		dBc	C
	f = 100 kHz, V_{IN_CM} = mid-supply – 0.5 V		–130			C
	f = 1 MHz, V_{IN_CM} = mid-supply – 0.5 V		–105			C
Second-order intermodulation distortion	f = 1 MHz, 200-kHz Tone Spacing, V_{OUT} Envelope = 1 V_{PP} V_{IN_CM} = mid-supply – 0.5 V		–90		dBc	C
Third-order intermodulation distortion	f = 1 MHz, 200-kHz Tone Spacing, V_{OUT} Envelope = 1 V_{PP} V_{IN_CM} = mid-supply – 0.5 V		–90		dBc	C
Input voltage noise	f = 100 KHz		4.6		nV/√Hz	C
Voltage noise 1/f corner frequency			215		Hz	C
Input current noise	f = 1 MHz		0.75		pA/√Hz	C

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7.6 Electrical Characteristics: V_S = 2.7 V (continued)

at V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE (continued)						
Current noise 1/f corner frequency			31.7		kHz	C
Overdrive recovery time, over/under	Overdrive = 0.5 V		55/60		ns	C
Closed-loop output impedance	f = 100 kHz		0.02		Ω	C
Channel-to-channel crosstalk (OPA2836)	f = 10 kHz		–120		dB	C
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	125		dB	A
Input referred offset voltage	T_A = 25°C	–400	±65	400	µV	A
	T_A = 0°C to 70°C	–680		680		B
	T_A = –40°C to 85°C	–760		760		
	T_A = –40°C to 125°C	–1060		1060		
Input offset voltage drift(2)	T_A = 0°C to 70°C	–6.2	±1	6.2	µV/°C	B
	T_A = –40°C to 85°C	–6	±1	6		
	T_A = –40°C to 125°C	–6.6	±1.1	6.6		
Input bias current(3)	T_A = 25°C	300	650	1000	nA	A
	T_A = 0°C to 70°C	190		1400		B
	T_A = –40°C to 85°C	120		1500		
	T_A = –40°C to 125°C	120		1800		
Input bias current drift(2)	T_A = 0°C to 70°C	–2	±0.33	2	nA/°C	B
	T_A = –40°C to 85°C	–1.9	±0.32	1.9		
	T_A = –40°C to 125°C	–2.1	±0.37	2.1		
Input offset current	T_A = 25°C	–180	±30	180	nA	A
	T_A = 0°C to 70°C	–200	±30	200		B
	T_A = –40°C to 85°C	–215	±30	215		
	T_A = –40°C to 125°C	–240	±30	240		
Input offset current drift(2)	T_A = 0°C to 70°C	–460	±77	460	pA/°C	B
	T_A = –40°C to 85°C	–575	±95	575		
	T_A = –40°C to 125°C	–600	±100	600		
INPUT						
Common-mode input range low	T_A = 25°C, < 3-dB degradation in CMRR limit		–0.2	0	V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit		–0.2	0	V	B
Common-mode input range high	T_A = 25°C, < 3-dB degradation in CMRR limit	1.5	1.6		V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit	1.5	1.6		V	B
Input operating voltage range	T_A = 25°C, < 6-dB degradation in THD		–0.3 to 1.75		V	C
Common-mode rejection ratio		91	114		dB	A
Input impedance common-mode			100 || 1.2		MΩ || pF	C
Input impedance differential mode			100 || 1		kΩ || pF	C

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7.6 Electrical Characteristics: V_S = 2.7 V (continued)

at V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
OUTPUT						
Output voltage low	T_A = 25°C, G = 5		0.15	0.2	V	A
	T_A = –40°C to 125°C, G = 5		0.15	0.2	V	B
Output voltage high	T_A = 25°C, G = 5	2.45	2.5		V	A
	T_A = –40°C to 125°C, G = 5	2.45	2.5		V	B
Output saturation voltage, high/low	T_A = 25°C, G = 5		80/40		mV	C
Output current drive	T_A = 25°C	±40	±45		mA	A
	T_A = –40°C to 125°C	±40	±45		mA	B
GAIN SETTING RESISTORS (OPA836IRUN ONLY)						
Resistor FB1 to FB2	DC resistance	1584	1600	1616	Ω	A
Resistor FB2 to FB3	DC resistance	1188	1200	1212	Ω	A
Resistor FB3 to FB4	DC resistance	396	400	404	Ω	A
Resistor tolerance	DC resistance	–1%		1%		A
Resistor temperature coefficient	DC resistance		<10		PPM	C
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current per amplifier	T_A = 25°C	0.7	0.95	1.15	mA	A
	T_A = –40°C to 125°C	0.6		1.4	mA	B
Power supply rejection (±PSRR)		91	108		dB	A
POWER DOWN						
Enable voltage threshold	Specified "on" above V_{S-} + 2.1 V			2.1	V	A
Disable voltage threshold	Specified "off" below V_{S-} + 0.7 V	0.7			V	A
Power-down pin bias current	$\overline{PD}$ = 0.5 V		20	500	nA	A
Power-down quiescent current	$\overline{PD}$ = 0. 5 V		0.5	1.5	µA	A
Turnon time delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value		200		ns	C
Turnoff time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value		25		ns	C

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.
(3) Current is considered positive out of the pin.

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7.7 Electrical Characteristics: V_S = 5 V

at V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		205		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		100			
	V_{OUT} = 100 mV_{PP}, G = 5		28			
	V_{OUT} = 100 mV_{PP}, G = 10		11.8			
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		118		MHz	C
Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 2		87		MHz	C
Bandwidth for 0.1-dB flatness	V_{OUT} = 2 V_{PP}, G = 2		29		MHz	C
Slew rate, rise	V_{OUT} = 2-V Step, G = 2		560		V/µs	C
Slew rate, fall	V_{OUT} = 2-V Step, G = 2		580		V/µs	C
Rise time	V_{OUT} = 2-V Step, G = 2		3		ns	C
Fall time	V_{OUT} = 2-V Step, G = 2		3		ns	C
AC PERFORMANCE (continued)						
Settling time to 1%, rise	V_{OUT} = 2-V Step, G = 2		22		ns	C
Settling time to 1%, fall	V_{OUT} = 2-V Step, G = 2		22		ns	C
Settling time to 0.1%, rise	V_{OUT} = 2-V Step, G = 2		30		ns	C
Settling time to 0.1%, fall	V_{OUT} = 2-V Step, G = 2		30		ns	C
Settling time to 0.01%, rise	V_{OUT} = 2-V Step, G = 2		40		ns	C
Settling time to 0.01%, fall	V_{OUT} = 2-V Step, G = 2		45		ns	C
Overshoot/Undershoot	V_{OUT} = 2-V Step, G = 2		7.5%/5%			C
Second-order harmonic distortion	f = 10 kHz		–133		dBc	C
	f = 100 kHz		–120			
	f = 1 MHz		–85			
Third-order harmonic distortion	f = 10 kHz		–140		dBc	C
	f = 100 kHz		–130			
	f = 1 MHz		–105			
Second-order intermodulation distortion	f = 1 MHz, 200 kHz Tone Spacing, V_{OUT} Envelope = 2 V_{PP}		–79		dBc	C
Third-order intermodulation distortion	f = 1 MHz, 200 kHz Tone Spacing, V_{OUT} Envelope = 2 V_{PP}		–91		dBc	C
Signal-to-noise ratio, SNR	f = 1 kHz, V_{OUT} = 1 V_{RMS}, 22 kHz bandwidth		0.00013%			C
			–117.6		dBc	
Total harmonic distortion, THD	f = 1 kHz, V_{OUT} = 1 V_{RMS}		0.00003%			C
			–130		dBc	
Input voltage noise	f = 100 KHz		4.6		nV/√Hz	C
Voltage noise 1/f corner frequency			215		Hz	C
Input current noise	f > 1 MHz		0.75		pA/√Hz	C
Current noise 1/f corner frequency			31.7		kHz	C
Overdrive recovery time, over/under	Overdrive = 0.5 V		55/60		ns	C
Closed-loop output impedance	f = 100 kHz		0.02		Ω	C
Channel to channel crosstalk (OPA2836)	f = 10 kHz		–120		dB	C
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	122		dB	A

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7.7 Electrical Characteristics: V_S = 5 V (continued)

at V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
Input referred offset voltage	T_A = 25°C	–400	±65	400	μV	A
	T_A = 0°C to 70°C	–685		685		B
	T_A = –40°C to 85°C	–765		765		
	T_A = –40°C to 125°C	–1080		1080		
Input offset voltage drift(2)	T_A = 0°C to 70°C	–6.3	±1.05	6.3	μV/°C	B
	T_A = –40°C to 85°C	–6.1	±1	6.1		
	T_A = –40°C to 125°C	–6.8	±1.1	6.8		
Input bias current(3)	T_A = 25°C	300	650	1000	nA	A
	T_A = 0°C to 70°C	190		1400		B
	T_A = –40°C to 85°C	120		1550		
	T_A = –40°C to 125°C	120		1850		
Input bias current drift(2)	T_A = 0°C to 70°C		±0.34	±2	nA/°C	B
	T_A = –40°C to 85°C		±0.34	±2		
	T_A = –40°C to 125°C		±0.38	±2.3		
DC PERFORMANCE (continued)						
Input offset current	T_A = 25°C		±30	±180	nA	A
	T_A = 0°C to 70°C		±30	±200		B
	T_A = –40°C to 85°C		±30	±215		
	T_A = –40°C to 125°C		±30	±250		
Input offset current drift(2)	T_A = 0°C to 70°C		±80	±480	pA/°C	B
	T_A = –40°C to 85°C		±100	±600		
	T_A = –40°C to 125°C		±110	±660		
INPUT						
Common-mode input range low	T_A = 25°C, < 3-dB degradation in CMRR limit		–0.2	0	V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit		–0.2	0	V	B
Common-mode input range high	T_A = 25°C, < 3-dB degradation in CMRR limit	3.8	3.9		V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit	3.8	3.9		V	B
Input linear operating voltage range	T_A = 25°C, < 6-dB degradation in THD		–0.3 to 4.05		V	C
Common-mode rejection ratio		94	116		dB	A
Input impedance common mode			100 || 1.2		MΩ || pF	C
Input impedance differential mode			100 || 1		kΩ || pF	C
OUTPUT						
Output voltage low	T_A = 25°C, G = 5		0.15	0.2	V	A
	T_A = –40°C to 125°C, G = 5		0.15	0.2	V	B
Output voltage high	T_A = 25°C, G = 5	4.75	4.8		V	A
	T_A = –40°C to 125°C, G = 5	4.75	4.8		V	B
Output saturation voltage, high/low	T_A = 25°C, G = 5		100/50		mV	C
Output current drive	T_A = 25°C	±40	±50		mA	A
	T_A = –40°C to 125°C	±40	±50		mA	B
GAIN SETTING RESISTORS (OPA836IRUN ONLY)						
Resistor FB1 to FB2	DC resistance	1584	1600	1616	Ω	A
Resistor FB2 to FB3	DC resistance	1188	1200	1212	Ω	A

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7.7 Electrical Characteristics: V_S = 5 V (continued)

at V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
Resistor FB3 to FB4	DC resistance	396	400	404	Ω	A
Resistor tolerance	DC resistance	–1		1%		A
Resistor temperature coefficient	DC resistance		<10		PPM	C
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current per amplifier	T_A = 25°C	0.8	1.0	1.2	mA	A
	T_A = –40°C to 125°C	0.65		1.5	mA	B
Power supply rejection (±PSRR)		94	108		dB	A
POWER DOWN						
Enable voltage threshold	Specified "on" above V_{S-} + 2.1 V			2.1	V	A
Disable voltage threshold	Specified "off" below V_{S-} + 0.7 V	0.7			V	A
Power-down pin bias current	$\overline{PD}$ = 0.5 V		20	500	nA	A
Power-down quiescent current	$\overline{PD}$ = 0.5 V		0.5	1.5	µA	A
Turnon time delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value		170		ns	C
Turnoff time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value		35		ns	C

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.
(3) Current is considered positive out of the pin.

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7.8 Typical Characteristics: V_S = 2.7 V

at V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{pp}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

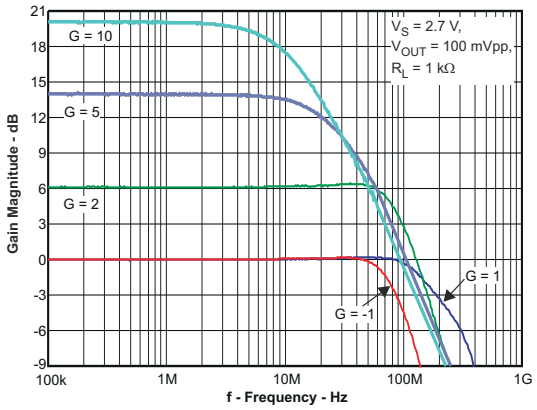

图 7-1. Small Signal Frequency Response

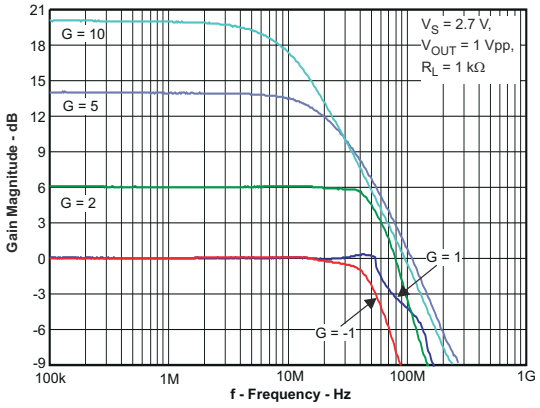

图 7-2. Large Signal Frequency Response

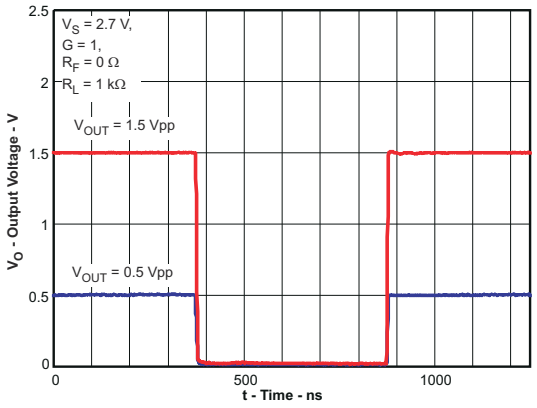

图 7-3. Noninverting Pulse Response

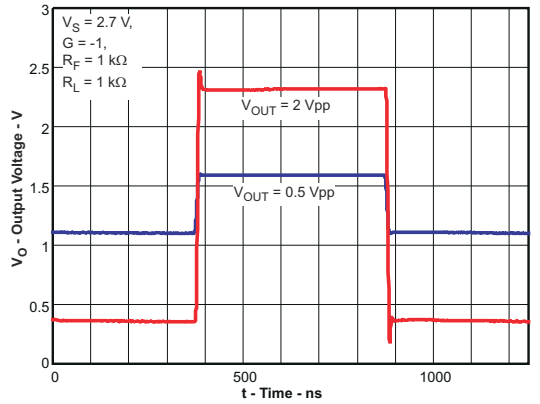

图 7-4. Inverting Pulse Response

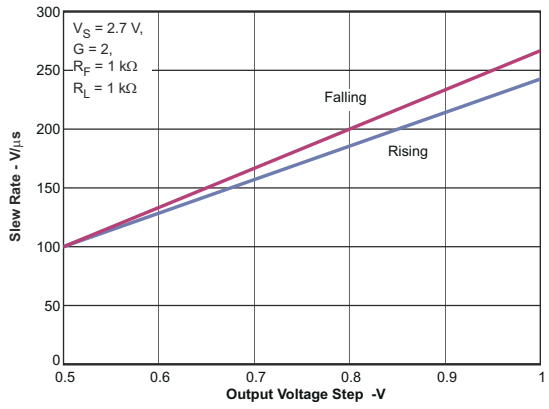

图 7-5. Slew Rate vs Output Voltage Step

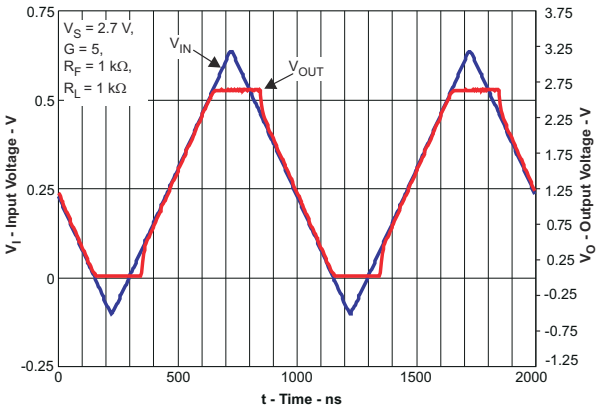

图 7-6. Output Overdrive Recovery

7.8 Typical Characteristics: V_S = 2.7 V

at V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{pp}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

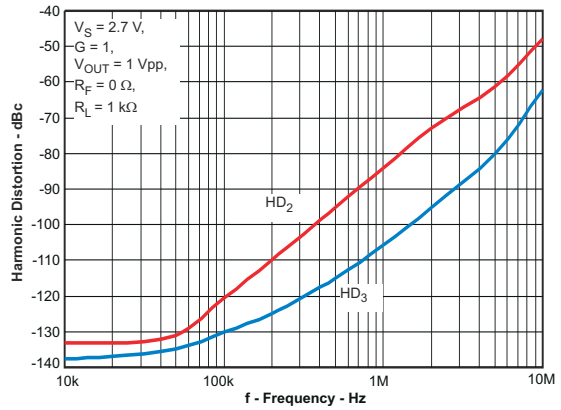

图 7-7. Harmonic Distortion vs Frequency

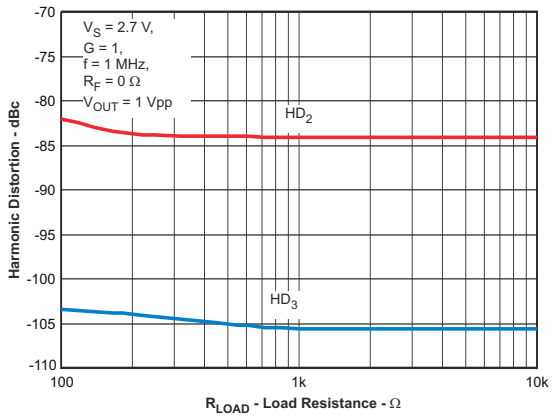

图 7-8. Harmonic Distortion vs Load Resistance

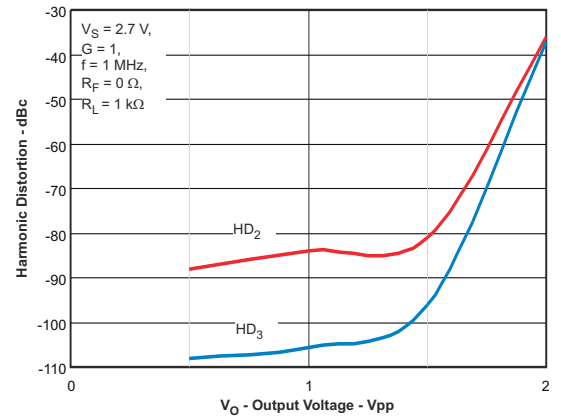

图 7-9. Harmonic Distortion vs Output Voltage

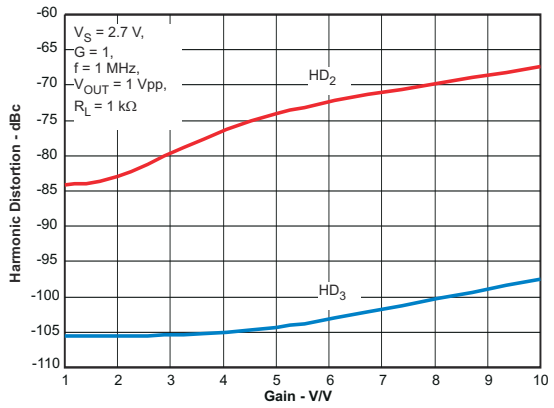

图 7-10. Harmonic Distortion vs Gain

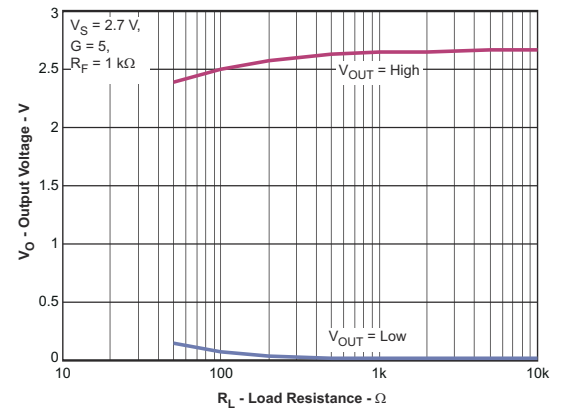

图 7-11. Output Voltage Swing vs Load Resistance

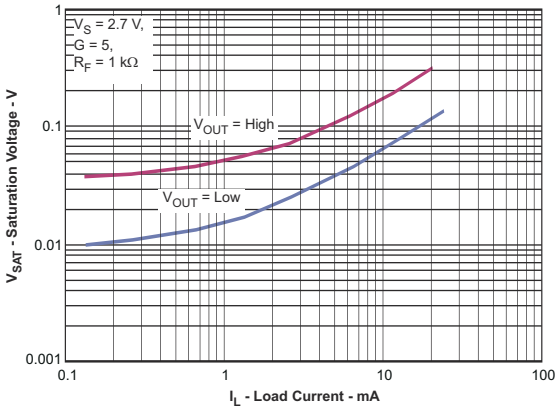

图 7-12. Output Saturation Voltage vs Load Current

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7.8 Typical Characteristics: V_S = 2.7 V

at V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{pp}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

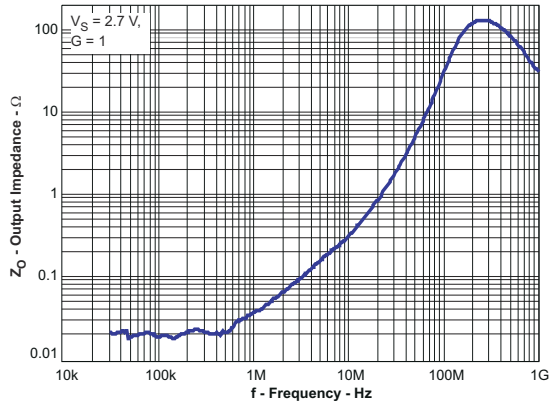


图 7-13. Output Impedance vs Frequency

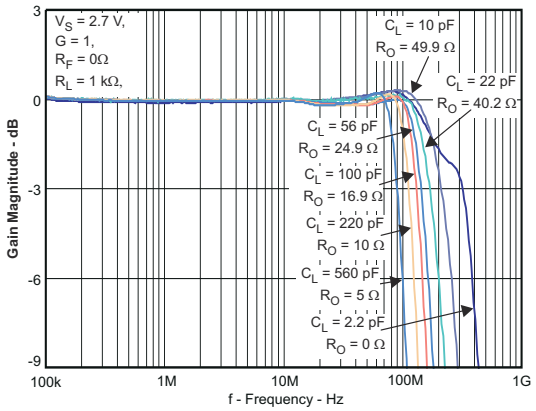
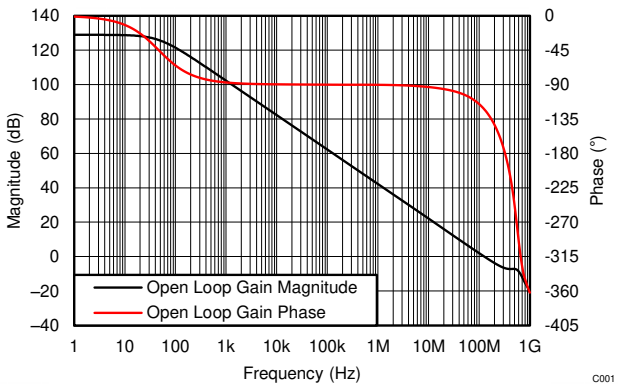
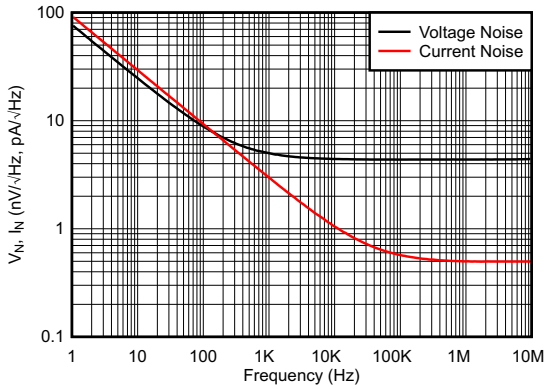


图 7-14. Frequency Response With Capacitive Load



V_S = 2.7 V

图 7-15. Open Loop Gain vs Frequency



V_S = 2.7 V

图 7-16. Input Referred Noise vs Frequency

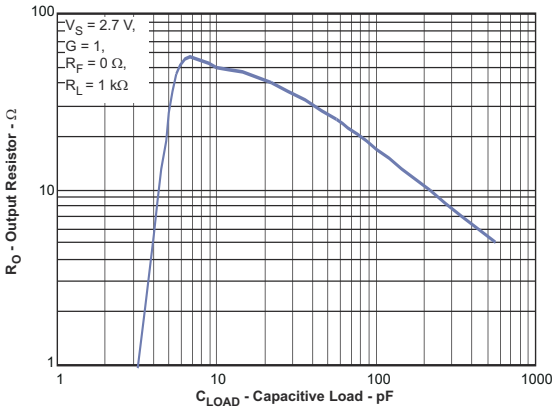


图 7-17. Series Output Resistor vs Capacitive Load

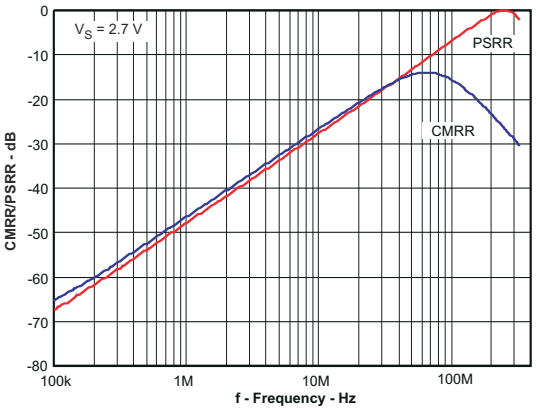


图 7-18. Common Mode/Power Supply Rejection Ratios vs Frequency

7.8 Typical Characteristics: V_S = 2.7 V

at V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{pp}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

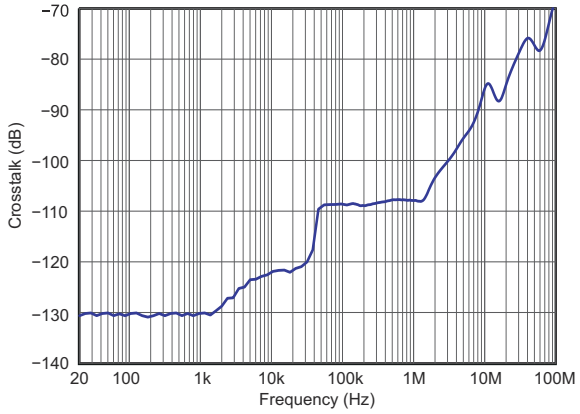


图 7-19. Crosstalk vs Frequency

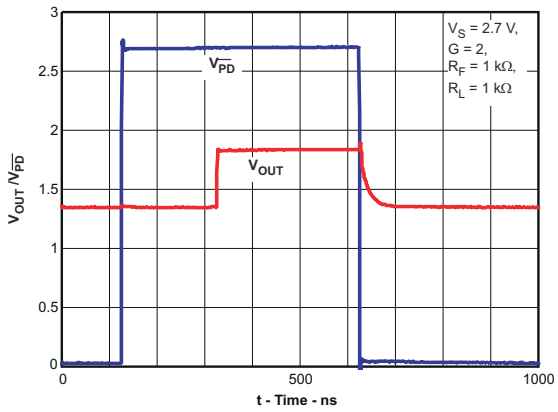


图 7-20. Power Down Response

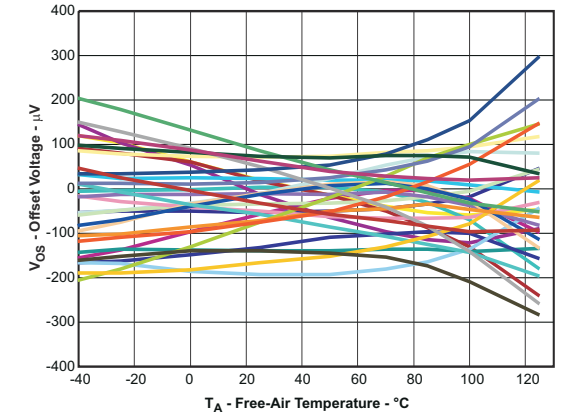


图 7-21. Input Offset Voltage vs Free-Air Temperature

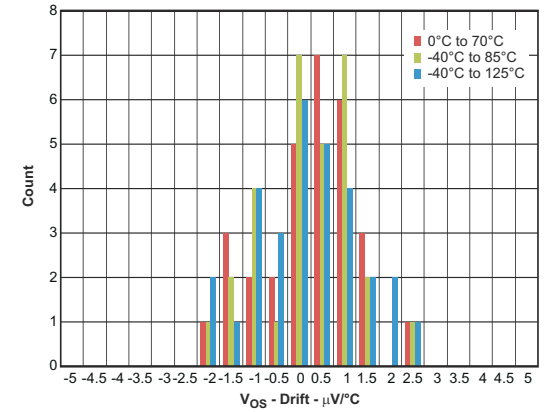


图 7-22. Input Offset Voltage Drift

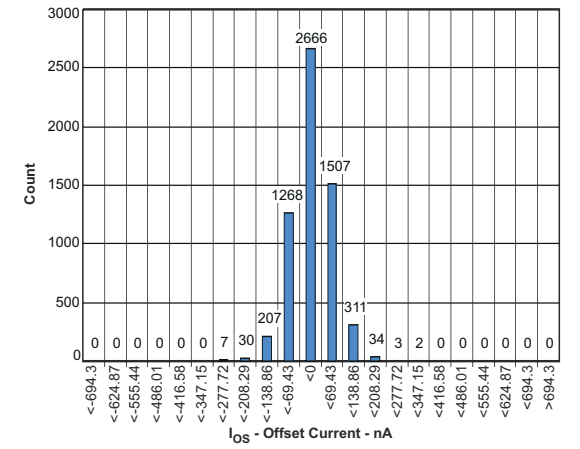


图 7-23. Input Offset Voltage

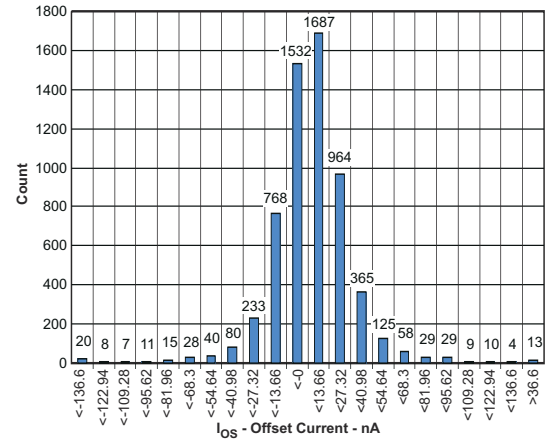


图 7-24. Input Offset Current

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7.8 Typical Characteristics: V_S = 2.7 V (continued)

at V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 V_{pp}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

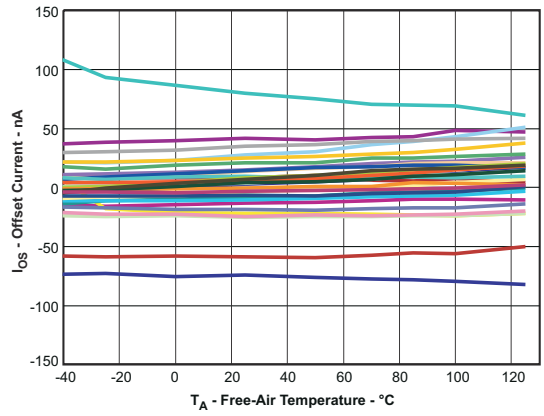

图 7-25. Input Offset Current vs Free-Air Temperature

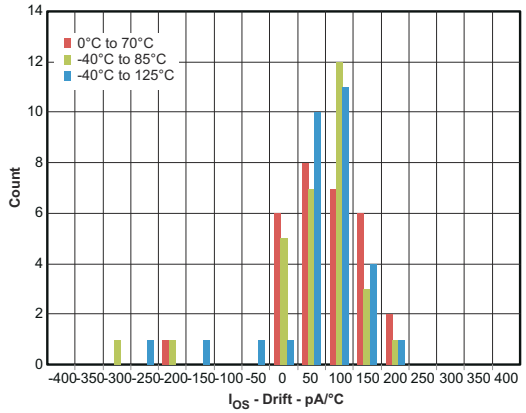

图 7-26. Input Offset Current Drift

7.9 Typical Characteristics: V_S = 5 V

at V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply unless otherwise noted. T_A = 25°C, unless otherwise noted.

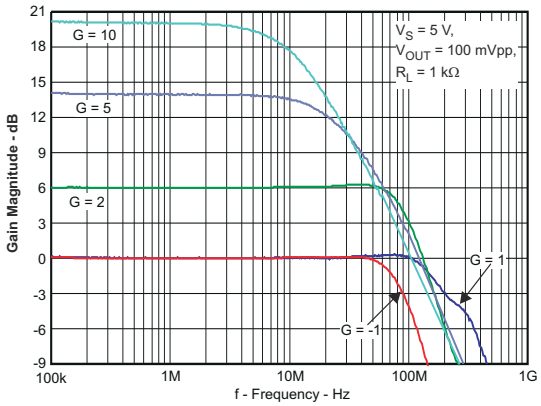

图 7-27. Small Signal Frequency Response

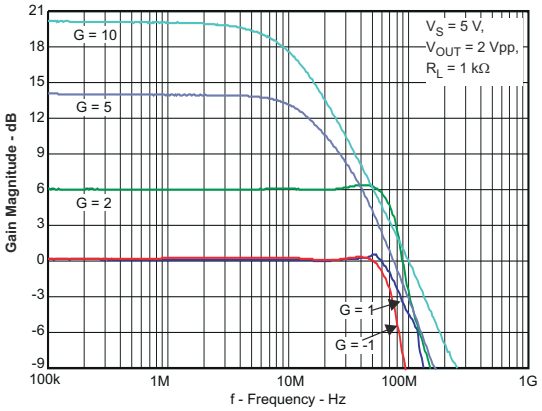

图 7-28. Large Signal Frequency Response

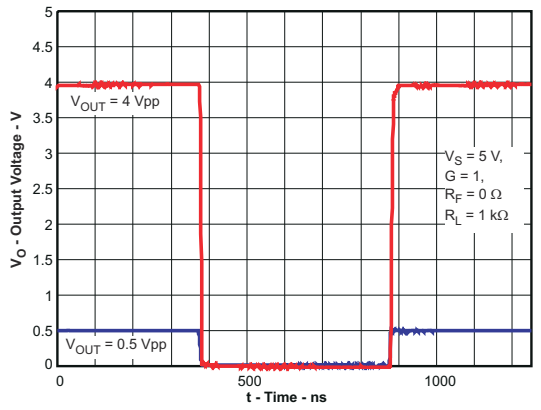

图 7-29. Noninverting Pulse Response

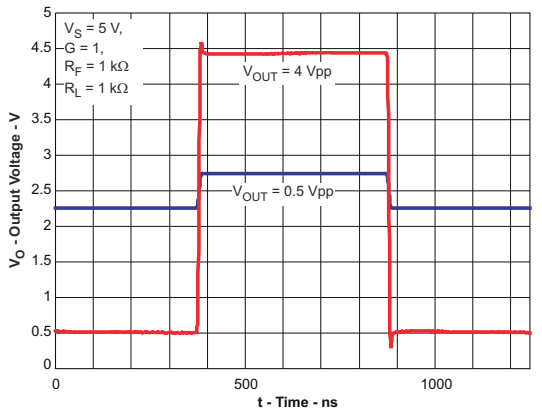

图 7-30. Inverting Pulse Response

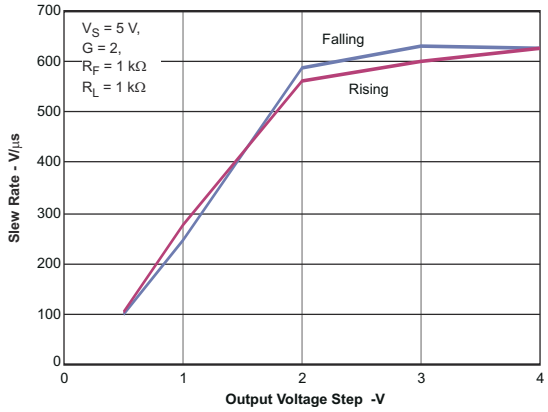

图 7-31. Slew Rate vs Output Voltage Step

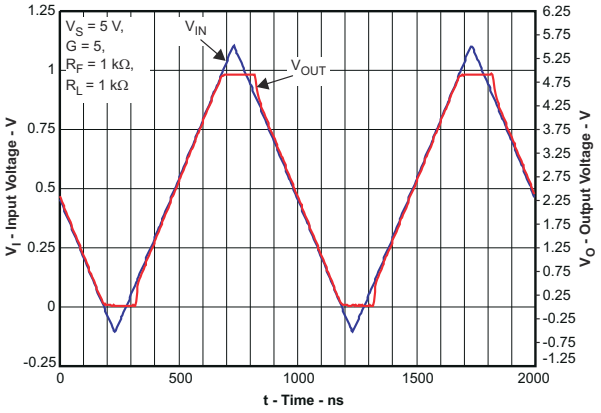

图 7-32. Output Overdrive Recovery

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7.9 Typical Characteristics: V_S = 5 V

at V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply unless otherwise noted. T_A = 25°C, unless otherwise noted.

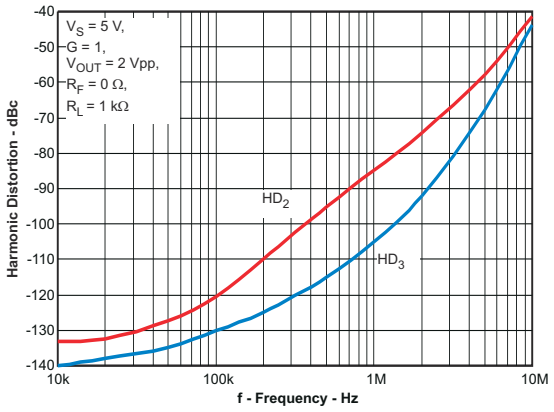

图 7-33. Harmonic Distortion vs Frequency

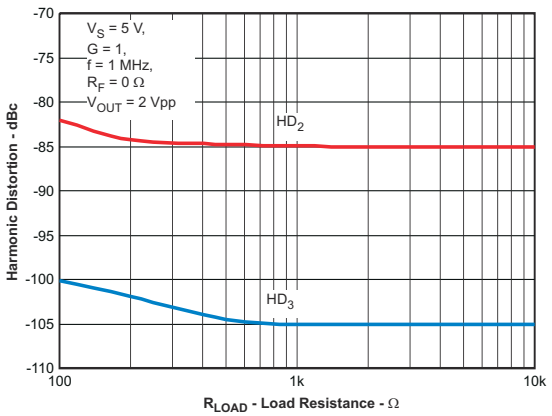

图 7-34. Harmonic Distortion vs Load Resistance

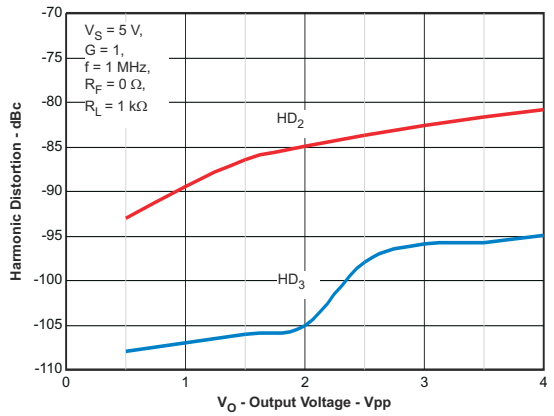

图 7-35. Harmonic Distortion vs Output Voltage

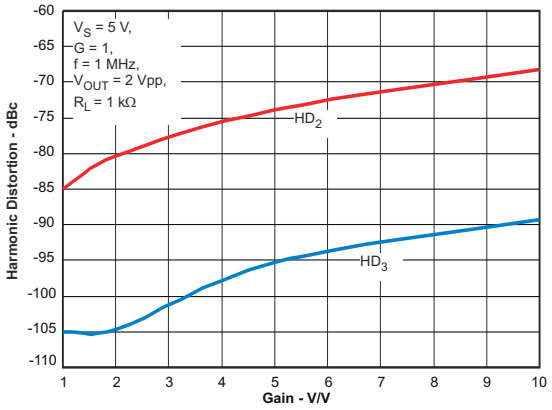

图 7-36. Harmonic Distortion vs Gain

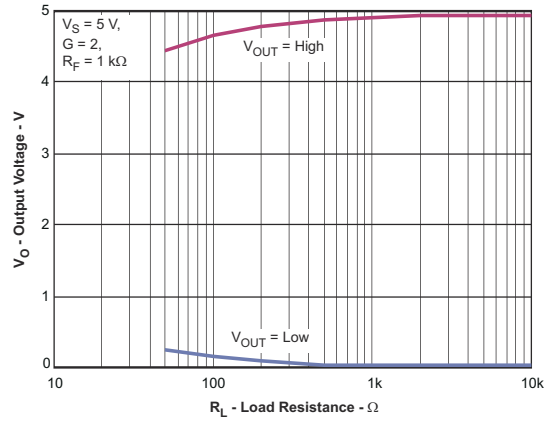

图 7-37. Output Voltage Swing vs Load Resistance

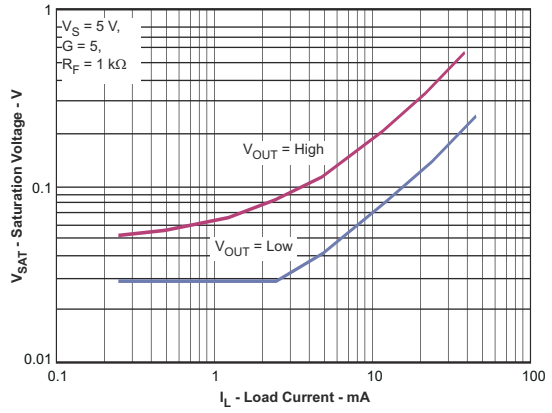

图 7-38. Output Saturation Voltage vs Load Current

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7.9 Typical Characteristics: V_S = 5 V

at V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply unless otherwise noted. T_A = 25°C, unless otherwise noted.

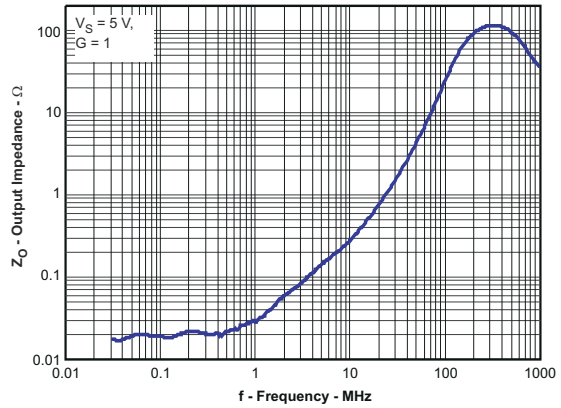


图 7-39. Output Impedance vs Frequency

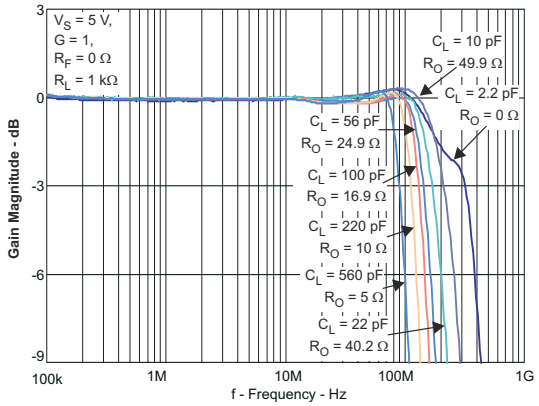
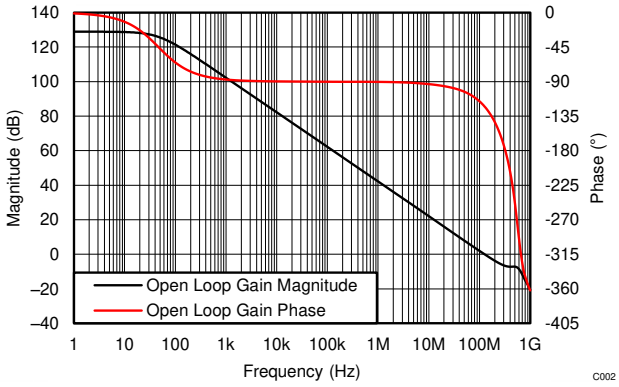
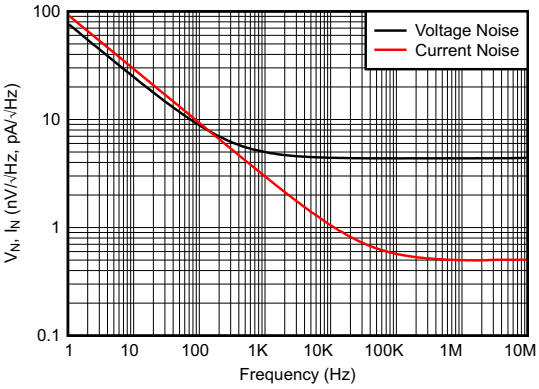


图 7-40. Frequency Response With Capacitive Load



V_S = 5.0 V

图 7-41. Open Loop Gain vs Frequency



V_S = 5.0 V

图 7-42. Input Referred Noise vs Frequency

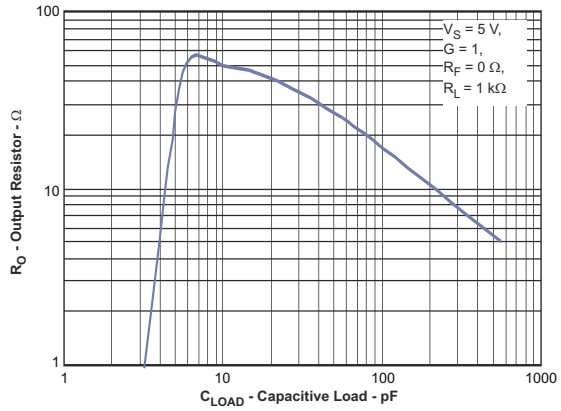


图 7-43. Series Output Resistor vs Capacitive Load

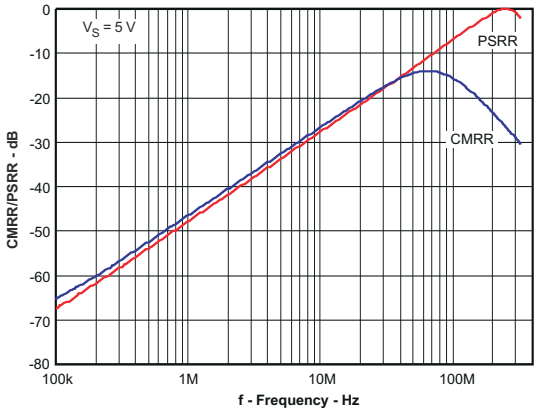


图 7-44. Common-Mode/Power Supply Rejection Ratios vs Frequency

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7.9 Typical Characteristics: V_S = 5 V

at V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply unless otherwise noted. T_A = 25°C, unless otherwise noted.

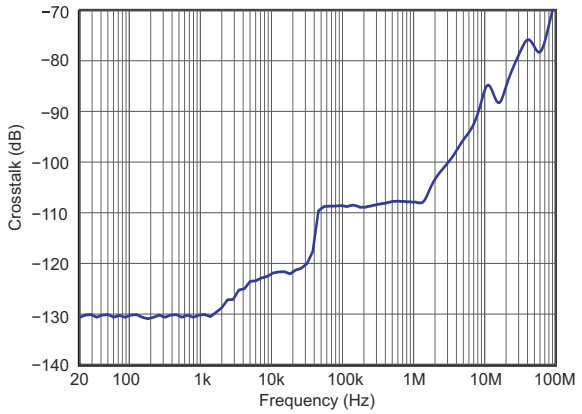

图 7-45. Crosstalk vs Frequency

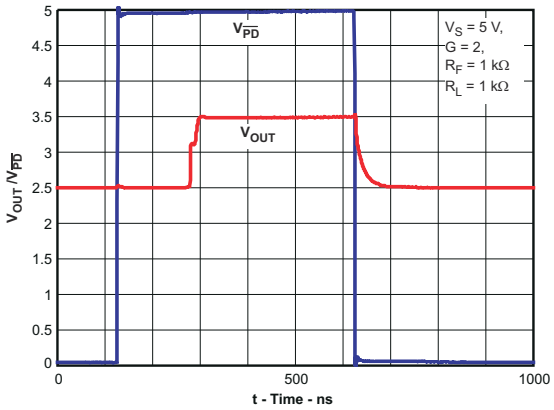

图 7-46. Power Down Response

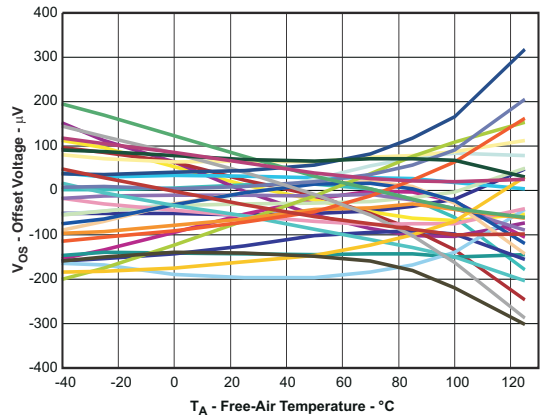

图 7-47. Input Offset Voltage vs Free-Air Temperature

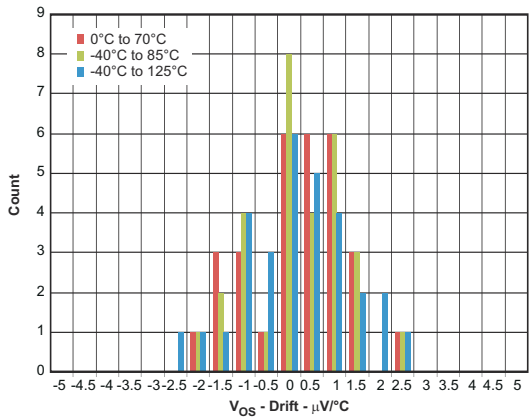

图 7-48. Input Offset Voltage Drift

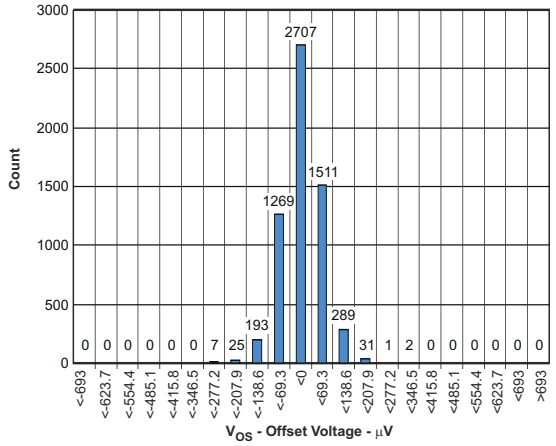

图 7-49. Input Offset Voltage

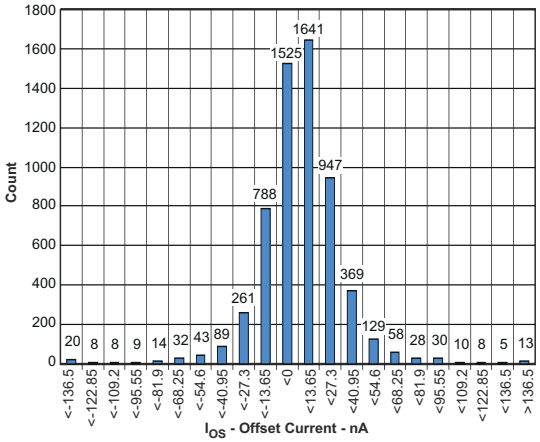

图 7-50. Input Offset Current

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7.9 Typical Characteristics: V_S = 5 V (continued)

at V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 1 kΩ, G = 1 V/V, input and output referenced to mid-supply unless otherwise noted. T_A = 25°C, unless otherwise noted.

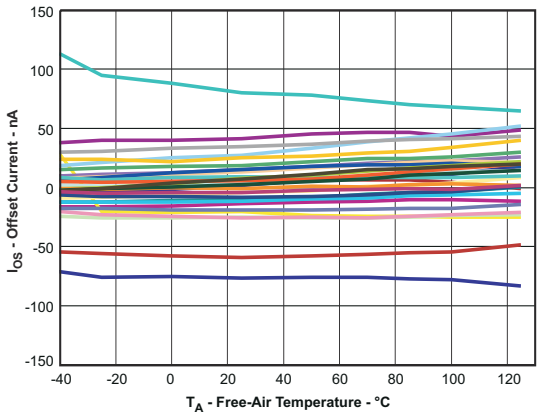

图 7-51. Input Offset Current vs Free-Air Temperature

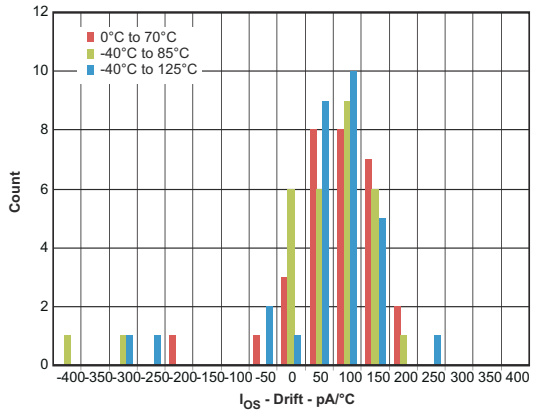

图 7-52. Input Offset Current Drift

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8 Detailed Description

8.1 Overview

The OPAx836 family of bipolar-input operational amplifiers offers excellent bandwidth of 205 MHz with ultra-low THD of 0.00003% at 1 kHz. The OPAx836 device can swing to within 200 mV of the supply rails while driving a 1-kΩ load. The input common-mode of the amplifier can swing to 200 mV below the negative supply rail. This level of performance is achieved at 1 mA of quiescent current per amplifier channel.

8.2 Functional Block Diagrams

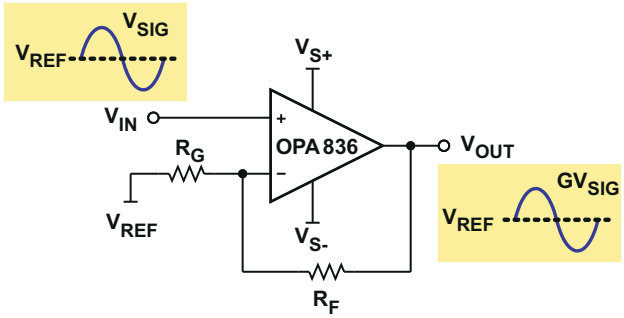

图 8-1. Noninverting Amplifier

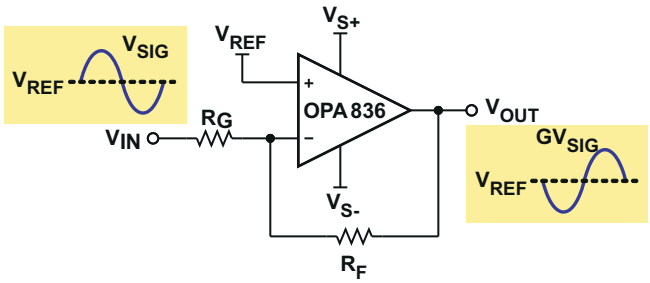

图 8-2. Inverting Amplifier

8.3 Feature Description

8.3.1 Input Common-Mode Voltage Range

When the primary design goal is a linear amplifier with high CMRR, it is important to not violate the input common-mode voltage range (V_{ICR}) of an operational amplifier.

The common-mode input range specifications in the table data use CMRR to set the limit. The limits are selected to ensure CMRR will not degrade more than 3 dB below the CMRR limit if the input voltage is kept within the specified range. The limits cover all process variations and most parts will be better than specified. The typical specifications are from 0.2 V below the negative rail to 1.1 V below the positive rail.

Assuming the operational amplifier is in linear operation, the voltage difference between the input pins is small (ideally 0 V) and input common-mode voltage is analyzed at either input pin with the other input pin assumed to be at the same potential. The voltage at V_{IN+} is simple to evaluate. In noninverting configuration, 图 8-1, the input signal, V_{IN}, must not violate the V_{ICR}. In inverting configuration, 图 8-2, the reference voltage, V_{REF}, must be within the V_{ICR}.

The input voltage limits have fixed headroom to the power rails and track the power supply voltages. For one 5-V supply, the linear input voltage ranges from –0.2 V to 3.9 V and from –0.2 V to 1.6 V for a 2.7-V supply. The delta headroom from each power supply rail is the same in either case: –0.2 V and 1.1 V.

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8.3.2 Output Voltage Range

The OPA836 and OPA2836 devices are rail-to-rail output (RRO) operational amplifiers. Rail-to-rail output typically means the output voltage swings within a couple hundred millivolts of the supply rails. There are different ways to specify this: one is with the output still in linear operation and another is with the output saturated. Saturated output voltages are closer to the power supply rails than linear outputs, but the signal is not a linear representation of the input. Linear output is a better representation of how well a device performs when used as a linear amplifier. Saturation and linear operation limits are affected by the output current, where higher currents lead to more loss in the output transistors.

Output Voltage Swing vs Load Resistance and Output Voltage Swing vs Load Resistance show saturated voltage-swing limits versus output load resistance and Output Saturation Voltage vs Load Current and Output Saturation Voltage vs Load Current show the output saturation voltage versus load current. Given a light load, the output voltage limits have nearly constant headroom to the power rails and track the power supply voltages. For example, with a 2-kΩ load and single 5-V supply, the linear output voltage ranges from 0.15 V to 4.8 V, and ranges from 0.15 V to 2.5 V for a 2.7-V supply. The delta from each power supply rail is the same in either case: 0.15 V and 0.2 V.

With devices like the OPA836 and OPA2836, where the input range is lower than the output range, typically the input will limit the available signal swing only in noninverting gain of 1. Signal swing in noninverting configurations in gains > +1 and inverting configurations in any gain is typically limited by the output voltage limits of the operational amplifier.

8.3.3 Power-Down Operation

The OPA836 and OPA2836 devices include a power-down mode. Under logic control, the amplifiers can switch from normal operation to a standby current of < 1.5 µA. When the $\overline{PD}$ pin is connected high, the amplifier is active. Connecting $\overline{PD}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a unity-gain buffer, the output stage is in a high dc-impedance state. To protect the input stage of the amplifier, the devices use internal, back-to-back ESD diodes between the inverting and noninverting input pins. This configuration creates a parallel low-impedance path from the amplifier output to the noninverting pin when the differential voltage between the pins exceeds a diode voltage drop. When the op amp is configured in other gains, the feedback (RF) and gain (RG) resistor network forms a parallel load.

The $\overline{PD}$ pin must be actively driven high or low and must not be left floating. If the power-down mode is not used, $\overline{PD}$ must be tied to the positive supply rail.

$\overline{PD}$ logic states are TTL with reference to the negative supply rail and V_{S-}. When the operational amplifier is powered from single-supply and ground and driven from logic devices with similar V_{DD}, voltages to the operational amplifier do not require any special consideration. When the operational amplifier is powered from a split supply, with V_{S-} below ground, an open-collector type of interface with pullup resistor is more appropriate. Pullup resistor values must be lower than 100 kΩ. Additionally, the drive logic must be negated due to the inverting action of an open-collector gate.

8.3.4 Low-Power Applications and the Effects of Resistor Values on Bandwidth

The OPA836 and OPA2836 devices are designed for the nominal value of R_F to be 1 kΩ in gains other than +1. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response, but it also loads the amplifier. For example; in gain of 2 with $R_F = R_G = 1$ kΩ, R_G to ground, and $V_{OUT} = 4$ V, 2 mA of current will flow through the feedback path to ground. In gain of +1, R_G is open and no current will flow to ground. In low-power applications, it is desirable to reduce the current in the feedback by increasing the gain-setting resistors values. Using larger value gain resistors has two primary side effects (other than lower power) due to their interaction with parasitic circuit capacitance:

- Lowers the bandwidth
- Lowers the phase margin
  - This causes peaking in the frequency response
  - This also causes overshoot and ringing in the pulse response

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图 8-3 shows the small-signal frequency response on OPA836EVM for noninverting gain of 2 with R_F and R_G equal to 1 kΩ, 10 kΩ, and 100 kΩ. The test was done with R_L = 1 kΩ. Due to loading effects of R_L, lower R_L values may reduce the peaking, but higher values will not have a significant effect.

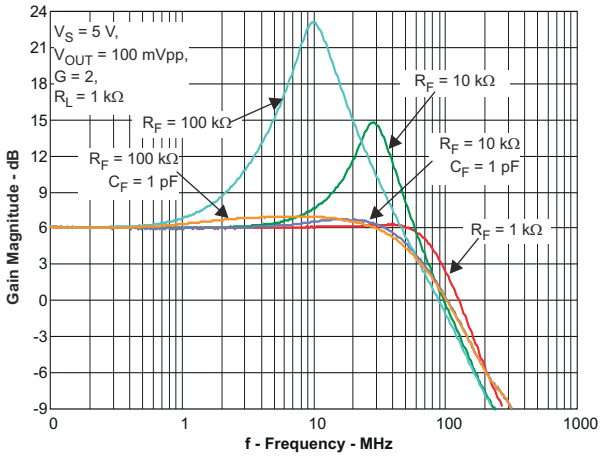

图 8-3. Frequency Response With Various Gain-Setting Resistor Values

As expected, larger value gain resistors cause lower bandwidth and peaking in the response (peaking in the frequency response is synonymous with overshoot and ringing in the pulse response). Adding 1-pF capacitors in parallel with R_F helps compensate the phase margin and restores flat frequency response. 图 8-4 shows the test circuit.

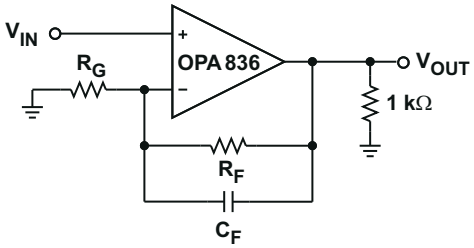

图 8-4. G = 2 Test Circuit for Various Gain-Setting Resistor Values

8.3.5 Driving Capacitive Loads

The OPA836 and OPA2836 devices can drive up to a nominal capacitive load of 2.2 pF on the output with no special consideration. When driving capacitive loads greater than 2.2 pF, TI recommends using a small resister (R_O) in series with the output as close to the device as possible. Without R_O, capacitance on the output interacts with the output impedance of the amplifier causing phase shift in the loop gain of the amplifier that will reduce the phase margin. This will cause peaking in the frequency response and overshoot and ringing in the pulse response. Interaction with other parasitic elements may lead to instability or oscillation. Inserting R_O will isolate the phase shift from the feedback path and restore the phase margin; however, R_O can limit the bandwidth slightly.

图 8-5 shows the test circuit and Series Output Resistor vs Capacitive Load shows the recommended values of R_O versus capacitive loads, C_L. See Frequency Response With Capacitive Load for the frequency response with various values.

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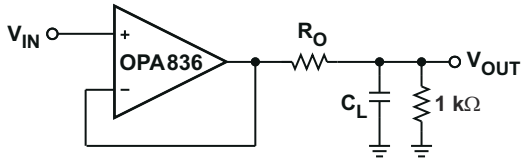

图 8-5. R_O versus C_L Test Circuit

8.4 Device Functional Modes

8.4.1 Split-Supply Operation (±1.25 V to ±2.75 V)

To facilitate testing with common lab equipment, the OPA836 EVM (see *OPA835DBV, OPA836DBV EVM*, SLOU314) is built to allow for split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers and other lab equipment have inputs and outputs with a ground reference.

图 8-6 shows a simple noninverting configuration analogous to 图 8-1 with ±2.5-V supply and V_{REF} equal to ground. The input and output will swing symmetrically around ground. For ease of use, split supplies are preferred in systems where signals swing around ground.

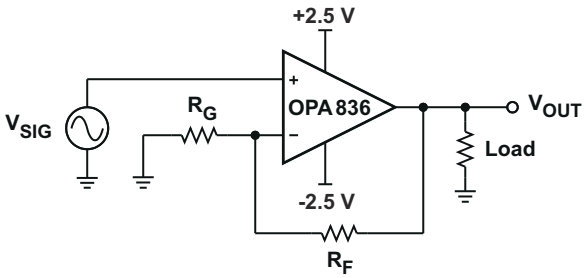

图 8-6. Split-Supply Operation

8.4.2 Single-Supply Operation (2.5 V to 5.5 V)

Often, newer systems use a single power supply to improve efficiency and reduce the cost of the power supply. The OPA836 and OPA2836 devices are designed for use with a single supply with no change in performance compared to a split supply, as long as the input and output are biased within the linear operation of the device.

To change the circuit from split supply to single supply, level shift of all voltages by half the difference between the power supply rails. For example, changing from ±2.5-V split supply to 5-V single supply is shown in 图 8-7.

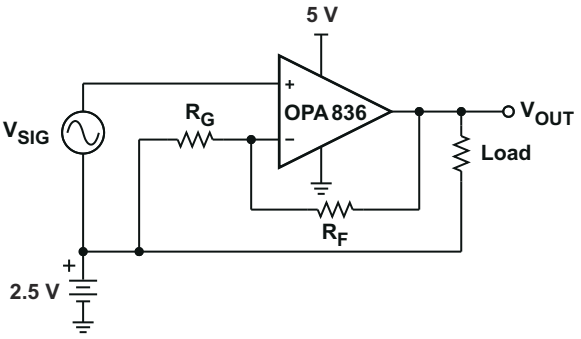

图 8-7. Single-Supply Concept

A practical circuit will have an amplifier or other circuit providing the bias voltage for the input, and the output of this amplifier stage provides the bias for the next stage.

图 8-8 shows a typical noninverting amplifiercircuit. With 5-V single-supply, a mid-supply reference generator is needed to bias the negative side through R_G. To cancel the voltage offset that would otherwise be caused by the

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input bias currents, R_1 is selected to be equal to R_F in parallel with R_G. For example, if gain of 2 is required and R_F = 1 kΩ, select R_G = 1 kΩ to set the gain and R_1 = 499 Ω for bias-current cancellation. The value for C depends on the reference; TI recommends a value of at least 0.1 µF to limit noise.

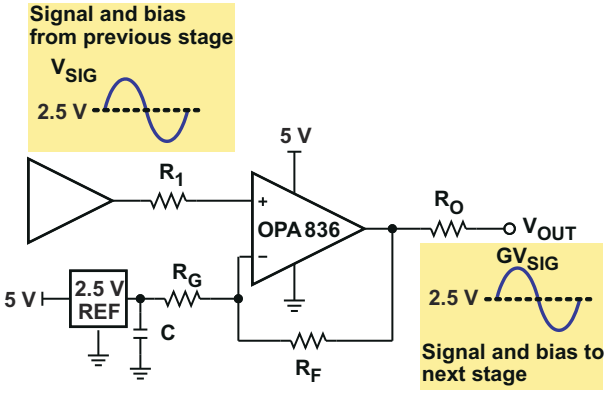

图 8-8. Noninverting Single Supply With Reference

图 8-9 shows a similar noninverting single-supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_G' and R_G" form a resistor divider from the 5-V supply and are used to bias the negative side with their parallel sum equal to the equivalent R_G to set the gain. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G' in parallel with R_G" (R_1= R_F || R_G' || R_G"). For example, if gain of 2 is required and R_F = 1 kΩ, selecting R_G' = R_G" = 2 kΩ gives equivalent parallel sum of 1 kΩ, sets the gain to 2, and references the input to mid supply (2.5 V). R_1 is then set to 499 Ω for bias-current cancellation. The resistor divider costs less than the 2.5 V reference in 图 8-8 but may increase the current from the 5-V supply.

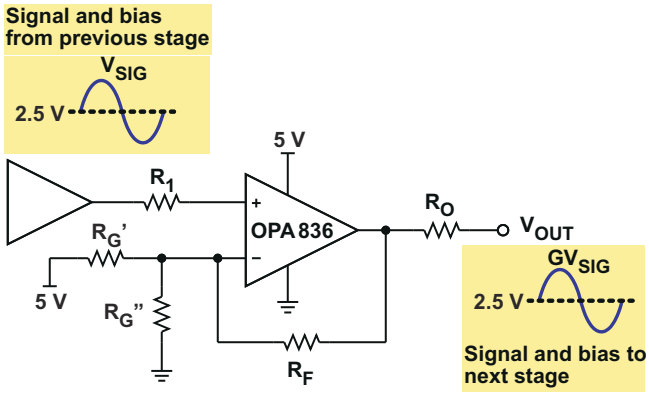

图 8-9. Noninverting Single Supply With Resistors

图 8-10 shows a typical inverting amplifier situation. With 5-V single supply, a mid-supply reference generator is needed to bias the positive side through R_1. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G. For example if gain of –2 is required and R_F = 1 kΩ, select R_G = 499 Ω to set the gain and R_1 = 332 Ω for bias-current cancellation. The value for C is dependent on the reference, but TI recommends a value of at least 0.1 µF to limit noise into the operational amplifier.

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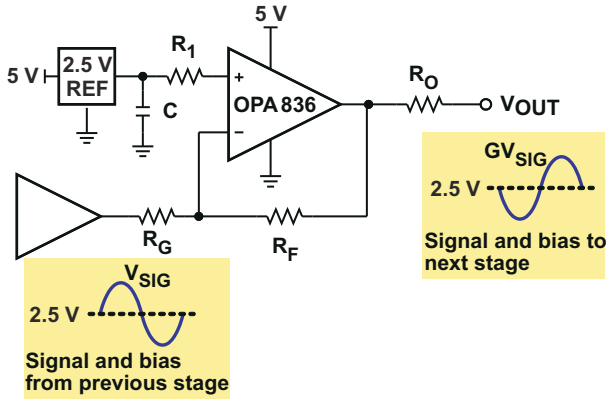

图 8-10. Inverting Single Supply With Reference

图 8-11 shows a similar inverting single-supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_1 and R_2 form a resistor divider from the 5-V supply and are used to bias the positive side. To cancel the voltage offset that would otherwise be caused by the input bias currents, set the parallel sum of R_1 and R_2 equal to the parallel sum of R_F and R_G. C must be added to limit coupling of noise into the positive input. For example if gain of –2 is required and R_F = 1 kΩ, select R_G = 499 Ω to set the gain. R_1 = R_2 = 665 Ω for mid-supply voltage bias and for operational amplifier input bias-current cancellation. A good value for C is 0.1 µF. The resistor divider costs less than the 2.5-V reference in 图 8-10 but may increase the current from the 5-V supply.

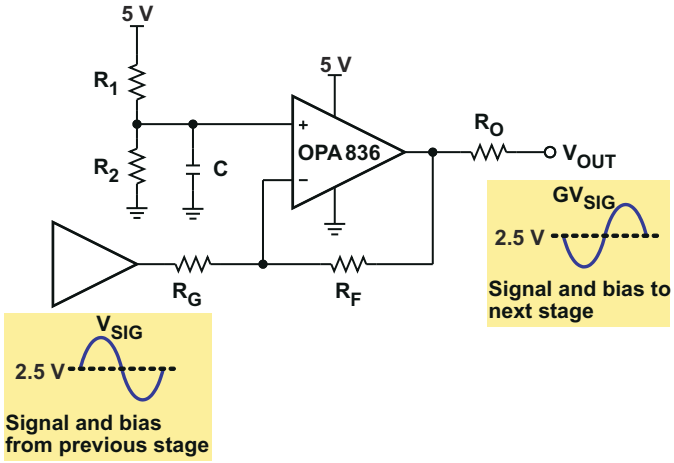

图 8-11. Inverting Single Supply With Resistors

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Noninverting Amplifier

The OPA836 and OPA2836 devices can be used as noninverting amplifiers with signal input to the noninverting input, V_{IN+} . A basic block diagram of the circuit is shown in 图 8-1.

If $V_{IN} = V_{REF} + V_{SIG}$, then the output of the amplifier may be calculated according to 方程式 1.

$$V_{OUT} = V_{SIG}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \quad (1)$$

The signal gain of the circuit is set by $G = 1 + \frac{R_F}{R_G}$, and V_{REF} provides a reference around which the input and output signals swing. Output signals are in-phase with the input signals.

The OPA836 and OPA2836 devices are designed for the nominal value of R_F to be 1 kΩ in gains other than +1. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. R_F = 1 kΩ must be used as a default unless other design goals require changing to other values. All test circuits used to collect data for this data sheet had R_F = 1 kΩ for all gains other than +1. Gain of +1 is a special case where R_F is shorted and R_G is left open.

9.1.2 Inverting Amplifier

The OPA836 and OPA2836 devices can be used as inverting amplifiers with signal input to the inverting input, V_{IN-} , through the gain setting resistor R_G. A basic block diagram of the circuit is shown in 图 8-2.

If $V_{IN} = V_{REF} + V_{SIG}$, then the output of the amplifier may be calculated according to 方程式 2.

$$V_{OUT} = V_{SIG}\left(\frac{-R_F}{R_G}\right) + V_{REF} \quad (2)$$

The signal gain of the circuit is set by $G = \frac{-R_F}{R_G}$, and V_{REF} provides a reference point around which the input and output signals swing. Output signals are 180° out-of-phase with the input signals. The nominal value of R_F must be 1 kΩ for inverting gains.

9.1.3 Instrumentation Amplifier

图 9-1 is an instrumentation amplifier that combines the high input impedance of the differential-to-differential amplifier circuit and the common-mode rejection of the differential-to-single-ended amplifier circuit. This circuit is often used in applications where high input impedance is required (such as taps from a differential line) or in cases where the signal source has a high output impedance.

If $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then the output of the amplifier may be calculated according to 方程式 3.

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$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right) + V_{REF} \quad (3)$$

The signal gain of the circuit is set by $G = \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right)$. V_{CM} is rejected, and V_{REF} provides a level shift around which the output signal swings. The single-ended output signal is in-phase with the differential input signal.

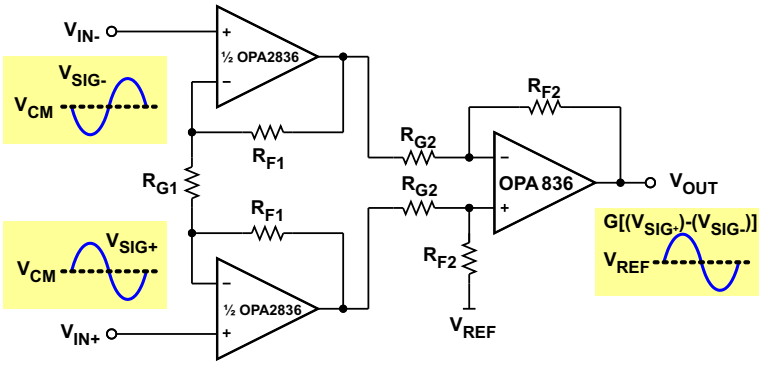

图 9-1. Instrumentation Amplifier

Integrated solutions are available, but the OPA836 device provides a much lower-power, high-frequency solution. For best CMRR performance, resistors must be matched. A good guideline to follow is CMRR ≈ the resistor tolerance; so, 0.1% tolerance will provide approximately 60-dB CMRR.

9.1.4 Attenuators

The noninverting circuit of 图 8-1 has minimum gain of 1. To implement attenuation, a resistor divider can be placed in series with the positive input, and the amplifier set for gain of 1 by shorting V_{OUT} to V_{IN-} and removing R_G. Because the operational amplifier input is high impedance, the resistor divider sets the attenuation.

The inverting circuit of 图 8-2 can be used as an attenuator by making R_G larger than R_F. The attenuation is the resistor ratio. For example, a 10:1 attenuator can be implemented with R_F = 1 kΩ and R_G = 10 kΩ.

9.1.5 Single-Ended-to-Differential Amplifier

图 9-2 shows an amplifier circuit that is used to convert single-ended signals to differential, and provides gain and level shifting. This circuit can be used for converting signals to differential in applications like line drivers for Cat5 cabling or driving differential-input SAR and ΔΣ ADCs.

With $V_{IN} = V_{REF} + V_{SIG}$, the output of the amplifier may be calculated according to 方程式 4.

$$V_{OUT+} = G \times V_{IN} + V_{REF} \quad \text{and } V_{OUT-} = -G \times V_{IN} + V_{REF} \quad \text{Where: } G = 1 + \frac{R_F}{R_G} \quad (4)$$

The differential-signal gain of the circuit is 2 × G, and V_{REF} provides a reference around which the output signal swings. The differential output signal is in-phase with the single-ended input signal.

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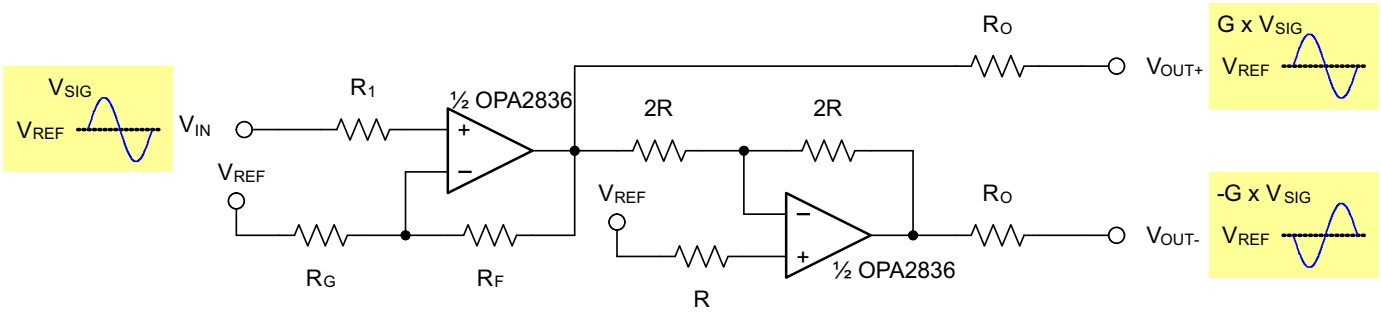

图 9-2. Single Ended to Differential Amplifier

Line termination on the output can be accomplished with resistors R_O. The differential impedance seen from the line will be 2 × R_O. For example, if 100-Ω Cat5 cable is used with double termination, the amplifier is typically set for a differential gain of 2 V/V (6 dB) with R_F = 0 Ω (short), R_G = open, 2R = 1 kΩ, R1 = 0 Ω, R = 499 Ω to balance the input bias currents, and R_O = 49.9 Ω for output line termination. This configuration is shown in 图 9-3.

For driving a differential-input ADC the situation is similar, but the output resistors, R_O are selected with a capacitor across the ADC input for optimum filtering and settling-time performance.

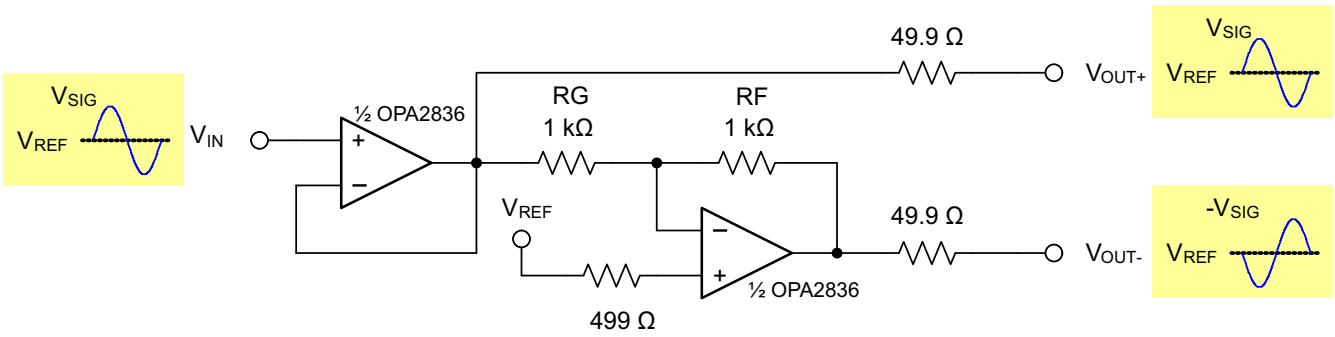

图 9-3. Cat5 Line Driver With Gain = 2 V/V (6 dB)

9.1.6 Differential-to-Signal-Ended Amplifier

图 9-4 shows a differential amplifier that is used to convert differential signals to single-ended and provides gain (or attenuation) and level shifting. This circuit can be used in applications like a line receiver for converting a differential signal from a Cat5 cable to a single-ended signal.

If $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then the output of the amplifier may be calculated according to 方程式 5.

$$V_{OUT} = \left(V_{IN+} - V_{IN-}\right) \times \left(\frac{R_F}{R_G}\right) + V_{REF} \tag{5}$$

The signal gain of the circuit is $G = \frac{R_F}{R_G}$, V_{CM} is rejected, and V_{REF} provides a level shift around which the output signal swings. The single ended output signal is in-phase with the differential input signal.

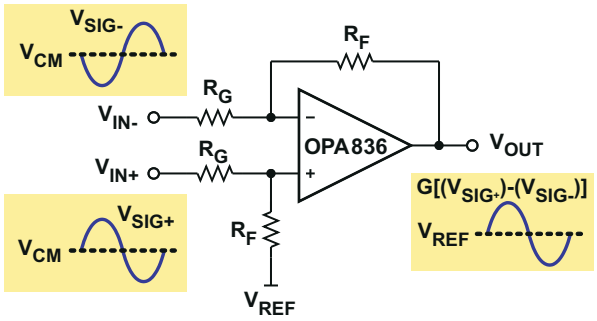

图 9-4. Differential to Single-Ended Amplifier

Line termination can be accomplished by adding a shunt resistor across the VIN+ and VIN- inputs. The differential impedance is the shunt resistance in parallel with the input impedance of the amplifier circuit, which is usually much higher. For low gain and low line impedance, the resistor value to add is approximately the impedance of the line. For example if 100-Ω Cat5 cable is used with a gain of 1 amplifier and $R_F = R_G = 1\ k\Omega$, adding a 100-Ω shunt across the input will give a differential impedance of 98 Ω, which is adequate for most applications.

For best CMRR performance, resistors must be matched. Assuming CMRR ≈ the resistor tolerance, a 0.1% tolerance will provide about 60-dB CMRR.

9.1.7 Differential-to-Differential Amplifier

图 9-5 shows a differential amplifier that is used to amplify differential signals. This circuit has high input impedance and is used in differential line driver applications where the signal source is a high-impedance driver (for example, a differential DAC) that must drive a line.

If $V_{IN\pm} = V_{CM} + V_{SIG\pm}$, then the output of the amplifier may be calculated according to 方程式 6.

$$V_{OUT\pm} = V_{IN\pm} \times \left(1 + \frac{2R_F}{R_G}\right) + V_{CM} \tag{6}$$

The signal gain of the circuit is set by $G = 1 + \frac{2R_F}{R_G}$, and V_{CM} passes with unity gain. The amplifier in essence combines two noninverting amplifiers into one differential amplifier that shares the R_G resistor, which makes R_G effectively half its value when calculating the gain. The output signals are in-phase with the input signals.

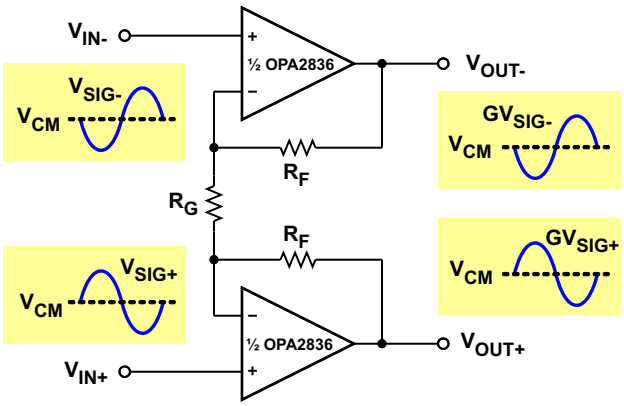

图 9-5. Differential to Differential Amplifier

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9.1.8 Gain Setting With OPA836 RUN Integrated Resistors

The OPA836 RUN package option includes integrated gain-setting resistors for smallest possible footprint on a printed circuit board (≈ 2.00 mm × 2.00 mm). By adding circuit traces on the PCB, gains of +1, –1, –1.33, +2, +2.33, –3, +4, –4, +5, –5.33, +6.33, –7, +8 and inverting attenuations of –0.1429, –0.1875, –0.25, –0.33, –0.75 can be achieved.

图 9-6 shows a simplified view of how the OPA836IRUN integrated gain-setting network is implemented. 表 9-1 lists the required pin connections for various noninverting and inverting gains (reference 图 8-1 and 图 8-2). 表 9-2 shows the required pin connections for various attenuations using the inverting-amplifier architecture (reference 图 8-2). Due to ESD protection devices being used on all pins, the absolute maximum and minimum input-voltage range, V_{S-} – 0.7 V to V_{S+} + 0.7 V, applies to the gain-setting resistors, so attenuation of large input voltages requires external resistors to implement.

The gain-setting resistors are laser trimmed to 1% tolerance with nominal values of 1.6 kΩ, 1.2 kΩ, and 400 Ω. The gain-setting resistors have excellent temperature coefficients, and gain drift is superior to the drift with external gain-setting resistors. The 500-Ω and 1.5-pF capacitor in parallel with the 1.6-kΩ gain-setting resistor provide compensation for best stability and pulse response.

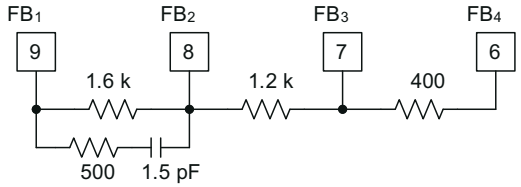

图 9-6. OPA836IRUN Gain-Setting Network

表 9-1. Gain Settings

NONINVERTING GAIN (图 8-1)	INVERTING GAIN (图 8-2)	SHORT PINS	SHORT PINS	SHORT PINS	SHORT PINS
1 V/V (0 dB)	—	1 to 9			—
2 V/V (6.02 dB)	–1 V/V (0 dB)	1 to 9	2 to 8	6 to GND	—
2.33 V/V (7.36 dB)	–1.33 V/V (2.5 dB)	1 to 9	2 to 8	7 to GND	—
4 V/V (12.04 dB)	–3 V/V (9.54 dB)	1 to 8	2 to 7	6 to GND	—
5 V/V (13.98 dB)	–4 V/V (12.04 dB)	1 to 9	2 to 7 or 8	7 to 8	6 to GND
6.33 V/V (16.03 dB)	–5.33 V/V (14.54 dB)	1 to 9	2 to 6 or 8	6 to 8	7 to GND
8 V/V (18.06 dB)	–7 V/V (16.90 dB)	1 to 9	2 to 7	6 to GND	—

表 9-2. Attenuator Settings

INVERTING GAIN (图 8-2)	SHORT PINS	SHORT PINS	SHORT PINS	SHORT PINS
–0.75 V/V (–2.5 dB)	1 to 7	2 to 8	9 to GND	—
–0.333 V/V (–9.54 dB)	1 to 6	2 to 7	8 to GND	—
–0.25 V/V (–12.04 dB)	1 to 6	2 to 7 or 8	7 to 8	9 to GND
–0.1875 V/V (–14.54 dB)	1 to 7	2 to 6 or 8	6 to 8	9 to GND
–0.1429 V/V (–16.90 dB)	1 to 6	2 to 7	9 to GND	—

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9.1.9 Pulse Application With Single-Supply

For pulsed applications, where the signal is at ground and pulses to a positive or negative voltage, the circuit bias-voltage considerations differ from those in an application with a signal that swings symmetrical about a reference point. 图 9-7 shows a circuit where the signal is at ground (0 V) and pulses to a positive value.

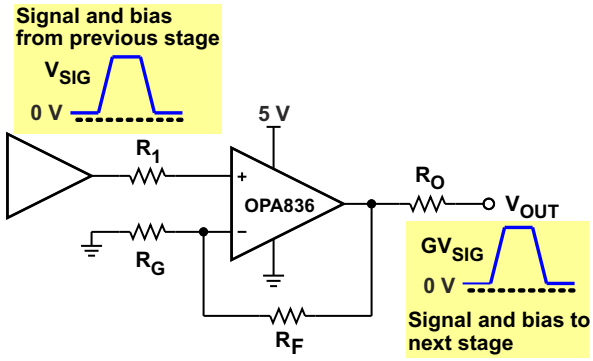

图 9-7. Noninverting Single Supply With Pulse

If the input signal pulses negative from ground, an inverting amplifier is more appropriate as shown in 图 9-8. A key consideration in noninverting and inverting cases is that the input and output voltages are kept within the limits of the amplifier. Because the V_{ICR} of the OPA836 device includes the negative supply rail, the OPA836 operational amplifier is well-suited to this application.

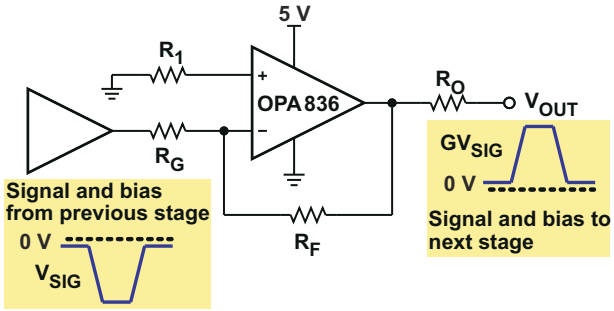

图 9-8. Inverting Single Supply With Pulse

9.1.10 ADC Driver Performance

The OPA836 device provides excellent performance when driving high-performance delta-sigma ($\Delta\Sigma$) and successive-approximation-register (SAR) ADCs in low-power audio and industrial applications.

To show achievable performance, the OPA836 device is tested as the drive amplifier for the ADS8326. The ADS8326 is a 16-bit, micro power, SAR ADC with pseudodifferential inputs and sample rates up to 250 kSPS. The device offers excellent noise and distortion performance in a small 8-pin SOIC or VSSOP (MSOP) package. Low power and small size make the ADS8326 and OPA836 devices an ideal solution for portable and battery-operated systems, remote data-acquisition modules, simultaneous multichannel systems, and isolated data acquisition.

With the circuit shown in 图 9-9 to test the performance, 图 9-10 shows the FFT plot with a 10-kHz input signal. The tabulated AC analysis is in 表 9-3.

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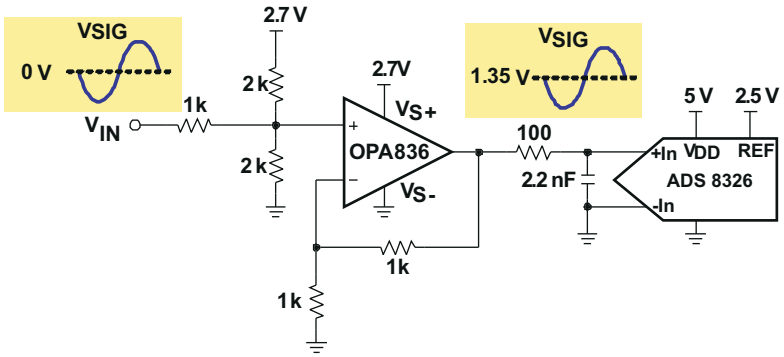


图 9-9. OPA836 and ADS8326 Test Circuit

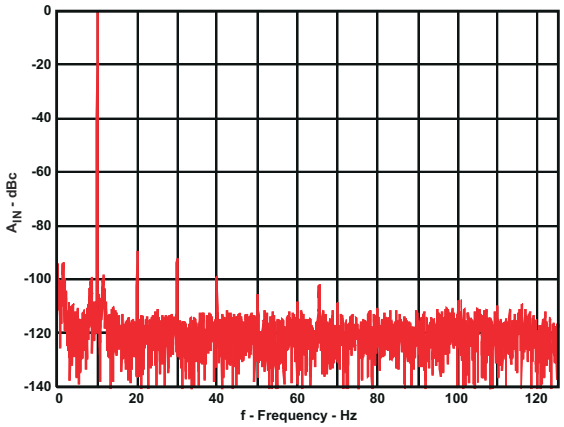


图 9-10. ADS8326 and OPA836 10-kHz FFT

表 9-3. AC Analysis

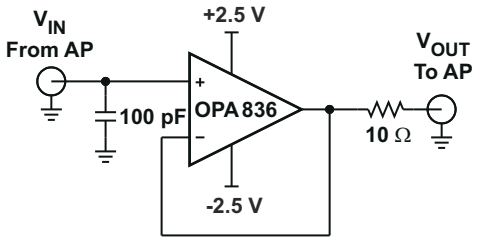
TONE (Hz)	SIGNAL (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
10k	– 0.85	83.3	– 86.6	81.65	88.9

9.2 Typical Applications

9.2.1 Audio Frequency Performance

The OPA836 and OPA2836 devices provide excellent audio performance with low quiescent power. To show performance in the audio band, an audio analyzer from Audio Precision (2700 series) tests THD+N and FFT at 1 V_{RMS} output voltage.

OPA836 Audio Precision Analyzer Test Circuit shows the circuit used for the audio-frequency performance test.



The 100-pF capacitor to ground on the input helped to decouple noise pick up in the lab and improved noise performance.

图 9-11. OPA836 Audio Precision Analyzer Test Circuit

9.2.1.1 Design Requirements

Design a low distortion, single-ended input to single-ended output audio amplifier using the OPA836 device. The 2700-series audio analyzer from Audio Precision is used as the signal source and also as the measurement system.

表 9-4. Design Requirements

CONFIGURATION	INPUT EXCITATION	PERFORMANCE TARGET	R_{Load}
OPA836 Unity Gain Config.	1 KHz Tone Frequency	>110 dBc SFDR	300 Ω and 100 kΩ

9.2.1.2 Detailed Design Procedure

The OPA836 device is tested in this application in a unity-gain buffer configuration. A buffer configuration is selected for maximum loop gain of the amplifier circuit. At higher closed-loop gains, the loop gain of the circuit reduces, which increases the harmonic distortion. The relationship between distortion and closed-loop gain at a fixed input frequency is shown in Harmonic Distortion vs Gain in 节 7.9. The test was performed under using resistive loads of 300 Ω and 100 KΩ. Harmonic Distortion vs Load Resistance shows the distortion performance of the amplifier versus the resistive load. Output loading, output swing, and closed-loop gain play a key role in determining the distortion performance of the amplifier.

Note

The 100-pF capacitor to ground on the input helped to decouple noise pickup in the lab and improved noise performance.

The Audio Precision was configured as a single-ended output in this application circuit. In applications where a differential output is available, the OPA836 device can be configured as a differential-to-single-ended amplifier as shown in 图 9-4. Power-supply bypassing is critical to reject noise from the power supplies. A 2.2-μF supply decoupling capacitor must be placed within 2 inches of the device and can be shared with other operational amplifiers on the same board. A 0.1-μF supply decoupling capacitor must be placed as close to the supply pins as possible, preferably within 0.1 inch. For a split supply, a capacitor is required for both supplies. A 0.1-μF capacitor placed directly between the supplies is also beneficial for improving system noise performance. If the output load is heavy, such as 16 Ω to 32 Ω, performance of the amplifier could begin to degrade. To drive such heavy loads, both channels of the OPA2836 device can be paralleled with their outputs isolated with 1-Ω resistors to reduce the loading effects.

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9.2.1.3 Application Curves

图 9-12 shows the THD+N performance with 100-kΩ and 300-Ω loads, and with A-weighting and with no weighting. Both loads show similar performance. With no weighting, the THD+N performance is dominated by the noise for both loads. A-weighting provides filtering that improves the noise, revealing the increased distortion with RL = 300 Ω.

图 9-13 and 图 9-14 show the FFT output with a 1-kHz tone and 100-kΩ and 300-Ω loads. To show relative performance of the device versus the test set, one channel has the OPA836 device in-line between the generator output and the analyzer. The other channel is in "Gen Mon" loopback mode, which internally connects the signal generator to the analyzer input. With 100-kΩ load, 图 9-13, the curves are indistinguishable from each other except for noise, which means the OPA836 device cannot be directly measured. With 300-Ω load, as shown in 图 9-14, the main difference between the curves is that the OPA836 device shows slightly higher even-order harmonics, but the performance of the test set masks the odd-order harmonics.

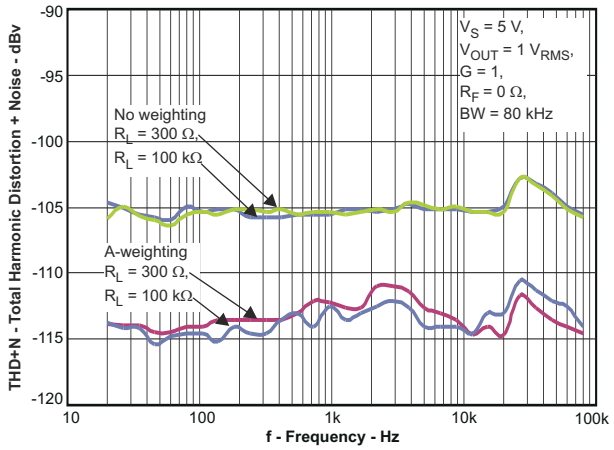

图 9-12. OPA836 1 V_{RMS} 20-Hz to 80-kHz THD+N

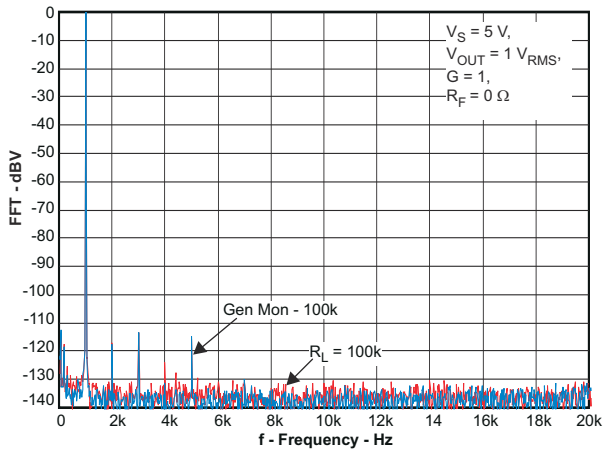

图 9-13. OPA836 and AP Gen Mon 10-kHz FFT Plot; V_{OUT} = 1 V_{RMS}, R_L = 100 kΩ

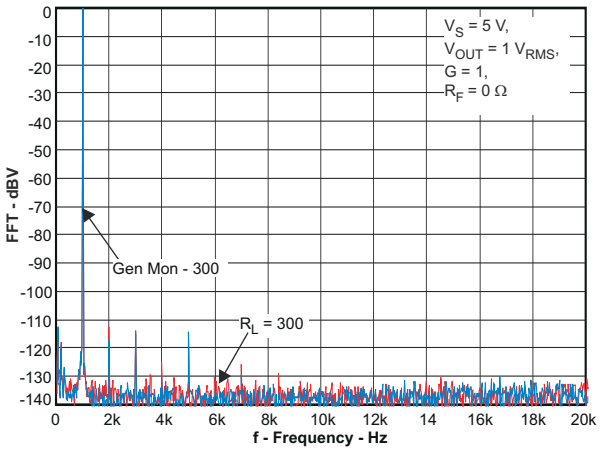

图 9-14. OPA836 and AP Gen Mon 10-kHz FFT Plot; V_{OUT} = 1 V_{RMS}, R_L = 300 Ω

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9.2.2 Active Filters

The OPA836 and OPA2836 devices are good choices for active filters. 图 9-15 and 图 9-16 show MFB and Sallen-Key circuits designed using the *WEBENCH® Filter Designer* to implement second-order low-pass Butterworth filter circuits. 图 9-17 shows the frequency response.

Other MFB and Sallen-Key filter circuits offer similar performance. The main difference is the MFB is an inverting amplifier in the pass-band and the Sallen-Key is noninverting. The primary advantage for each is the Sallen-Key in unity gain has no resistor gain-error term, and thus no sensitivity to gain error, while the MFB has better attenuation properties beyond the bandwidth of the operational amplifier.

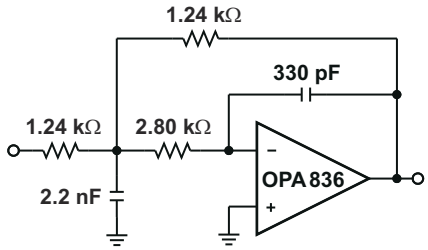

图 9-15. MFB 100-kHz Second-Order Low-Pass Butterworth Filter Circuit

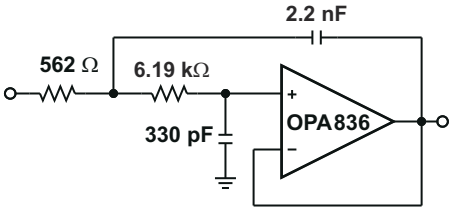

图 9-16. Sallen-Key 100-kHz Second-Order Low-Pass Butterworth Filter Circuit

9.2.2.1 Application Curve

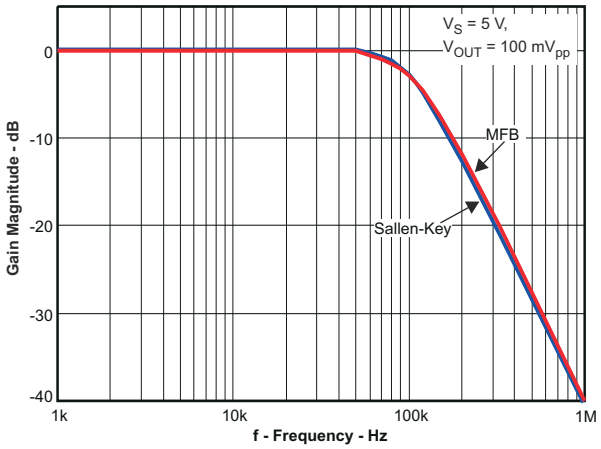

图 9-17. MFB and Sallen-Key Second Order Low-Pass Butterworth Filter Response

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10 Power Supply Recommendations

The OPAx836 devices are intended to work in a supply range of 2.7 V to 5 V. Supply-voltage tolerances are supported with the specified operating range of 2.5 V (7% on a 2.7-V supply) and 5.5 V (10% on a 5-V supply). Good power-supply bypassing is required. Minimize the distance (< 0.1 inch) from the power-supply pins to high frequency, 0.1-μF decoupling capacitors. A larger capacitor (2.2 μF is typical) is used along with a high frequency, 0.1-μF supply decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors for each supply to ground. If necessary, place the larger capacitors farther from the device and share these capacitors among several devices in the same area of the PCB. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) reduces second harmonic distortion.

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11 Layout

11.1 Layout Guidelines

The *OPA835DBV, OPA836DBV EVM* (SLOU314) can be used as a reference when designing the circuit board. TI recommends following the EVM layout of the external components near the amplifier, ground-plane construction, and power routing. General guidelines are listed as follows:

1. Signal routing must be direct and as short as possible into and out of the operational amplifier.
2. The feedback path must be short and direct avoiding vias if possible especially with G = +1.
3. Ground or power planes must be removed from directly under the negative input and output pins of the amplifier.
4. TI recommends placing a series output resistor as close to the output pin as possible. See *Series Output Resistor vs Capacitive Load* (Series Output Resistor vs Capacitive Load) for recommended values for the expected capacitive load.
5. A 2.2-µF power-supply decoupling capacitor must be placed within two inches of the device and can be shared with other operational amplifiers. For spit supply, a capacitor is required for both supplies.
6. A 0.1-µF power-supply decoupling capacitor must be placed as close to the power supply pins as possible, preferably within 0.1 inch. For split supply, a capacitor is required for both supplies.
7. The $\overline{PD}$ pin uses TTL logic levels. If the pin is not used, it must be tied to the positive supply to enable the amplifier. If the pin is used, it must be actively driven. A bypass capacitor is not necessary, but is used for robustness in noisy environments.

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11.2 Layout Example

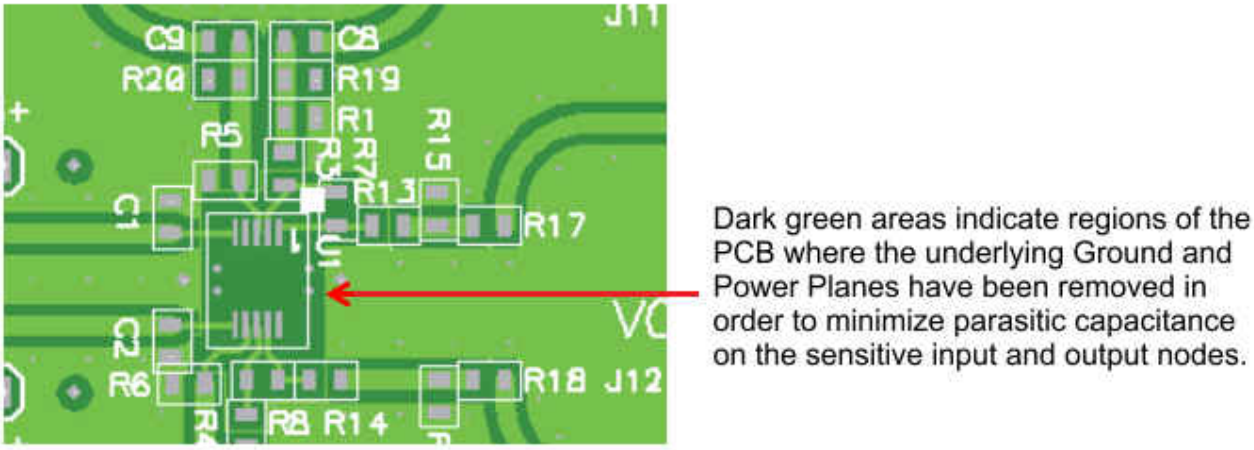

图 11-1. Top Layer

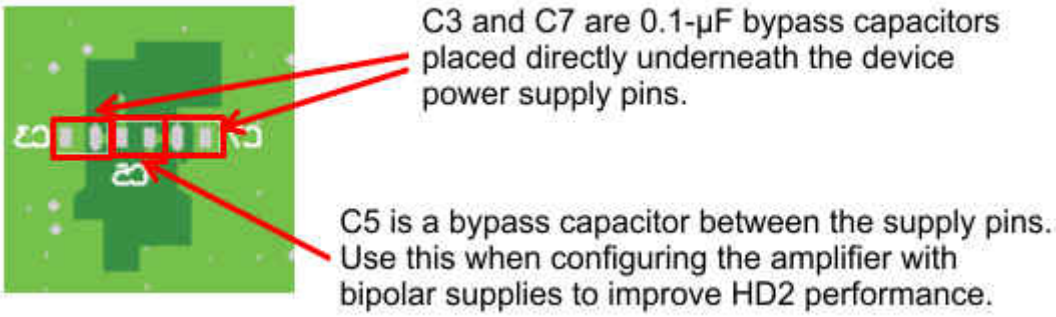

图 11-2. Bottom Layer

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

WEBENCH® Filter Designer

12.1.2 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPA835DBV, OPA836DBV EVM* user's guide

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2836ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2836	Samples
OPA2836IDGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2836	Samples
OPA2836IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2836	Samples
OPA2836IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2836	Samples
OPA2836IRMCR	ACTIVE	UQFN	RMC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2836	Samples
OPA2836IRMCT	ACTIVE	UQFN	RMC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2836	Samples
OPA2836IRUNR	ACTIVE	QFN	RUN	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2836	Samples
OPA2836IRUNT	ACTIVE	QFN	RUN	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2836	Samples
OPA836IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	QTL	Samples
OPA836IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	QTL	Samples
OPA836IRUNR	ACTIVE	QFN	RUN	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	836	Samples
OPA836IRUNT	ACTIVE	QFN	RUN	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	836	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

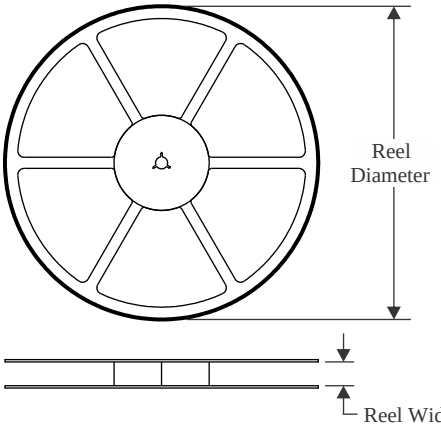
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

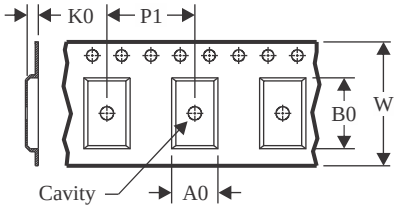
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

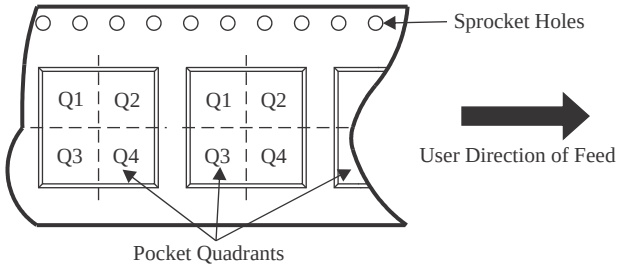


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

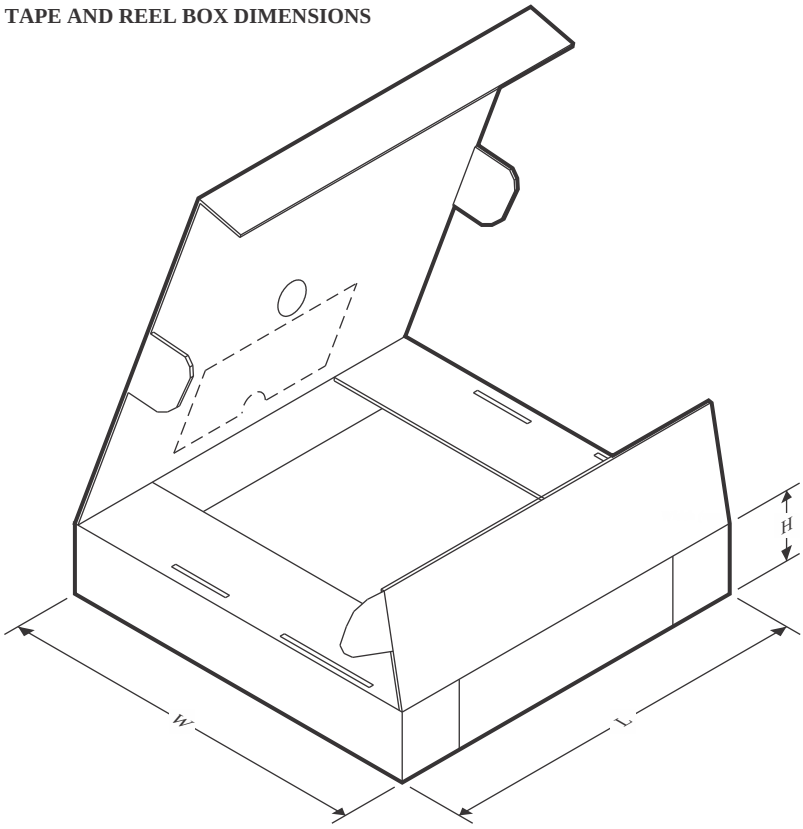
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2836IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2836IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2836IRMCR	UQFN	RMC	10	3000	180.0	9.5	2.3	2.3	1.1	2.0	8.0	Q2
OPA2836IRMCT	UQFN	RMC	10	250	180.0	9.5	2.3	2.3	1.1	2.0	8.0	Q2
OPA2836IRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2836IRUNT	QFN	RUN	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA836IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA836IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA836IRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA836IRUNT	QFN	RUN	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

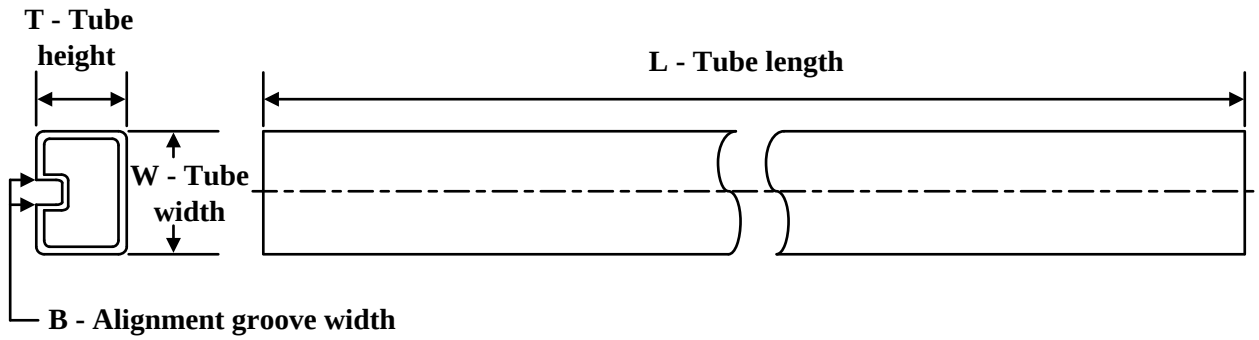
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2836IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
OPA2836IDR	SOIC	D	8	2500	340.5	338.1	20.6
OPA2836IRMCR	UQFN	RMC	10	3000	205.0	200.0	30.0
OPA2836IRMCT	UQFN	RMC	10	250	205.0	200.0	30.0
OPA2836IRUNR	QFN	RUN	10	3000	210.0	185.0	35.0
OPA2836IRUNT	QFN	RUN	10	250	210.0	185.0	35.0
OPA836IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA836IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
OPA836IRUNR	QFN	RUN	10	3000	210.0	185.0	35.0
OPA836IRUNT	QFN	RUN	10	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

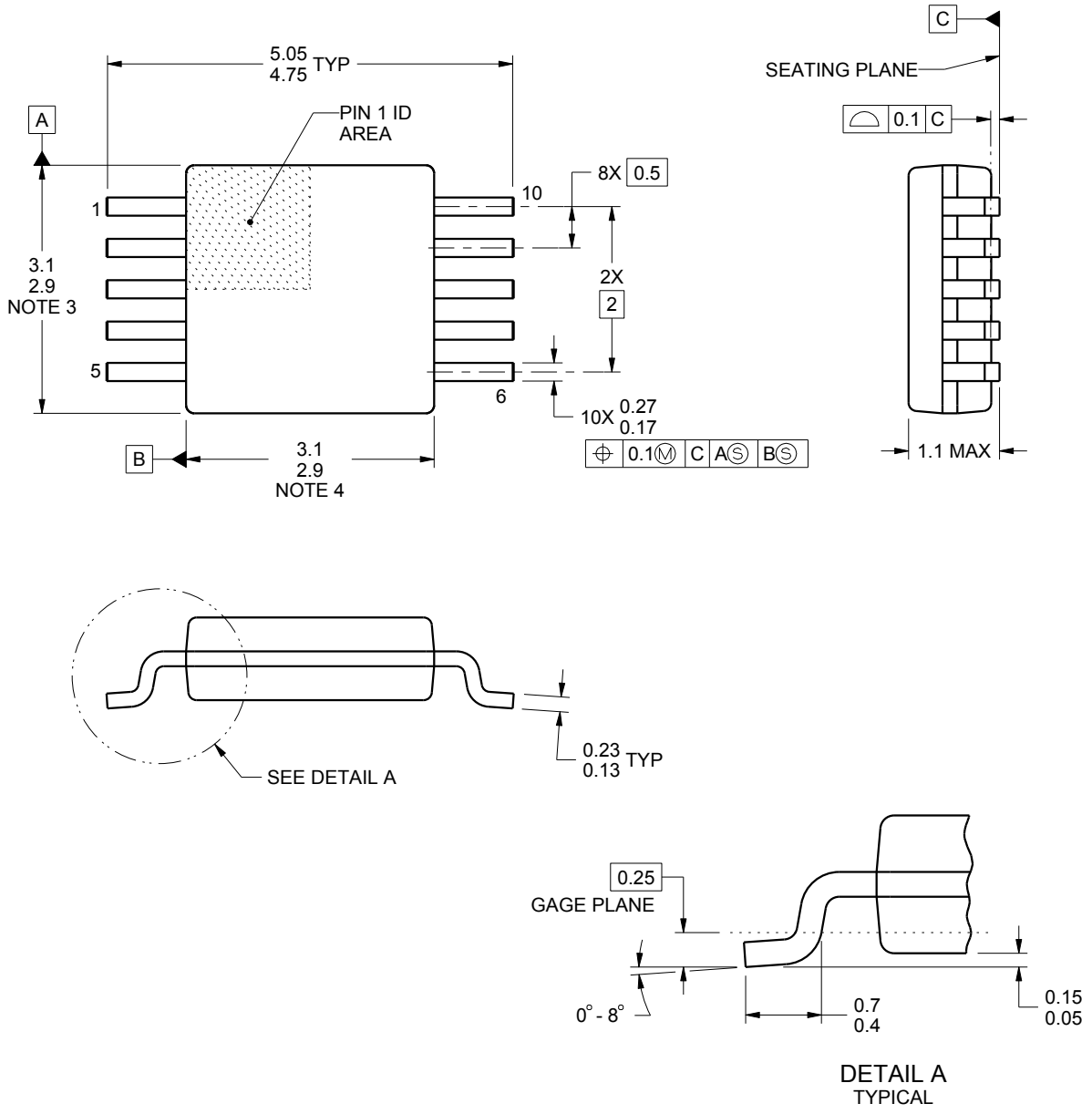
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2836ID	D	SOIC	8	75	507	8	3940	4.32
OPA2836IDGS	DGS	VSSOP	10	80	330	6.55	500	2.88

PACKAGE OUTLINE

DGS0010A

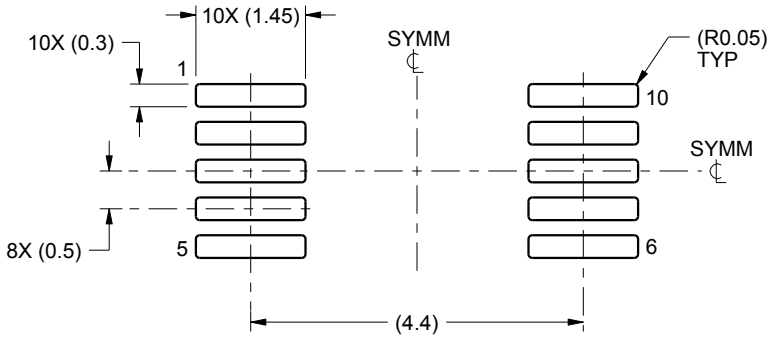
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

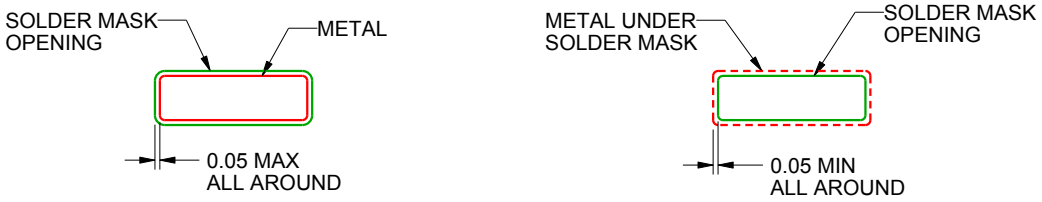


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

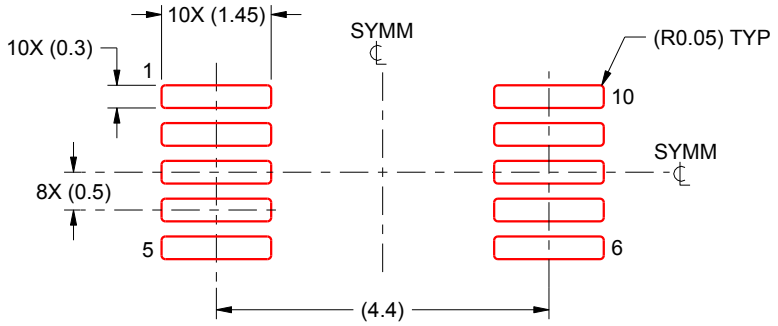


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

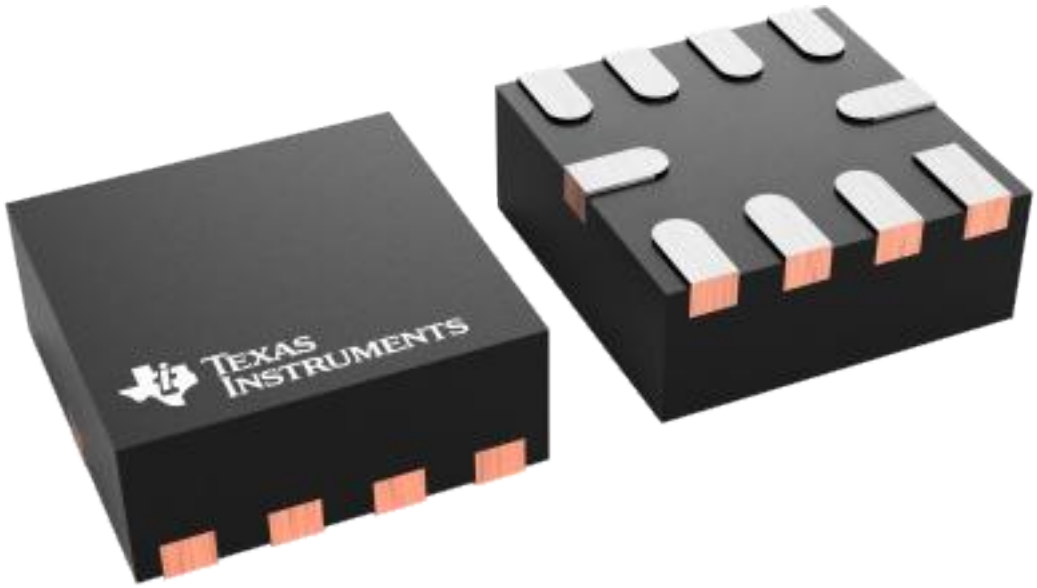
RUN 10

WQFN - 0.8 mm max height

2 X 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



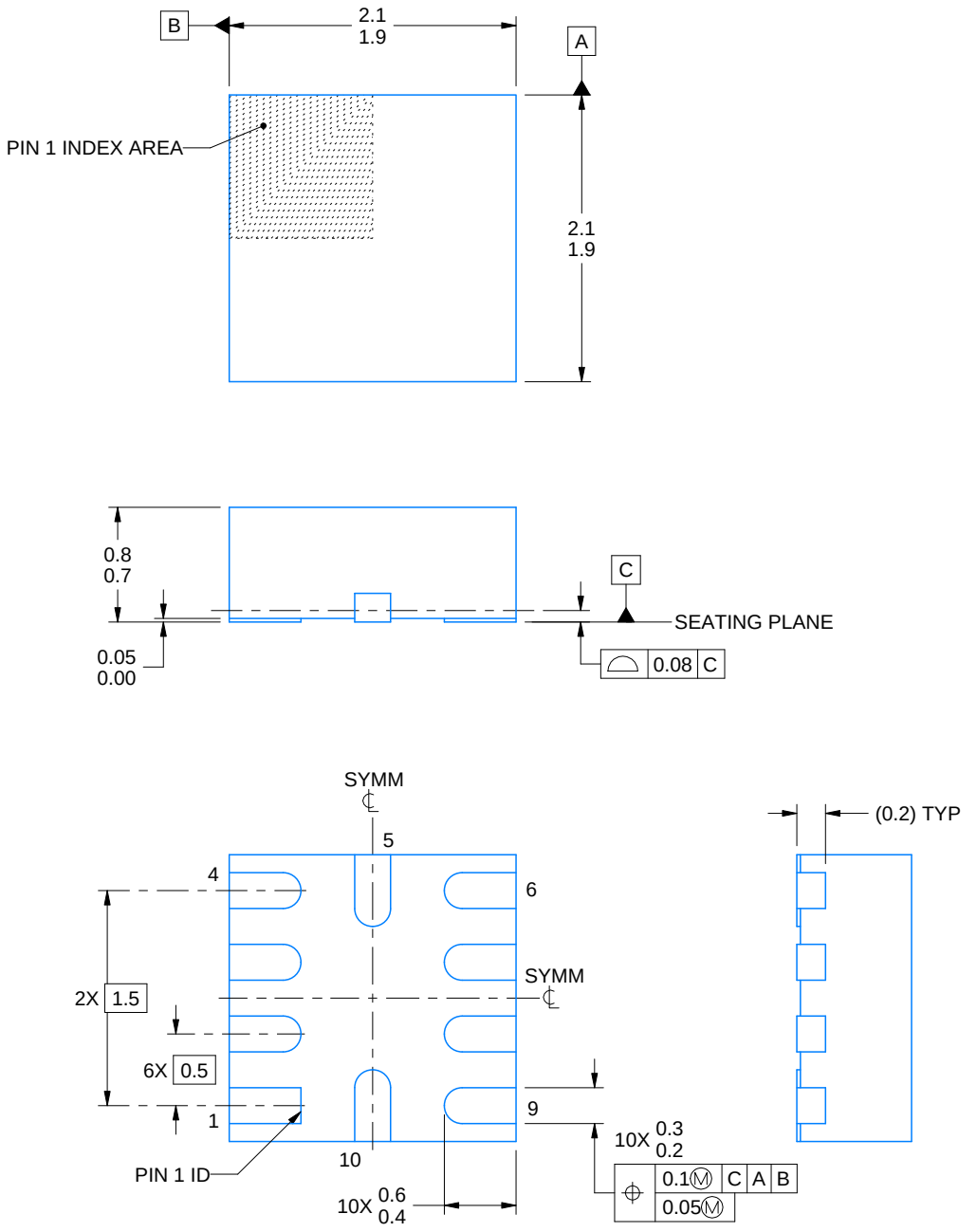
4228249/A

RUN0010A

PACKAGE OUTLINE

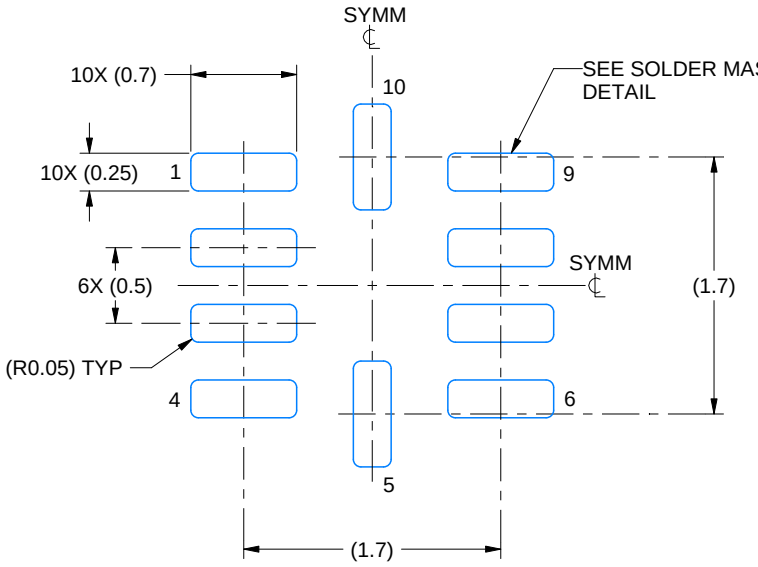
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

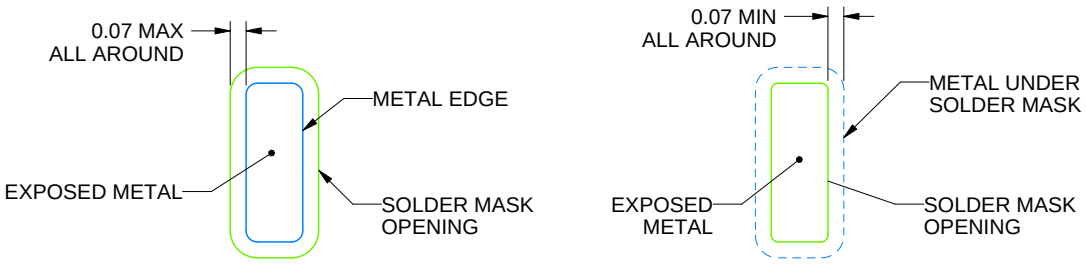


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4220470/A 05/2020

NOTES: (continued)

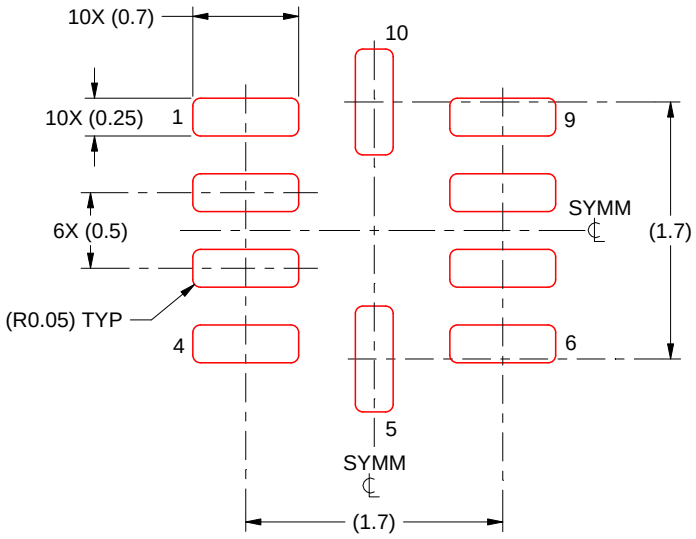
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUN0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

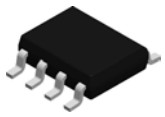


SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4220470/A 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

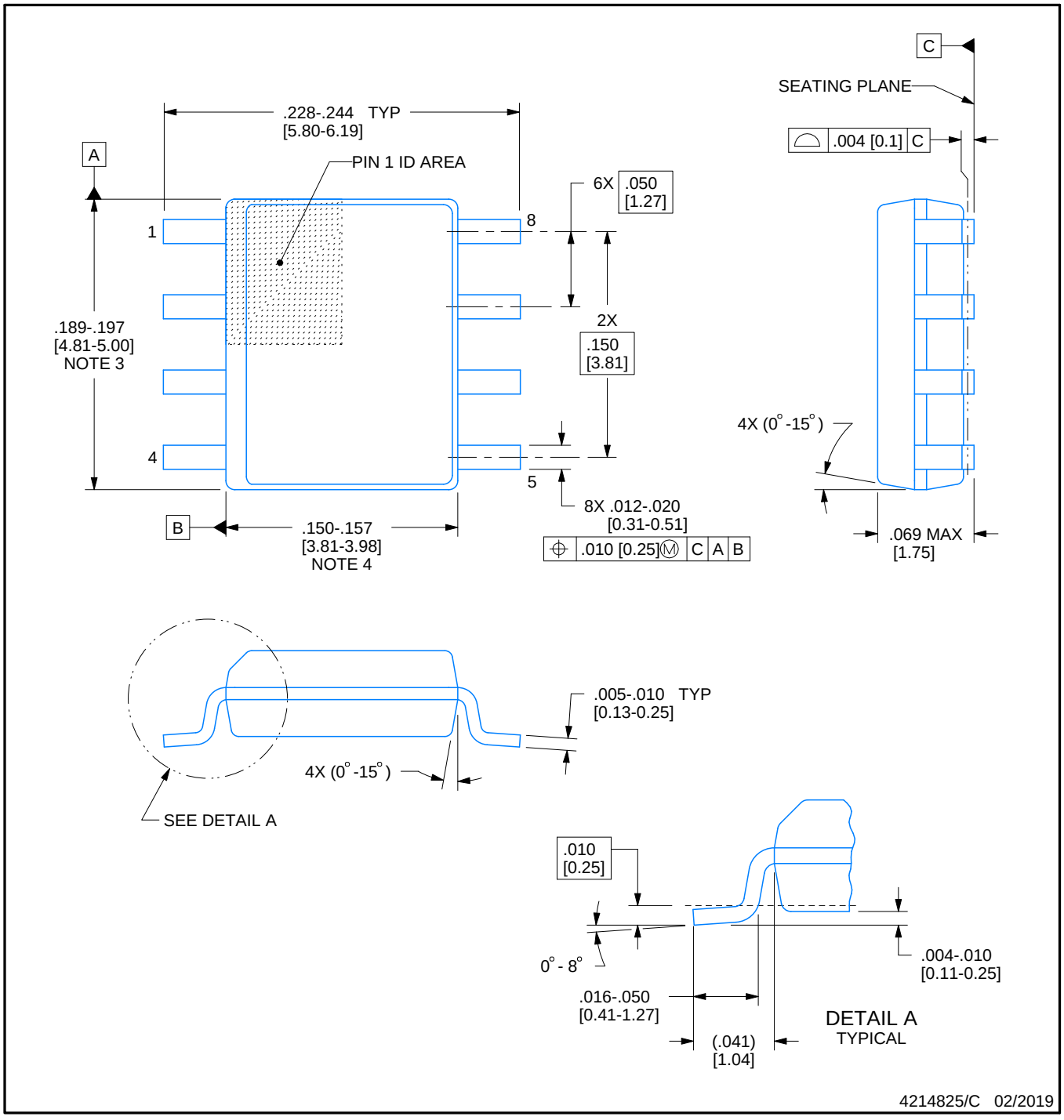


PACKAGE OUTLINE

D0008A

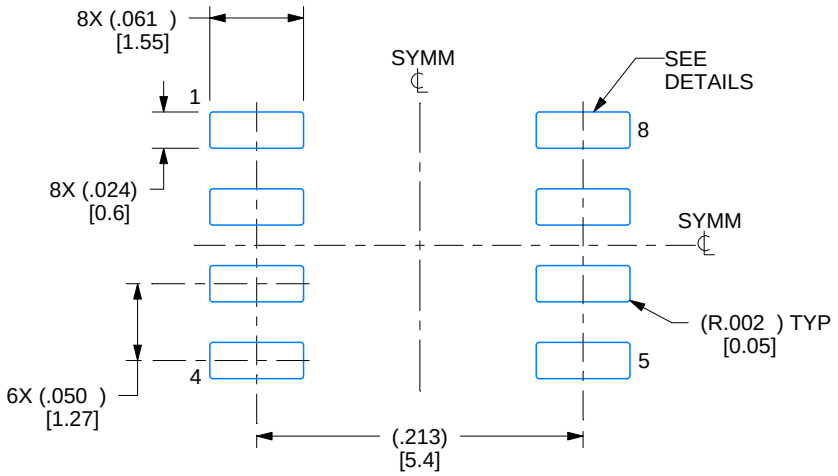
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

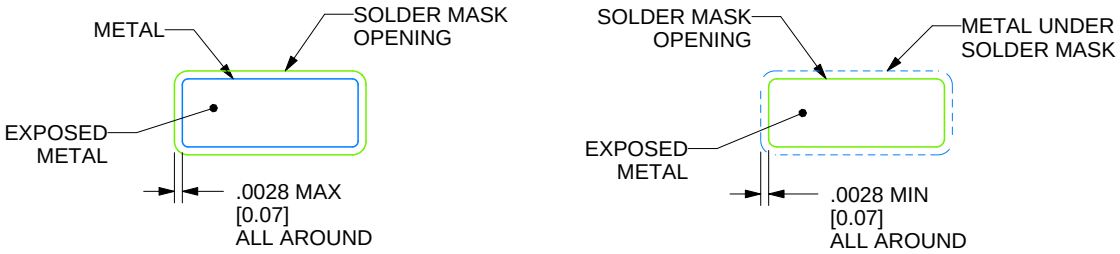


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

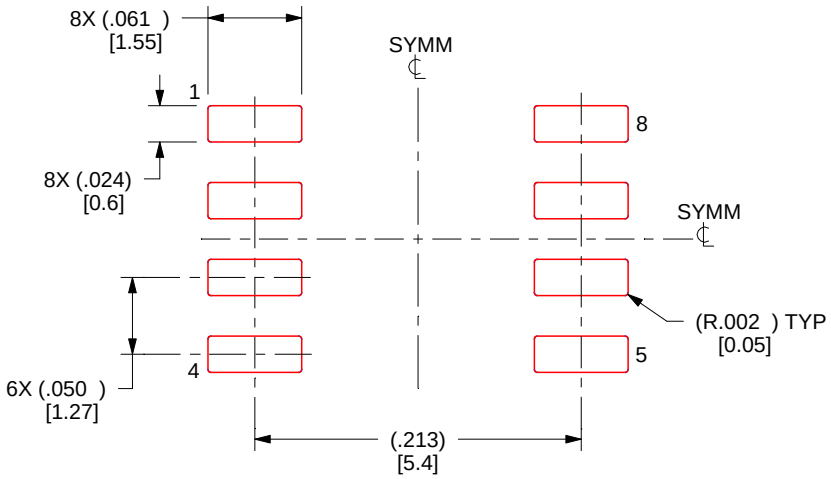
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

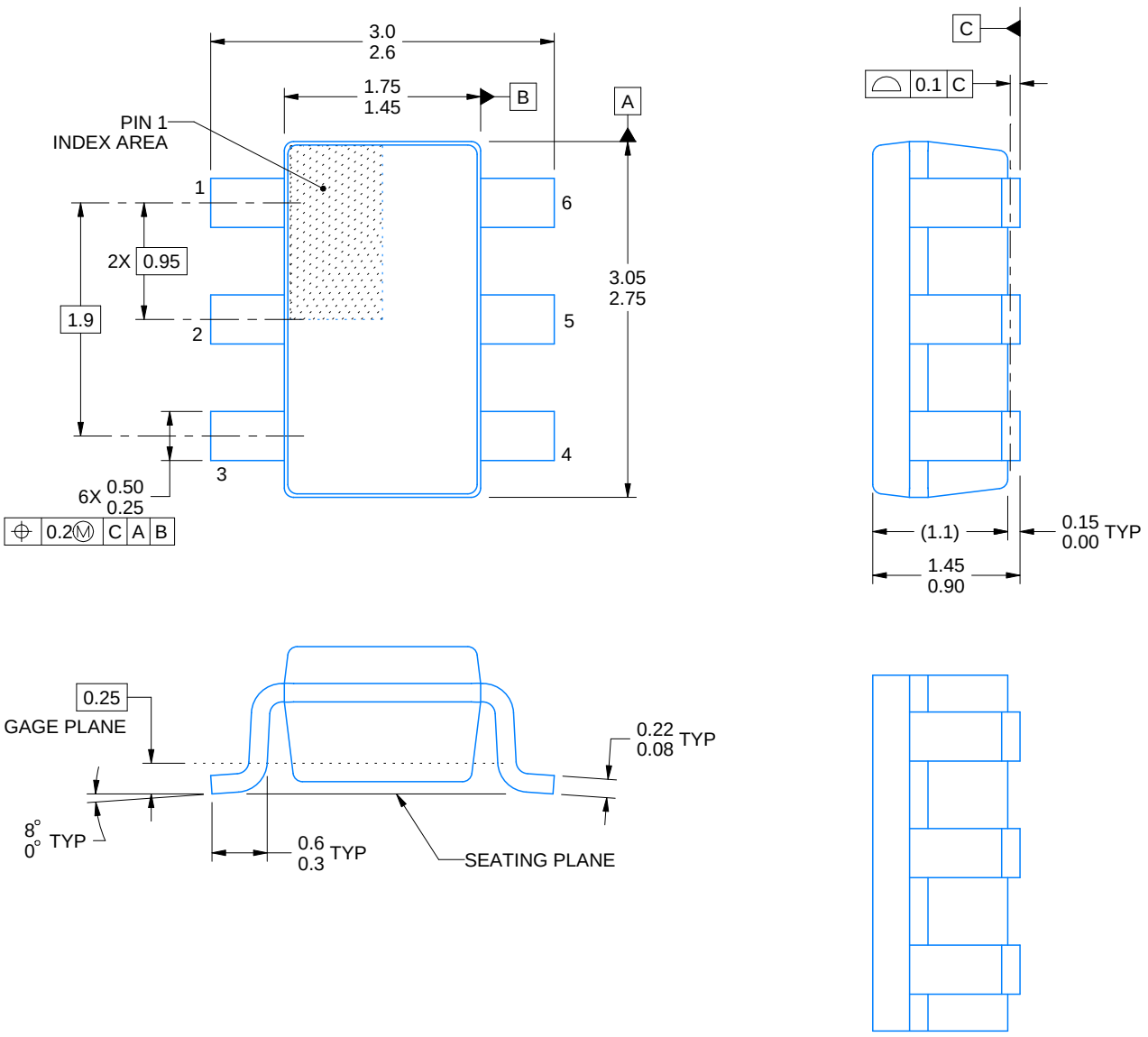
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

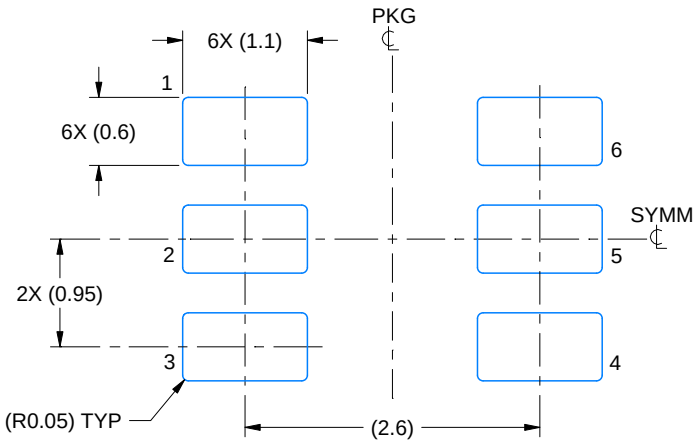


ALTERNATIVE PACKAGE SINGULATION VIEW

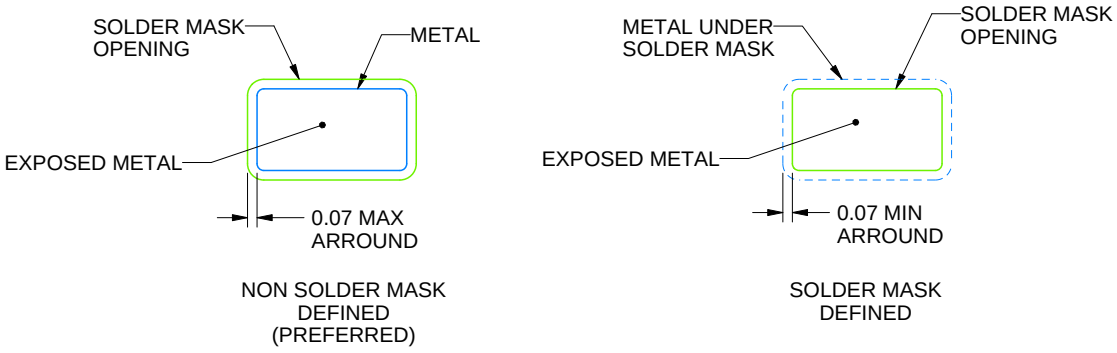
4214840/F 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

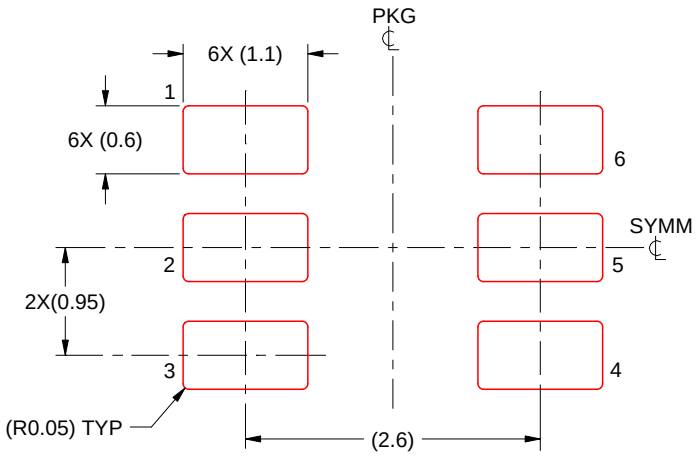


SOLDER MASK DETAILS

4214840/F 05/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



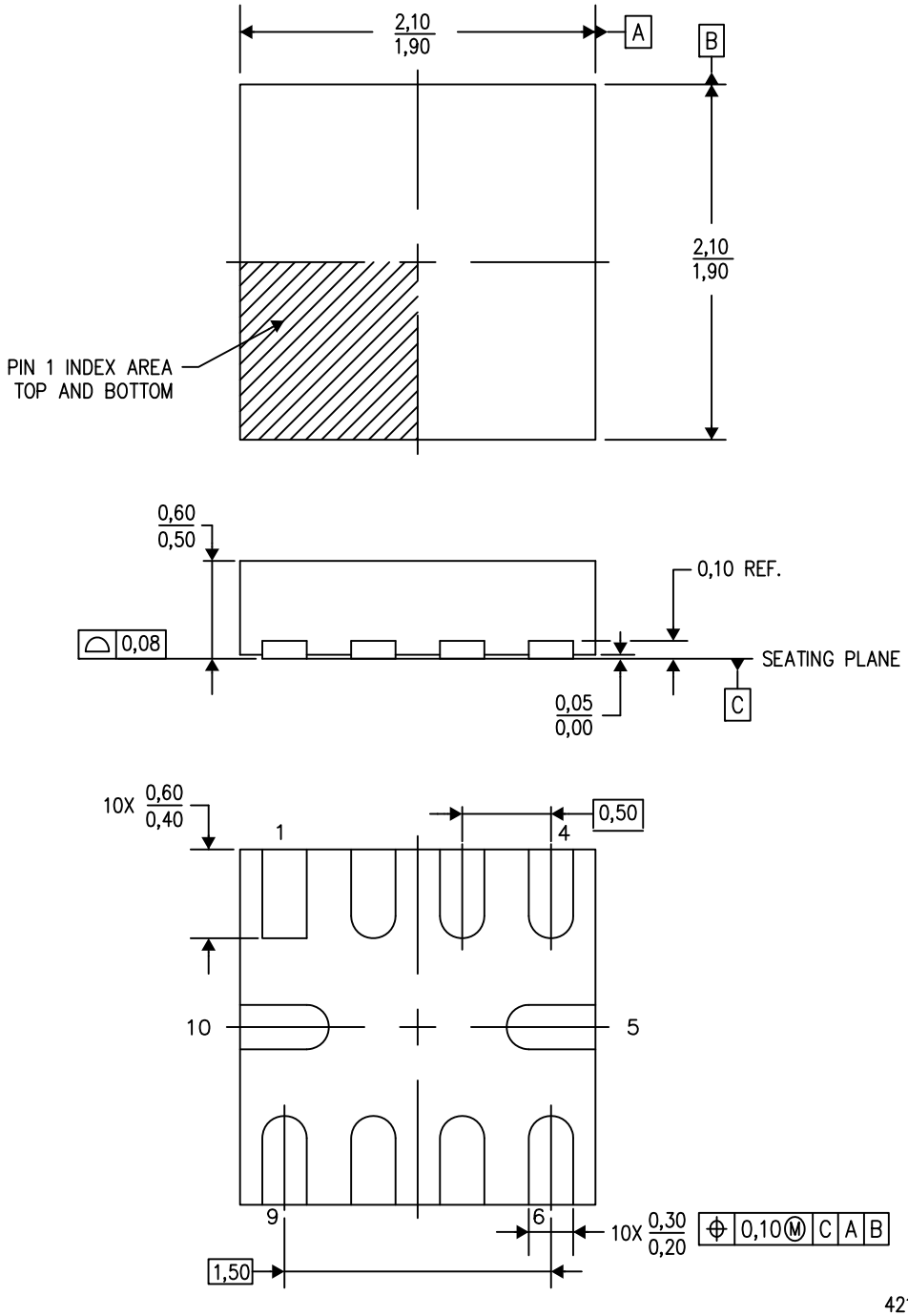
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

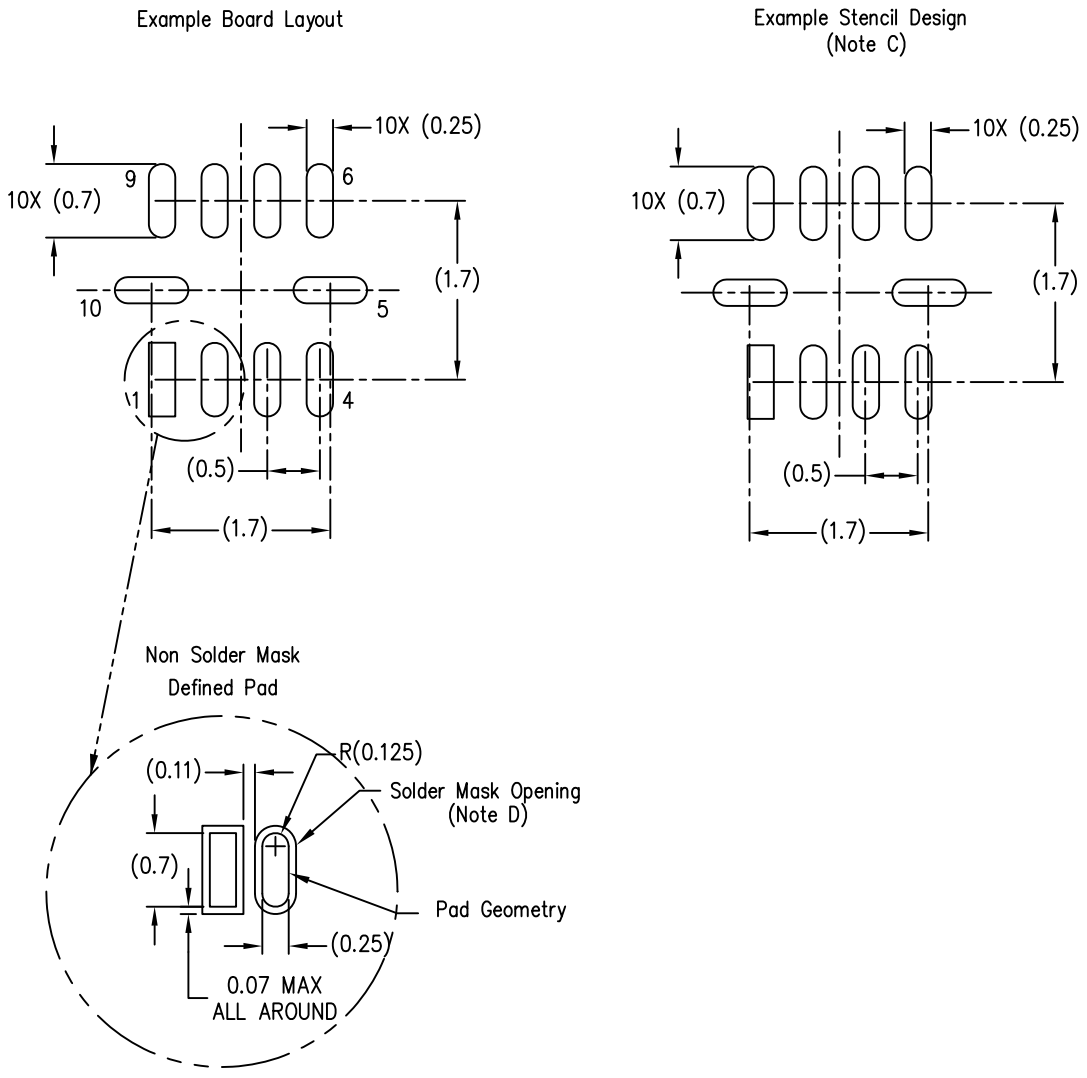
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RMC (S–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.

RMC (S–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



4221693/A 10/2014

NOTES:
A. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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