

IRHNKC9A7130 (JANSR2N7648U3CE)

PD-97977A

Radiation Hardened Power MOSFET
Surface Mount (SMD-0.5e Ceramic Lid)
100V, 35A, N-channel, R9 Superjunction Technology

Features

- Low $R_{DS(on)}$
- Fast switching
- Single event effect (SEE) hardened
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Ceramic package
- Light weight
- Enhanced Surface mount package for direct-to-PCB mounting
- ESD rating: class 2 per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives
- Electric propulsion

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R9 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 89.8MeV·cm²/mg. Their combination of low $R_{DS(on)}$ and faster switching times reduces the power losses and increases power density in today's high speed switching applications such as DC-DC converters and motor controllers. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 **Ordering options**

Part number	Package	Screening Level	TID Level
IRHNKC9A7130	SMD-0.5e (Ceramic Lid)	COTS	100 krad (Si)
JANSR2N7648U3CE	SMD-0.5e (Ceramic Lid)	JANS	100 krad (Si)
IRHNKC9A3130	SMD-0.5e (Ceramic Lid)	COTS	300 krad (Si)
JANSF2N7648U3CE	SMD-0.5e (Ceramic Lid)	JANS	300 krad (Si)

Product Summary

- **BV_{DS}** : 100V
- **I_D** : 35A
- **$R_{DS(on), max}$** : 34m Ω
- **$Q_{G, max}$** : 48nC
- **REF**: MIL-PRF-19500/775



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Absolute Maximum Ratings

1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 12V, T_C = 25^{\circ}C$	Continuous Drain Current	35	A
$I_{D2} @ V_{GS} = 12V, T_C = 100^{\circ}C$	Continuous Drain Current	22	A
$I_{DM} @ T_C = 25^{\circ}C$	Pulsed Drain Current ¹	140	A
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/ $^{\circ}C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ²	605	mJ
I_{AR}	Avalanche Current ¹	35	A
E_{AR}	Repetitive Avalanche Energy ¹	7.5	mJ
dv/dt	Peak Diode Reverse Recovery ³	13	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^{\circ}C$
	Lead Temperature	300 (for 5s)	
	Weight	1.0 (Typical)	

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.² $V_{DD} = 100V$, starting $T_J = 25^{\circ}C$, $L = 2.5mH$, Peak $I_L = 22A$, $V_{GS} = 20V$ ³ $I_{SD} \leq 35A$, $di/dt \leq 980A/\mu s$, $V_{DD} \leq 100V$, $T_J \leq 150^{\circ}C$

Device Characteristics

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.1	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	34	m Ω	$V_{GS} = 12V, I_{D2} = 22A^1$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} \geq V_{GS}, I_D = 1mA$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-8.9	—	mV/ $^\circ\text{C}$	
G_{fs}	Forward Transconductance	14	—	—	S	$V_{DS} = 15V, I_{D2} = 22A^1$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	$V_{DS} = 80V, V_{GS} = 0V$
		—	—	10		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_G	Total Gate Charge	—	—	48	nC	$I_{D1} = 35A$
Q_{GS}	Gate-to-Source Charge	—	—	25		$V_{DS} = 50V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	9.0		$V_{GS} = 12V$
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	$I_{D1} = 35A^{**}$ $V_{DD} = 50V$ $R_G = 7.5\Omega$ $V_{GS} = 12V$
t_r	Rise Time	—	—	56		
$t_{d(off)}$	Turn-Off Delay Time	—	—	38		
t_f	Fall Time	—	—	27		
$L_s + L_D$	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	1800	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	440	—		
C_{rss}	Reverse Transfer Capacitance	—	3.3	—		
R_G	Gate Resistance	—	1.0	—	Ω	$f = 1.0MHz$, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

¹ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	35	A	
I_{SM}	Pulsed Source Current (Body Diode) ¹	—	—	140	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$, $I_S = 35\text{A}$, $V_{GS} = 0\text{V}$ ²
t_{rr}	Reverse Recovery Time	—	140	210	ns	$T_J = 25^\circ\text{C}$, $I_F = 35\text{A}$, $V_{DD} \leq 25\text{V}$
Q_{rr}	Reverse Recovery Charge	—	820	—	nC	$di/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	$^\circ\text{C}/\text{W}$

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics - Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25^\circ\text{C}$, Post Total Dose Irradiation ^{3, 4}

Symbol	Parameter	Up to 300krads (Si) ⁵		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	V	$V_{GS} = 0\text{V}$, $I_D = 1\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	$V_{DS} \geq V_{GS}$, $I_D = 1\text{mA}$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Leakage Reverse	—	-100		$V_{GS} = -20\text{V}$
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	$V_{DS} = 80\text{V}$, $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) ²	—	36	$\text{m}\Omega$	$V_{GS} = 12\text{V}$, $I_{D2} = 22\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (SMD-0.5e Ceramic Lid) ²	—	34	$\text{m}\Omega$	$V_{GS} = 12\text{V}$, $I_{D2} = 22\text{A}$
V_{SD}	Diode Forward Voltage	—	1.2	V	$V_{GS} = 0\text{V}$, $I_F = 35\text{A}$

¹ Repetitive Rating; Pulse width limited by maximum junction temperature.

² Pulse width $\leq 300\text{ }\mu\text{s}$; Duty Cycle $\leq 2\%$

³ Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 12\text{V}$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁴ Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 80\text{V}$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.

⁵ Part numbers IRHNKC9A7130 (JANSR2N7648U3CE), and IRHNKC9A3130 (JANSF2N7648U3CE)

IRHNKC9A7130 (JANSR2N7648U3CE)

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5e Ceramic Lid)

Device Characteristics

2.4.2 Single Event Effects – Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

LET (MeV·cm ² /mg)	Energy (MeV)	Range (μm)	V _{DS} (V)			
			V _{GS} = 0V	V _{GS} = -1V	V _{GS} = -5V	V _{GS} = -10V
37 ± 5%	417 ± 7.5%	50 ± 7.5%	100	100	100	100
59.8 ± 5%	753 ± 7.5%	60 ± 7.5%	100	100	100	100
89.8 ± 5%	1515 ± 7.5%	82 ± 7.5%	100	100	—	—

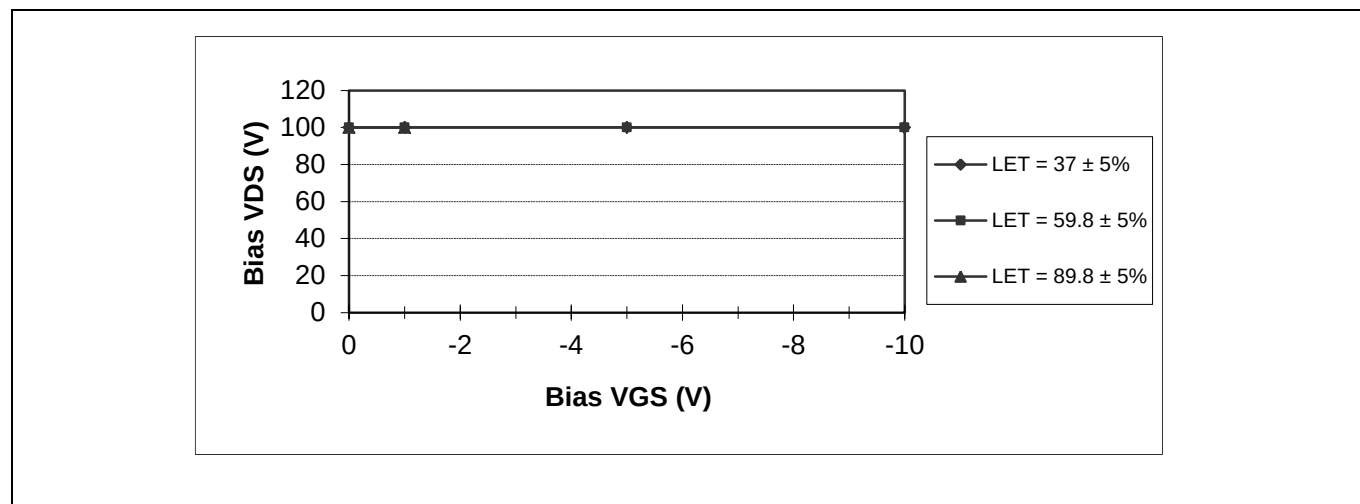


Figure 1 Typical Single Event Effect, Safe Operating Area

IRHNKC9A7130 (JANSR2N7648U3CE)

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5e Ceramic Lid)

Electrical Characteristics Curves (Pre-irradiation)

3 Electrical Characteristics Curves (Pre-irradiation)

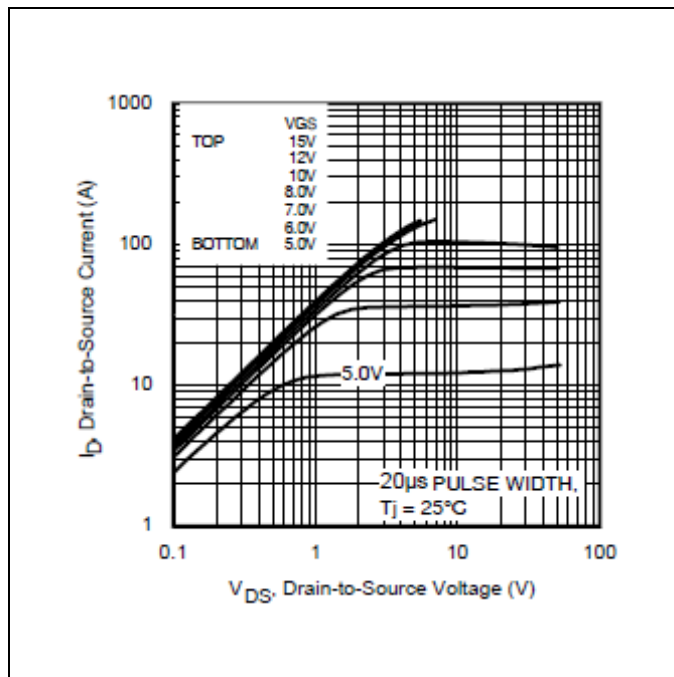


Figure 2 Typical Output Characteristics

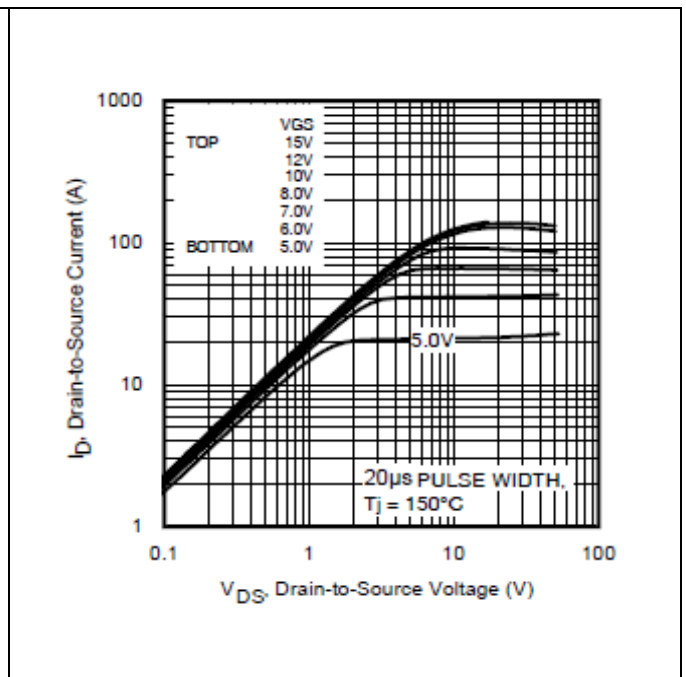


Figure 3 Typical Output Characteristics

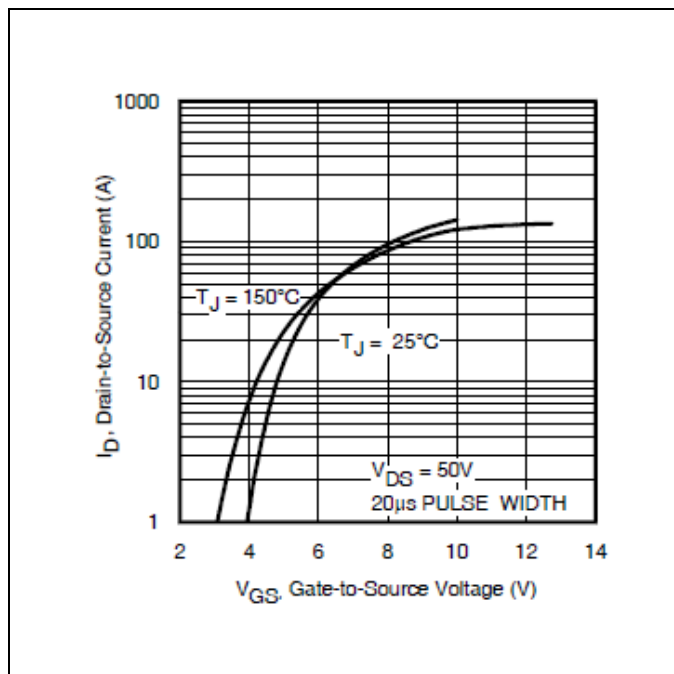


Figure 4 Typical Transfer Characteristics

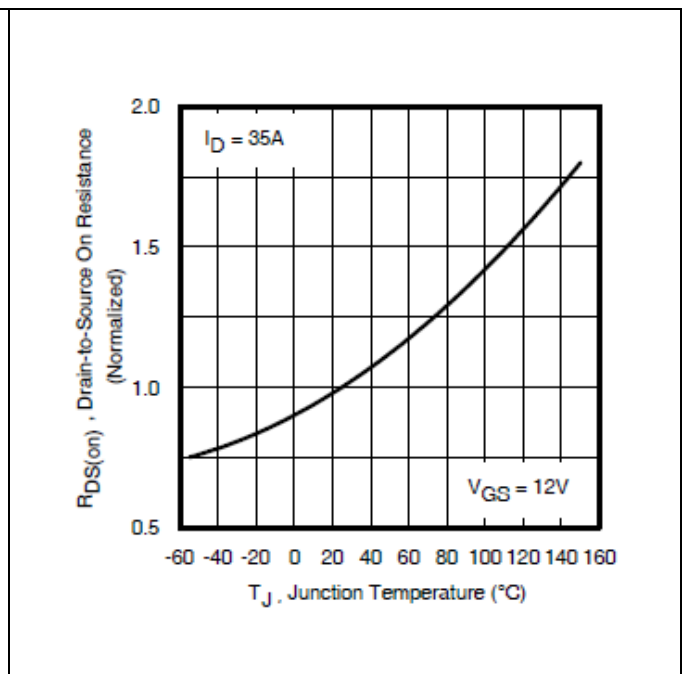


Figure 5 Normalized On-Resistance Vs. Temperature

IRHNKC9A7130 (JANSR2N7648U3CE)

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5e Ceramic Lid)

Electrical Characteristics Curves (Pre-irradiation)

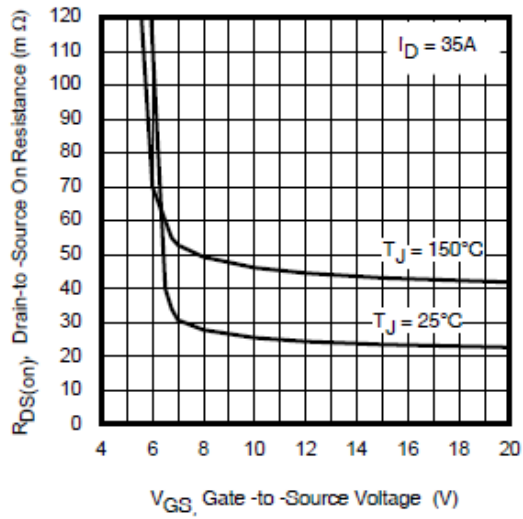


Figure 6 Typical On-Resistance Vs. Gate Voltage

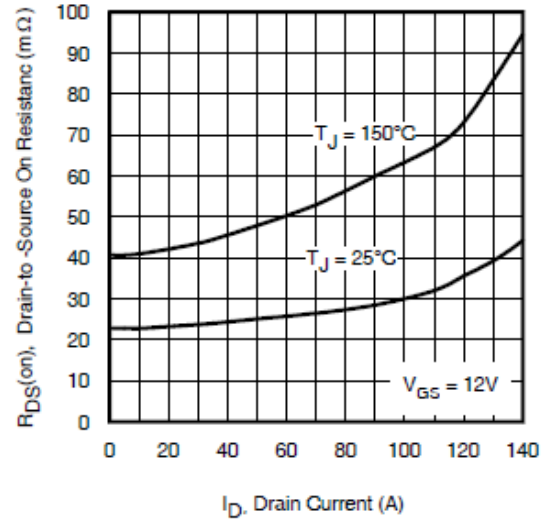


Figure 7 Typical On-Resistance Vs. Drain Current

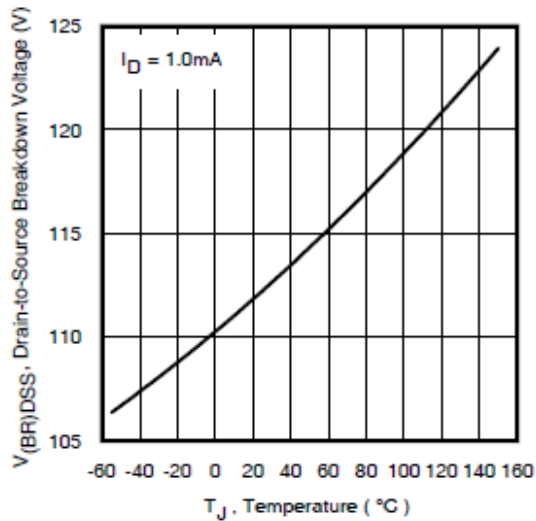


Figure 8 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

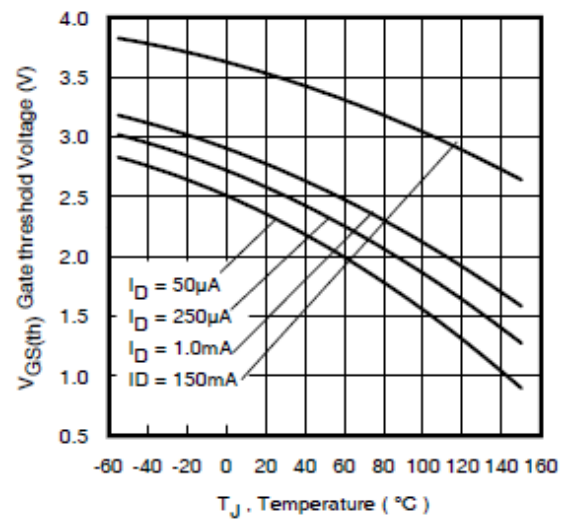


Figure 9 Typical Threshold Voltage Vs. Temperature

IRHNKC9A7130 (JANSR2N7648U3CE)

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5e Ceramic Lid)

Electrical Characteristics Curves (Pre-irradiation)

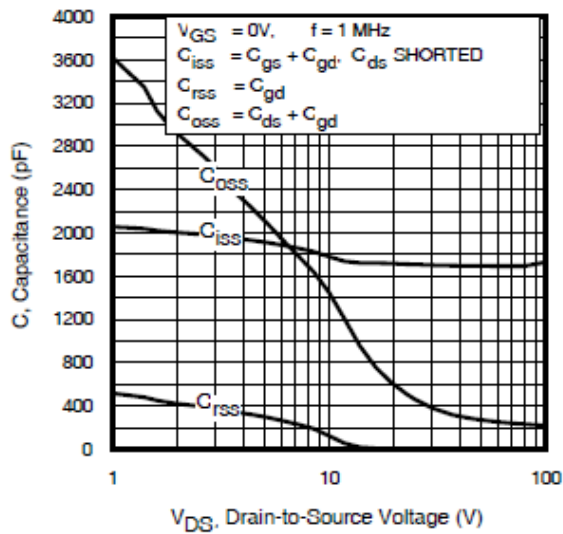


Figure 10 Typical Capacitance Vs. Drain-to-Source Voltage

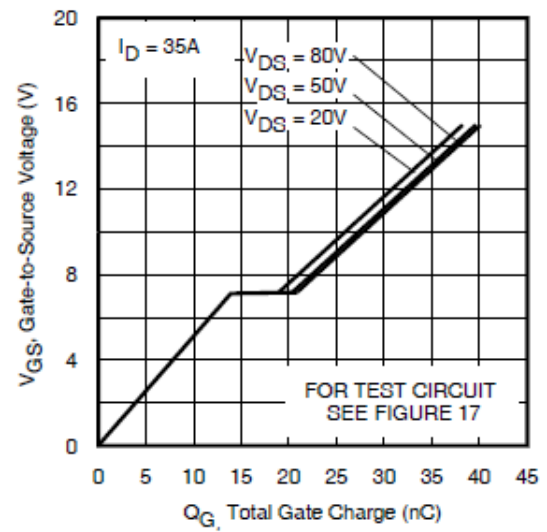


Figure 11 Typical Gate Charge Vs. Gate-to-Source Voltage

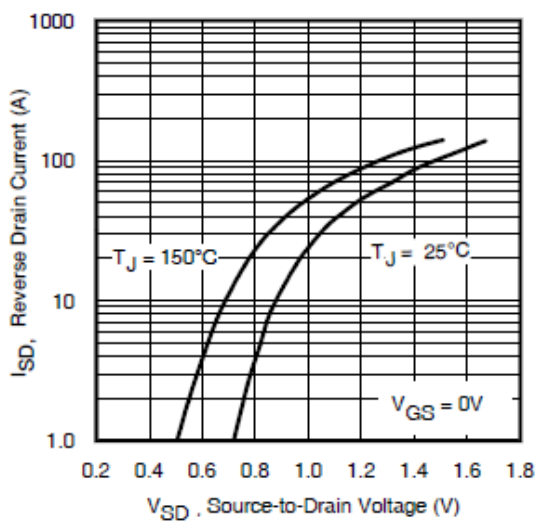


Figure 12 Typical Source-Drain Vs. Diode Forward Voltage

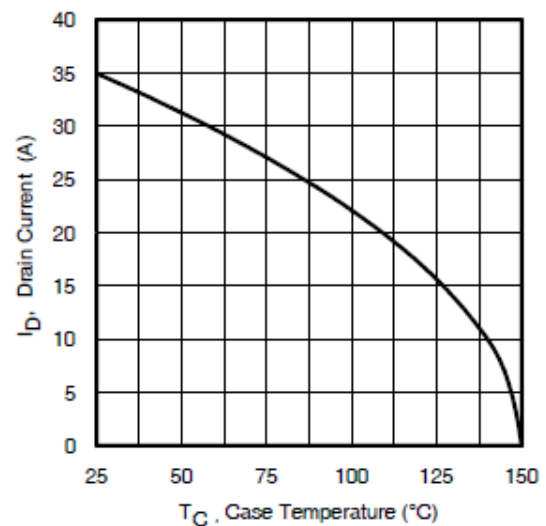


Figure 13 Maximum Drain Current Vs. Case Temperature

IRHNKC9A7130 (JANSR2N7648U3CE)

Radiation Hardened Power MOSFET Surface Mount (SMD-0.5e Ceramic Lid)

Electrical Characteristics Curves (Pre-irradiation)

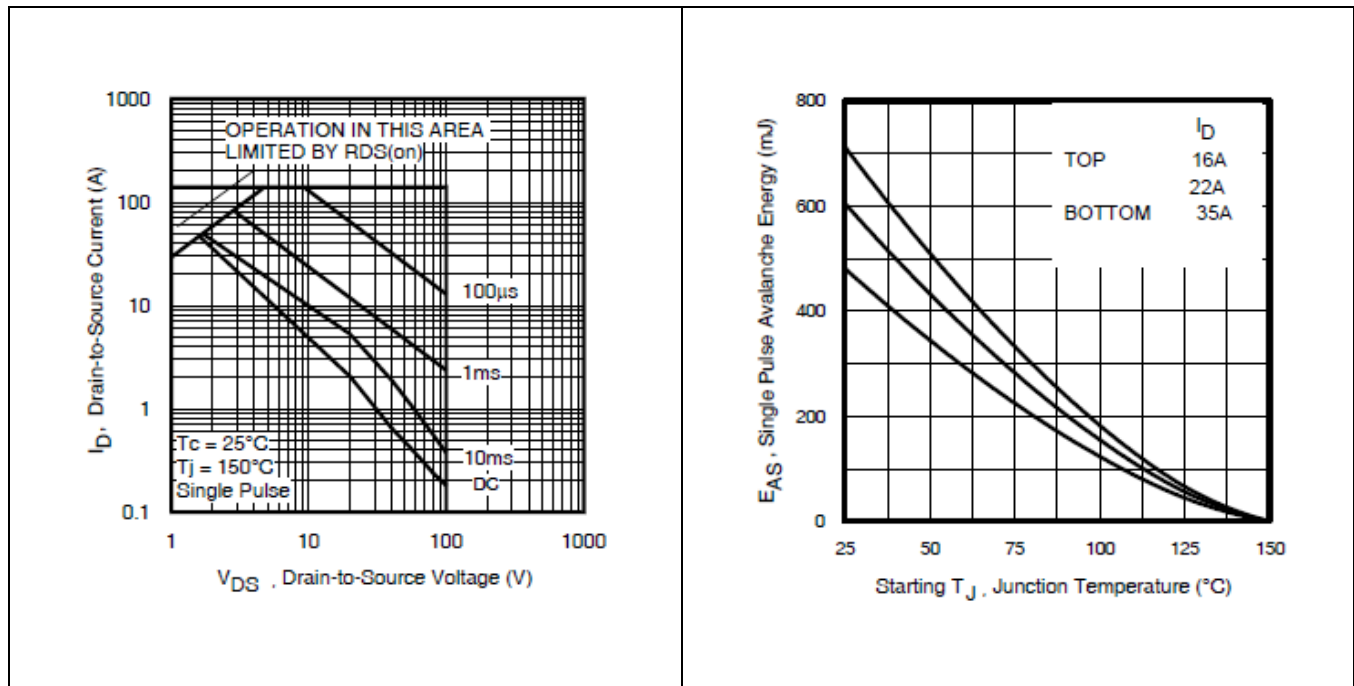


Figure 14 Maximum Safe Operating Area

Figure 15 Maximum Avalanche Energy Vs. Junction Temperature

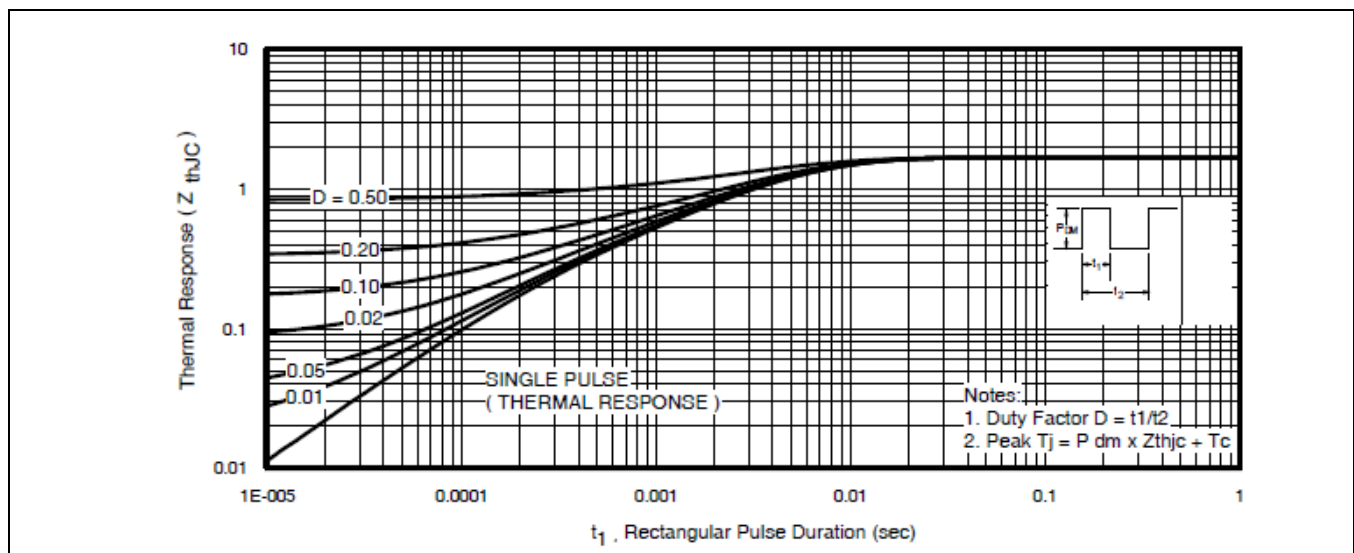


Figure 16 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

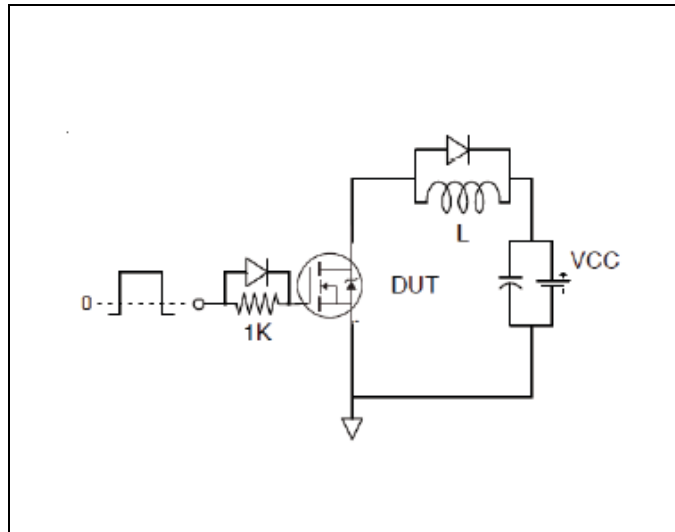


Figure 17 Gate Charge Test Circuit

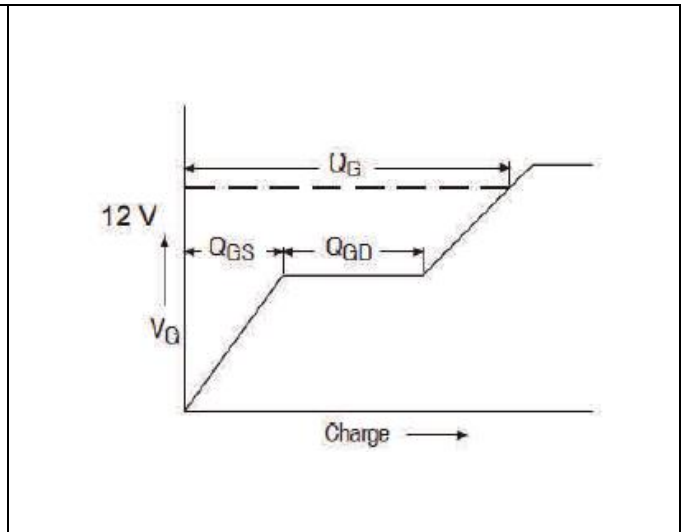


Figure 18 Gate Charge Waveform

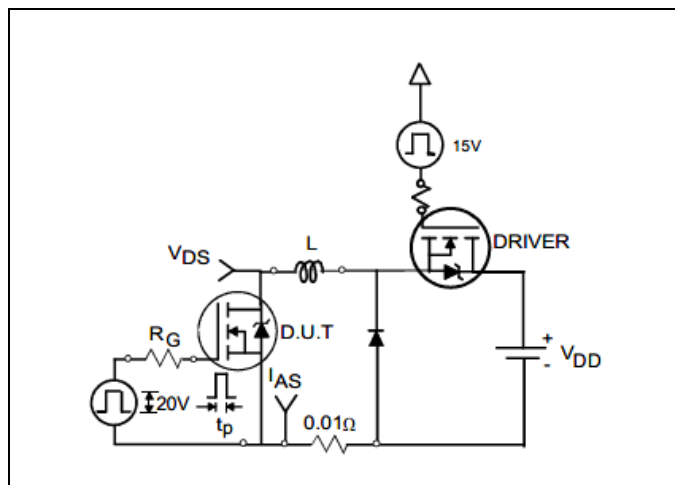


Figure 19 Unclamped Inductive Test Circuit

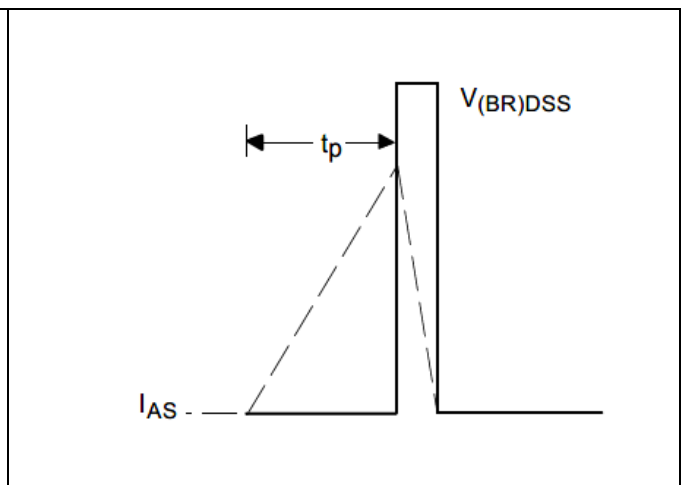


Figure 20 Unclamped Inductive Waveform

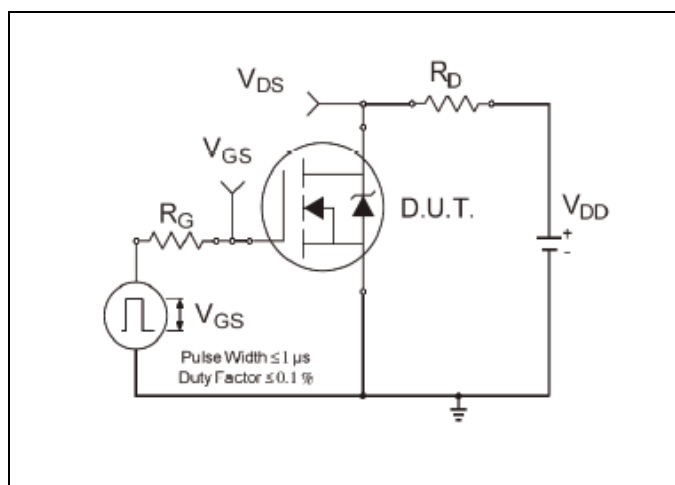


Figure 21 Switching Time Test Circuit

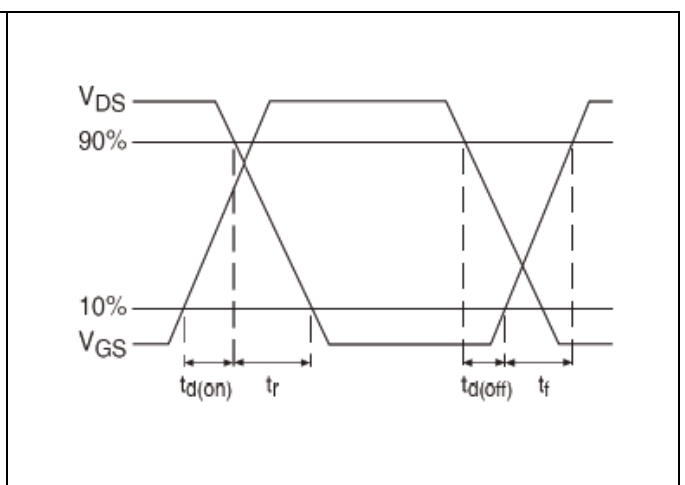
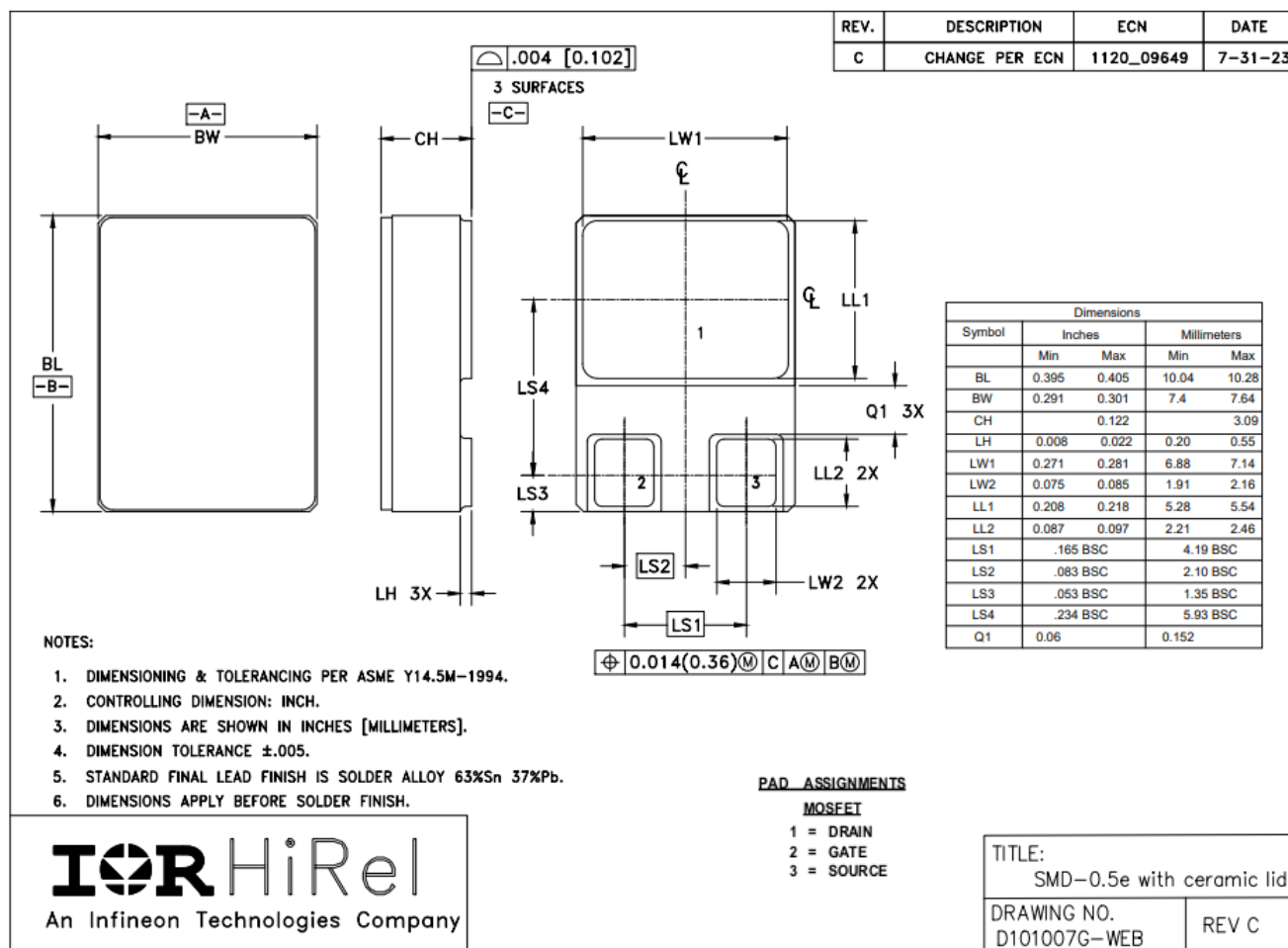


Figure 22 Switching Time Waveforms

Package outline

5 Package outline

Note: For the most updated package outline, please see the website: [SMD-0.5e with Ceramic Lid](#)



Revision history

Revision history

Document version	Date of release	Description of changes
	11/13/2023	Preliminary datasheet with PPD number (PPD-97977)
Rev A	12/05/2023	Final datasheet with PD number

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