

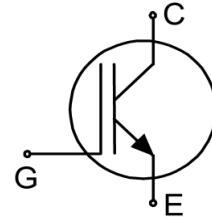
EDT3 IGBT for Automotive Applications

IGBT

Quality Requirement Category: Automotive

Features

- 750V trench + field stop technology
- Low $V_{CE(sat)}$
- Low switching losses
- Short tail current
- Positive temperature coefficient
- Integrated gate resistor
- Easy paralleling
- Solderable/sinterable front side pads¹
- 185°C maximum junction temperature



Applications

- Drives

Description

- Recommended for power modules

Product Validation

- Technology qualified for Automotive Applications. Product validation according to AEC-Q101.

Key Performance Parameters

Chip Type	V_{CE}	I_{Cn}	Die Size	Package
IGC100T75H12RDYA	750V	320A	99.93mm ²	Sawn on foil

¹ Depending on customer specific assembly process

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1 Parameters and Characteristics

Table 1 Mechanical Parameters

Raster size		9.27 x 10.78	mm ²
Area total		99.93	mm ²
Emitter pad size		See chip drawing	
Gate pad size		See chip drawing	
Silicon thickness		77	μm
Wafer size		300	mm
Maximum possible chips per wafer		612	
Passivation frontside		Photoimide	
Pad metal		NiP/Pd	
Backside metal		NiP/Pd	
Die bond ¹		Soft solder or sinter	
Frontside interconnect ¹		Soft solder or sinter	
Reject ink dot size		Inkless	
Storage environment (<6 months)	For original and sealed MBB bags ²	Ambient atmosphere air, temperature 17°C – 25°C	

¹ Depending on customer specific assembly process

² https://www.infineon.com/dgdl/Storage_of_Products_Supplied_by_Infineon_Technologie.pdf?fileId=5546d461641369bf01643b95d8500011

Table 2 Maximum Ratings¹

Parameter	Symbol	Conditions	Value	Unit
Collector-emitter voltage	V_{CES}	$25^{\circ}\text{C} \leq T_{vj} \leq 185^{\circ}\text{C}$	750	V
		$T_{vj} = -40^{\circ}\text{C}^2$	710	
DC collector current, limited by $T_{vj\ max}$	I_C		- ³	A
Pulsed collector current, t_p limited by $T_{vj\ max}$	$I_{C,pulse}$		960	A
Gate-emitter voltage	V_{GE}		±20	V
Virtual junction temperature	T_{vj}		-40 ... +185	°C
Short circuit withstand time ^{1/4/5}	t_{sc}	$V_{GE} \leq 15\text{V}, V_{CC} \leq 470\text{V}, T_{vj} \leq 175^{\circ}\text{C}$	3	µs
		$V_{GE} \leq 15\text{V}, V_{CC} \leq 470\text{V}, T_{vj} \leq 185^{\circ}\text{C}$	2.5	
Reverse bias safe operating area	$RBSOA$	$I_{C,max} = 640\text{A}, V_{CE,max} = V_{CES}, -40^{\circ}\text{C} \leq T_{vj} \leq 185^{\circ}\text{C}$		

Table 3 Static Characteristics (Tested on Wafer), $T_{vj}=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter saturation voltage	V_{CESat}	$V_{GE} = 15\text{V}, I_C = 64\text{A}$	-	0.94	1.03	V
Gate-emitter threshold voltage	$V_{GE(th)}$	$I_C = 3.2\text{mA}, V_{GE} = V_{CE}$	5.2	5.9	6.5	V
Zero gate voltage collector current	I_{CES}	$V_{CE} = 750\text{V}, V_{GE} = 0\text{V}$	-	-	100	μA
Gate-emitter leakage current	I_{GES}	$V_{CE} = 0\text{V}, V_{GE} = 20\text{V}$	-	-	600	nA
Integrated gate resistor	r_G		-	2	-	Ω

¹ Not subject to production test - verified by design/characterization.

² V_{CES} increases linearly between -40°C and 25°C .

³ Depending on thermal properties of assembly.

⁴ Allowed number of short circuits: <1000; time between short circuits: >1s.

⁵ Depending on electrical design of assembly.

Table 4 Electrical Characteristics¹

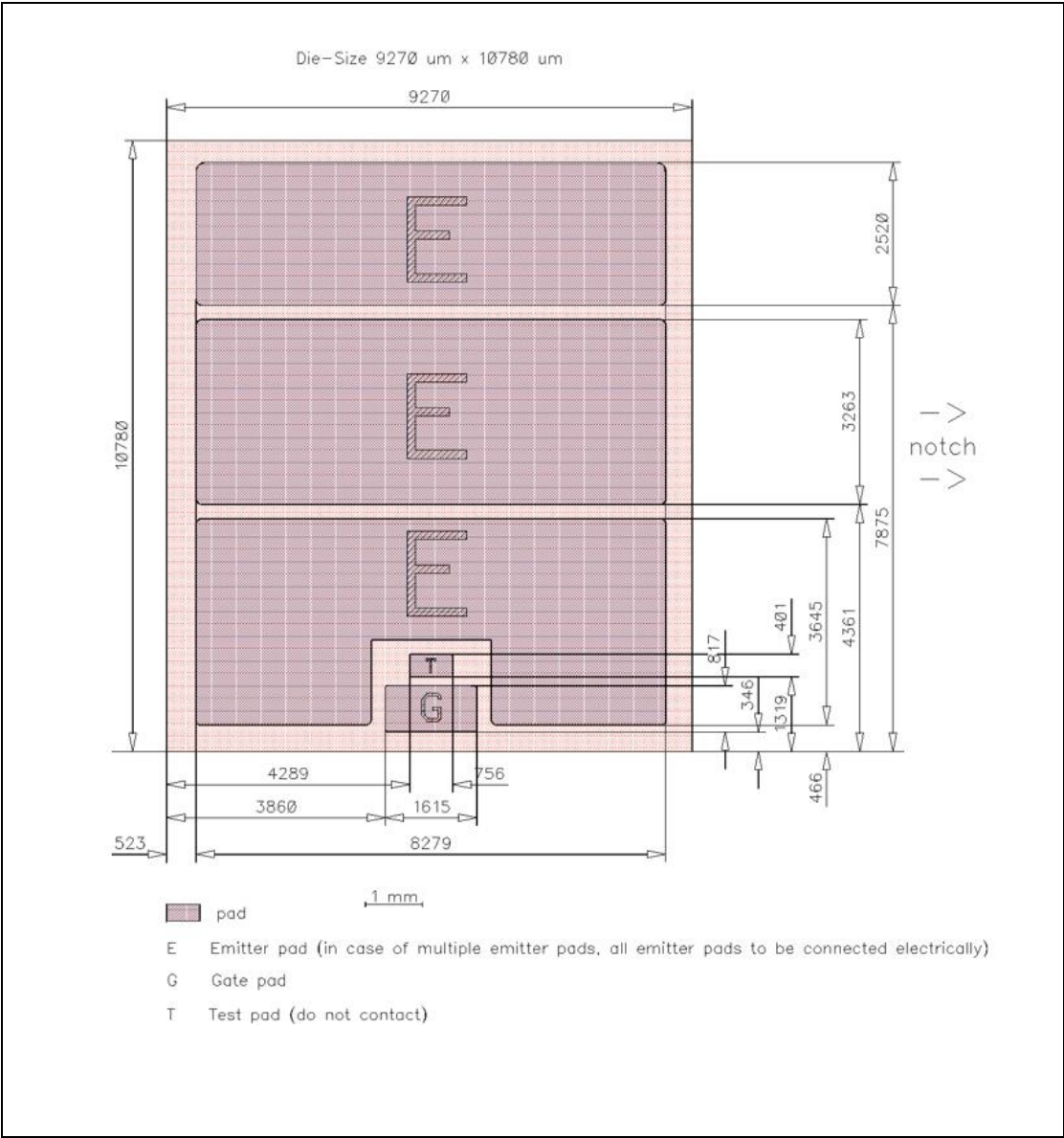
Parameter	Symbol	Conditions		Value			Unit
				min.	typ.	max.	
Collector-emitter saturation voltage	V_{CEsat}	$V_{GE} = 15V,$ $I_C = 200A$	$T_{vj} = 25^{\circ}C$	-	1.15	1.28	V
			$T_{vj} = 185^{\circ}C$	-	1.2	-	
		$V_{GE} = 15V,$ $I_C = 320A$	$T_{vj} = 25^{\circ}C$	-	1.29	1.44	
			$T_{vj} = 185^{\circ}C$	-	1.43	-	
Input capacitance	C_{ies}	$V_{CE} = 25V,$ $V_{GE} = 0V, f = 100kHz$ $T_{vj} = 25^{\circ}C$			18600		pF
Output capacitance	C_{oes}				670		
Reverse transfer capacitance	C_{res}				120		
Gate charge	Q_G	$V_{CE} = 470V, I_C = 320A$ $V_{GE} = -8V...+15V$		-	820	-	nC

2 Further Electrical Characteristics

Note: Switching characteristics and thermal properties are dependent on module design and mounting technology and can therefore not be specified for a bare die.

¹ Not subject to production test - verified by design/characterization.

3 Chip Drawing



4 Bare Die Product Specifics

Note: Test coverage at wafer level for IGBTs cannot cover the full range of customer application conditions. Therefore it is the responsibility of the customer to test all performance characteristics, which are relevant for their specific application, at the package level, including RBSOA and SCSOA.

Description

- AQL 0.1 for visual inspection according to failure catalogue

Revision History

Document version	Date of release	Description of changes
V1.00	2024-May-03	Initial datasheet

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