

# **512Mb/1Gb SEMPER™ Flash**

**Octal interface, 1.8V/3.0V**

## **Features**

- Infineon 45-nm MIRRORBIT™ technology that stores two data bits in each memory array cell
- Sector architecture options
  - Uniform: Address space consists of all 256KB sectors
  - Hybrid:
    - Configuration 1 - Address space consists of thirty-two 4 KB sectors grouped either on the top or the bottom while the remaining sectors are all 256KB
    - Configuration 2 - Address space consists of thirty-two 4 KB sectors equally split between top and bottom while the remaining sectors are all 256KB
- Page programming buffer of 256 or 512 bytes
- OTP secure silicon array of 1024 bytes (32 × 32 bytes)
- Octal interface (8S-8S-8S, 8D-8D-8D)
  - JEDEC eXpanded serial peripheral interface (SPI) (JESD251) compliant
  - SDR option runs up to 200-MBps (200 MHz clock speed)
  - DDR option runs up to 400-MBps (200 MHz clock speed)
  - Supports data strobe (DS) to simplify the read data capture in high-speed systems
- Functional safety features
  - Functional safety ISO26262 ASIL B compliant and ASIL D ready
  - Infineon Endurance Flex architecture provides high-endurance and long retention partitions
  - Interface CRC detects errors on communication interface between host controller and SEMPER™ Flash device
  - Data integrity CRC detects errors in memory array
  - SafeBoot reports device initialization failures, detects configuration corruption and provides recovery options
  - Built-in error correcting code (ECC) corrects single-bit error and detects double-bit error (SECEDED) on memory array data
  - Sector erase status indicator for power loss during erase
- Protection features
  - Legacy block protection (LBP) for memory array and device configuration
  - Advanced sector protection (ASP) for individual memory array sector based protection
- AutoBoot enables immediate access to the memory array following power-on
- Hardware reset through CS# signaling method (JEDEC) OR individual RESET# pin
- Serial flash discoverable parameters (SFDP) describing device functions and features
- Device identification, manufacturer identification and unique identification
- Data integrity
  - 512 Mb devices
    - Min. 1,280,000 program-erase cycles for the main array
  - 1 Gb devices
    - Min. 2,560,000 program-erase cycles for the main array
  - All devices
    - Min. 300,000 program-erase cycles for the 4 KB sectors
    - Minimum 25 years data retention

# 512Mb/1Gb SEMPER™ Flash

## Octal interface, 1.8V/3.0V



### Performance summary

- Supply voltage
  - 1.7 V to 2.0 V (HS-T)
  - 2.7 V to 3.6 V (HL-T)
- Grade / temperature range
  - Industrial (–40°C to +85°C)
  - Industrial plus (–40°C to +105°C)
  - Automotive AEC-Q100 grade 3 (–40°C to +85°C)
  - Automotive AEC-Q100 grade 2 (–40°C to +105°C)
  - Automotive AEC-Q100 grade 1 (–40°C to +125°C)
- Packages
  - 512 Mb: 24-ball BGA 6 × 8 mm
  - 1Gb: 24-ball BGA 8 × 8 mm

## Performance summary

**Table 1** Maximum read rates

| Transaction           | Initial access latency (Cycles) | Clock rate (MHz) | MBps  |
|-----------------------|---------------------------------|------------------|-------|
| SPI Read              | 0                               | 50               | 6.25  |
| SPI Read Fast         | 10                              | 166              | 20.75 |
| Octal Read SDR (HS-T) | 16                              | 200              | 200   |
| Octal Read SDR (HL-T) | 14                              | 166              | 166   |
| Octal Read DDR (HS-T) | 23                              | 200              | 400   |
| Octal Read DDR (HL-T) | 20                              | 166              | 332   |

**Table 2** Typical program and erase rates

| Operation                                           | KBps      |
|-----------------------------------------------------|-----------|
| 256B Page programming (4 KB Sector / 256 KB Sector) | 595 / 533 |
| 512B Page programming (4 KB Sector / 256 KB Sector) | 753 / 898 |
| 256KB Sector Erase                                  | 331       |
| 4KB Sector Erase                                    | 95        |

**Table 3** Typical current consumption

| Operation        | HL-T current (mA) | HS-T current (mA) |
|------------------|-------------------|-------------------|
| SDR Read 50 MHz  | 10                | 10                |
| SDR Read (Octal) | 75 (166 MHz)      | 156 (200 MHz)     |
| DDR Read (Octal) | 75 (166 MHz)      | 156 (200 MHz)     |
| Program          | 50                | 50                |
| Erase            | 50                | 50                |
| Standby          | 0.014             | 0.011             |
| Deep Power Down  | 0.0022            | 0.0013            |

## Data integrity

**Table 4** Program / erase (PE) endurance - high endurance (256KB sectors)

| Sectors in partition            | Minimum PE cycles        | Minimum retention time | Unit  |
|---------------------------------|--------------------------|------------------------|-------|
|                                 | 512-Mb and 1-Gb products |                        |       |
| 512 (Default for 1Gb devices)   | 2,560,000                | 2                      | Years |
| 508                             | 2,540,000                |                        |       |
| 504                             | 2,520,000                |                        |       |
| ...                             | ...                      |                        |       |
| 256 (Default for 512Mb devices) | 1,280,000                |                        |       |
| 252                             | 1,260,000                |                        |       |
| ...                             | ...                      |                        |       |
| 28                              | 140,000                  |                        |       |
| 24                              | 120,000                  |                        |       |
| 20                              | 100,000                  |                        |       |

**Note** Minimum cycles is for entire High Endurance Partition.

**Table 5** Program / erase endurance - long retention partition (256 KB sectors)

| Minimum PE cycles | Minimum retention time | Unit  |
|-------------------|------------------------|-------|
| 500               | 25                     | Years |

**Note** Minimum cycles is for each sector.

**Table 6** Program / erase endurance 4 KB sector and non-volatile register array

| Flash memory type                                                                                                                                                 | Minimum cycles | Unit      | Minimum retention time | Unit  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-----------|------------------------|-------|
| Program/Erase cycles per 4KB sector                                                                                                                               | 500            | PE cycles | 25                     | Years |
|                                                                                                                                                                   | 300,000        |           | 2                      |       |
| Program/Erase cycles per Persistent Protection Bits (PPB) array or non-volatile register array                                                                    | 500            |           | 25                     |       |
| <b>Note</b> It is required to restrict the power loss events to 300 times per sector during program or erase operation to achieve the mentioned endurance cycles. |                |           |                        |       |
| <b>Note</b> Each write transaction to a non-volatile register causes a PE cycle on the entire non-volatile register array.                                        |                |           |                        |       |

## Table of contents

|                                                                 |           |
|-----------------------------------------------------------------|-----------|
| <b>Features .....</b>                                           | <b>1</b>  |
| <b>Performance summary .....</b>                                | <b>2</b>  |
| <b>Data integrity .....</b>                                     | <b>3</b>  |
| <b>Table of contents .....</b>                                  | <b>4</b>  |
| <b>1 Pinout and signal description.....</b>                     | <b>6</b>  |
| <b>2 Interface overview .....</b>                               | <b>8</b>  |
| 2.1 General description .....                                   | 8         |
| 2.2 Signal protocols .....                                      | 10        |
| 2.3 Transaction protocol .....                                  | 11        |
| 2.4 Register naming convention .....                            | 21        |
| 2.5 Transaction naming convention .....                         | 21        |
| <b>3 Address space maps .....</b>                               | <b>22</b> |
| 3.1 SEMPER™ Flash memory array .....                            | 22        |
| 3.2 ID address space .....                                      | 26        |
| 3.3 JEDEC JESD216 SFDP space.....                               | 26        |
| 3.4 SSR address space .....                                     | 26        |
| 3.5 Registers .....                                             | 27        |
| <b>4 Features.....</b>                                          | <b>30</b> |
| 4.1 Error detection and correction.....                         | 30        |
| 4.2 Endurance Flex architecture (wear leveling) .....           | 34        |
| 4.3 Interface CRC.....                                          | 38        |
| 4.4 Data integrity CRC.....                                     | 42        |
| 4.5 Data protection schemes .....                               | 43        |
| 4.6 SafeBoot .....                                              | 54        |
| 4.7 AutoBoot .....                                              | 58        |
| 4.8 Read transactions .....                                     | 59        |
| 4.9 Write transactions.....                                     | 63        |
| 4.10 Program.....                                               | 66        |
| 4.11 Erase .....                                                | 68        |
| 4.12 Suspend and resume embedded operation.....                 | 70        |
| 4.13 Reset .....                                                | 73        |
| 4.14 Power modes .....                                          | 78        |
| 4.15 Power up and power down .....                              | 80        |
| <b>5 Registers.....</b>                                         | <b>82</b> |
| 5.1 Register naming convention .....                            | 83        |
| 5.2 Status Register 1 (STR1x).....                              | 83        |
| 5.3 Status Register 2 (STR2x).....                              | 87        |
| 5.4 Configuration Register 1 (CFR1x) .....                      | 89        |
| 5.5 Configuration register 2 (CFR2x) .....                      | 92        |
| 5.6 Configuration Register 3 (CFR3x) .....                      | 94        |
| 5.7 Configuration Register 4 (CFR4x) .....                      | 97        |
| 5.8 Configuration Register 5 (CFR5x) .....                      | 100       |
| 5.9 Interface CRC Enable Register (ICEV) .....                  | 101       |
| 5.10 Interface CRC Check-value Register (ICRV) .....            | 101       |
| 5.11 Memory Array Data Integrity Check CRC Register (DCRV)..... | 102       |
| 5.12 ECC Status Register (ESCV).....                            | 102       |
| 5.13 ECC Address Trap Register (EATV).....                      | 104       |
| 5.14 ECC Error Detection Count Register (ECTV).....             | 105       |
| 5.15 Advanced Sector Protection register (ASPO) .....           | 106       |
| 5.16 ASP Password Register (PWDO) .....                         | 109       |
| 5.17 ASP PPB Lock Register (PPLV) .....                         | 109       |

|                                                                  |            |
|------------------------------------------------------------------|------------|
| 5.18 ASP PPB Access Register (PPAV) .....                        | 110        |
| 5.19 ASP Dynamic Block Access Register (DYAV).....               | 110        |
| 5.20 AutoBoot Register (ATBN) .....                              | 111        |
| 5.21 Sector Erase Count Register (SECV) .....                    | 112        |
| 5.22 INT# Pin Configuration Register (INCV) - octal only .....   | 113        |
| 5.23 INT# Pin Status Register (INSV) - Octal only .....          | 115        |
| 5.24 Endurance Flex Architecture Selection Register (EFXx) ..... | 116        |
| <b>6 Transaction table.....</b>                                  | <b>120</b> |
| 6.1 SPI (1S-1S-1S) transaction table .....                       | 120        |
| 6.2 Octal (8S-8S-8S, 8D-8D-8D) transaction table .....           | 124        |
| <b>7 Electrical characteristics .....</b>                        | <b>129</b> |
| 7.1 Absolute maximum ratings[35] .....                           | 129        |
| 7.2 Operating range .....                                        | 129        |
| 7.3 Thermal resistance .....                                     | 130        |
| 7.4 Capacitance characteristics .....                            | 130        |
| 7.5 Latchup characteristics .....                                | 130        |
| 7.6 DC characteristics .....                                     | 131        |
| 7.7 AC test conditions .....                                     | 136        |
| <b>8 Timing characteristics.....</b>                             | <b>137</b> |
| 8.1 Timing waveforms .....                                       | 144        |
| <b>9 Device identification .....</b>                             | <b>147</b> |
| 9.1 JEDEC SFDP Rev D.....                                        | 147        |
| 9.2 Manufacturer and Device ID .....                             | 173        |
| 9.3 Unique Device ID .....                                       | 173        |
| <b>10 Package diagrams .....</b>                                 | <b>174</b> |
| <b>11 Ordering information .....</b>                             | <b>176</b> |
| 11.1 Valid combinations — standard grade.....                    | 177        |
| 11.2 Valid combinations — automotive grade / AEC-Q100 .....      | 178        |
| <b>Revision history .....</b>                                    | <b>179</b> |

# 1 Pinout and signal description

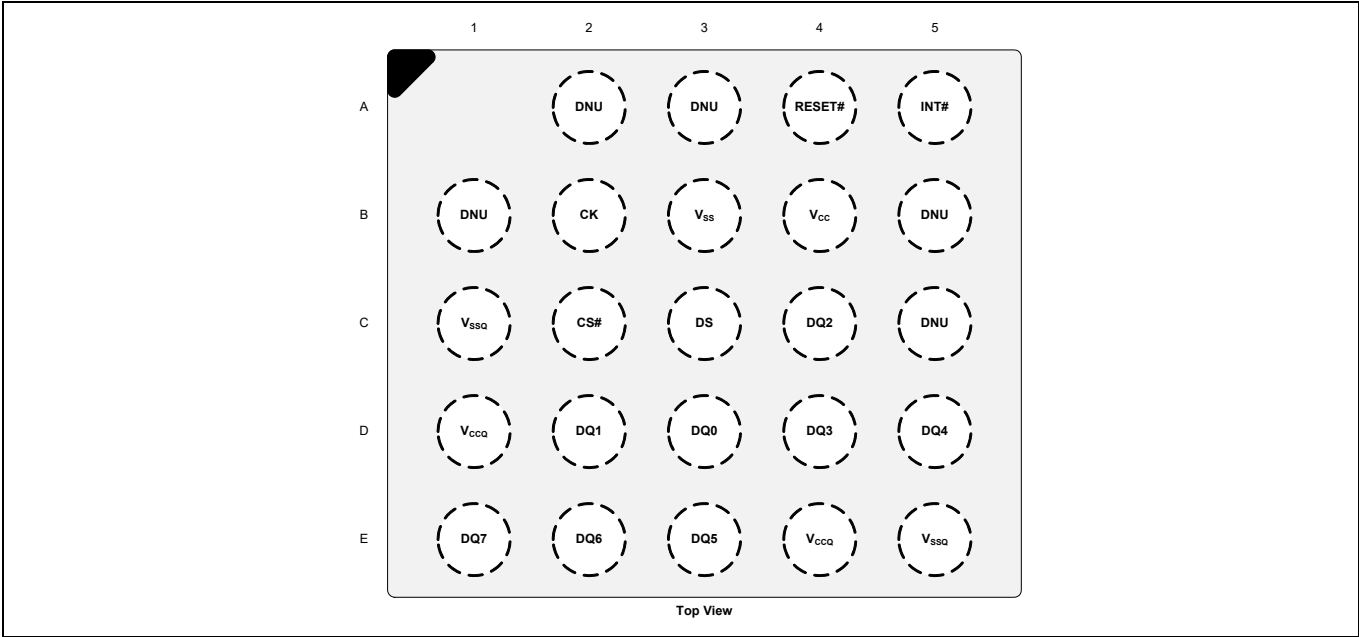


Figure 1 24-ball BGA pinout configuration<sup>[1]</sup>

## Note

- Flash memory devices in BGA packages can be damaged if exposed to ultrasonic cleaning methods. The package data integrity or both may be compromised if the package body is exposed to temperatures above

**Table 7**      **Signal description**

| Symbol           | Type                 | Mandatory / optional | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------------|----------------------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CS#              | Input                | Mandatory            | <b>Chip Select (CS#).</b> All bus transactions are initiated with a HIGH to LOW transition on CS# and terminated with a LOW to HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the active mode. When CS# is driven HIGH, the device enters standby mode, unless an internal embedded operation is in progress. All other input pins are ignored and the output pins are put in high impedance state. On parts where the pin configuration offers a dedicated RESET# pin, it remains active when CS# is HIGH. |
| CK               |                      |                      | <b>Clock (CK).</b> Clock provides the timing of the serial interface. Transactions are latched on the rising edge of the clock. In SDR protocol, command, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock. In DDR protocol, command, address and data inputs are latched on both edges of the clock, and data is output on both edges of the clock.                                                                                                         |
| DS               | Output               |                      | <b>Read Data Strobe (DS).</b> DS is used for data read operations only and indicates output data valid for SDR/DDR modes. During a read transaction while CS# is LOW, DS toggles to synchronize data output until CS# goes High.                                                                                                                                                                                                                                                                                                       |
| DQ[7:0]          | Input/Output         |                      | <b>Serial Data (DQ[7:0]).</b> Bidirectional signals that transfer command, address and data information.<br><b>Legacy (x1) SPI Interface.</b> DQ[0] is an input (SI) and DQ[1] is an output (SO).<br><b>Octal (x8) Interface.</b> DQ[7:0] are input and output.                                                                                                                                                                                                                                                                        |
| RESET#           | Input (weak pull-up) | Optional             | <b>Hardware Reset (RESET#).</b> When LOW, the device will self initialize and return to the array read state. DS and DQ[7:0] are placed into the high impedance state when RESET# is LOW. RESET# includes a weak pull-up, meaning, if RESET# is left unconnected it will be pulled up to the HIGH state on its own.                                                                                                                                                                                                                    |
| INT#             | Output (Open Drain)  |                      | <b>System Interrupt (INT#).</b> When LOW, the device is indicating that an internal event has occurred. This signal is intended to be used as a system level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output. The recommended pull-up resistor for the INT# outputs is 5 kΩ to 10 kΩ.                                                                                                                                                                                            |
| V <sub>CC</sub>  | Power supply         | Mandatory            | Core Power Supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| V <sub>CCQ</sub> |                      |                      | Input / Output Power Supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| V <sub>SS</sub>  | Ground supply        |                      | Core Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| V <sub>SSQ</sub> |                      |                      | Input / Output Ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| DNU              | –                    | –                    | Do Not Use                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

## 2 Interface overview

### 2.1 General description

The SEMPER™ flash octal family of products are high-speed CMOS, MIRRORBIT™ NOR flash devices that are compliant with the JEDEC JESD251 eXpanded SPI (xSPI) specification. SEMPER™ is designed for Functional Safety with development according to ISO 26262 standard to achieve ASIL-B compliance and ASIL-D readiness.

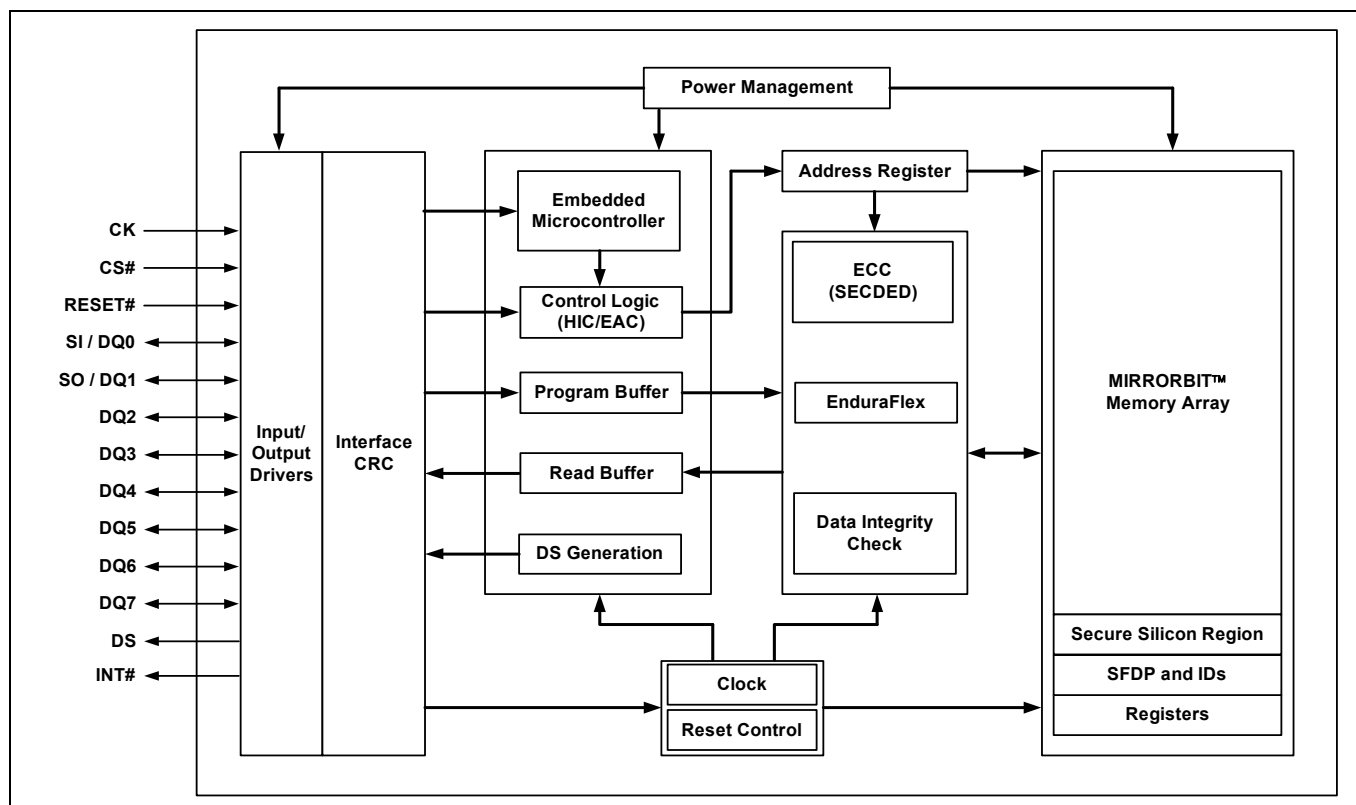
SEMPER™ Flash with Octal Interface devices support both the octal peripheral interface (OPI) as well as Legacy x1 Serial Peripheral Interface (SPI). Both interfaces serially transfer transactions reducing the number of interface connection signals. SPI supports SDR whereas OPI supports both SDR and DDR.

Read operations from the device are burst oriented. Read transactions can be configured to use either a wrapped or linear burst. Wrapped bursts read from a single page whereas linear bursts can read the whole memory array.

The erased state of each memory bit is a logic 1. Programming changes a logic 1 (HIGH) to a logic 0 (LOW). Only an erase operation can change a memory bit from a 0 to a 1. An erase operation must be performed on a complete sector (4KBs or 256KBs).

SEMPER™ Flash provides a flexible sector architecture. The address space can be configured as either a uniform 256 KB sector array, or a hybrid configuration 1 where thirty-two 4 KB sectors are either grouped at the top or at the bottom while the remaining sectors are all 256 KB, or a hybrid configuration 2 where the thirty-two 4 KB sectors are equally split between the top and the bottom while the remaining sectors are all 256 KB.

The Page Programming Buffer used during a single programming operation is configurable to either 256 bytes or 512 bytes. The 512 byte option provides the highest programming throughput.



**Figure 2** Logic block diagram

The SEMPER™ Flash with Octal Interface family consists of multiple densities with, 1.8 V and 3.0 V core and I/O voltage options.

The device control logic is subdivided into two parallel operating sections: the Host Interface Controller (HIC) and the Embedded Algorithm Controller (EAC). The HIC monitors signal levels on the device inputs and drives outputs as needed to complete read, program, and write data transfers with the host system. The HIC delivers data from the currently entered address map on read transfers; places write transfer address and data information into the EAC command memory, and notifies the EAC of power transition, and write transfers. The EAC interrogates the command memory, after a program or write transfer, for legal command sequences and performs the related embedded algorithms.

Changing the non-volatile data in the memory array requires a sequence of operations that are part of embedded algorithms (EA). The algorithms are managed entirely by the internal EAC. The main algorithms perform programming and erase of the main flash array data. The host system writes command codes to the flash device. The EAC receives the command, performs all the necessary steps to complete the transaction, and provides status information during the progress of an EA.

In addition to the mandatory SPI signals CK, CS#, SI/DQ0, SO/DQ1, and DQ[7:2], the SEMPER™ Flash with Octal Interface device also includes RESET#, DS and INT# signals. The RESET# transition from LOW to HIGH returns the device to the default state that occurs after an internal power-on reset (POR). The Data Strobe (DS) is synchronized with the output data during read transactions enabling host system to capture data at high clock frequency operation. The INT# is an open-drain output that can provide an interrupt to the device master to indicate when the device transitions from busy to ready at the end of a program or erase operation or to indicate the detection of an error (ECC) during read.

Infineon Endurance Flex architecture provides system designers the ability to customize the NOR flash endurance and retention for their specific application. The host defines partitions for high endurance or long retention, providing up to 1+ million cycles or 25 years of data retention.

The SEMPER™ Flash with Octal interface device supports error detection and correction by generating an embedded hamming error correction code during memory array programming. This ECC code is then used for single-bit and double-bit error detection and single-bit correction during read.

The SEMPER™ Flash with Octal Interface device has built-in diagnostic features providing the host system with the device status.

- Program and Erase Operation: Reporting of program or erase success, failure and suspend status
- error detection and correction: 1-bit and/or 2-bit error status with address trapping and error count
- Data Integrity Check: Error detection over memory array contents
- Interface CRC: Error detection over device interface
- SafeBoot: Reporting of proper flash device initialization and configuration corruption recovery
- Sector Erase Status: Reporting of erase success or failure status per sector
- Sector Erase Counter: Counts the number of erase cycles per sector

## 2.2 Signal protocols

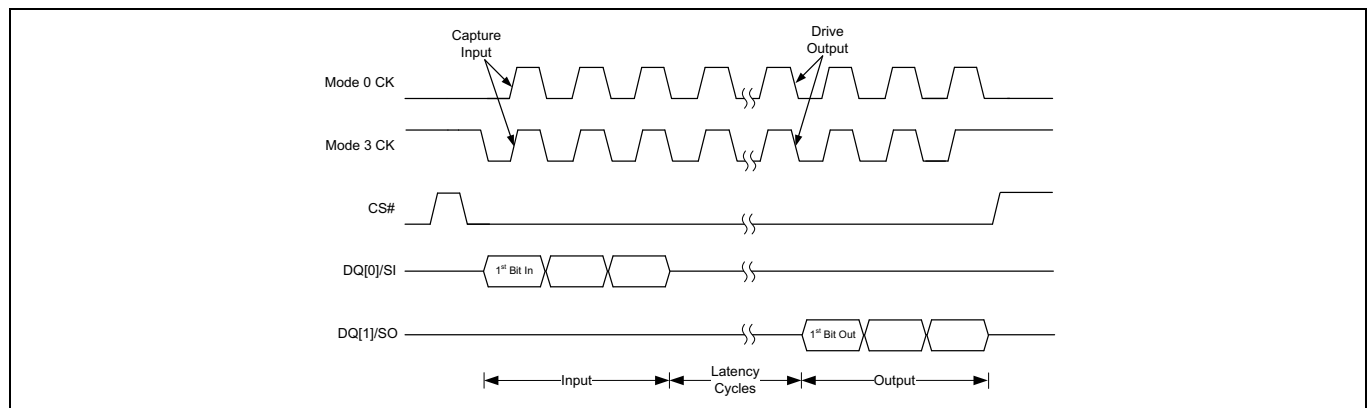
### 2.2.1 SEMPER™ flash octal and SPI clock modes

The SEMPER™ flash with octal interface device can be driven by an embedded microcontroller (bus master) in either of the following two clocking modes:

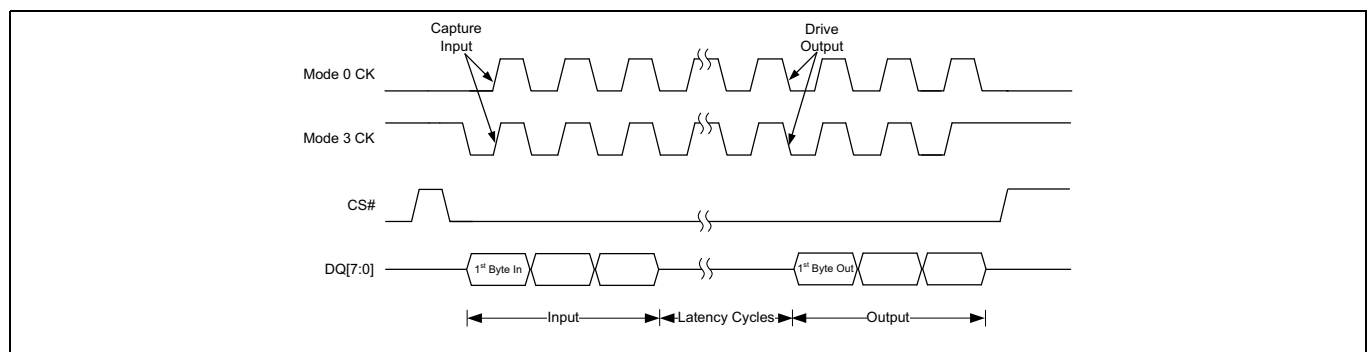
- **Mode 0** with Clock Polarity LOW at the fall of CS# and staying LOW until it goes HIGH at capture input.
- **Mode 3** with Clock Polarity HIGH at the fall of CS# then going LOW to HIGH at capture input.

For these two modes, data is latched into the device on the rising edge of the CK signal in SDR protocol and both edges of the CK signal in DDR protocol. The output data in SDR protocol is available on the falling edge of the CK clock signal and the output data in DDR protocol is available on the rising edge of the CK clock signal.

The difference between the two modes is the clock polarity when the bus master is in Standby mode and not transferring any data.

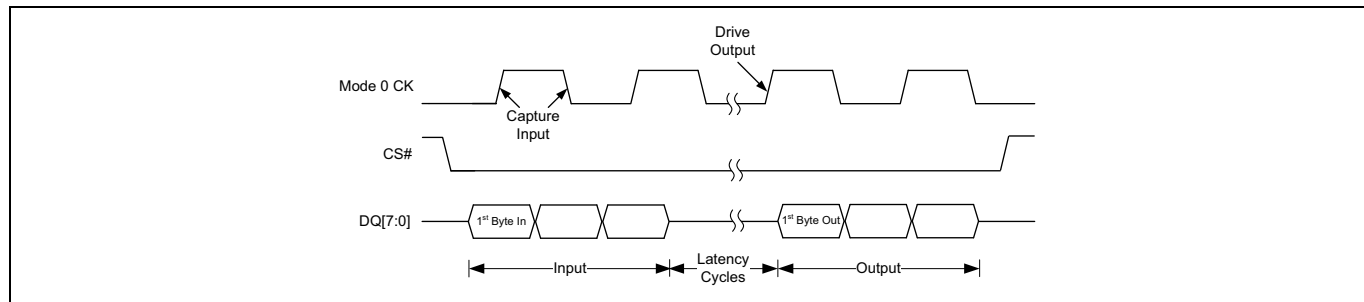


**Figure 3 SPI SDR mode support**



**Figure 4 Octal SDR mode support**

For SEMPER™ flash octal DDR mode operation, only clock Mode 0 is supported.



**Figure 5** Octal DDR mode support

## 2.3 Transaction protocol

### Transaction

- During the time that CS# is active (LOW), the clock signal (CK) is toggled while command information is first transferred on the data (DQ) signals followed by address and data from the host to the flash device. The clock continues to toggle during the transfer of read data from the flash device to the host or write data from the host to the flash device. When the host has transferred the desired amount of data, the host drives the CS# inactive (HIGH). The period during which CS# is active is called a transaction on the bus.
- While CS# is inactive, the CK is not required to toggle.
- The command transfer occurs at the beginning of every transaction. The address, latency cycles, and data transfer phases are optional and their presence depends on the protocol mode or command transferred.

### Transaction capture

- CK marks the transfer of each bit or group of bits between the host and memory. Command, address and write data bits transfer occurs on CK rising edge in SDR transactions, or on every CK edge, in DDR transactions.

### Note

- All attempts to read the flash memory array during a program or erase (embedded operations) are ignored. The embedded operation will continue to execute without any effect. A very limited set of commands are accepted during an embedded operation. These are discussed in **“Suspend and resume embedded operation”** on page 70.

### Protocol terminology

- The number of DQ signals used during the transaction depends on the current protocol mode or command transferred. The latency cycles do not use the DQ signals for information transfer. The protocol mode options are described by the data rate and the DQ width (number of DQ signals) used during the command, address, and data phases in the following format:  
WR-WR-WR, where:
  - The first WR is the command bit width and rate.
  - The second WR is the address bit width and rate.
  - The third WR is the data bit width and rate.
- The bit width value may be 1, or 8. R has a value of S for SDR or D for DDR. SDR has the same transfer value during the rising and falling edge of a clock cycle. DDR can have different transfer values during the rising and falling edges of each clock.

## Interface overview

- Examples:
  - 1S-1S-1S means that the command is 1 bit wide SDR, the address is 1 bit wide SDR, and the data is one bit wide SDR.
  - 8D-8D-8D means that the command, address, and data transfers are always 8 bits wide DDR.

## Protocols definition

- Protocol modes defined for the SEMPER™ flash octal interface:
  - 1.1S-1S-1S: One DQ signal used during command transfer, address transfer, and data transfer. All phases are SDR.
  - 2.8S-8S-8S: Eight DQ signals used during command transfer, address transfer, and data transfer. All phases are SDR.
  - 3.8D-8D-8D: Eight DQ signals used during command transfer, address transfer, and data transfer. All phases are DDR.

## 1S-1S-1S protocol

- The 1S-1S-1S mode is the preferred default protocol following Power-On-Reset (POR), but flash devices can be configured to reset into the Octal mode.
- Each transaction begins with an 8-bit (1-byte) command. The command selects the type of information transfer or device operation to be performed.
- This protocol uses SI/DQ[0] to transfer information from host to flash device and SO/DQ[1] to transfer information from flash device to host. On each DQ, information is placed on the DQ line in Most Significant bit (MSb) to Least Significant bit (LSb) order within each byte. Sequential address bytes are transferred in highest order to lowest order sequence. Sequential data bytes are transferred in lowest address to highest address order.
- In 1S-1S-1S, DQ[7:2] are not used for data transfer period. Hence, the DQ[7:2] signals will be high impedance.

## 8S-8S-8S and 8D-8D-8D protocols

- Each transaction begins with a 16-bit (two same bytes) command. The command selects the type of information transfer or device operation to be performed.
- Supports 4-byte addressing only.
- This protocol uses DQ[7:0] signals. The LSb of each byte is placed on DQ[0] with each higher order bit on the successively higher numbered DQ signals. Sequential address bytes are transferred in highest order to lowest order sequence. Sequential data bytes in SDR are transferred in lowest address to highest address order. Sequential data bytes in DDR are transferred only in byte pairs (words) where the byte order depends on the order in which the bytes are written or programmed in that protocol mode. Sequential data bytes are transferred in lowest address to highest address order.
- In this protocol, during the period of data transfer in a read transaction, the Data Strobe (DS) signal is driven by the flash device and transitions are synchronized (Edge aligned in DDR and center aligned in SDR protocol) with the DQ signal data transitions. DS is used as an additional output signal with the same timing characteristics as other data outputs but with the guarantee of transitioning with every data bit transferred.

“Serial peripheral interface (SPI, 1S-1S-1S)” on page 13 show all transaction formats by protocol mode.

### 2.3.1 Serial peripheral interface (SPI, 1S-1S-1S)

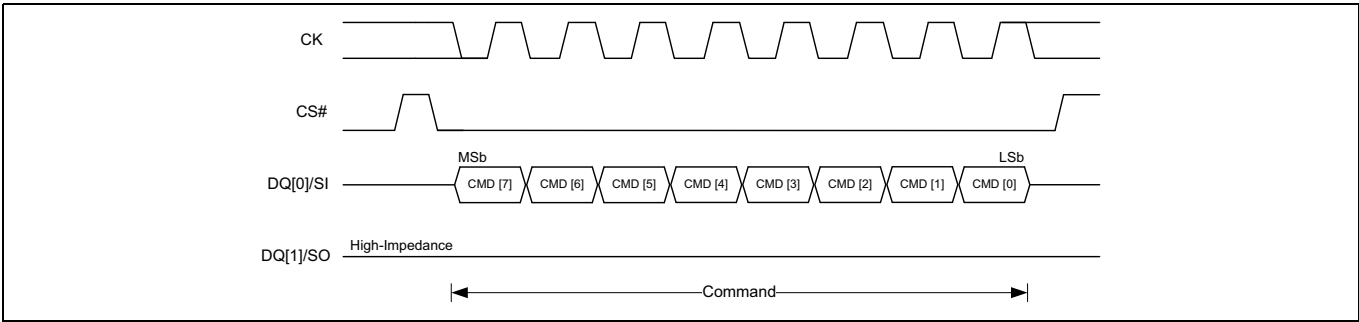


Figure 6 SPI transaction with command input

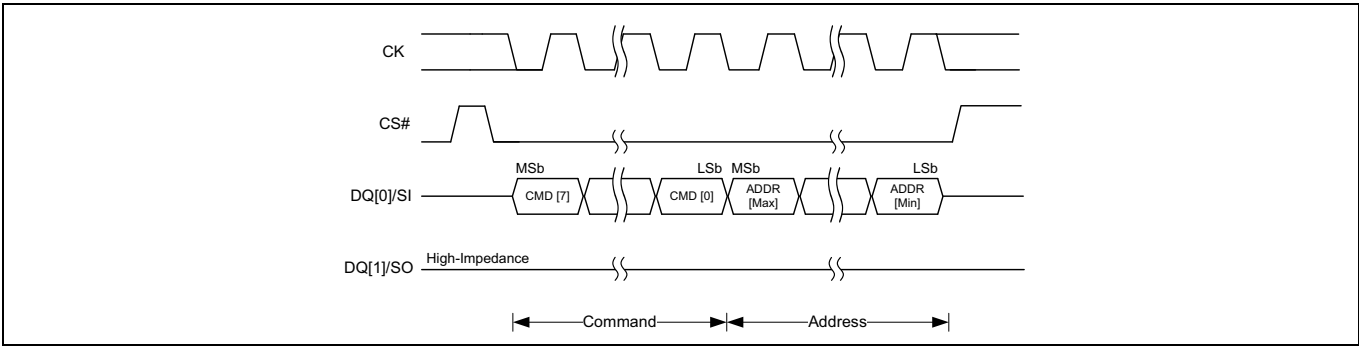


Figure 7 SPI transaction with command and address input

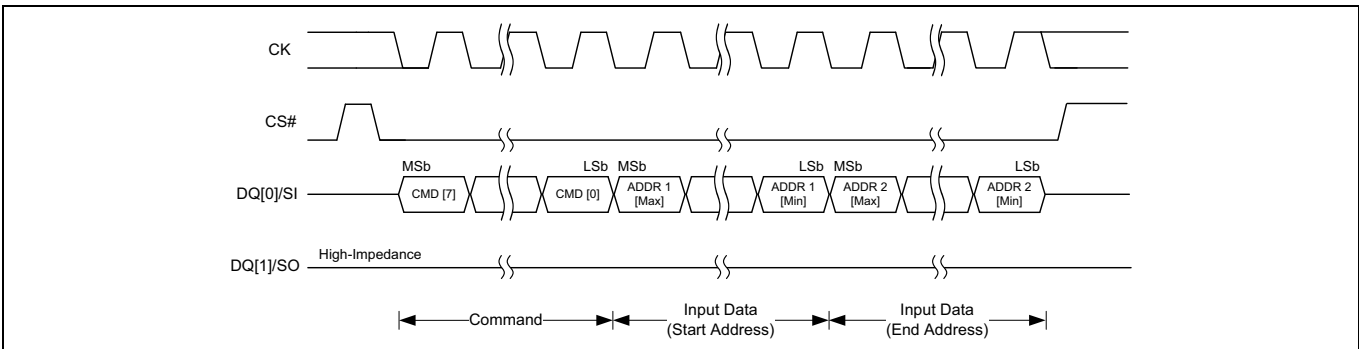


Figure 8 SPI transaction with command and two input addresses

Interface overview

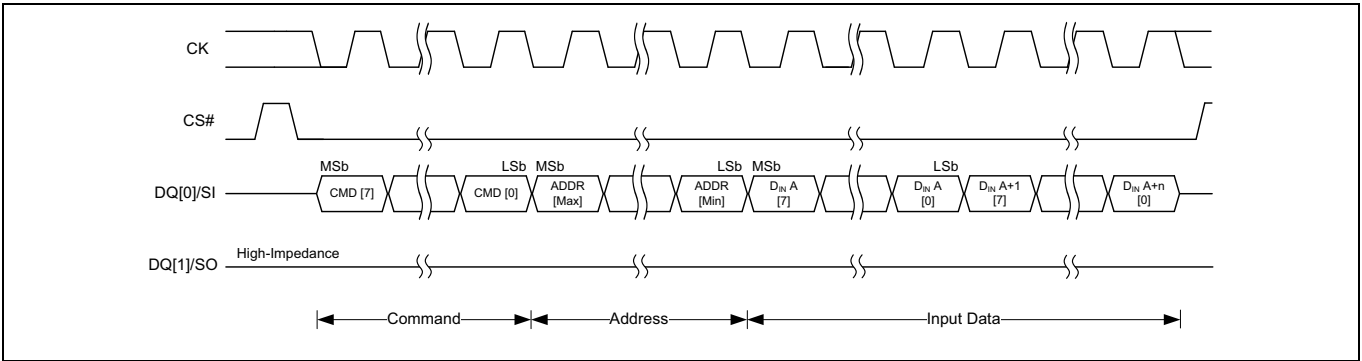


Figure 9 SPI program transaction with command, address, and data input

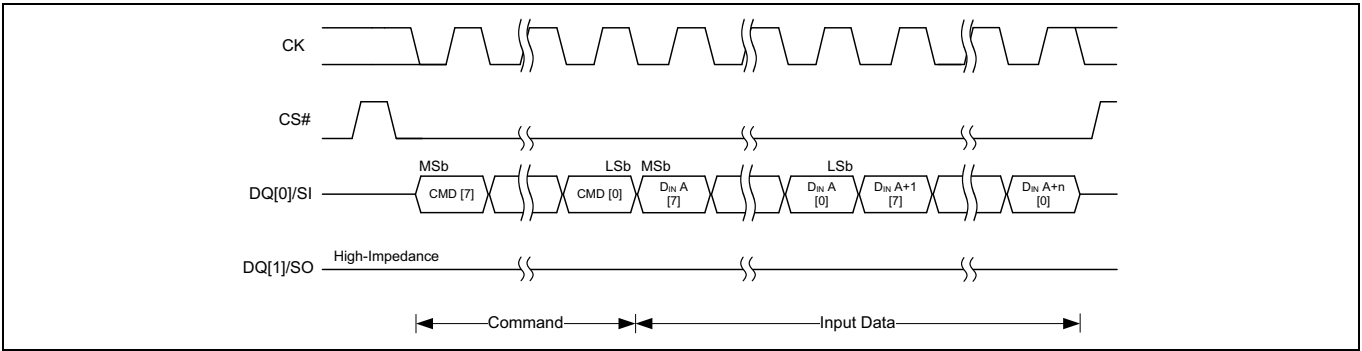


Figure 10 SPI program transaction with command and data input

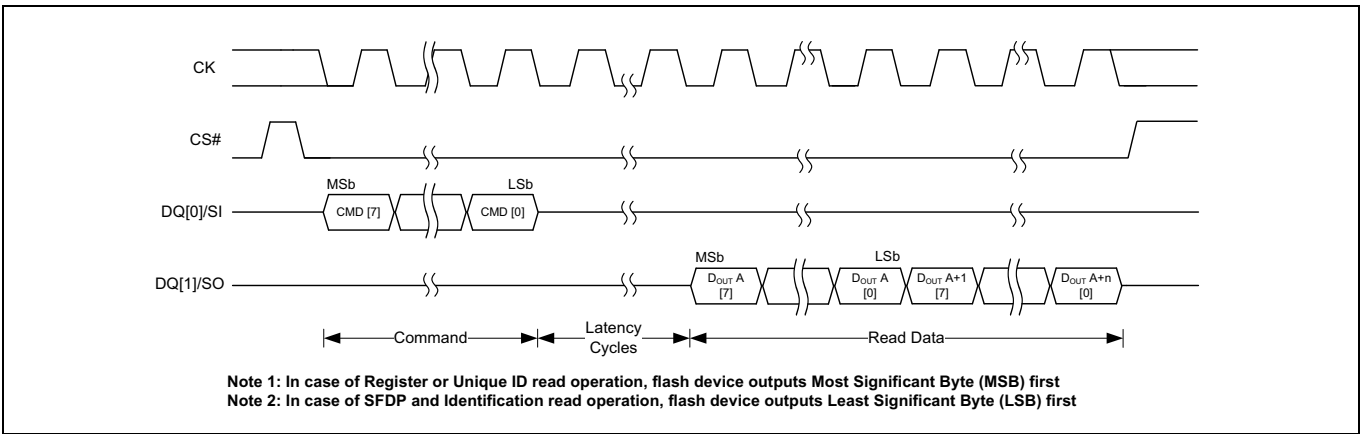
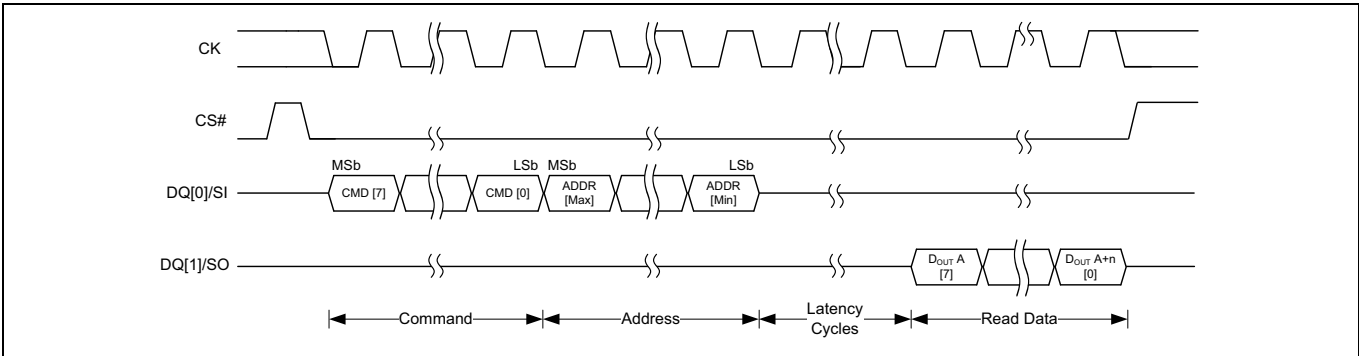
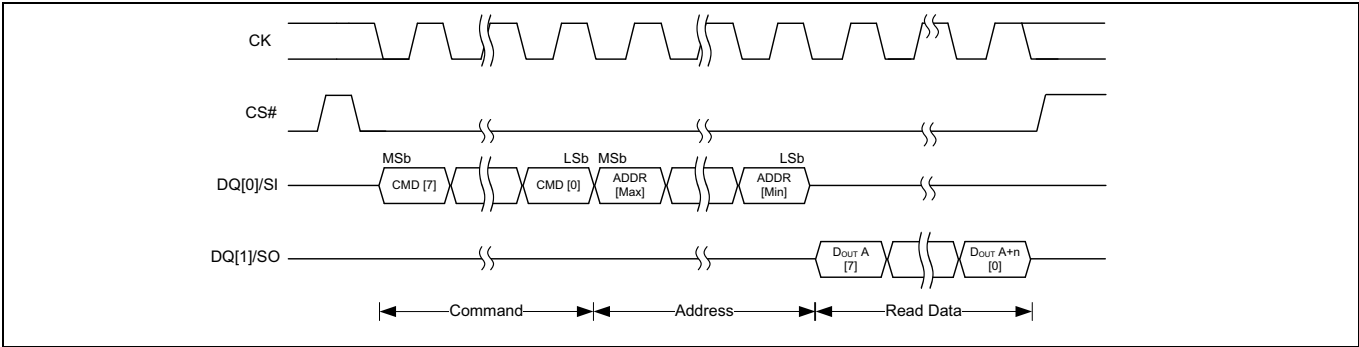


Figure 11 SPI read transaction with command input (output latency)

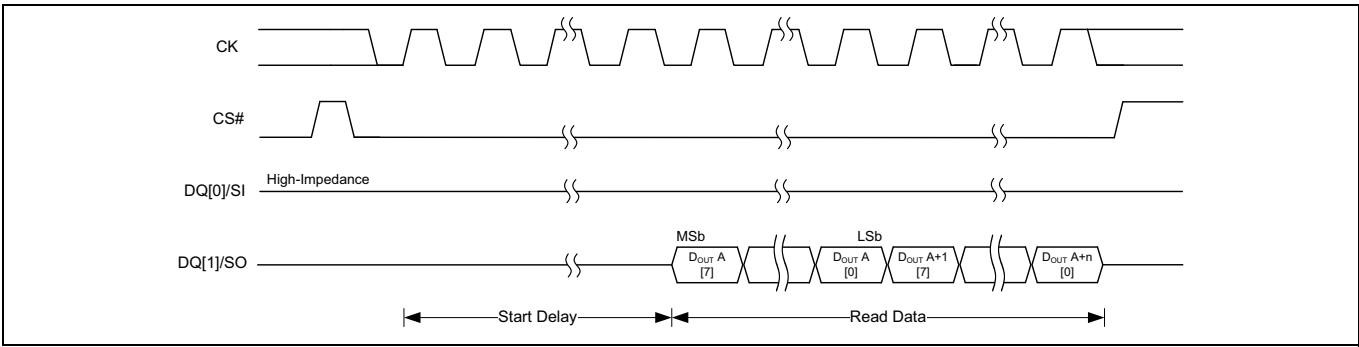
Interface overview



**Figure 12** SPI read transaction with command and address input (output latency)



**Figure 13** SPI read transaction with command and address input (no output latency)



**Figure 14** SPI transaction with output data sequence (AutoBoot)

2.3.2 Octal peripheral interface (octal, 8S-8S-8S and 8D-8D-8D)

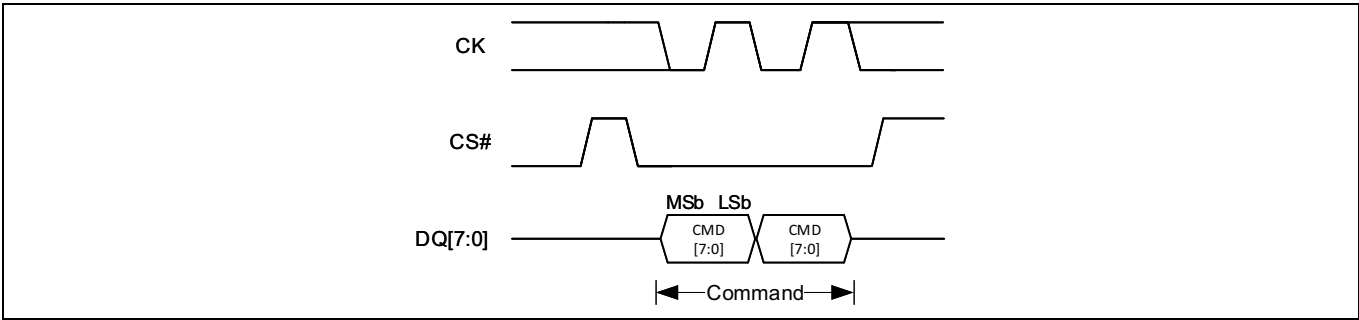


Figure 15 Octal SDR transaction with command input

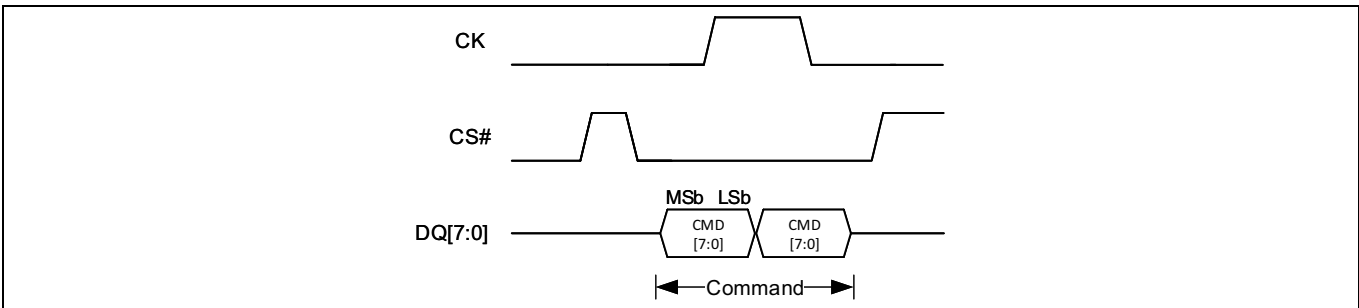
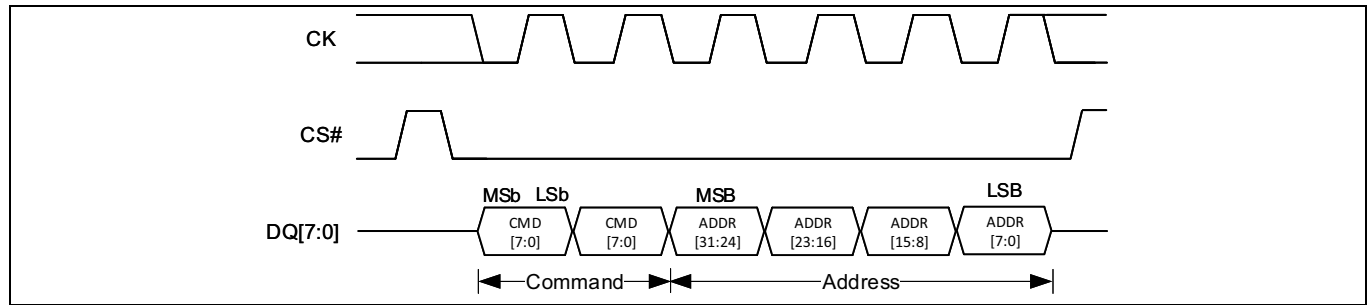
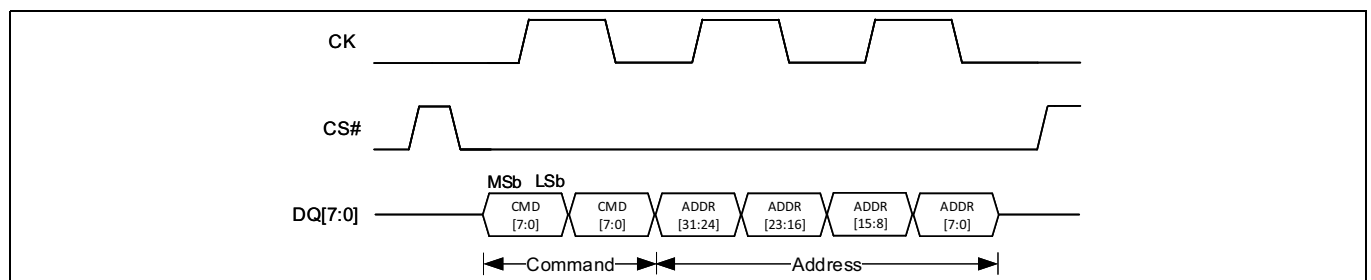


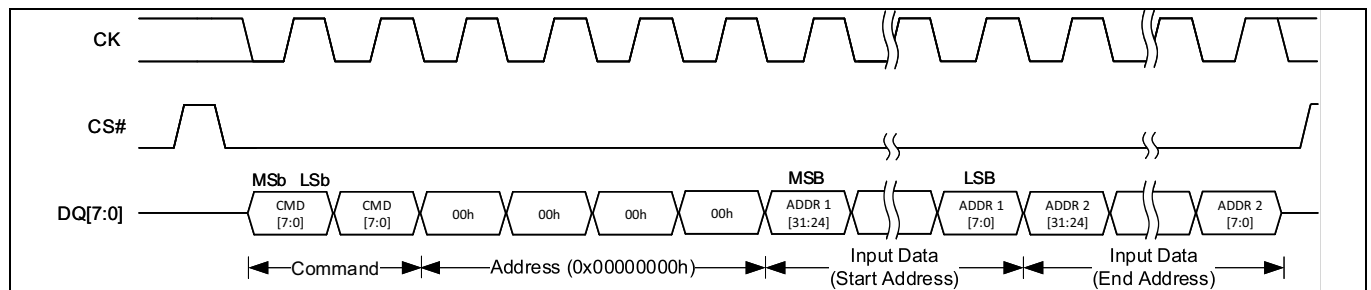
Figure 16 Octal DDR transaction with command input



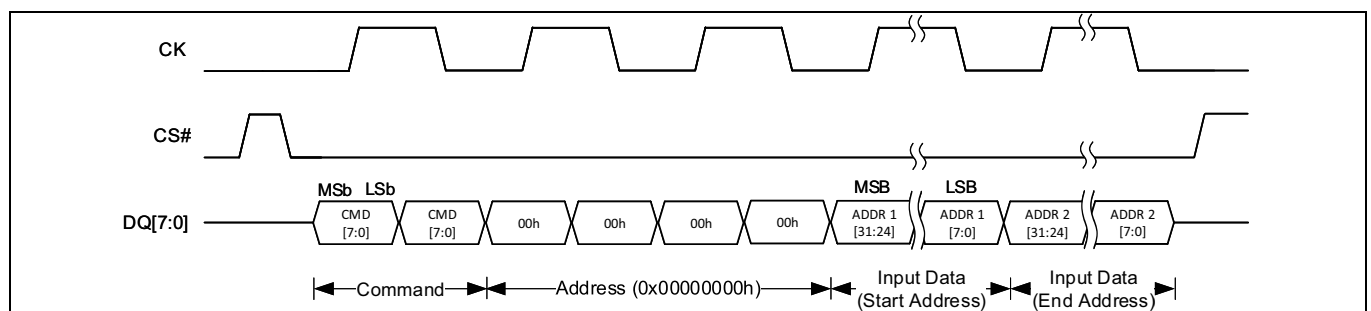
**Figure 17** Octal SDR transaction with command and address input



**Figure 18** Octal DDR transaction with command and address input<sup>[2]</sup>



**Figure 19** Octal SDR transaction with command and two input addresses



**Figure 20** Octal DDR transaction with command and two input addresses

**Note**

- The LSb of the address always be zero in any Octal DDR transactions with the address input.

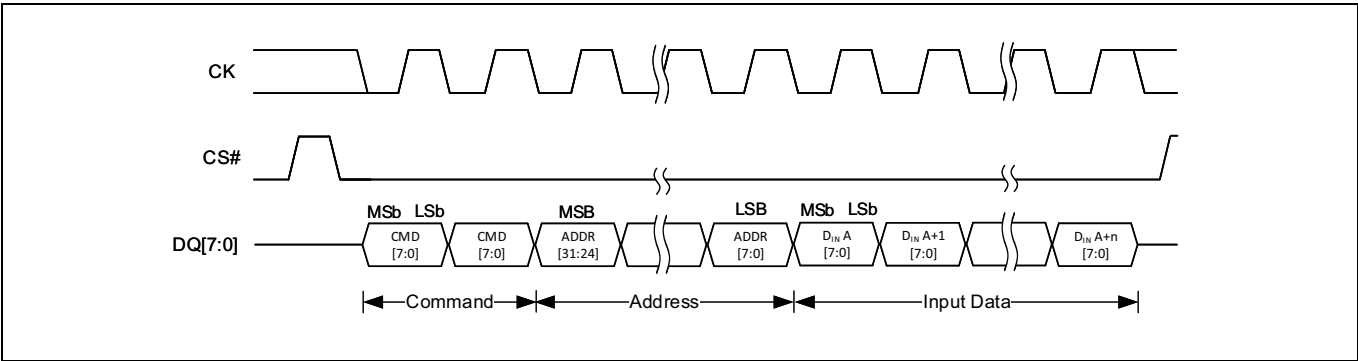


Figure 21 Octal SDR program transaction with command, address, and data input

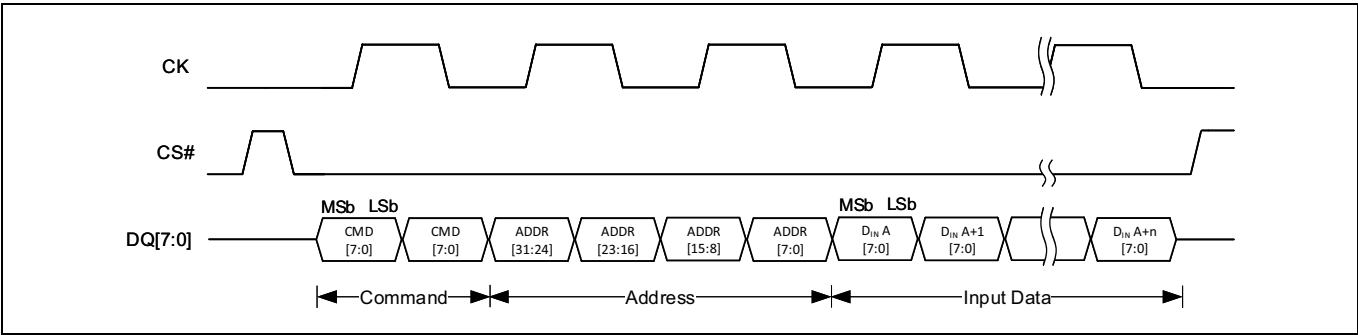


Figure 22 Octal DDR program transaction with command, address, and data input<sup>[3]</sup>

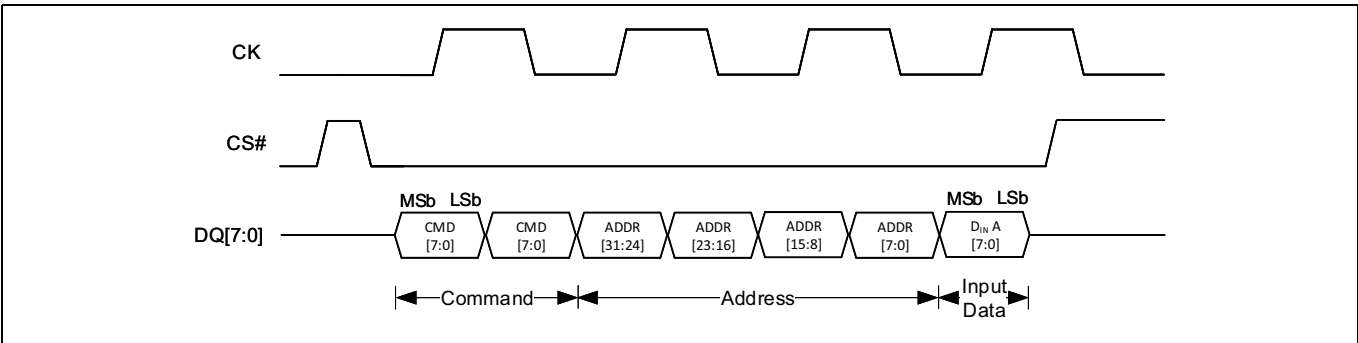
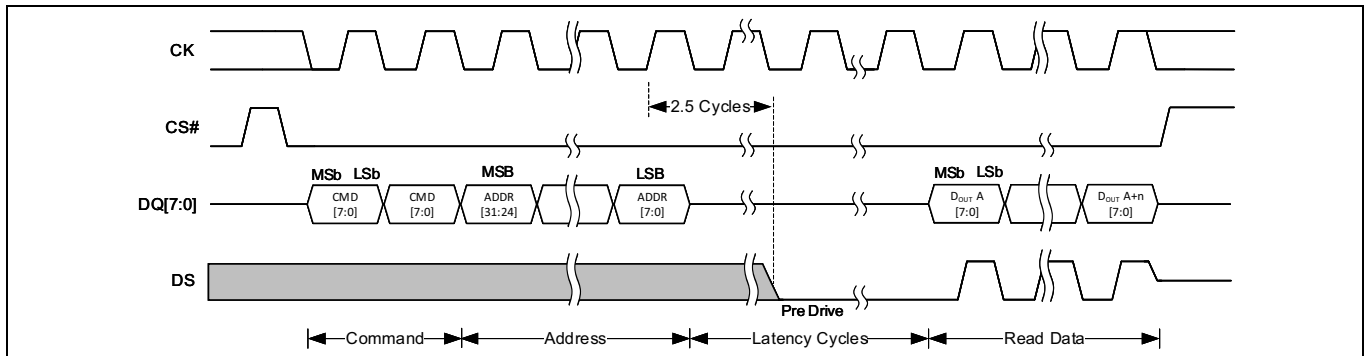


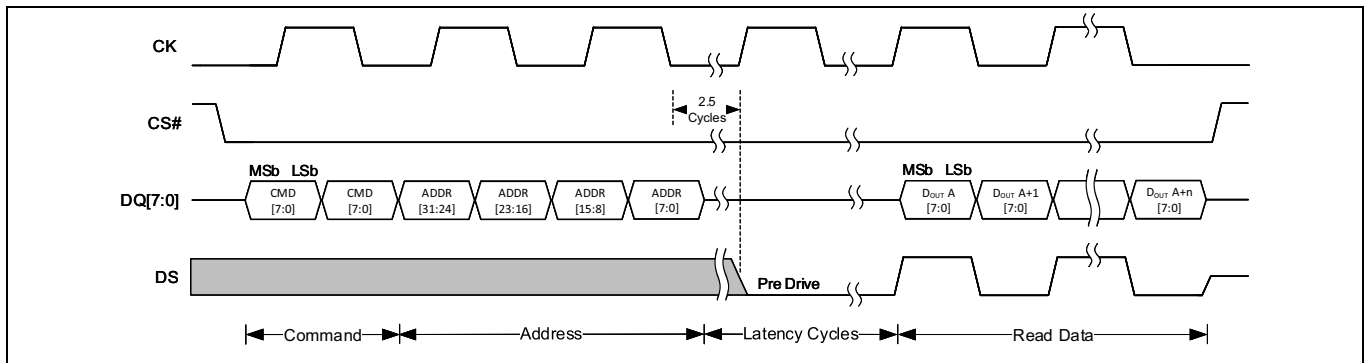
Figure 23 Octal DDR program transaction with command, address, and single byte data input<sup>[3]</sup>

**Note**

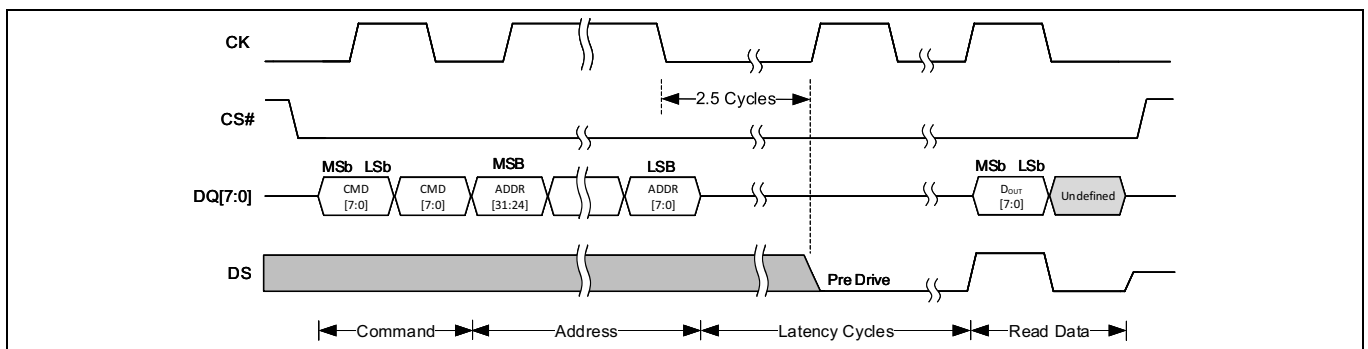
3. The LSb of the address always be zero in any Octal DDR transactions with the address input.



**Figure 24 Octal SDR read transaction with command and address input (output latency)**



**Figure 25 Octal DDR read transaction with command and address input (output latency)<sup>[4, 5]</sup>**



**Figure 26 Octal DDR single byte read transaction with command and address input (output latency)<sup>[6]</sup>**

## Notes

4. The LSb of the address always be zero in any Octal DDR transactions with the address input.
5. Read Interface CRC Transaction is supported with Octal DDR only.

Interface overview

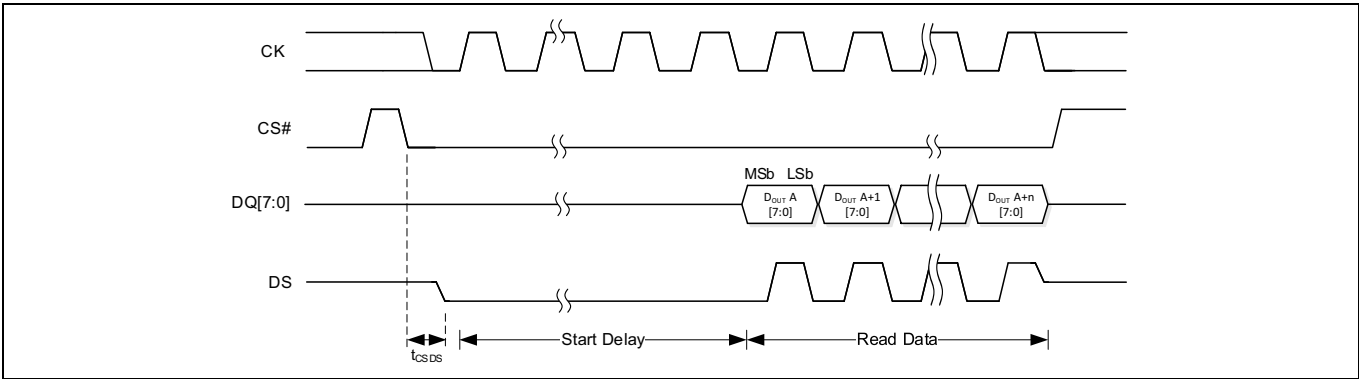


Figure 27 Octal SDR transaction with output data sequence (AutoBoot)

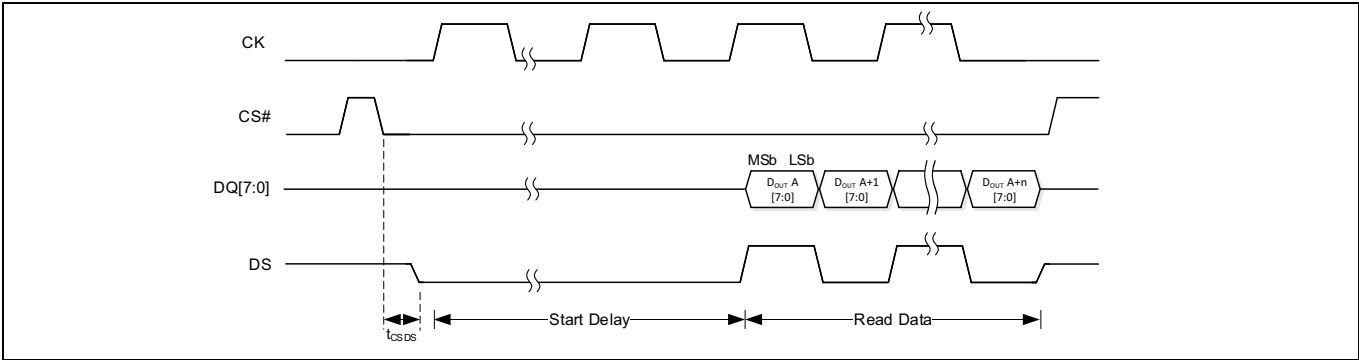


Figure 28 Octal DDR transaction with output data sequence (AutoBoot)

## 2.4 Register naming convention

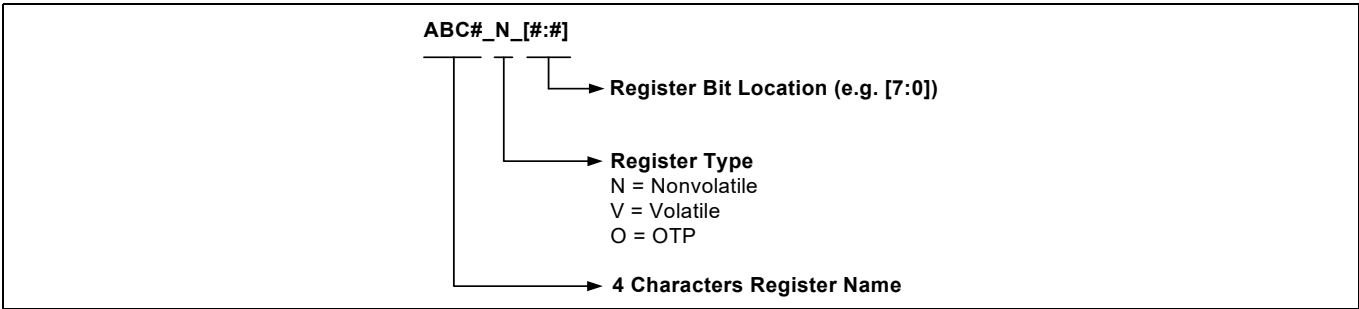


Figure 29 Register naming convention

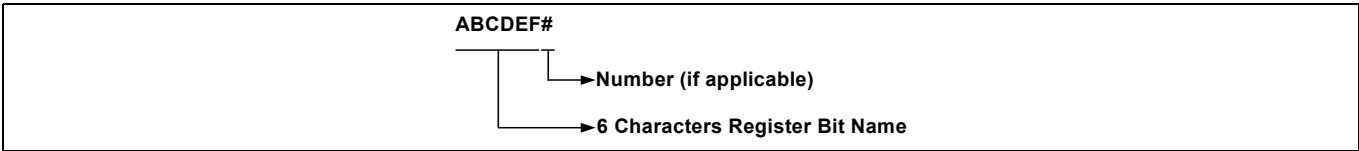


Figure 30 Register bit naming convention

## 2.5 Transaction naming convention

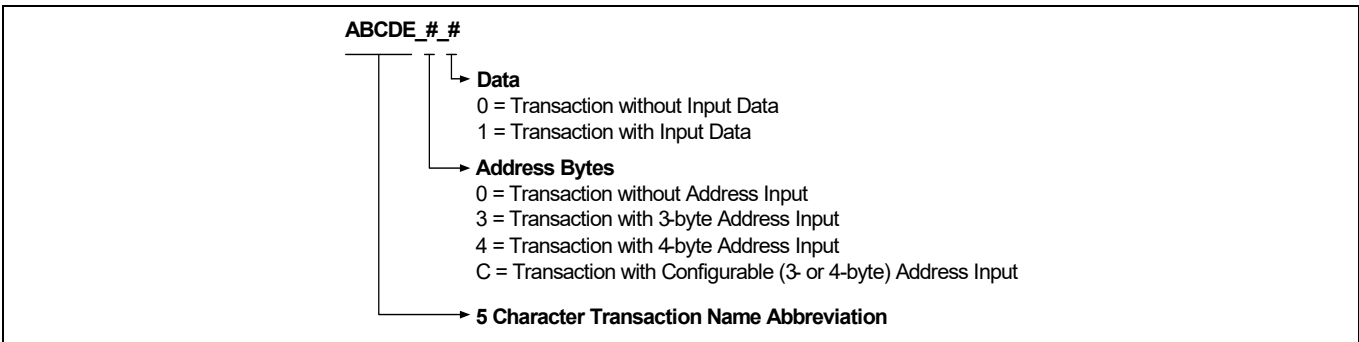
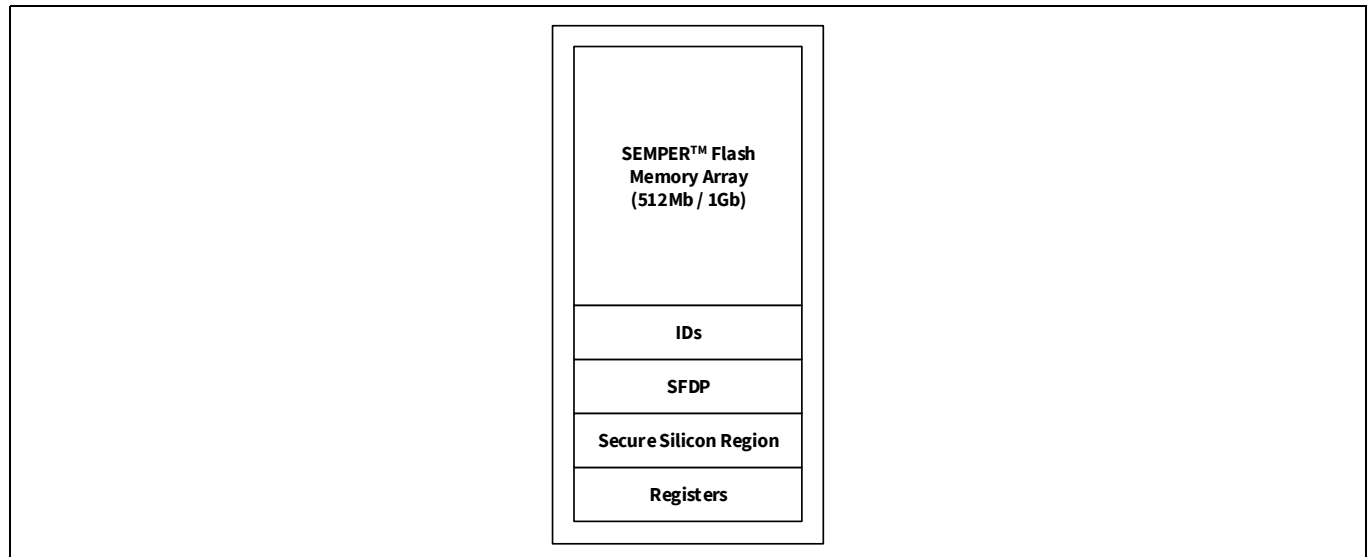


Figure 31 Transaction naming convention

### 3 Address space maps

The HL-T/HS-T family supports 24-bit as well as 32-bit (4-byte) addresses, to enable 512 Mb or 1 Gb density devices. 4-byte addresses allow direct addressing of up to 4GB (32Gb) address space. The address byte option can be changed by writing the respective configuration registers OR there are separate transactions also available to enter (EN4BA\_0\_0) and exit (EX4BA\_0\_0) the 4-byte address mode.



**Figure 32** HL-T/HS-T address space map overview

#### 3.1 SEMPER™ Flash memory array

The main flash array is divided into units called physical sectors.

The HL-T/HS-T family sector architecture supports the following options:

- 512 Mb, 1 Gb supports 256 KB Uniform sector options
- 512 Mb, 1 Gb Hybrid sector options
  - Physical set of thirty-two 4 KB sectors and one 128 KB sector at the top or bottom of address space with all remaining sectors of 256 KB
  - Physical set of sixteen 4 KB sectors and one 192 KB sector at both the top and bottom of the address space with all remaining sectors of 256 KB

The combination of the sector architecture selection bits in Configuration Register-1 and Configuration Register-3 support the different sector architecture options of the HL-T/HS-T family. See **“Registers”** on page 82 for more information.

**Table 8**      **256KB uniform sector address map<sup>[7]</sup>**

| Sector size (KB) | S28HL01GT and S28HS01GT |              |                                                                    | S28HL512T and S28HS512T |              |                                                                    |
|------------------|-------------------------|--------------|--------------------------------------------------------------------|-------------------------|--------------|--------------------------------------------------------------------|
|                  | Sector count            | Sector range | Byte address range (sector starting address–sector ending address) | Sector count            | Sector range | Byte address range (sector starting address–sector ending address) |
| 256              | 512                     | SA00         | 00000000h–0003FFFFh                                                | 256                     | SA00         | 00000000h–0003FFFFh                                                |
|                  |                         | :            | :                                                                  |                         | :            | :                                                                  |
|                  |                         | SA511        | 07FC0000h–07FFFFFFh                                                |                         | SA255        | 03FC0000h–03FFFFFFh                                                |

**Note**

7. Configuration: CFR3N[3] = 1.

**Table 9**      **Bottom hybrid configuration one thirty-two 4KB sectors and 256KB uniform sectors address map<sup>[8]</sup>**

| Sector size (KB) | S28HL01GT and S28HS01GT |              |                                                                    | S28HL512T and S28HS512T |              |                                                                    |
|------------------|-------------------------|--------------|--------------------------------------------------------------------|-------------------------|--------------|--------------------------------------------------------------------|
|                  | Sector count            | Sector range | Byte address range (sector starting address–sector ending address) | Sector count            | Sector range | Byte address range (sector starting address–sector ending address) |
| 4                | 32                      | SA00         | 00000000h–00000FFFh                                                | 32                      | SA00         | 00000000h–00000FFFh                                                |
|                  |                         | :            | :                                                                  |                         | :            | :                                                                  |
|                  |                         | SA31         | 0001F000h–0001FFFFh                                                |                         | SA31         | 0001F000h–0001FFFFh                                                |
| 128              | 1                       | SA32         | 00020000h–0003FFFFh                                                | 1                       | SA32         | 00020000h–0003FFFFh                                                |
| 256              | 511                     | SA33         | 00040000h–0007FFFFh                                                | 255                     | SA33         | 00040000h–0007FFFFh                                                |
|                  |                         | :            | :                                                                  |                         | :            | :                                                                  |
|                  |                         | SA543        | 07FC0000h–07FFFFFFh                                                |                         | SA287        | 03FC0000h–03FFFFFFh                                                |

**Note**

8. Configuration: CFR3N[3] = 0, CFR1N[6] = 0, CFR1N[2] = 0.

**Table 10**      **Top hybrid configuration one thirty-two 4KB sectors and 256KB uniform sectors address map<sup>[9]</sup>**

| Sector size (KB) | S28HL01GT and S28HS01GT |              |                                                                    | S28HL512T and S28HS512T |              |                                                                    |
|------------------|-------------------------|--------------|--------------------------------------------------------------------|-------------------------|--------------|--------------------------------------------------------------------|
|                  | Sector count            | Sector range | Byte address range (Sector starting address–sector ending address) | Sector count            | Sector range | Byte address range (Sector starting address–sector ending address) |
| 256              | 511                     | SA00         | 00000000h–0003FFFFh                                                | 255                     | SA00         | 00000000h–0003FFFFh                                                |
|                  |                         | :            | :                                                                  |                         | :            | :                                                                  |
|                  |                         | SA510        | 07F80000h–07FBFFFFh                                                |                         | SA254        | 03F80000h–03FBFFFFh                                                |
| 128              | 1                       | SA511        | 07FC0000h–07FDFFFFh                                                | 1                       | SA255        | 03FC0000h–03FDFFFFh                                                |
| 4                | 32                      | SA512        | 07FE0000h–07FE0FFFh                                                | 32                      | SA256        | 03FE0000h–03FE0FFFh                                                |
|                  |                         | :            | :                                                                  |                         | :            | :                                                                  |
|                  |                         | SA543        | 07FFF000h–07FFFFFFh                                                |                         | SA287        | 03FFF000h–03FFFFFFh                                                |

**Note**

9. Configuration: CFR3N[3] = 0, CFR1N[6] = 0, CFR1N[2] = 1.

**Table 11**      **Hybrid configuration 2 bottom sixteen and top sixteen 4 KB sectors address map<sup>[10]</sup>**

| Sector size (KB) | S28HL01GT and S28HS01GT |              |                                                                    | S28HL512T and S28HS512T |              |                                                                    |
|------------------|-------------------------|--------------|--------------------------------------------------------------------|-------------------------|--------------|--------------------------------------------------------------------|
|                  | Sector count            | Sector range | Byte address range (Sector starting address–sector ending address) | Sector count            | Sector range | Byte address range (Sector starting address–sector ending address) |
| 4                | 16                      | SA00         | 00000000h–00000FFFh                                                | 16                      | SA00         | 00000000h–00000FFFh                                                |
|                  |                         | :            | :                                                                  |                         | :            | :                                                                  |
|                  |                         | SA15         | 0000F000h–0000FFFFh                                                |                         | SA15         | 0000F000h–0000FFFFh                                                |
| 192              | 1                       | SA16         | 00010000h–0003FFFFh                                                | 1                       | SA16         | 00010000h–0003FFFFh                                                |
| 256              | 510                     | SA17         | 00040000h–0007FFFFh                                                | 254                     | SA17         | 00040000h–0007FFFFh                                                |
|                  |                         | :            | :                                                                  |                         | :            | :                                                                  |
|                  |                         | SA526        | 07F80000h–07FBFFFFh                                                |                         | SA270        | 03F80000h–03FBFFFFh                                                |

**Note**

10. Configuration: CFR3N[3] = 0, CFR1N[6] = 1.

**Table 11**      **Hybrid configuration 2 bottom sixteen and top sixteen 4 KB sectors**  
**address map<sup>[10]</sup> (Continued)**

| Sector size (KB) | S28HL01GT and S28HS01GT |              |                                                                    | S28HL512T and S28HS512T |              |                                                                    |
|------------------|-------------------------|--------------|--------------------------------------------------------------------|-------------------------|--------------|--------------------------------------------------------------------|
|                  | Sector count            | Sector range | Byte address range (Sector starting address–sector ending address) | Sector count            | Sector range | Byte address range (Sector starting address–sector ending address) |
| 192              | 1                       | SA527        | 07FC0000h–07FEFFFFh                                                | 1                       | SA271        | 03FC0000h–03FEFFFFh                                                |
| 4                | 16                      | SA528        | 07FF0000h–07FF0FFFh                                                | 16                      | SA272        | 03FF0000h–03FF0FFFh                                                |
|                  |                         | :            | :                                                                  |                         | :            | :                                                                  |
|                  |                         | SA543        | 07FFF000h–07FFFFFFh                                                |                         | SA287        | 03FFF000h–03FFFFFFh                                                |

**Note**

10.Configuration: CFR3N[3] = 0, CFR1N[6] = 1.

These are condensed tables that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 4 KB sectors have the pattern xxxxx000h–xxxxxFFFh. All 256KB sectors have the pattern xxx00000h–xxx3FFFFh, xxx40000h–xxx7FFFFh, xx80000h–xxxCFFFFh, or xxD0000h–xxxFFFFFFh.

### 3.2 ID address space

This particular region of the memory is assigned to manufacturer, device, and unique identification:

- The manufacturer identification is assigned by JEDEC (see [Table 94](#)).
- The device identification is assigned by Infineon (see [Table 94](#)).
- A 64-bit unique number is located in 8 bytes of the Unique Device ID address space. This Unique ID can be used as a software readable serial number that is unique for each device. (see [Table 95](#)).

There is no address space defined for these IDs as they can be read by providing the respective transactions only. The transactions do not need the address to read these IDs. The data in this address space is read-only data.

### 3.3 JEDEC JESD216 SFDP space

The SFDP standard provides a consistent method of describing the functional and feature capabilities of this serial flash device in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features. The SFDP address space has a header starting at address zero that identifies the SFDP data structure and provides a pointer to each parameter. The SFDP address space is programmed by Infineon and read-only for the host system (see [Table 90](#) through [Table 93](#)).

**Table 12 SFDP overview address map**

| Byte address | Description                                                                              |
|--------------|------------------------------------------------------------------------------------------|
| 0000h        | Location zero within JEDEC JESD216D SFDP space - start of SFDP header                    |
| ...          | Remainder of SFDP header followed by undefined space                                     |
| 0100h        | Start of SFDP parameter tables The SFDP parameter table data starting at 0100h           |
| ...          | Remainder of SFDP parameter tables followed by either more parameters or undefined space |

### 3.4 SSR address space

Each HS/L-T family memory device has a 1024-byte SSR which is OTP address space. This address space is separate from the main flash array. The SSR area is divided into 32 individually lockable, 32-byte aligned and length regions.

In the 32-byte region starting at address zero:

- The sixteen lowest bytes contain a 128-bit random number. The random number cannot be written to, erased or programmed and any attempts will return an PRGERR flag.
- The next four bytes are used to provide one bit per secure region (32 bits in total) to permanently protect once set to '0' from writing, erasing or programming.
- All other bytes are reserved.

The remaining regions are erased when shipped from Infineon, and are available for programming of additional permanent data.

**Table 13**      **SSR address map**

| Region    | Byte address range | Contents                                                                                                                                              | Initial delivery state            |
|-----------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|
| Region 0  | 000h               | LSB of Infineon programmed random number                                                                                                              | Infineon programmed random number |
|           | ...                | ...                                                                                                                                                   |                                   |
|           | 00Fh               | MSB of Infineon programmed random number                                                                                                              |                                   |
|           | 010h to 013h       | Region locking bits<br>Byte 10h [bit 0] locks region 0 from programming when = 0<br>...<br>Byte 13h [bit 7] locks region 31 from programming when = 0 | All Bytes = FFh                   |
|           | 014h to 01Fh       | Reserved for Future Use (RFU)                                                                                                                         |                                   |
| Region 1  | 020h to 03Fh       | Available for User Programming                                                                                                                        |                                   |
| Region 2  | 040h to 05Fh       |                                                                                                                                                       |                                   |
| ...       | ...                |                                                                                                                                                       |                                   |
| Region 31 | 3E0h to 3FFh       |                                                                                                                                                       |                                   |

### 3.5 Registers

Registers are small groups of memory cells used to configure how the HS/L-T family memory device operates, or to report the status of device operations. The registers are accessed by specific commands and addresses.

**Table 14** shows the address map for every available register in this flash memory device.

**Table 14**      **Register address map**

| Function             | Register type                 | Register name             | Volatile component address (hex) | Non-volatile component address (hex) |
|----------------------|-------------------------------|---------------------------|----------------------------------|--------------------------------------|
| Device status        | Status Register 1             | STR1N[7:0],<br>STR1V[7:0] | 0x00800000                       | 0x00000000                           |
|                      | Status Register 2             | STR2V[7:0]                | 0x00800001                       | N/A                                  |
| Device configuration | Configuration Register 1      | CFR1N[7:0],<br>CFR1V[7:0] | 0x00800002                       | 0x00000002                           |
|                      | Configuration Register 2      | CFR2N[7:0],<br>CFR2V[7:0] | 0x00800003                       | 0x00000003                           |
|                      | Configuration Register 3      | CFR3N[7:0],<br>CFR3V[7:0] | 0x00800004                       | 0x00000004                           |
|                      | Configuration Register 4      | CFR4N[7:0],<br>CFR4V[7:0] | 0x00800005                       | 0x00000005                           |
|                      | Configuration Register 5      | CFR5N[7:0],<br>CFR5V[7:0] | 0x00800006                       | 0x00000006                           |
| Interface CRC        | Interface CRC Enable Register | ICEV[7:0]                 | 0x00800008                       | N/A                                  |

**Table 14**      **Register address map** (Continued)

| Function                             | Register type                                                    | Register name | Volatile component address (hex) | Non-volatile component address (hex) |
|--------------------------------------|------------------------------------------------------------------|---------------|----------------------------------|--------------------------------------|
| Infineon Endurance Flex architecture | Infineon Endurance Flex Architecture Selection Register 0 [1:0]  | EFX00[7:0]    | N/A                              | 0x00000050                           |
|                                      | Infineon Endurance Flex Architecture Selection Register 1 [7:0]  | EFX10[7:0]    |                                  | 0x00000052                           |
|                                      | Infineon Endurance Flex Architecture Selection Register 1 [10:8] | EFX10[10:8]   |                                  | 0x00000053                           |
|                                      | Infineon Endurance Flex Architecture Selection Register 2 [7:0]  | EFX20[7:0]    |                                  | 0x00000054                           |
|                                      | Infineon Endurance Flex Architecture Selection Register 2 [10:8] | EFX20[10:8]   |                                  | 0x00000055                           |
|                                      | Infineon Endurance Flex Architecture Selection Register 3 [7:0]  | EFX30[7:0]    |                                  | 0x00000056                           |
| Infineon Endurance Flex architecture | Infineon Endurance Flex Architecture Selection Register 3 [10:8] | EFX30[10:8]   | N/A                              | 0x00000057                           |
|                                      | Infineon Endurance Flex Architecture Selection Register 4 [7:0]  | EFX40[7:0]    |                                  | 0x00000058                           |
|                                      | Infineon Endurance Flex Architecture Selection Register 4 [10:8] | EFX40[10:8]   |                                  | 0x00000059                           |
| Interrupt pin                        | Interrupt Configuration Register                                 | INCV[7:0]     | 0x00800068                       | N/A                                  |
|                                      | Interrupt Status Register                                        | INSV[7:0]     | 0x00800067                       |                                      |
| Error correction                     | ECC Status Register                                              | ESCV[7:0]     | 0x00800089                       |                                      |
|                                      | ECC Error Detection Count Register [7:0]                         | ECTV[7:0]     | 0x0080008A                       |                                      |
|                                      | ECC Error Detection Count Register [15:8]                        | ECTV[15:8]    | 0x0080008B                       |                                      |
|                                      | ECC Address Trap Register [7:0]                                  | EATV[7:0]     | 0x0080008E                       |                                      |
|                                      | ECC Address Trap Register [15:8]                                 | EATV[15:8]    | 0x0080008F                       |                                      |
|                                      | ECC Address Trap Register [23:16]                                | EATV[23:16]   | 0x00800040                       |                                      |
|                                      | ECC Address Trap Register [31:24]                                | EATV[31:24]   | 0x00800041                       |                                      |

**Table 14**      **Register address map** (Continued)

| Function                | Register type                                       | Register name | Volatile component address (hex) | Non-volatile component address (hex) |
|-------------------------|-----------------------------------------------------|---------------|----------------------------------|--------------------------------------|
| AutoBoot                | AutoBoot Register [7:0]                             | ATBN[7:0]     | N/A                              | 0x00000042                           |
|                         | AutoBoot Register [15:8]                            | ATBN[15:8]    |                                  | 0x00000043                           |
|                         | AutoBoot Register [23:16]                           | ATBN[23:16]   |                                  | 0x00000044                           |
|                         | AutoBoot Register [31:24]                           | ATBN[31:24]   |                                  | 0x00000045                           |
| Erase Count             | Sector Erase Count Register [7:0]                   | SECV[7:0]     | 0x00800091                       | N/A                                  |
|                         | Sector Erase Count Register [15:8]                  | SECV[15:8]    | 0x00800092                       |                                      |
|                         | Sector Erase Count Register [23:16]                 | SECV[23:16]   | 0x00800093                       |                                      |
| Data Integrity Check    | Data Integrity Check CRC Register [7:0]             | DCRV[7:0]     | 0x00800095                       | N/A                                  |
|                         | Data Integrity Check CRC Register [15:8]            | DCRV[15:8]    | 0x00800096                       |                                      |
|                         | Data Integrity Check CRC Register [23:16]           | DCRV[23:16]   | 0x00800097                       |                                      |
|                         | Data Integrity Check CRC Register [31:24]           | DCRV[31:24]   | 0x00800098                       |                                      |
| Protection and Security | Advanced Sector Protection Register [7:0]           | ASPO[7:0]     | N/A                              | 0x00000030                           |
|                         | Advanced Sector Protection Register [15:8]          | ASPO[15:8]    |                                  | 0x00000031                           |
|                         | ASP PPB Lock Register (Persistent Protection Block) | PPLV[7:0]     | 0x0080009B                       | N/A                                  |
|                         | ASP Password Register [7:0]                         | PWDO[7:0]     | N/A                              | 0x00000020                           |
|                         | ASP Password Register [15:8]                        | PWDO[15:8]    |                                  | 0x00000021                           |
|                         | ASP Password Register [23:16]                       | PWDO[23:16]   |                                  | 0x00000022                           |
|                         | ASP Password Register [31:24]                       | PWDO[31:24]   |                                  | 0x00000023                           |
|                         | ASP Password Register [39:32]                       | PWDO[39:32]   |                                  | 0x00000024                           |
| Protection and Security | ASP Password Register [47:40]                       | PWDO[47:40]   |                                  | 0x00000025                           |
|                         | ASP Password Register [55:48]                       | PWDO[55:48]   |                                  | 0x00000026                           |
|                         | ASP Password Register [63:56]                       | PWDO[63:56]   |                                  | 0x00000027                           |

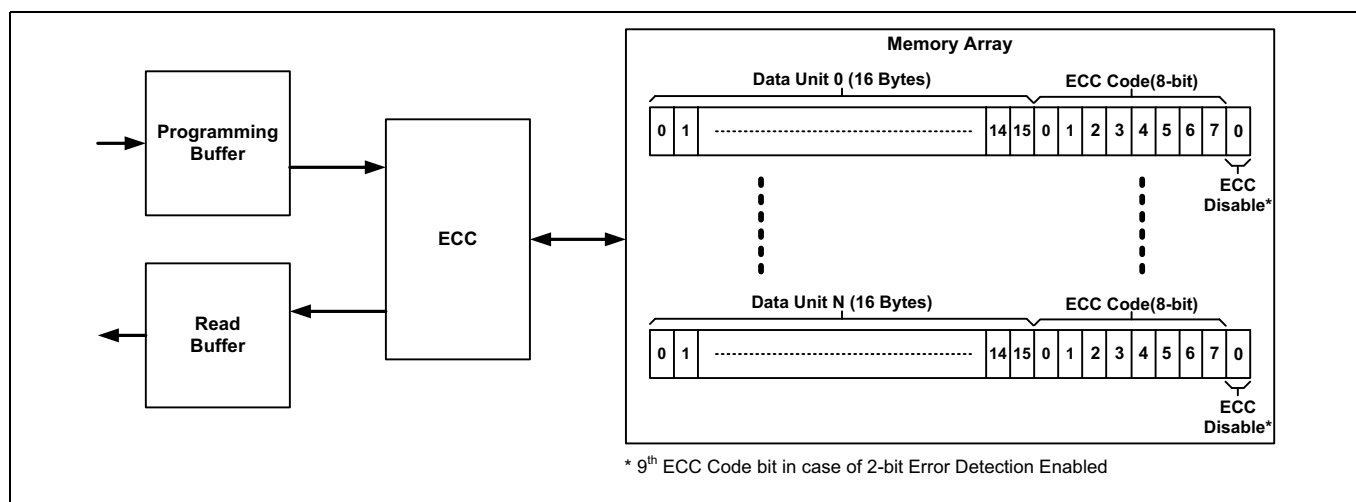
## 4 Features

### 4.1 Error detection and correction

HL-T/HS-T family devices support error detection and correction by generating an embedded Hamming error correction code during memory array programming. This ECC code is then used for error detection and correction during read operations. The ECC is based on a 16-byte data unit. When the 16-byte data unit is loaded into the Program Buffer and is transferred to the 128-bits flash memory array Line for programming (after an erase), an 8-bit Error Correction Code (ECC) for each data unit is also programmed into a portion of the memory array that is not visible to the host system software. This ECC information is then checked during each Flash array read operation. Any 1-bit error within the data unit will be corrected by the ECC logic. The 16-byte data unit is the smallest program granularity on which ECC is enabled.

When any amount of data is first programmed within a 16-byte data unit, the ECC value is set for the entire data unit. If additional data is subsequently programmed into the same data unit, without an erase, then the ECC for that data unit is disabled and the 1-bit ECC disable bit is set. A sector erase is needed to again enable ECC on that data unit.

These are automatic operations transparent to the user. The transparency of the ECC feature enhances data reliability for typical programming operations which write data once to each data unit while also facilitating software compatibility with previous generations of products by still allowing for single-byte programming and bit-walking (in this case, ECC will be disabled) in which the same data unit is programmed more than once.



**Figure 33 16-byte ECC data unit example**

SEMPER™ NOR flash supports 2-bit error detection as the default ECC configuration. In this configuration, any 1-bit error in a data unit is corrected and any 2-bit error is detected and reported. The 16-byte unit data requires a 9-bit Error Correction Code for 2-bit error detection. When 2-bit error detection is enabled, byte-programming, bit-walking, or multiple program operations to the same data unit (without an erase) are not allowed and will result in a Program Error. Changing the ECC mode from 1-bit error detection to 2-bit error detection, or from 2-bit error detection to 1-bit error detection will invalidate all data in the memory array. When changing the ECC mode, the host must first erase all sectors in the device. If the ECC mode is changed without erasing programmed data, subsequent read operations will result in undefined behavior.

#### 4.1.1 ECC error reporting

There are five methods for reporting to the host system when ECC errors are detected.

- ECC Data Unit Status provides the status of 1-bit or 2-bit errors in data units.
- ECC Status Register provides the status of 1-bit or 2-bit errors since the last ECC clear or reset.
- The Address Trap Register captures the address location of the first ECC error encountered after POR or reset during memory array read.
- An ECC Error Detection counter keeps a tally of the number of 1-bit or 2-bit errors that have occurred in data units during reads.
- The Interrupt (INT#) output can be enabled to indicate when either a 1-bit or 2-bit error is detected as data is read.

##### 4.1.1.1 ECC Data Unit Status (EDUS)

- The status of ECC in each data unit is provided by the 8-bit ECC Data Unit Status.
- The ECC status transaction outputs the ECC status of the addressed data unit. The contents of the ECC Data Unit status then indicate, for the selected data unit, whether there is a 1-bit error corrected, 2-bit error detected, or the ECC is disabled for that data unit.

**Table 15**      **ECC Data Unit Status**

| Bits      | Field name | Function                             | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----------|------------|--------------------------------------|------------------------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EDUS[7:4] | RESRVD     | Reserved For Future Use              | V => R                                         | 0000                        | These bits are Reserved for future use.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| EDUS[3]   | ECC2BD     | ECC Error 2-bit Error Detection Flag | V => R                                         | 0                           | <p>This bit indicates whether a two bit error is detected in the data unit, if two bit ECC error detection is enabled CFR4V[3] = 1. When CFR4V[3] = 0 and 2-bit error detection is disabled, ECC2BD bit will always be '0'.</p> <p><b>Note:</b> If 2 bit error detection is enabled (CFR4V[3] = 1), the ECCOFF bit will not be set to 1b while performing single byte programming or bit walking in a data unit that was already partially programmed. An attempt to do such byte programming or bit walking will result in a Program Error.</p> <p>Selection Options:<br/> 1 = Two Bit Error detected<br/> 0 = No error</p> |
| EDUS[2]   | RESRVD     | Reserved For Future Use              | V => R                                         | 0                           | This bit is Reserved for future use.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

**Table 15**      **ECC Data Unit Status** (Continued)

| Bits    | Field name | Function                                            | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                    |
|---------|------------|-----------------------------------------------------|------------------------------------------------|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EDUS[1] | ECC1BC     | ECC Error 1-bit Error Detection and Correction Flag | V => R                                         | 0                           | This bit indicates whether an error was corrected in the data unit.<br><br>Selection Options:<br>1 = Single Bit Error corrected in the addressed data unit<br>0 = No single bit error was corrected in the addressed data unit |
| EDUS[0] | ECCOFF     | Data Unit ECC Off/On Flag                           | V => R                                         | 0                           | This bit indicates whether the ECC syndrome is off in the data unit.<br><br>Selection Options:<br>1 = ECC is OFF in the selected data unit<br>0 = ECC is ON in the selected data unit<br><br>Dependency: CFR4x[3]              |

#### 4.1.1.2      **ECC Status Register (ECSV)**

- An 8-bit ECC Status Register provides the status of 1-bit or 2-bit errors during normal reads since last ECC clear or reset. ECC Status Register does not have user programmable non-volatile bits, all defined bits are volatile read only bits. The default state of these bits are set by hardware.
- ECC Status Register can be accessed through the Read Any Register transaction. The correct sequence for Read Any Register based ECSV is read as follows:
  - Read data from memory array using any of the Read transaction
  - ECSV is updated by the device
  - Read Any Register of ECSV provides the status of any ECC event since the last clear or reset.
- ECSV is cleared by POR, CS# Signaling Reset, Hardware/Software reset, or a Clear ECC Status Register transaction.

#### 4.1.1.3      **ECC Error Address Trap (EATV)**

- A 32-bit register is provided to capture the ECC data unit address where an ECC error is first encountered during a read of the flash array. Only the address of the first enabled error type ("2-bit only" or "1-bit or 2-bit" as selected in CFR4N[3]) encountered after POR, hardware reset, or the ECC Clear transaction is captured. The EATV Register is only updated during Read transactions.

The EATV Register contains the address that was accessed when the error was detected. The failing bits may not be located at the exact address indicated in the register, but will be located within the aligned 16-byte ECC data unit where the error was detected. If errors are found in multiple ECC data units during a single read operation, only the address of the first failing ECC unit address is captured in the EATV Register.

When 2-bit error detection is not enabled and the same ECC unit is programmed more than once, ECC error detection for that ECC unit is disabled, therefore no error can be recognized to trap the address.

The Address Trap Register has a valid address when the ECC Status Register (ECSV) bit 3 or 4 = 1.

- The Address Trap Register can be read using the Read Any Register transaction.
- Clear ECC Status Register transaction, POR, or CS# Signaling/Hardware/Software reset clears the Address Trap Register.

#### **4.1.1.4 ECC Error Detection Counter (ECTV)**

- A 16-bit register is provided to count the number of 1-bit or 2-bit errors that occur as data is read from the flash memory array. Only errors recognized in the main array will cause the Error Detection Counter to increment. ECTV Register is only updated during Read transaction. Read ECC Status transaction does not affect the ECTV Register.

The 16-bit Error Detection Counter will not increment beyond FFFFh. However, the ECC continues to work.

Note that during continuous read operations, when a 1-bit or a 2-bit error is detected, the clock may continue toggling and the memory device will continue incrementing the data address and placing new data on the DQ signals; any additional data units with errors that are encountered will be counted until CS# is brought back HIGH.

During a read transaction only one error is counted for each data unit found with an error. Each read transaction will cause a new read of the target data unit. If multiple read transactions access the same data unit containing an error, the error counter will increment each time that data unit is read.

When 2-bit error detection is not enabled and the same data unit is programmed more than once, ECC error detection for that data unit is disabled so, no error can be recognized or counted.

- The ECC Error Detection Counter Register can be read using the Read Any Register transaction.
- ECTV Register is set to 0 on POR, CS# Signaling/Hardware/Software Reset or with Clear ECC Status Register transaction.

#### **4.1.1.5 INT# Output**

- HL-T/HS-T supports INT# output pin to indicate to the host system that an event has occurred within the flash device. The user can configure the INT# output pin to transition to the active (LOW) state when:
  - 2-bit ECC error is detected
  - 1-bit ECC error is detected
  - Transitioning from the Busy to the Ready state

The INT# pin is only available in BGA package. Operation is controlled with the Interrupt Configuration Register (INCV) where the INT# output (normally HIGH) is enabled. The Interrupt Configuration Register determines when an internal event is enabled to trigger a HIGH to LOW transition on the INT# output pin.

The Interrupt Status Register (INSV) indicates the enabled internal event(s) that have occurred since the last time the INSV was cleared.

If enabled, the INT# output pin will then transition from HIGH to LOW upon the occurrence of an enabled event. Once the host recognizes that INT# has transitioned to the LOW state the INSV Register can be read to determine which internal event was responsible. INT# output status during POR, Hardware Reset, Software Reset, DPD Exit, or CS# Signaling Reset is not valid.

- The INCV and INSV can be accessed through Read Any Register transaction from the SPI and Octal interfaces. Write Any Register transaction to INCV is only supported in the Octal interface.
- The INT# output can be forced to transition back to the HIGH state (returned HIGH by an external pull-up resistance) using the following methods:
  - Disable the INT# output by loading a 1 into bit 7 of the Interrupt Configuration Register.
  - Reset the appropriate bit (by writing a 1) in the INSV bit that indicates which internal event occurred to cause the output to go LOW. All INSV bits that are LOW and are also enabled in the INSV must be reset before the INT# output will return HIGH.
  - The INT# output will also be returned to the default (disabled, High-Z) state with CS# Signaling Reset, Hardware Reset (RESET# = LOW) or a POR. Hardware Reset and POR disable all interrupts by setting the Interrupt Configuration Register back to the default (all interrupts disabled) state.
  - Clearing ECC Status Register after the ECC event forces the INT# output to HIGH state.

#### 4.1.2 ECC related registers and transactions

**Table 16** ECC related registers and transactions

| Related registers                                                           | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|-----------------------------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| Configuration Register - 4 (CFR4N, CFR4V) (see <a href="#">Table 58</a> )   | Read Any Register (RDARG_C_0)                               | Read Any Register (RDARG_4_0)                                 |
| ECC Status Register (ECSV) (see <a href="#">Table 64</a> )                  | Write Enable (WRENB_0_0)                                    | Write Enable (WRENB_0_0)                                      |
| ECC Address Trap Register (EATV) (see <a href="#">Table 65</a> )            | Write Any Register (WRARG_C_1)                              | Write Any Register (WRARG_4_1)                                |
| ECC Error Detection Counter Register (ECTV) (see <a href="#">Table 66</a> ) | Read ECC Status (RDECC_4_0)                                 | Read ECC Status (RDECC_4_0)                                   |
| Interrupt Configuration Register (INCV) (see <a href="#">Table 74</a> )     | Clear ECC Status Register (CLECC_0_0)                       | Clear ECC Status Register (CLECC_0_0)                         |
| Interrupt Status Register (INSV) (see <a href="#">Table 75</a> )            | –                                                           | –                                                             |

#### 4.2 Endurance Flex architecture (wear leveling)

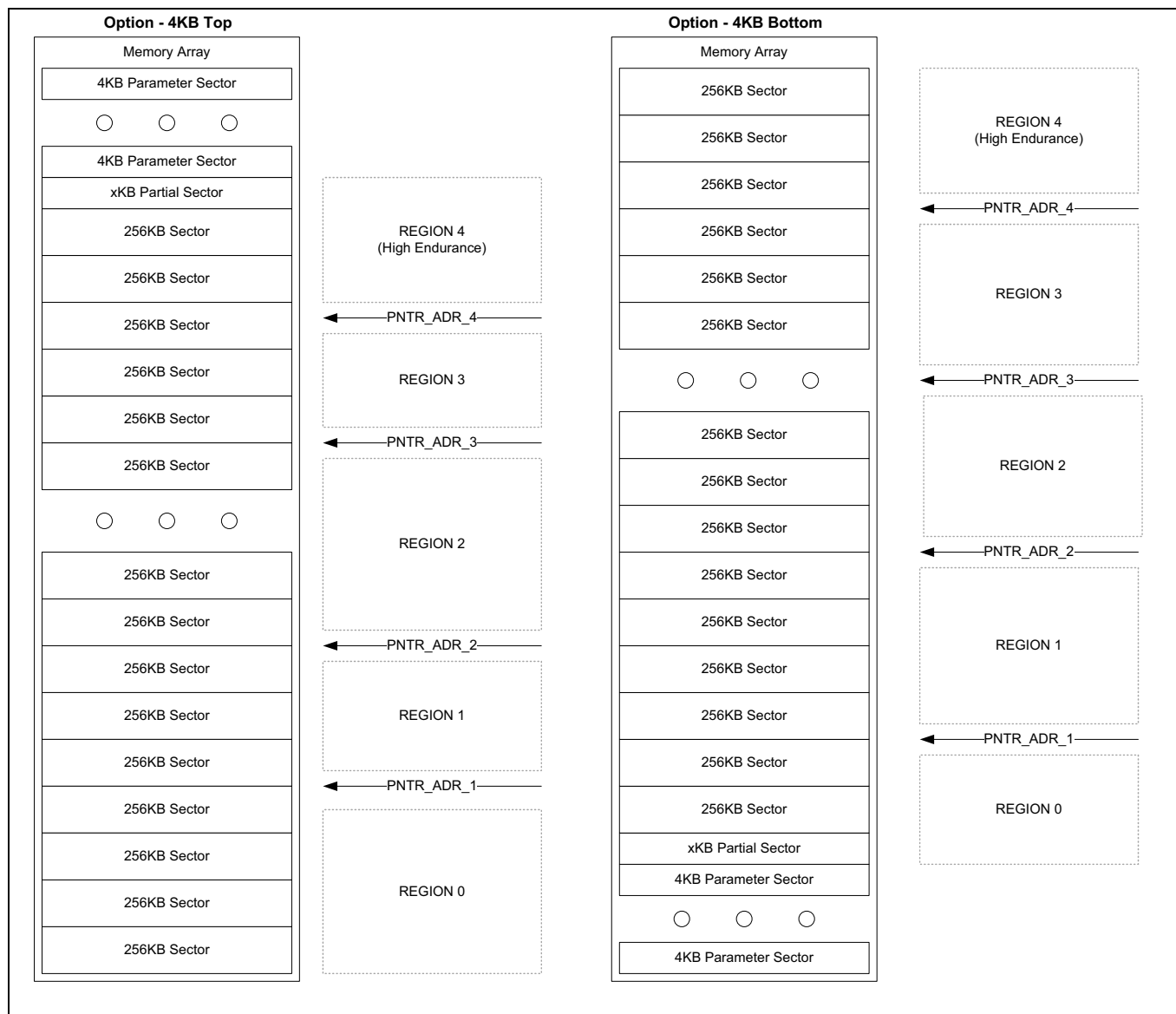
Infineon Endurance Flex architecture allows partitioning of the main memory array into regions which can be configured as either high endurance or long retention. Endurance Flex implements wear leveling in high endurance regions where program/erase cycles are spread evenly across all the sectors which are part of the wear leveling pool. This greatly improves the reliability of the device by avoiding premature wear-out of an individual sector.

Architecturally, Endurance Flex's wear leveling algorithm is based on a mapping of logical sectors to physical sectors. During the lifetime of the part, this mapping is changed to maintain a uniform distribution of program/erase cycles over all physical sectors. The logical to physical mapping information is stored in a dedicated flash array which is updated when sectors are swapped. Sector swaps occur when an erase transaction is given.

Endurance Flex's high endurance region requires a minimum set of 20 sectors. To provide flexibility between configuring long retention, high endurance, or both regions, a four pointer architecture is provided. The factory default setting designates all sectors as high endurance as part of the wear leveling pool with all pointers disabled. The four pointers can be used to form a maximum of five regions which can each be configured as long retention or high endurance.

**Figure 34** provides an overview of the Endurance Flex architecture. It shows the five possible regions based on different sector architecture.

**Note** 4KB sectors are not part of the Endurance Flex architecture.



**Figure 34**      **Endurance Flex architecture overview**

Features

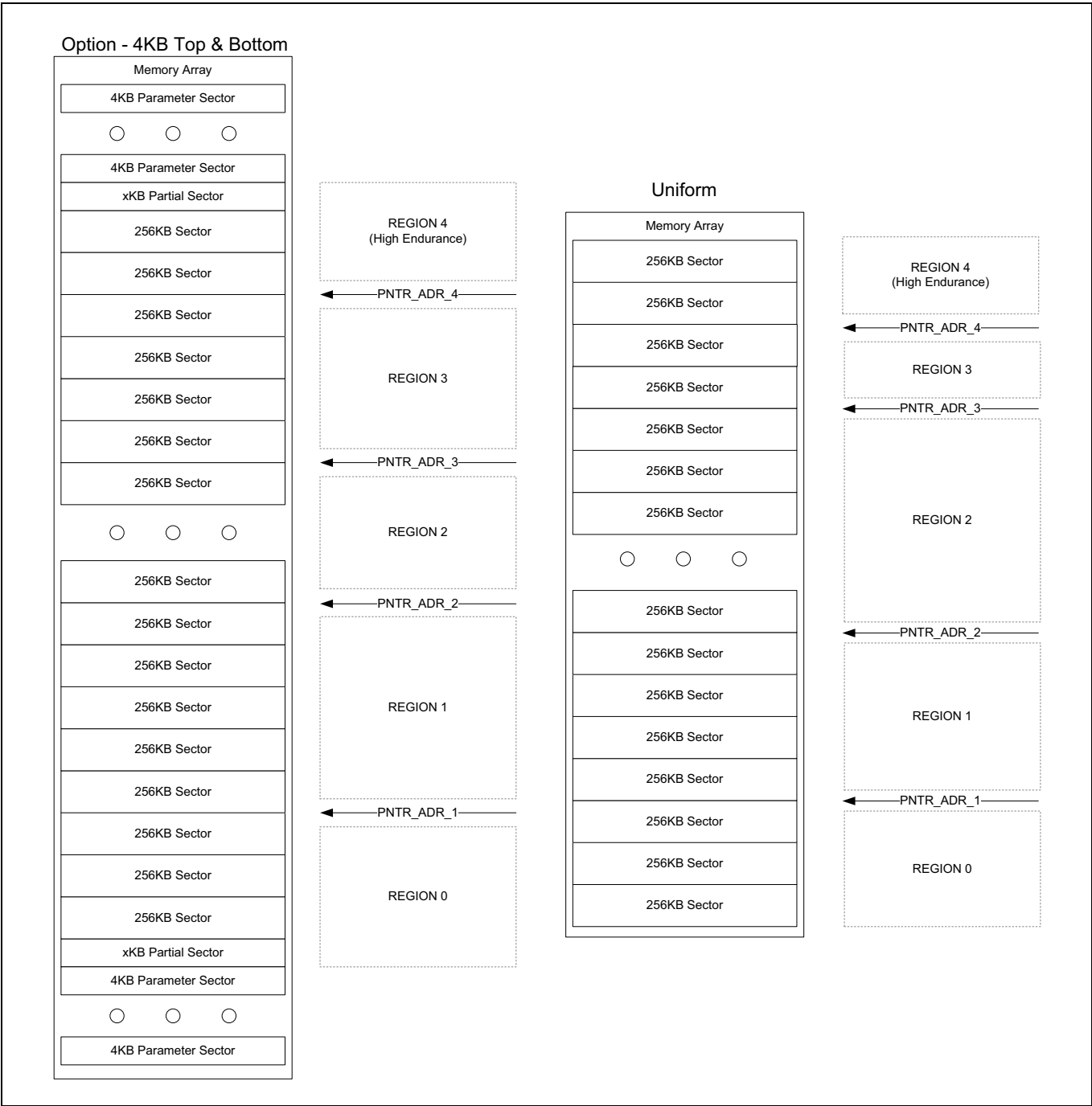


Figure 35 Endurance Flex architecture overview (Continued)

**Table 17**      **Region definitions**<sup>[11, 12, 13, 14]</sup>

| Region | Lower limit       | Upper limit       |
|--------|-------------------|-------------------|
| 0      | Sector 0          | Address Pointer 1 |
| 1      | Address Pointer 1 | Address Pointer 2 |
| 2      | Address Pointer 2 | Address Pointer 3 |
| 3      | Address Pointer 3 | Address Pointer 4 |
| 4      | Address Pointer 4 | Highest Sector    |

**Notes**

11. The pointer addresses must obey the following rules:

- Pointer#4 address > Pointer#3 address
- Pointer#3 address > Pointer#2 address
- Pointer#2 address > Pointer#1 address

12. 4KB sectors are excluded.

13. It is required that the high data endurance and long data retention regions are configured at the time the device is first powered-up by the customer. Once configured, they can never be changed again.

14. The minimum size of any high endurance region is 20 sectors.

#### 4.2.1 Configuration 1: Maximum endurance - single high endurance region

Maximum endurance is achieved when all 256KB sectors are designated as high endurance. All sectors must be designated as high endurance using the Endurance Flex pointer architecture. Maximum endurance pointer configuration is shown in [Table 18](#).

**Table 18**      **Endurance Flex pointer values for maximum endurance configuration**<sup>[15]</sup>

| Pointer # | Pointer address<br>EPTADn[8:0] | Region type<br>ERGNTn | Pointer enable#<br>EPTEBn | Global region selection<br>GBLSEL | Wear leveling enable<br>WRLVEN |
|-----------|--------------------------------|-----------------------|---------------------------|-----------------------------------|--------------------------------|
| 0         | N/A                            | N/A                   | N/A                       | 1'b1                              | 1'b1                           |
| 1         | 9'b11111111                    | 1'b1                  | 1'b1                      | N/A                               | N/A                            |
| 2         | 9'b11111111                    |                       |                           |                                   |                                |
| 3         | 9'b11111111                    |                       |                           |                                   |                                |
| 4         | 9'b11111111                    |                       |                           |                                   |                                |

**Note**

15. This is also the default configuration of the device.

#### 4.2.2 Configuration 2: Two region selection - one long retention region and one high endurance region

Sectors for long retention or high endurance must be delineated using the Endurance Flex pointer architecture. Region 0 is defined as long retention and consists of 16 sectors. Region 1 is defined as high endurance and has 240 sectors. The pointer setup for two region configuration is shown in [Table 19](#). The number of pointers defined is based on the number of regions configured.

**Table 19**      **Endurance Flex pointer values for two region configuration**

| Pointer # | Pointer address<br>EPTADn[8:0] | Region type<br>ERGNTn | Pointer enable#<br>EPTEBn | Global region selection<br>GBLSEL | Wear leveling enable<br>WRLVEN |
|-----------|--------------------------------|-----------------------|---------------------------|-----------------------------------|--------------------------------|
| 0         | N/A                            | N/A                   | N/A                       | 1'b0                              | 1'b1                           |
| 1         | 9'b000010000                   | 1'b1                  | 1'b0                      | N/A                               | N/A                            |
| 2         | 9'b111111111                   | 1'b1                  | 1'b1                      |                                   |                                |
| 3         |                                |                       |                           |                                   |                                |
| 4         |                                |                       |                           |                                   |                                |

### 4.2.3 Endurance Flex related registers and transaction

**Table 20** Endurance Flex related registers and transactions

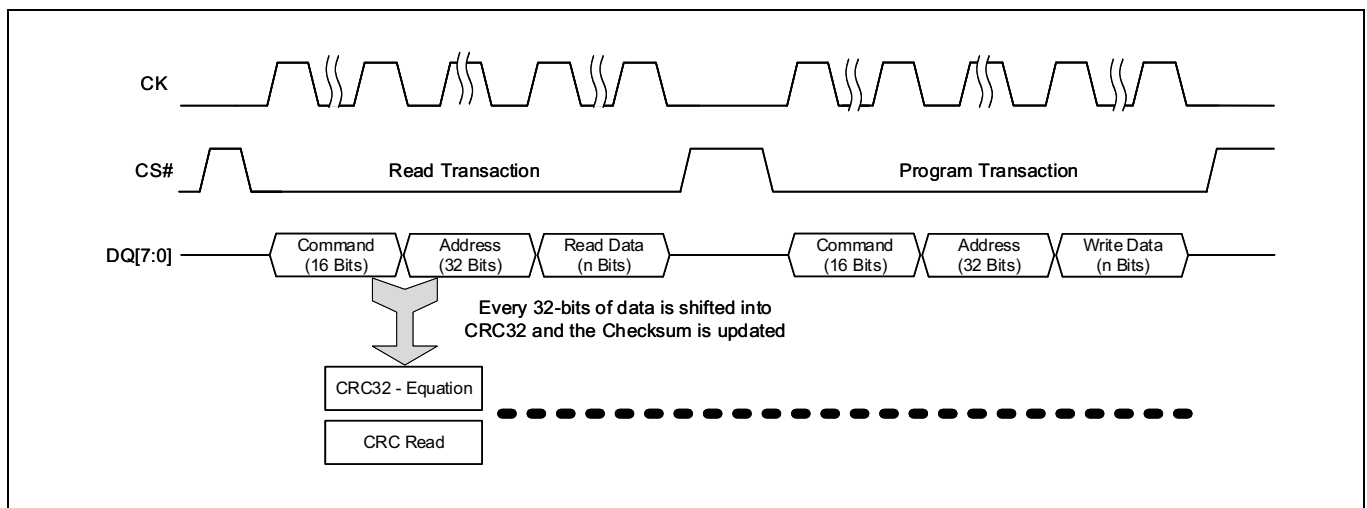
| Related registers                                                                                                                                                                               | Related SPI transactions<br>(see Table 81) | Related octal transactions<br>(see Table 82) |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|----------------------------------------------|
| Endurance Flex architecture<br>Selection Registers (EFX40, EFX30,<br>EFX20, EFX10, EFX00) (see<br>“ <a href="#">Endurance Flex Architecture<br/>Selection Register (EFXx)</a> ” on<br>page 116) | Read Any Register (RDARG_C_0)              | Read Any Register (RDARG_4_0)                |
|                                                                                                                                                                                                 | Write Any Register (WRARG_C_1)             | Write Any Register (WRARG_4_1)               |

### 4.3 Interface CRC

Interface CRC performs a hardware accelerated CRC calculation on the communication between a host and the device, ensuring the integrity of information transferred. A CRC is an error-detecting code commonly used in devices to detect accidental changes to raw data. Interface CRC protection is a configuration option (ICEV[0] - ITCRCE).

The Interface CRC method in HL-T/HS-T family devices relies entirely on the host to verify the CRC check-value and take appropriate actions. The device calculates the CRC check-value which the host reads using the Read Interface CRC transaction (RDCRC\_4\_0). The check-value calculated includes all transaction contents while CS# is LOW, namely command, address and data. This CRC checksum can be generated across either a single transaction or a set of transactions. The only limitation is that the data size over which the slave is calculating the CRC checksum must be less than  $2^{32}$  bits.

The host must also calculate the CRC check-value over the same transaction sequence. When ready, the host can read the device’s calculated CRC check-value and compare it with its own. If there is a mismatch, the host can choose to repeat the complete transaction sequence.



**Figure 36** CRC calculation overview

#### Notes

- At the end of the CRC read transaction, the device resets the CRC check-value and reinitializes the CRC polynomial.
  - CRC32 Polynomial:  $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
- The CRC polynomial between the host and the device must be identical.
- Interface CRC is supported with Octal DDR protocol only.

## Features

- The Interface CRC check-value will reset to 0xFFFFFFFFh under the following conditions:
  - POR
  - Hardware reset
  - Software reset
  - CS# signaling reset
  - A read of the Interface CRC check-value
- Exit from deep power down

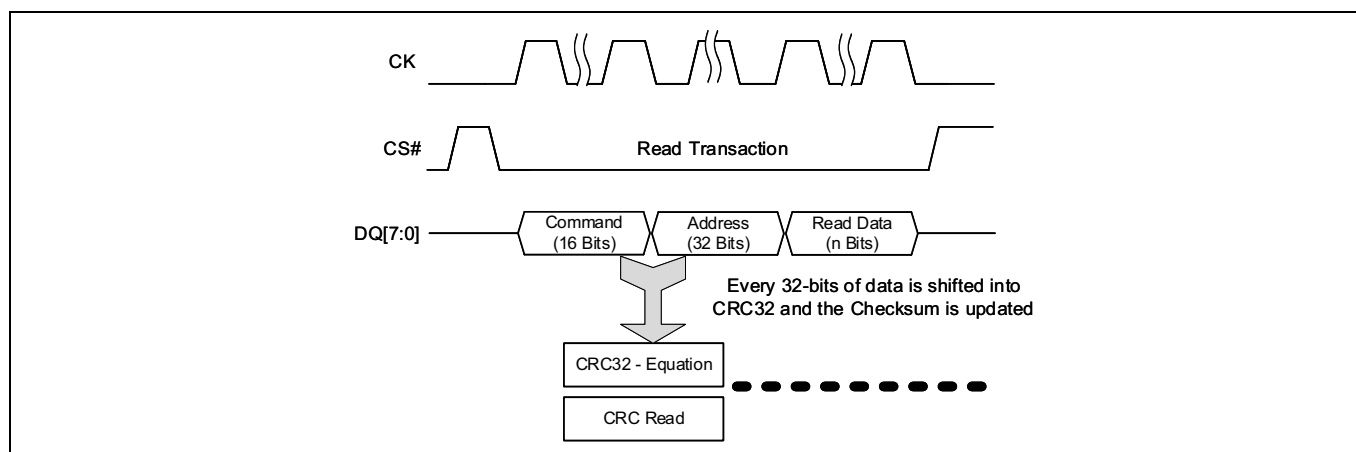
## Notes

- If a transaction is aborted before the command is legally received, i.e. the transfer length is cut short by CS# de-asserting early - the transferred data will still be clocked into the CRC check-value, but it is no longer guaranteed. When using Interface CRC, only valid, non-aborted transactions must be used.
- It is required to read Interface CRC value before any Volatile Status Register read and Clear Interface CRC value after any Volatile Status Register read(s).
- When Interface CRC is disabled, the interface CRC register value becomes indeterminate. It is recommended to read the interface CRC register before disabling the interface CRC feature, and again after enabling the interface CRC feature to re-initialize the CRC calculation.

### 4.3.1 Read

The read operation is performed when the host specifies the READ transaction while CS# is LOW. The device then provides the data from the memory based on the address. Any number of bytes can be read (burst reads) to consecutive addresses without issuing a new READ transaction.

For transaction protection, the device performs the CRC over the entire transaction sequence (CS# LOW state) using the CRC32 polynomial. Once the CS# is brought HIGH, the CRC calculation is stopped and the check-value latched into the CRC Register. If multiple READ transactions are executed by the host, the device continues updating the CRC check-value between every CS# LOW cycle.



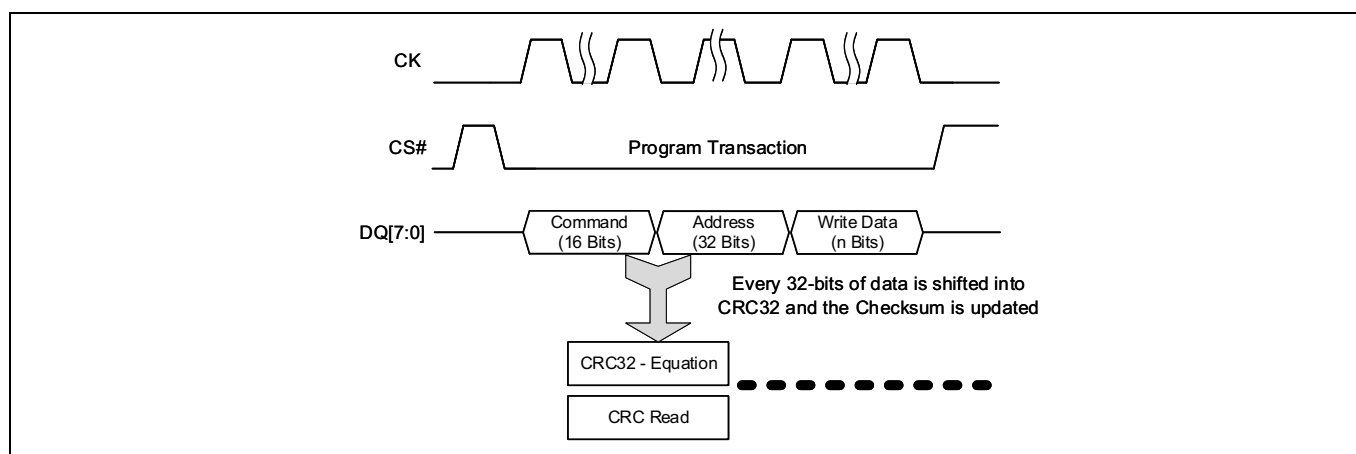
**Figure 37** Read CRC protection

**Note** Back to back Interface CRC read transaction will not show the CRC checksum value being reset. At the end of each read interface CRC register transaction, the interface CRC register will get reset and updates itself with new CRC checksum value after getting a transaction with valid input data for at least three clock cycles.

### 4.3.2 Program / erase

The program operation is performed when the host specifies a program transaction while CS# is LOW. Up to 256 bytes / 512 bytes can be written (burst writes) to consecutive addresses without issuing a new program transaction. The erase operation is performed when the host specifies an erase transaction while CS# is LOW. Either a single sector or the complete device can be erased.

For transaction protection, the slave device will perform the CRC over the entire instruction sequence (CS# LOW state) using the proposed CRC32 polynomial. Once the CS# is brought HIGH to complete the Program / Erase transaction, the CRC calculation will be stopped and the checksum latched into the CRC Register. If multiple Program / Erase transactions are executed by the host, the slave will continue updating the CRC checksum between every CS# LOW cycle.



**Figure 38 Program CRC protection**

The host device will read the CRC checksum from the slave device using the Read Interface CRC transaction. The slave device will include the RDCRC\_4\_0 transaction as part of the CRC checksum and then place the checksum data on the data bus. If the host device upon receiving the slave's CRC checksum finds a mismatch with its own calculated CRC checksum, it can re-issue the Program / Erase transaction to the slave device. For Flash, multiple Program / Erase to the same location due to CRC checksum errors will affect data endurance. [Figure 39](#) shows the solution to this issue.

Features

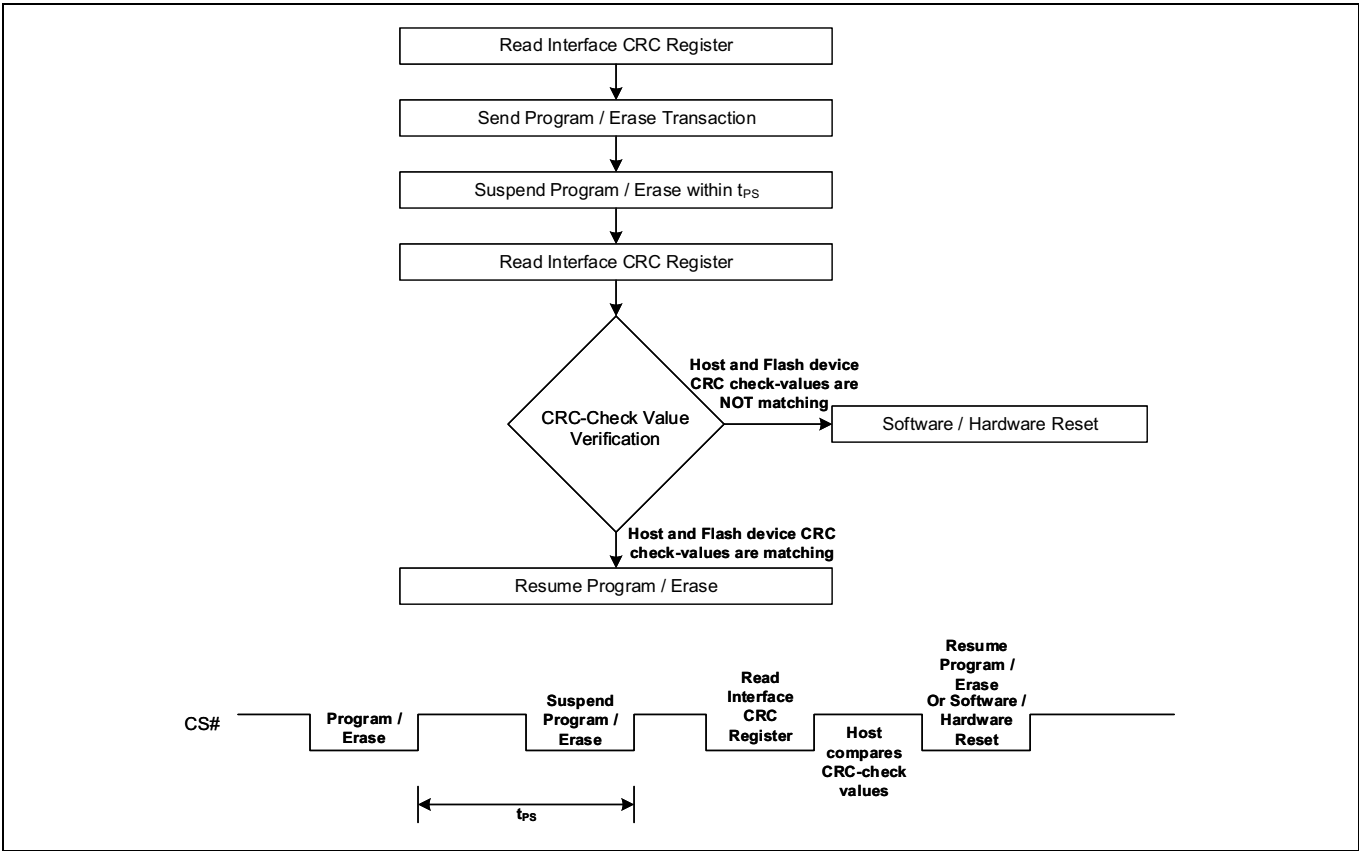


Figure 39 Interface CRC flow for program and erase transactions

### 4.3.3 Interface CRC related registers and transaction

Table 21 Interface CRC related registers and transactions

| Related registers                                      | Related SPI transactions<br>(see Table 81) | Related octal transactions<br>(see Table 82) |
|--------------------------------------------------------|--------------------------------------------|----------------------------------------------|
| Interface CRC Enable Register (ICEV)<br>(see Table 61) | N/A                                        | Read Interface CRC Register<br>(RDCRC_4_0)   |

## 4.4 Data integrity CRC

HL-T/HS-T family devices have a group of transactions to perform a hardware accelerated CRC calculation over a user defined address range in the memory array. The calculation is another type of embedded operation similar to programming or erase in which the device is busy while the calculation is in progress. The CRC operation uses the same CRC32 polynomial as Interface CRC to determine the CRC check-value.

CRC32 Polynomial:  $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$

The check-value generation sequence is started by entering the DICHK\_4\_1 transaction. The transaction includes loading the beginning address into the CRC Start Address Register and identifying the beginning of the address range that will be covered by the CRC calculation. The transaction also includes loading the ending address into the CRC End Address Register. Bringing CS# HIGH starts the CRC calculation. The CRC process calculates the check-value on the data contained at the starting address through the ending address.

During the calculation period the device goes into the Busy state (STR1V[0] - RDYBSY = 1). Once the check-value calculation is completed, the device returns to the Ready state (STR1V[0] - RDYBSY = 0) and the calculated check-value is available to be read. The check-value is stored in the Data Integrity CRC Register (DCRV[31:0]) and can be read using Read Any Register transaction.

The check-value calculation can only be initiated when the device is in Standby State; and once started it can be suspended with the CRC Suspend transaction (SPEPD\_0\_0) to read data from the memory array. During the Suspended state the CRC Suspend Status Bit in the Status Register 2 will be set (STR2V[4] - DICRCS = 1). Once suspended, the host can read the Status Register, read data from the array and can resume the CRC calculation by using the CRC Resume transaction RSEPD\_0\_0.

The Ending Address (ENDADD) must be at least 4 bytes higher than the Starting Address (STRADD). If  $ENDADD < STRADD + 3$ , the check-value calculation will abort and the device will return to the Ready state (STR1V[0] - RDYBSY = 0). Data Integrity CRC abort status bit will be set (STR2V[3] - DICRCA = 1) to indicate the aborted condition. The DICRCA bit can be cleared, once set, by Software reset or a valid subsequent CRC command execution. If  $ENDADD < STRADD + 3$ , the check-value will hold indeterminate data.

**Note** Any invalid transaction during CRC check-value calculation can corrupt the check-value data.

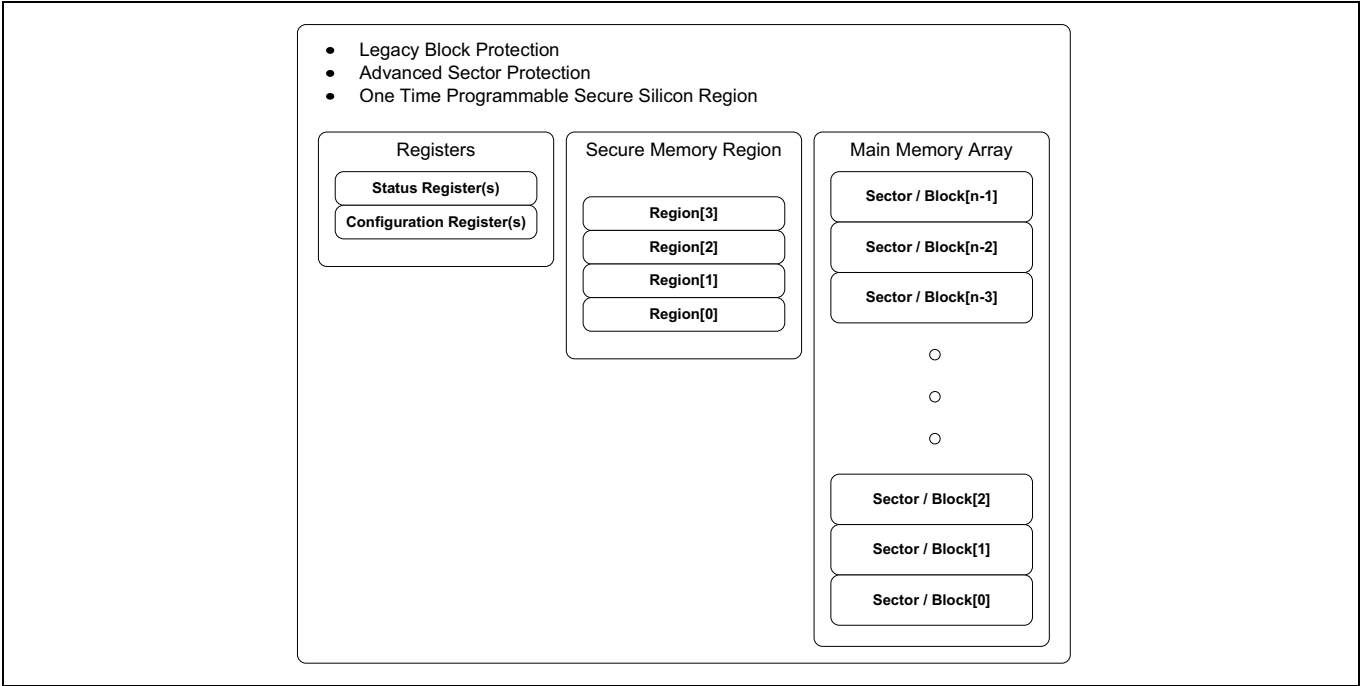
### 4.4.1 Data integrity check related registers and transactions

**Table 22 Data integrity CRC related registers and transactions**

| Related registers                                                   | Related SPI transactions<br>(see Table 81)                | Related octal transactions<br>(see Table 82)              |
|---------------------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|
| Status Register 1 (STR1N, STR1V)<br>(see Table 47)                  | Data Integrity Check (DICHK_4_1)                          | Data Integrity Check (DICHK_4_1)                          |
| Status Register 2 (STR2V)<br>(see Table 50)                         | Suspend Erase/Program/Data<br>Integrity Check (SPEPD_0_0) | Suspend Erase/Program/Data<br>Integrity Check (SPEPD_0_0) |
| Data Integrity CRC Check-Value<br>Register (DCRV)<br>(see Table 63) | Resume Erase/Program/ Data<br>Integrity Check (RSEPD_0_0) | Resume Erase/Program/ Data<br>Integrity Check (RSEPD_0_0) |

#### 4.5 Data protection schemes

Data protection is required to safeguard against unintended changes to stored data and device configuration. This includes inadvertent erasing or programming the memory array as well as writing to the configuration registers, which can alter the functionality of the device. Three types of protection schemes are discussed which range from protecting either a single or a group of sectors to either a portion or the complete memory array. **Figure 40** shows an overview of different protection schemes along with applicable data regions.



**Figure 40** Data protection and security (write/program/erase) schemes

#### 4.5.1 Legacy block protection (LBP)

The Legacy Block Protection (LBP), is a block based data protection scheme. LBP supports compatibility with legacy serial NOR flash devices. LBP provides protection for data in the memory array and device configuration by protecting Status and Configuration registers.

##### 4.5.1.1 Memory array protection

The protection for the memory array is with block size selection which is achieved through a combination of bits present in the Status Register 1 (STR1N[4:2]/STR1V[4:2] - LBPROT[2:0]) and Configuration Register 1 (CFR1N[5]/CFR1V[5] - TBPROT). [Table 23](#) provides the LBP memory array block selection summary.

**Table 23 Legacy block memory array protection selection**

| CFR1N[5]/<br>CFR1V[5]<br>TBPROT | STR1N[4]/<br>STR1V[4]<br>LBPROT[2] | STR1N[3]/<br>STR1V[3]<br>LBPROT[1] | STR1N[2]/<br>STR1V[2]<br>LBPROT[0] | Memory array<br>block size | 512 Mb (KBs) | 1 Mb (KBs) |
|---------------------------------|------------------------------------|------------------------------------|------------------------------------|----------------------------|--------------|------------|
| 0                               | 0                                  | 0                                  | 0                                  | None                       | 0            | 0          |
| 0                               | 0                                  | 0                                  | 1                                  | Upper 64th                 | 1024         | 2048       |
| 0                               | 0                                  | 1                                  | 0                                  | Upper 32nd                 | 2048         | 4096       |
| 0                               | 0                                  | 1                                  | 1                                  | Upper 16th                 | 4096         | 8192       |
| 0                               | 1                                  | 0                                  | 0                                  | Upper 8th                  | 8192         | 16384      |
| 0                               | 1                                  | 0                                  | 1                                  | Upper 4th                  | 16384        | 32768      |
| 0                               | 1                                  | 1                                  | 0                                  | Upper Half                 | 32768        | 65536      |
| 0                               | 1                                  | 1                                  | 1                                  | All sectors                | 65536        | 131072     |
| 1                               | 0                                  | 0                                  | 0                                  | None                       | 0            | 0          |
| 1                               | 0                                  | 0                                  | 1                                  | Lower 64th                 | 1024         | 2048       |
| 1                               | 0                                  | 1                                  | 0                                  | Lower 32nd                 | 2048         | 4096       |
| 1                               | 0                                  | 1                                  | 1                                  | Lower 16th                 | 4096         | 8192       |
| 1                               | 1                                  | 0                                  | 0                                  | Lower 8th                  | 8192         | 16384      |
| 1                               | 1                                  | 0                                  | 1                                  | Lower 4th                  | 16384        | 32768      |
| 1                               | 1                                  | 1                                  | 0                                  | Lower Half                 | 32768        | 65536      |
| 1                               | 1                                  | 1                                  | 1                                  | All sectors                | 65536        | 131072     |

#### 4.5.1.2 Configuration protection

LBP has selection bits in Configuration Register 1 (CFR1N[4,0]/CFR1V[4,0] - PLPROT, TLPROT), which either permanently or temporarily protect Status and Configuration registers, thereby again protecting the device's configuration. The temporary protection remains in effect until the next power down or hardware reset or CS# signaling reset.

**Table 24** Option 2 - Legacy block configuration protection selection<sup>[16]</sup>

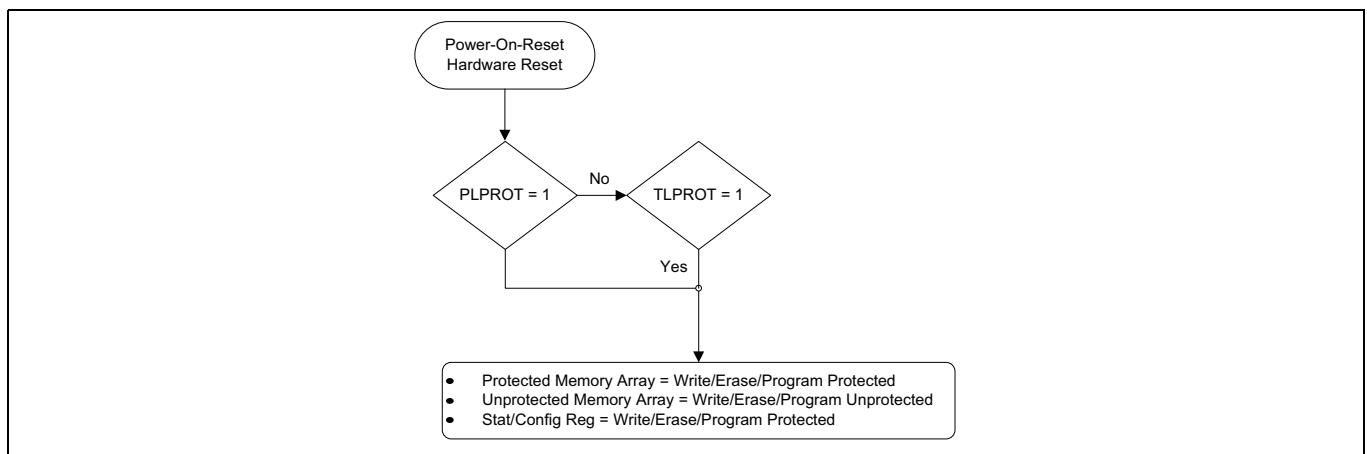
| CFR1N[4] /<br>CFR1V[4]<br>PLPROT | CFR1N[0] /<br>CFR1V[0]<br>TLPROT | Register protection status                                                                                  |
|----------------------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------|
| 0                                | 0                                | Status and Configuration registers are unprotected                                                          |
| 1                                | X                                | Status and Configuration registers are permanently protected (TBPROT, LBPROT[2:0], SP4KBS, TB4KBS)          |
| 0                                | 1                                | Status and Configuration registers are Protected till next Power down (TBPROT, LBPROT[2:0], SP4KBS, TB4KBS) |

**Note**

16. Protecting the configuration also protects the memory array blocks which have been selected for protection.

#### 4.5.1.3 Legacy block protection flowchart

The LBP protection scheme flowchart is shown in [Figure 41](#).



**Figure 41** Legacy block protection flowchart

#### 4.5.1.4 LBP related registers and transactions

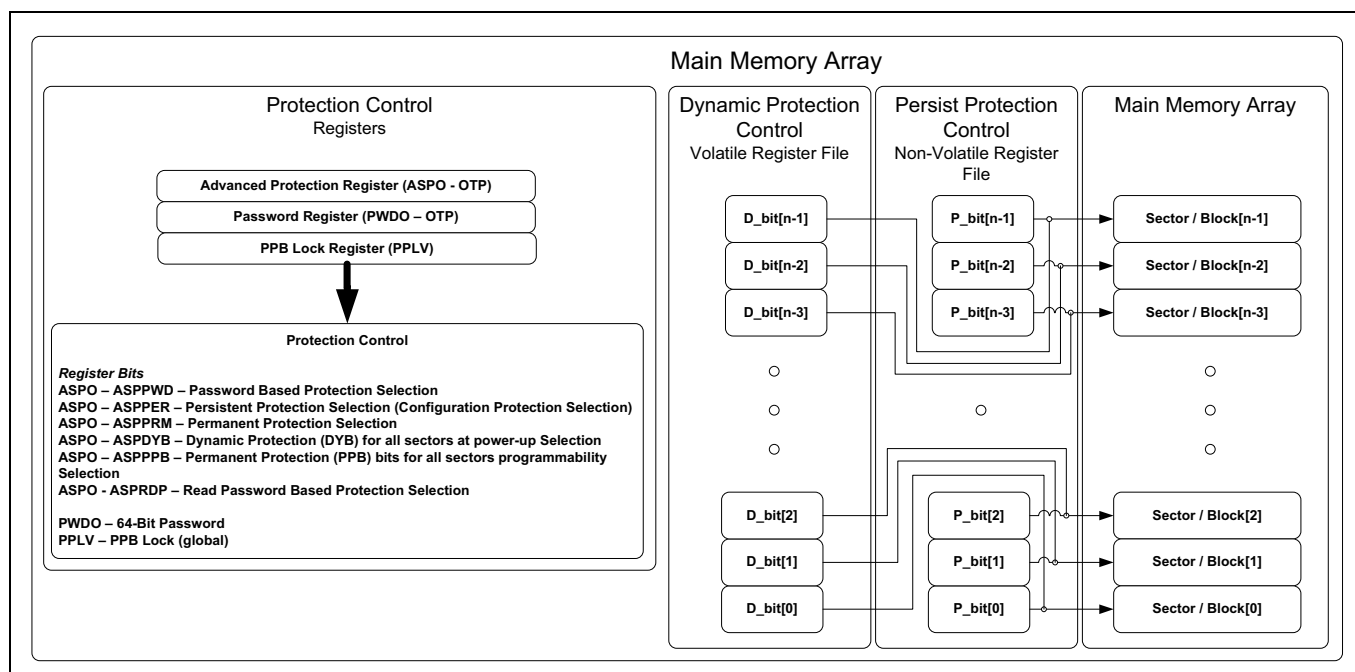
**Table 25** LBP related registers and transactions

| Related registers                                                          | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|----------------------------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| Status Register 1 (STR1N, STR1V)<br>(see <a href="#">Table 47</a> )        | Read Any Register (RDARG_C_0)                               | Read Any Register (RDARG_4_0)                                 |
| Configuration Register 1 (CFR1N, CFR1V)<br>(see <a href="#">Table 51</a> ) | Write Any Register (WRARG_C_1)                              | Write Any Register (WRARG_4_1)                                |
|                                                                            | Read Status Register 1 (RDSR1_0_0)                          | Read Status Register 1 (RDSR1_4_0)                            |
|                                                                            | Write Enable (WRENB_0_0)                                    | Write Enable (WRENB_0_0)                                      |

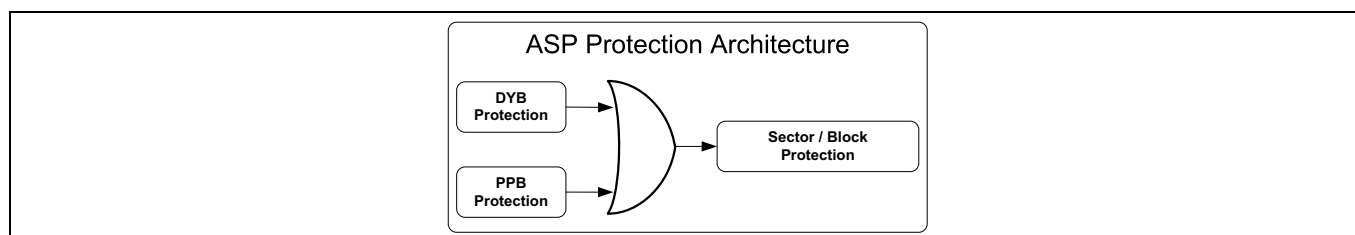
## 4.5.2 Advanced sector protection (ASP)

The advanced sector protection scheme allows each memory array sector to be independently controlled for protection against erasing or programming, either by volatile or non-volatile locking features. The non-volatile locking configuration can also be locked, as well as password-protected.

The main memory array sectors are protected against erase and program by volatile (DYB) and non-volatile (PPB) protection bit pairs. Each DYB/PPB bit pair can be individually set to '0' protecting the related sector or cleared to '1' unprotecting the related sector. DYB protection bits can be set and cleared as often as needed whereas PPB bits being non-volatile must adhere to their respective technology based endurance requirements. **Figure 42** shows an overview of ASP.



**Figure 42** Advanced sector protection (Non-volatile)



**Figure 43** DYB and PPB protection control

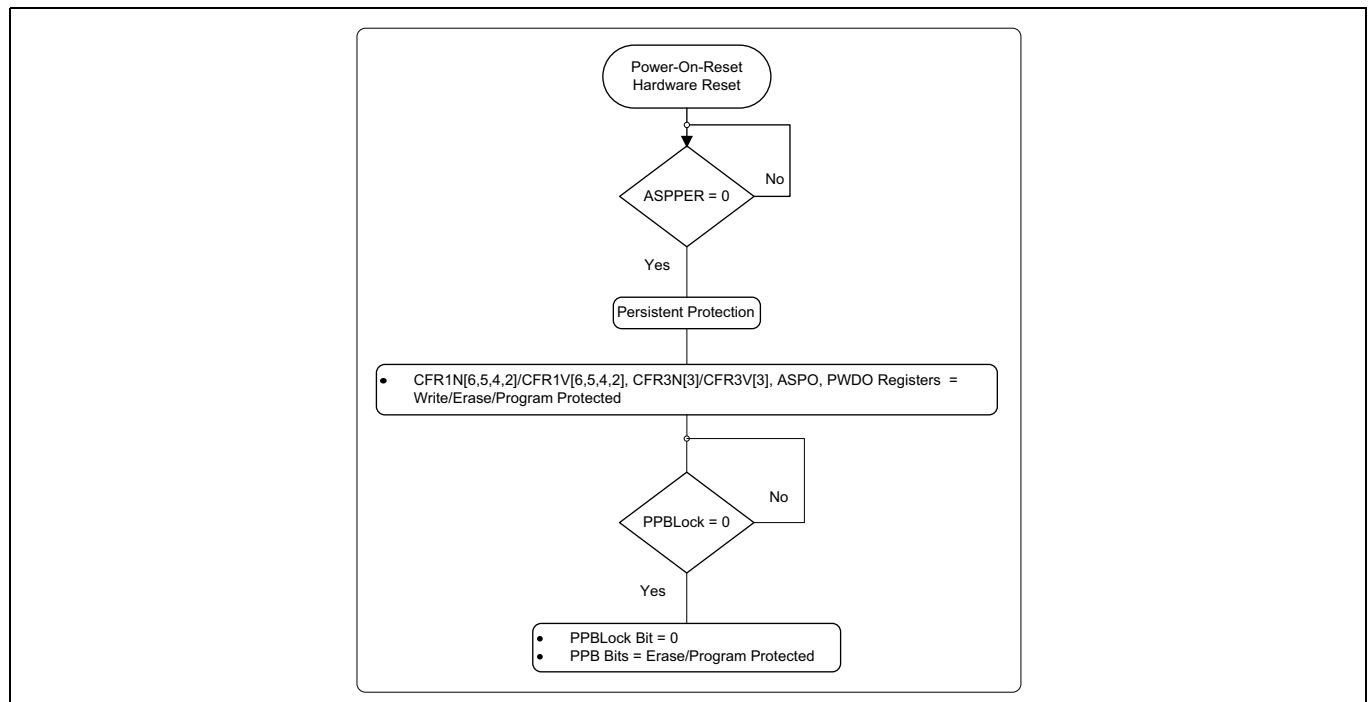
ASP provides a rich set of configuration options producing multiple data protection schemes which can be employed based on design or system needs. These configuration options are discussed in **“Configuration protection”** on page 47 through **“ASP related registers and transactions”** on page 52.

#### 4.5.2.1 Configuration protection

ASP provides provisions to protect device's configuration through persistent protection scheme. Selecting bit 1 in Advanced Sector Protection Register (ASPO[1] - ASPPER) selects the Persistent Protection scheme and protects the following registers or register bits from write or program.

- CFR1V[6,5,4,2]/CFR1N[6,5,4,2] - SP4KBS, TBPROT, PLPROT, TB4KBS
- CFR3N[3]/CFR3V[3] - UNHYSA
- ASPO[15:0]
- PWDO[63:0]

The persistent protection scheme flowchart is shown in **Figure 44**.

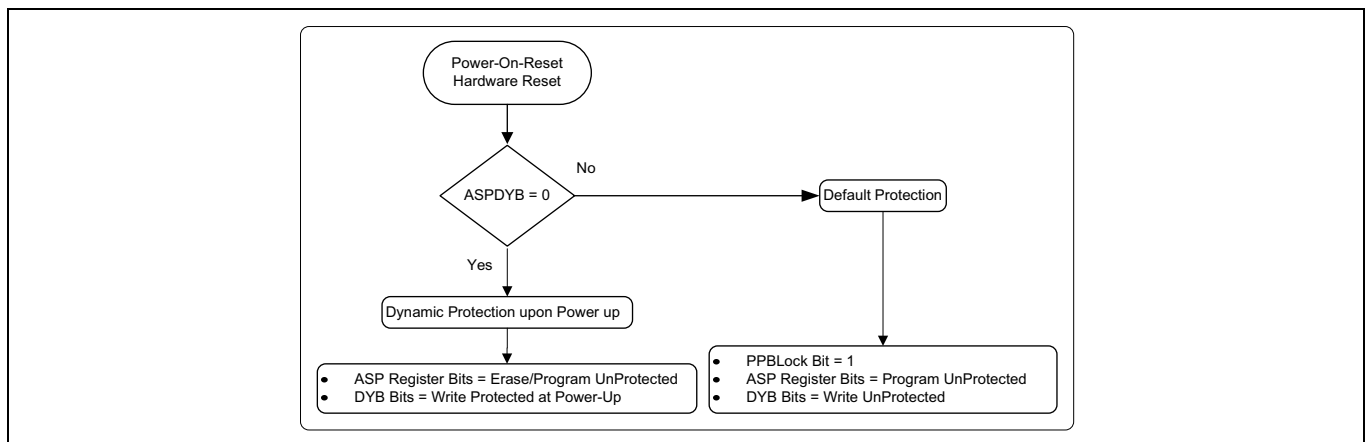


**Figure 44** Persistent protection scheme flowchart

#### 4.5.2.2 Dynamic DYB (volatile) sector protection

Dynamic protection bits (DYB) are volatile and unique for each sector and can be individually modified. DYBs only control protection for sectors that have their PPBs cleared. By issuing the DYB Write transaction, the DYB are set to 0 or cleared to 1, thus placing each sector in the protected or unprotected state respectively. This feature allows software to easily protect sectors against inadvertent changes, yet does not prevent the easy removal of protection when changes are needed. The DYB can be set to '0' or cleared to '1' as often as needed.

In dynamic sector protection scheme, an option is provided to reset all DYB volatile protection bits to '0' upon power up (protected), essentially protecting all sectors from erase or program. Selecting bit 4 in the Advanced Sector Protection Register (ASPO[4] - ASPDYB) selects the dynamic protection (DYB) for all sectors at power-up protection scheme. These DYB bits can be individually set to '1', if desired. The Dynamic Sector Protection scheme flowchart showing power up protection is shown in **Figure 45**.



**Figure 45** Dynamic sector protection scheme flowchart

#### 4.5.2.3 Permanent/temporary PPB (non-volatile) sector protection

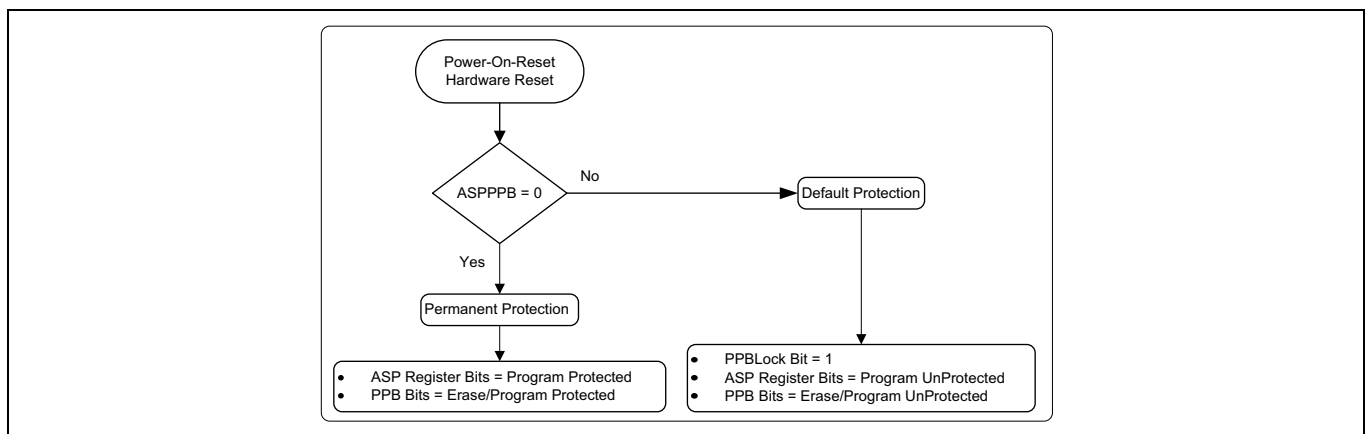
Each non-volatile bit (PPB) provides non-volatile protection for an individual memory sector, which remains locked (protection enabled) until its corresponding bit is cleared to 1. There are two options to control the PPB based non-volatile selection in ASP, namely permanent and temporary.

#### 4.5.2.4 Permanent PPB protection scheme

The PPB are located in a separate non-volatile flash array. One of the PPB bits is assigned to each sector. When a PPB is programmed to 0 its related sector is protected from program and erase operations. The PPB are programmed individually but must be erased as a group, similar to the way individual words may be programmed in the main array but an entire PPB sector must be erased at the same time. Programming a PPB bit requires the typical word programming time. During a PPB bit programming operation or PPB bit erasing, the Status Register can be accessed to determine when the operation has completed. Erasing all the PPBs requires typical sector erase time.

Permanent PPB based protection scheme, as the name applies, is permanent and can never be altered. Once the PPB architecture is decided, selecting bit 0 in Advanced Sector Protection Register (ASPO[0]) enables the Permanent Protection for all PPB bits essentially disabling all PPB erase and program operations. ASPO is also protected from write or program.

The Permanent PPB Protection scheme flowchart is shown in [Figure 46](#).



**Figure 46** Permanent PPB sector protection flowchart

#### 4.5.2.5 Temporary PPB protection scheme

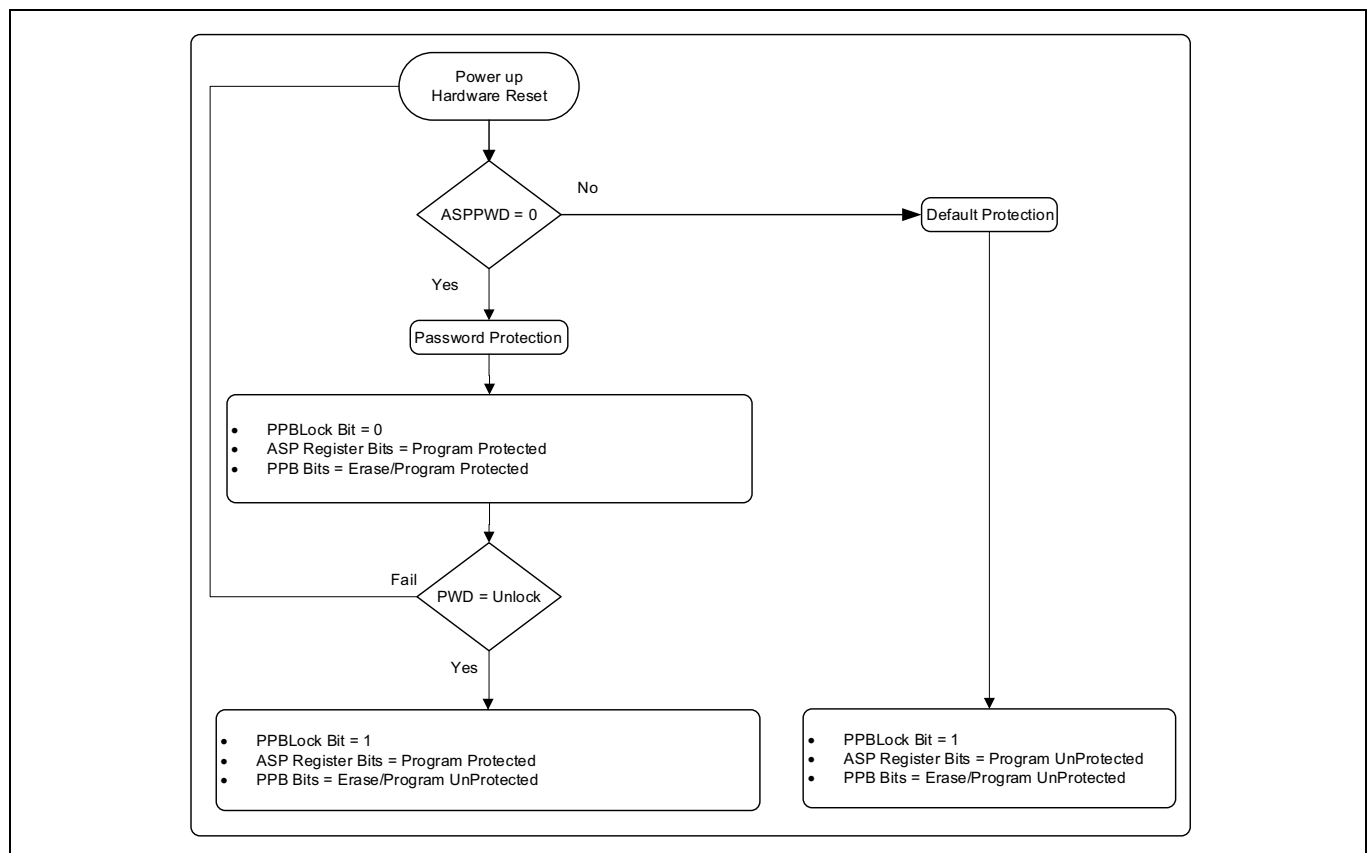
PPB based non-volatile protection architecture can be temporarily locked where erasing and programming of the individual PPB bits is inhibited. The Persistent Protection Lock Bit (PPBLock) is a volatile bit for protecting all PPB bits. When cleared to 0, it locks all PPBs and when set to 1, it allows the PPBs to be changed. There is only one PPB Lock Bit per device. The PPBLock transaction (WRPLB\_0\_0) is used to clear the bit to 0. The PPB Lock Bit must be cleared to 0 only after all the PPBs are configured to the desired settings. The PPB Lock Bit is set to 1 during POR or a hardware reset. When cleared with the PPBLock transaction, no software command sequence can set PPBLock, only another hardware reset or Power-Up can set PPBLock.

**Note** Temporary PPB protection does not require any ASP configuration.

#### 4.5.2.6 Password protection scheme

Password protection scheme allows an even higher level of security by requiring a 64-bit password for setting PPB Lock. In addition to this password requirement, after power-up or hardware reset, the PPB Lock Bit is cleared to 0 to ensure protection at Power-Up. Successful execution of the Password Unlock command by entering the entire password sets the PPB Lock Bit to 1, allowing for sector PPB modifications. Selecting bit 2 in Advanced Sector Protection Register (ASPO[2] - ASPPWD) selects the password protection scheme. Password protection scheme also protects ASPO from write or program.

**Note** A password must be programmed before selecting the password protection scheme. The password unlock SPI transaction (PWDUL\_0\_1) or Octal transaction (PWDUL\_4\_1) is used to provide a password for comparison. The password protection scheme flowchart is shown in **Figure 47**.

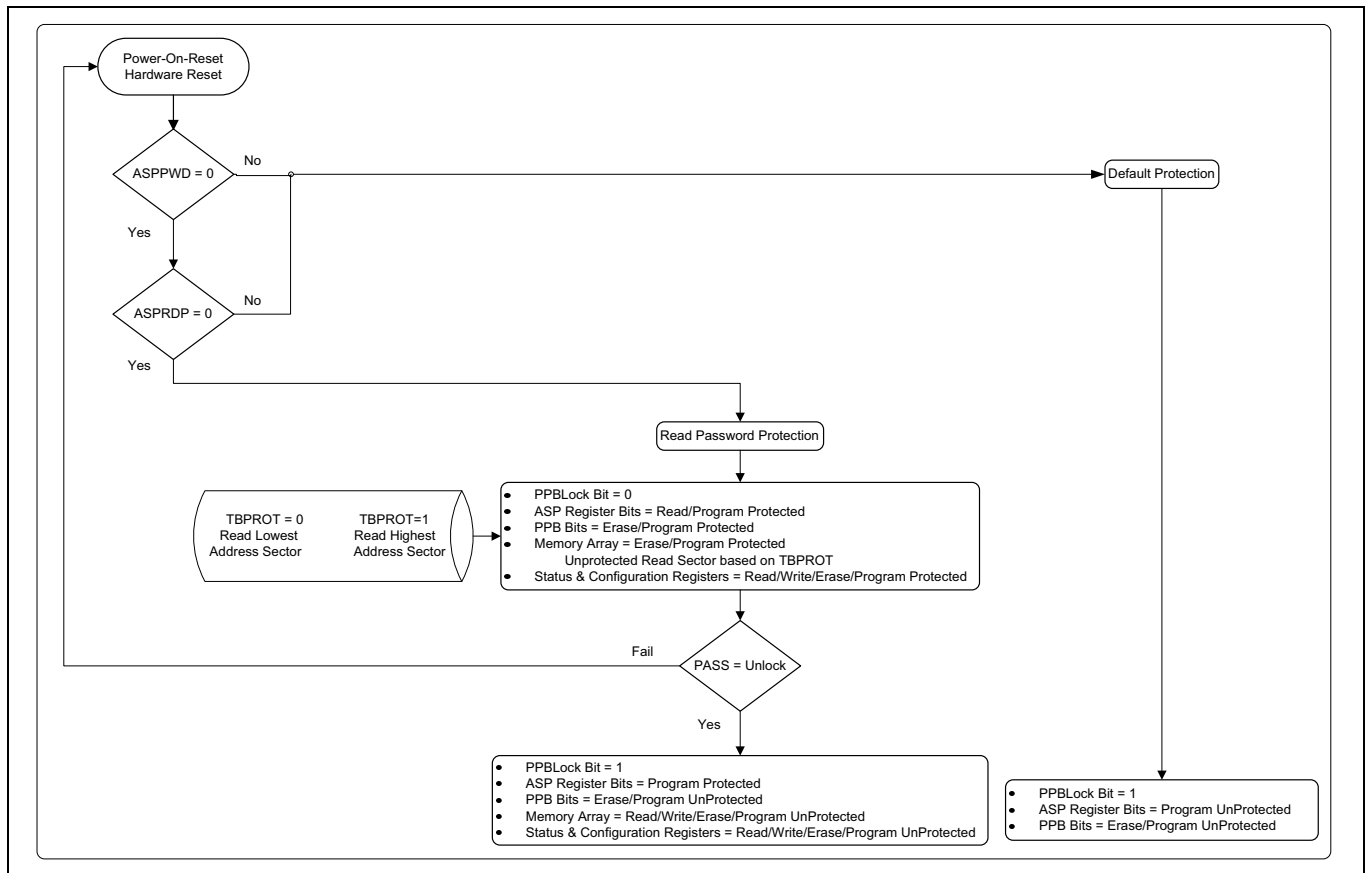


**Figure 47** Password protection scheme flowchart

#### 4.5.2.7 Read password protection scheme

The read password protection scheme replaces the password protection scheme and provides the most data protection. The read password protection scheme enables protecting the flash memory array from read, program, and erase. Only the lowest or highest (256-KB) sector address range, selected by bit 5 of Configuration Register 1 (CFR1x[5] - TBPROT), remains readable until a successful password unlock transaction is complete. A '0' selects from the top most sector and a '1' selects from the bottom most sector irrespective of the sector address supplied in the read transaction. Note that reads from the read-protected portion of the array will alias back to the readable sector.

**Note** A password must be programmed before selecting the read password protection scheme. The password unlock SPI transaction (PWDUL\_0\_1) or Octal transaction (PWDUL\_4\_1) is used to provide a password for comparison. The read password protection scheme flowchart is shown in **Figure 48**.



**Figure 48** Read password protection scheme flowchart

#### 4.5.2.8 PPB bits - OTP selection

ASP provides a configuration option to permanently disable the PPB erase transaction (ERPPB\_0\_0). This makes all PPB bits one-time programmable. With this option, once the PPB protection is selected, it can never be changed. Selecting bit 3 in Advanced Sector Protection Register (ASPO[3] - ASPPPB) makes PPB bits OTP.

#### 4.5.2.9 General ASP guidelines

- Persistent protection (ASPPER) and password protection (ASPPWD) are mutually exclusive - only one option can be programmed.
- Read password protection (ASPRDP) if desired, must be programmed at the same time as password protection (ASPPWD).
- Once the password is programmed and verified, the password protection scheme (ASPPWD) must be programmed (to 0) to prevent reading the password.
- When the read password scheme and password protection scheme are enabled (i.e. ASPO[5] - ASPRDP, ASPO[2] - ASPPWD are programmed to 0), then all addresses are redirected to the boot sector until the password unlocking sequence is properly entered with the correct password. At which time, the Read Password Mode is disabled and all addressing will select the proper location.
- Programming memory spaces or writing registers is not allowed when Read Password Protection Mode is active.

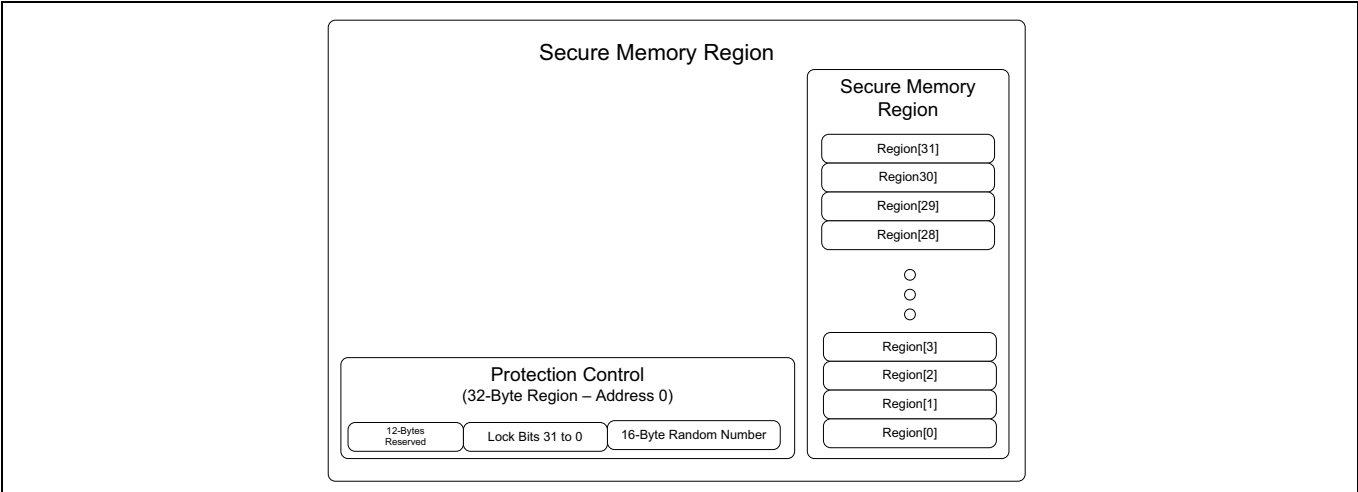
#### 4.5.2.10 ASP related registers and transactions

**Table 26 ASP related registers and transactions**

| Related registers                                                          | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|----------------------------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| Advanced Sector Protection Register (ASPO) (see <a href="#">Table 67</a> ) | Read Dynamic Protection Bit (RDDYB_4_0)                     | Read Dynamic Protection Bit (RDDYB_4_0)                       |
|                                                                            | Write Dynamic Protection Bit (WRDYB_4_1)                    | Write Dynamic Protection Bit (WRDYB_4_1)                      |
|                                                                            | Read Persistent Protection Bit (RDPPB_4_0)                  | Read Persistent Protection Bit (RDPPB_4_0)                    |
|                                                                            | Program Persistent Protection Bit (PRPPB_4_0)               | Program Persistent Protection Bit (PRPPB_4_0)                 |
|                                                                            | Erase Persistent Protection Bit (ERPPB_0_0)                 | Erase Persistent Protection Bit (ERPPB_0_0)                   |
|                                                                            | Write PPB Protection Lock Bit (WRPLB_0_0)                   | Write PPB Protection Lock Bit (WRPLB_0_0)                     |
|                                                                            | Read Password Protection Mode Lock Bit (RDPLB_0_0)          | Read Password Protection Mode Lock Bit (RDPLB_4_0)            |
|                                                                            | Password Unlock (PWDUL_0_1)                                 | Password Unlock (PWDUL_4_1)                                   |
|                                                                            | Write Enable (WRENB_0_0)                                    | Write Enable (WRENB_0_0)                                      |
|                                                                            | Read Any Register (RDARG_C_0)                               | Read Any Register (RDARG_4_0)                                 |
| Configuration Register 1 (CFR1N, CFR1V) (see <a href="#">Table 51</a> )    | Write Any Register (WRARG_C_1)                              | Write Any Register (WRARG_4_1)                                |

### 4.5.3 Secure silicon region (SSR)

Secure silicon region is a 1024 byte memory region (separate from the main memory array). The 1024 bytes are divided into 32, individually lockable 32-byte regions. [Figure 49](#) provides an overview of SSR.



**Figure 49** OTP protection (non-volatile)

The first 32-byte region (starting at address 0) provides the protection mechanism for the other 32-byte regions. The sixteen lowest bytes of this region contain a 128-bit random number. The random number cannot be written to, erased or programmed. The next four bytes (32 bits in total) of this region provide protection from programming if set to '0' for the remaining 32-byte regions - one bit per 32-byte region. All other bytes are reserved.

**Note** Attempting to Erase or Program the 128-bit random number will result in ERSERR or PRGERR respectively. A hardware Reset is required to bring the device back to Standby mode.

#### 4.5.3.1 SSR related registers and transactions

**Table 27** SSR related registers and transactions

| Related registers | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|-------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| N/A               | Program Secure Silicon Region (PRSSR_4_1)                   | Program Secure Silicon Region (PRSSR_4_1)                     |
|                   | Read Secure Silicon Region (RDSSR_4_0)                      | Read Secure Silicon Region (RDSSR_4_0)                        |

## 4.6 SafeBoot

SEMPER™ flash memory devices contain an embedded microcontroller which is used to initialize the device, manage embedded operations, and perform other advanced functionality. An initialization failure of this embedded microcontroller or corruption of the non-volatile configuration registers can render the flash device unusable. Barring a catastrophic event, such as permanent corruption of the embedded microcontroller firmware, it is possible to recover the device.

The SafeBoot feature allows Status Register polling to detect an embedded microcontroller initialization failure or configuration register corruption through error signatures.

### 4.6.1 Microcontroller initialization failure detection

If the microcontroller embedded in the flash device fails to initialize, a hardware reset can recover the device, unless it is a catastrophic failure. This hardware reset must be initiated by the Host controller. Upon detecting a failed microcontroller initialization, the Flash device automatically reverts to its Default Boot mode (1S-1S-1S) and provides a failure signature in its Status Register. [Table 28](#) shows the device's Status Register bits upon detecting an initialization failure.

**Table 28 Status Register 1 power-on detection signature**

| Bit      | Field name  | Function                                                                                                                                                      | Detection signature |
|----------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| STR1V[7] | RESRVD      | Reserved for Future Use                                                                                                                                       | 0                   |
| STR1V[6] | PRGERR      | Programming Error Status Flag                                                                                                                                 | 1                   |
| STR1V[5] | ERSERR      | Erasing Error Status Flag                                                                                                                                     | 1                   |
| STR1V[4] | LBPROT[2:0] | Legacy Block Protection based memory Array size selection<br><b>Note:</b> LBPRIT[2:0] can be anything from 000 to 111 based on Block Protection configuration | 0                   |
| STR1V[3] |             |                                                                                                                                                               | 0                   |
| STR1V[2] |             |                                                                                                                                                               | 0                   |
| STR1V[1] | WRPGEN      | Write/Program Enable Status Flag                                                                                                                              | 0                   |
| STR1V[0] | RDYBSY      | Device Ready/Busy Status Flag                                                                                                                                 | 1                   |

**Table 29 Interface configuration upon detecting power-on failure<sup>[17]</sup>**

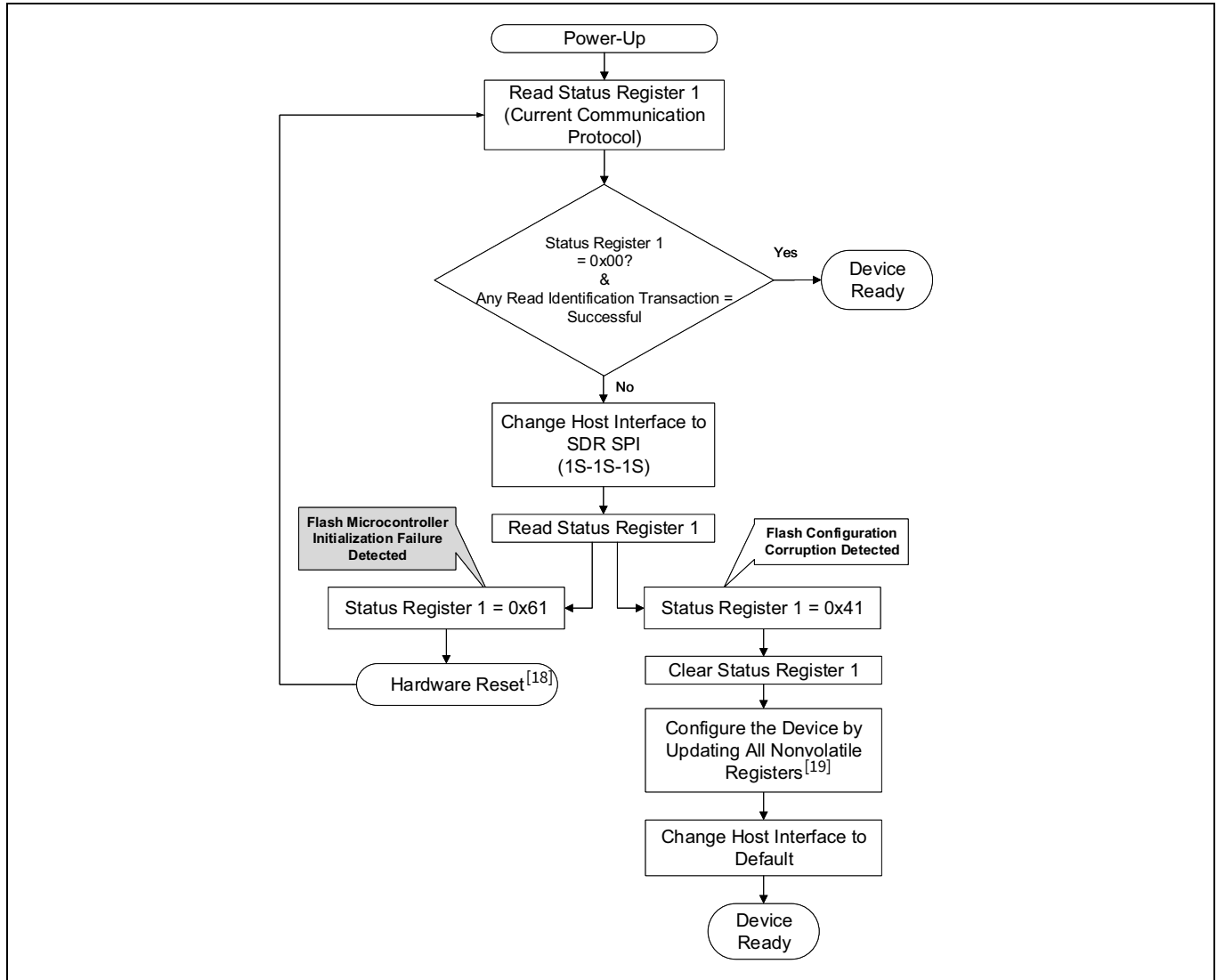
| Interface      | Transactions supported                      | Register type                   | Address (# of bytes) | Frequency of operation                                                         | Register read latency (# of clock cycles) | Output impedance |
|----------------|---------------------------------------------|---------------------------------|----------------------|--------------------------------------------------------------------------------|-------------------------------------------|------------------|
| SPI (1S-1S-1S) | Read Status Register 1<br>Read Any Register | Status Register (Volatile Only) | 4                    | Maximum (allowed for Read Status Register 1 and Read Any Register transaction) | 2                                         | 45 Ω             |

**Note**

17. For reading the Status Register, providing the non-volatile Status Register address to Read Any Register transaction will produce indeterminate results.

#### 4.6.1.1 Host polling behavior

The host will need to go through a Status Register polling sequence to determine if an initialization failure has occurred in the device. The flowchart for the sequence is shown in **Figure 50**.



**Figure 50 Host polling sequence for microcontroller initialization failure detection**

**Note** The polling sequence must start from the higher I/O interface configuration to lower I/O interface configuration only. For example, 8D-8D-8D to 1S-1S-1S.

#### Notes

- 18.If you have Vcc within specifications and a hardware reset does not resolve the issue, replace the flash device.
- 19.As soon as first Write Any Register transaction updates the Non-volatile Status Register or Configuration Register, all remaining non-volatile status and configuration registers go back to the predefined state (STR1N = 0x00, CFR1N = 0x00, CFR2N = 0x00, CFR3N = 0x00, CFR4N = 0x00, CFR5N = 0x40). It is recommended to initiate

#### 4.6.1.2 Microcontroller initialization failure detection related registers and transactions

**Table 30** Microcontroller initialization failure related registers and transactions

| Related registers                                    | Related SPI transactions<br>(see Table 81) | Related octal transactions<br>(see Table 82) |
|------------------------------------------------------|--------------------------------------------|----------------------------------------------|
| Status Register 1 Volatile (STR1V)<br>(see Table 47) | Read Any Register (RDARG_C_0)              | N/A                                          |
|                                                      | Read Status Register -1<br>(RDSR1_0_0)     |                                              |

#### 4.6.2 Configuration corruption detection

If during device's configuration update, such as writing to a non-volatile register, a power loss occurs or a hardware reset is initiated, the write any register transaction will get interrupted. The device will return to Standby mode, but the non-volatile register data is most likely corrupted since the embedded write operation was prematurely terminated. During the next power-up, the configuration corruption is detected and the device reverts to its Default Boot mode (1S-1S-1S) and allows rewriting the configuration again. The device will maintain the configured protection scheme.

Table 31 shows the device's Status Register bits upon detecting a configuration corruption.

**Table 31** Status Register 1 configuration corruption detection signature

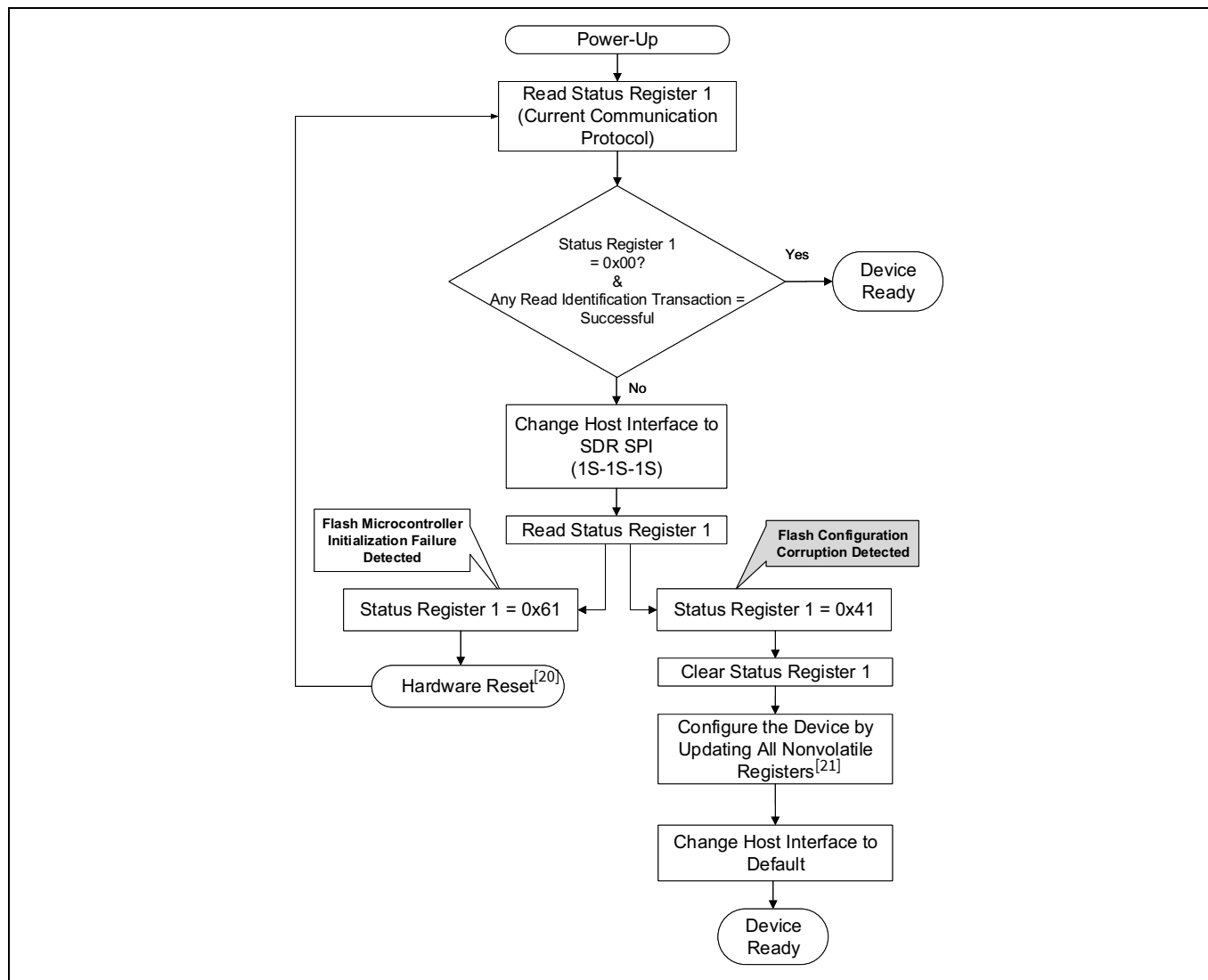
| Bit      | Field name  | Function                                                                                        | Detection signature |
|----------|-------------|-------------------------------------------------------------------------------------------------|---------------------|
| STR1V[7] | RESRVD      | Reserved for Future Use                                                                         | 0                   |
| STR1V[6] | PRGERR      | Programming Error Status Flag                                                                   | 1                   |
| STR1V[5] | ERSERR      | Erasing Error Status Flag                                                                       | 0                   |
| STR1V[4] | LBPROT[2:0] | Legacy Block Protection based memory Array size selection                                       | 0                   |
| STR1V[3] |             | <b>Note</b> LBPRIT[2:0] can be anything from 000 to 111 based on Block Protection configuration | 0                   |
| STR1V[2] |             |                                                                                                 | 0                   |
| STR1V[1] | WRPGEN      | Write/Program Enable Status Flag                                                                | 0                   |
| STR1V[0] | RDYBSY      | Device Ready/Busy Status Flag                                                                   | 1                   |

**Table 32** Interface configuration upon detecting configuration corruption

| Interface      | Transactions supported          | Address (# of bytes) | Frequency of operation | Register read latency (# of clock cycles) | Output impedance |
|----------------|---------------------------------|----------------------|------------------------|-------------------------------------------|------------------|
| SPI (1S-1S-1S) | All SPI (1S-1S-1S) Transactions | 4                    | Maximum                | 2                                         | 45 Ω             |

#### 4.6.2.1 Host polling behavior

The host will need to go through a Status Register polling sequence to determine if a Configuration corruption has occurred in the device. The flowchart for the sequence is shown in **Figure 51**.



**Figure 51** Host polling sequence for configuration corruption detection

**Note** The polling sequence must start from a higher I/O interface configuration to a lower I/O interface configuration. As an example, 8D-8D-8D to 1S-1S-1S. Not the other way around.

#### Notes

20.If you have Vcc within specifications and a hardware reset does not resolve the issue, replace the flash device.

21.As soon as first Write Any Register transaction updates the Non-volatile Status Register or Configuration Register, all remaining non-volatile status and configuration registers go back to the predefined state (STR1N = 0x00, CFR1N = 0x00, CFR2N = 0x00, CFR3N = 0x00, CFR4N = 0x00, CFR5N = 0x40). It is recommended to initiate

#### 4.6.2.2 Configuration corruption detection related registers

**Table 33 Configuration corruption detection related registers and transactions**

| Related registers                                    | Related SPI transactions<br>(see Table 81) | Related octal transactions<br>(see Table 82) |
|------------------------------------------------------|--------------------------------------------|----------------------------------------------|
| Status Register 1 Volatile (STR1V)<br>(see Table 47) | All 1S-1S-1S Transactions                  | N/A                                          |

### 4.7 AutoBoot

AutoBoot allows the host to read data from HL-T/HS-T family of devices after power up or after a hardware reset without having to send any read transactions (including the address). Based on the device configuration, data is output on the interface I/Os once CS# is brought LOW and CK is toggled.

The starting address for the read data is specified in the AutoBoot Register (ATBN[31:9] - STADR[22:0]). This starting address can be at any page boundary location in the memory (512 byte page boundary). Also identified in the AutoBoot Register is a starting delay which is represented as the number of clock cycles (ATBN[8:1] - STDLY[7:0]). This delay is instituted before the data is read out. The delay can be programmed to meet the host's requirements but a minimum amount is required to meet the memory access times based on the frequency for operation. It is highly recommended to check the Status Register 1 value after successful or unsuccessful AutoBoot execution to verify the configuration corruption (SafeBoot).

#### Notes

- Wrap function must be disabled for AutoBoot.
- AutoBoot is disabled when the Read Password feature is enabled, as part of the advanced sector protection. It is recommended to disable AutoBoot (ATBN[0] - ATBTEN) when Read Password feature is enabled.
- Autoboot with Interface CRC enabled requires reading out at least 4 words of data.
- It is highly recommended to assign first AutoBoot address in the Long Retention region.

#### 4.7.1 AutoBoot related registers and transactions

**Table 34 AutoBoot related registers and transactions**

| Related registers                          | Related SPI transactions<br>(see Table 81) | Related octal transactions<br>(see Table 82)                                                             |
|--------------------------------------------|--------------------------------------------|----------------------------------------------------------------------------------------------------------|
| AutoBoot Register (ATBN)<br>(see Table 72) | Read Any Register (RDARG_C_0)              | Read Any Register (RDARG_4_0)                                                                            |
|                                            | Write Any Register (WRARG_C_1)             | Write Any Register (WRARG_4_1)                                                                           |
|                                            | AutoBoot Transaction<br>(see Figure 14)    | AutoBoot Octal SDR Transaction<br>(see Figure 27) /<br>AutoBoot Octal DDR Transaction<br>(see Figure 28) |

## 4.8 Read transactions

HL-T/HS-T supports different read transactions to access different memory maps, namely: Read Memory array, Read Device Identification, Read Register, Read Secure Silicon, Read Protection DYB and PPB bits.

These read transactions can use any of these three interfaces and protocols:

- SPI interface with SDR (1S-1S-1S) protocol, transfers the one byte command one bit per CK rising edge
- Octal interface with SDR (8S-8S-8S) protocol, transfers the two byte command eight bits per CK rising edge
- Octal interface with DDR (8D-8D-8D) protocol, transfers the two byte command eight bits per CK rising and falling edge

These read transactions use the following features:

- The read transactions require latency cycles following the address to allow time to access the memory array (except RDAY1\_4\_0 and RDAY1\_C\_0 of 1S-1S-1S protocol) (see [Table 55](#)).
- Data Strobe (DS) output enables the memory controller to capture data at the center of the data eye (see [“Data strobe \(DS\)”](#) on page 63).
- The read transaction has the option of wrapped read length and alignment groups of 8-, 16-, 32-, or 64-bytes (see [Table 58](#) and [Table 59](#)).

### 4.8.1 Read identification transactions

There are three unique identification transactions, and each support all three Protocols (1S-1S-1S), (8S-8S-8S), and (8D-8D-8D) (see [“Transaction table”](#) on page 120).

#### 4.8.1.1 Read device identification transaction

The Read Device Identification (RDIDN\_0\_0, RDIDN\_4\_0) transaction provides read access to manufacturer identification and device identification. The SPI mode has no address cycles, whereas the Octal mode has four dummy addresses (00h). The transaction uses latency cycles set by (CFR3V[7:6]) to enable maximum clock frequency of 166 MHz under SPI mode, 166 MHz under HL-T Octal, and 200MHz under HS-T Octal mode (see [Table 55](#)). The Octal mode supports the DS for capture of data (see [“Transaction table”](#) on page 120).

#### 4.8.1.2 Read SFDP transaction

The Read Serial Flash Discoverable Parameters (RSFDP\_3\_0, RSFDP\_4\_0) transaction provides access to the JEDEC Serial Flash Discovery Parameters (SFDP) (see [“Transaction table”](#) on page 120). The transaction uses a 3-byte address in SPI mode and 4-byte address in Octal mode address. If a non-zero address is set, the selected location in the SFDP space is the starting point of the data read. This enables random access to any parameter in the SFDP space. Continuous (sequential) read is supported with this transaction. Eight latency cycles are required. Read SFDP Transaction is not supported in Read Password mode before the password is provided. The maximum clock frequency for the Read SFDP transaction is 156 MHz under SPI mode, 92 MHz under Octal SDR mode, and 85MHz under Octal DDR mode.

#### 4.8.1.3 Read unique identification transaction

Read Unique Identification (RDUID\_0\_0, RDUID\_4\_0) transaction is similar to Read Device Identification transaction, but accesses a different 64-bit number, which is unique to each device. It is factory programmed.

#### 4.8.1.4 Read identification related register and transaction

**Table 35** Read identification related registers and transactions

| Related registers                                                          | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|----------------------------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| Configuration Register 3 (CFR3N, CFR3V)<br>(see <a href="#">Table 56</a> ) | Read Identification (RDIDN_0_0)                             | Read Identification (RDIDN_4_0)                               |
| Configuration Register 5 (CFR5N, CFR5V)<br>(see <a href="#">Table 60</a> ) | Read Serial Flash Discoverable (RSFDP_3_0)                  | Read Serial Flash Discoverable (RSFDP_4_0)                    |
|                                                                            | Read Unique Identification (RDUID_0_1)                      | Read Unique Identification (RDUID_4_1)                        |

### 4.8.2 Read memory array transactions

Memory array data can be read from the memory starting at any byte boundary. Data bytes are sequentially read from incrementally higher byte addresses until the host ends the data transfer by driving CS# input HIGH. If the byte address reaches the maximum address of the memory array, the read will continue at address zero of the array.

#### 4.8.2.1 SPI read and read fast transactions

The SPI Read and Read Fast transactions (1S-1S-1S) are supported for Host systems that require backward compatibility to legacy SPI. This protocol does not support the DS for capture of data. The option of wrapped read length is available. The Read transaction is for maximum clock frequency of 50 MHz and requires no latency cycles. The Read Fast Transaction uses latency cycles set by (CFR2V[3:0]) to enable maximum clock frequency of 166 MHz (see [“Transaction table”](#) on page 120).

#### 4.8.2.2 Read Octal SDR transaction

The Read Octal SDR transaction provides high data throughput using SDR (8S-8S-8S) protocol. This protocol supports the DS for capture of data. The option of wrapped read length is available. This transaction uses latency cycles set by (CFR2V[3:0]) to enable maximum 166 or 200 MHz clock frequency (see [“Transaction table”](#) on page 120).

#### 4.8.2.3 Read Octal DDR transaction

The Read Octal DDR transaction provides the fastest data throughput using DDR (8D-8D-8D) protocol. This protocol only supports the DS for capture of data. The option of wrapped read length is available. This transaction uses latency cycles set by (CFR2V[3:0]) to enable maximum 166 or 200 MHz clock frequency (see [“Transaction table”](#) on page 120).

#### 4.8.2.4 Read memory array related registers and transactions

**Table 36** Read memory array related registers and transactions

| Related registers                                                          | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|----------------------------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| Configuration Register 2 (CFR2N, CFR2V)<br>(see <a href="#">Table 54</a> ) | Read (RDAY1_4_0, RDAY1_C_0)                                 | Read Octal SDR (RDAY1_4_0)                                    |
| Configuration Register 4 (CFR4N, CFR4V)<br>(see <a href="#">Table 58</a> ) | Read Fast (RDAY2_C_0)                                       | Read Octal DDR (RDAY2_4_0)                                    |
| Configuration Register 5 (CFR5N, CFR5V)<br>(see <a href="#">Table 60</a> ) | –                                                           | –                                                             |

#### 4.8.3 Read registers transactions

There are multiple registers for reporting embedded operation status or controlling device configuration options. Registers contain both volatile and non-volatile bits. There are two ways to read the Registers. The Read Any Register transaction provides a way to read all device registers: non-volatile and volatile by address selection. There are also dedicated Register Read transactions, which are defined per register and only read the contents of that register. These Read Register Transactions support all three Protocols (1S-1S-1S), (8S-8S-8S) and (8D-8D-8D) (see [“Transaction table”](#) on page 120).

##### 4.8.3.1 Read any register

The Read Any Register transaction is the best way to read all device registers, both non-volatile and volatile. The transaction includes the address of the register to be read (see [“Transaction table”](#) on page 120). This is followed by a number of latency cycles set by (CFR2V[3:0]) for reading non-volatile registers and CFR3V[7:6] for reading volatile registers. See [Table 55](#) for NV Registers latency cycles and [Table 57](#) for Volatile Registers latency cycles. Then, the selected register contents are returned. In SPI mode, if the read access is continued, the same addressed register contents are returned until the transaction is terminated; only one byte register location is read by each Read Any Register transaction. For registers with more than one byte of data, the Read Any Register transaction must again be used to read each byte of data. The Octal mode supports the DS for capture of data (see [“Transaction table”](#) on page 120).

The maximum clock frequency for the Read Any Register transaction is 166 MHz under SPI mode, 166 MHz under HL-T Octal mode, and 200 MHz under HS-T Octal mode.

The Read Any Register transaction can be used during embedded operations to read Status Register 1 (STR1V). It is not used for reading registers such as ASP PPB Access Register (PPAV) and ASP Dynamic Block Access Register (DYAV). There are separate commands required to select and read the location in the array accessed. The Read Any Register transaction will read invalid data from the PASS Register locations if the ASP Password protection mode is selected by programming ASPR[2:0]. Reading undefined locations provides undefined data.

##### 4.8.3.2 Read status registers transaction

The Read Status Register (RDSR1\_0\_0/RDSR1\_4\_0, RDSR2\_0\_0/RDSR2\_4\_0) transactions allow the registers' volatile contents be read. The SPI mode has no address cycles whereas the Octal mode has four dummy address of “00h”. The transaction uses latency cycles set by (CFR3V[7:6]) for reading volatile registers to enable maximum clock frequency of 166 MHz under SPI mode, 166 MHz under HL-T Octal mode, and 200 MHz under HS-T Octal mode (see [Table 55](#)). The Octal mode supports the DS for capture of data (see [“Transaction table”](#) on page 120).

The volatile version of Status Registers contents can be read at any time, even while a program, erase, or write operation is in progress.

It is possible to read Status Register 1 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read. This is limited to only under SPI mode.

#### **4.8.3.3 Read dynamic protection bit (DYB) access register transaction**

The Read DYB Access Register (RDDYB\_4\_0) transaction reads the contents of the DYB Access Register. The transaction uses latency cycles set by (CFR3V[7:6]) for reading volatile registers to enable maximum clock frequency of 166 MHz under SPI mode, 166 MHz under HL-T Octal mode, and 200 MHz under HS-T Octal mode (see [Table 55](#)). The Octal mode supports the DS for capture of data (see [“Transaction table”](#) on page 120). It is possible to read DYB Access register continuously, however the address of the DYB register does not increment, so the entire DYB array cannot be read in this fashion. Each location must be read with a separate Read DYB transaction.

#### **4.8.3.4 Read persistent protection bit (PPB) access register transaction**

The Read PPB Access Register (RDPBB\_4\_0) transaction reads the contents of the PPB Access Register. The transaction uses latency cycles set by (CFR2V[3:0]) to enable maximum clock frequency of 166 MHz under SPI mode, 166 MHz under HL-T Octal mode, and 200 MHz under HS-T Octal mode (see [Table 55](#)). The Octal mode supports the DS for capture of data (see [“Transaction table”](#) on page 120). It is possible to read PPB Access Register continuously, however the address of the PPB register does not increment, so the entire PPB array cannot be read in this fashion. Each location must be read with a separate Read PPB transaction.

#### **4.8.3.5 Read PPB lock registers transaction**

The Read PPB Lock Register (RDPLB\_0\_0, RDPLB\_4\_0) transactions allow the content of the non-volatile registers to be read. The SPI mode has no address cycles, whereas the Octal mode has four required address bytes of “00h”. The transaction uses latency cycles set by (CFR3V[7:6]) for reading volatile registers to enable maximum clock frequency of 166 MHz under SPI mode, 166 MHz under HL-T Octal mode, and 200 MHz under HS-T Octal mode. The Octal mode supports the DS for capture of data (see [“Transaction table”](#) on page 120). It is possible to read PPB Lock Bit continuously.

#### **4.8.3.6 Read ECC data unit status**

The Read ECC Data Unit Status (RDECC\_4\_0) transaction is used to determine the ECC status of the addressed unit data. In this transaction, the LSb of the address must be aligned to an ECC data unit. This transaction uses latency cycles set by (CFR3V[7:6]) for reading volatile registers to enable maximum clock frequency of 166 MHz under SPI mode, 166 MHz under HL-T Octal mode, and 200 MHz under HS-T Octal mode. The Octal mode supports the DS for capture of data (see [“Transaction table”](#) on page 120).

The byte contents of the ECC Status for the selected ECC unit is then output. Any following data will be indeterminate. To read the next ECC unit status, another RDECC\_4\_0 transaction should be sent out to the next address, incremented by 16 [Data Unit size/8] bytes.

#### 4.8.3.7 Read register related registers and transactions

**Table 37** Read register related registers and transactions

| Related registers                                                       | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|-------------------------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| Configuration Register 2 (CFR2N, CFR2V) (see <a href="#">Table 54</a> ) | Read Any Register (RDARG_C_0)                               | Read Any Register (RDARG_4_0)                                 |
| Configuration Register 3 (CFR3N, CFR3V) (see <a href="#">Table 56</a> ) |                                                             |                                                               |
| Configuration Register 5 (CFR5N, CFR5V) (see <a href="#">Table 60</a> ) | Read Status Register 1 (RDSR1_0_0)                          | Read Status Register 1 (RDSR1_4_0)                            |
|                                                                         | Read Status Register 2 (RDSR2_0_0)                          | Read Status Register 2 (RDSR2_4_0)                            |
|                                                                         | Read DYB (RDDYB_4_0)                                        | Read DYB (RDDYB_4_0)                                          |
|                                                                         | Read PPB (RDPPB_4_0)                                        | Read PPB (RDPPB_4_0)                                          |
|                                                                         | Read PPB Lock (RDPLB_0_0)                                   | Read PPB Lock (RDPLB_4_0)                                     |
|                                                                         | Read ECC Status (RDECC_4_0)                                 | Read ECC Status (RDECC_4_0)                                   |

#### 4.8.4 Data strobe (DS)

A data strobe (DS) is transmitted externally, along with data, for use in data capture at the host. During the period of data transfer in read transactions, the DS signal is driven by the device and transitions with the DQ signal data transitions. DS is used as an additional output signal with the same timing characteristics as other data outputs but with the guarantee of transitioning with every data bit transferred. DS is edge-aligned with data for DDR READs and is center-aligned with data for SDR READs. A pre-drive on DS exists to ensure DS is driven LOW immediately after 2.5 clock cycle after last address byte input to the device.

#### 4.9 Write transactions

There are write transactions for writing to the Registers. These write transactions can use any of following three protocols:

- SPI interface with SDR (1S-1S-1S) protocol, transfers the one byte command one bit per CK rising edge
- Octal interface with SDR (8S-8S-8S) protocol, transfers the two byte command eight bits per CK rising edge
- Octal interface with DDR (8D-8D-8D) protocol, transfers the two byte command eight bits per CK rising and falling edge

##### 4.9.1 Write enable transaction

The Write Enable (WRENB\_0\_0) transaction sets the Write Program Enable Status (WRPGEN) bit of the Status Register 1 (STR1V[1]) to 1. The WRPGEN bit must be set to 1 by issuing the Write Enable (WRENB\_0\_0) Transaction to enable write, program, and erase transactions (see [“Transaction table”](#) on page 120).

##### 4.9.2 Write disable transaction

The Write Disable (WRDIS\_0\_0) transaction clears the Write Program Enable Status (WRPGEN) bit of the Status Register 1 (STR1V[1]) to 0.

The WRPGEN bit can be cleared to 0 by issuing the Write Disable (WRDIS\_0\_0) transaction to disable commands that requires WRPGEN be set to 1 for execution. The WRDIS\_0\_0 transaction can be used by the user to protect memory areas against inadvertent write, program, or erase operations that can corrupt the contents of the memory. The WRDIS\_0\_0 transaction is ignored during an embedded operation while RDYBSY bit = 1 (STR1V[0]) (see [“Transaction table”](#) on page 120).

### 4.9.3 Clear program and erase failure flags transaction

The Clear Program and Erase Failure Flags (CLPEF\_0\_0) transaction resets bit STR1V[5] (Erase Error Flag) and bit STR1V[6] (Program Error Flag) to 0. This transaction will be accepted even when the device remains busy with RDYBSY set to 1, as the device does remain busy when either error bit is set. The WRPGEN bit will be unchanged after this command is executed (see “[Transaction table](#)” on page 120).

### 4.9.4 Clear ECC status register transaction

The Clear ECC Status Register (CLECC\_0\_0) transaction resets bit ECSV[4] (2-bit ECC Detection), bit ECSV[3] (1-bit ECC Correction), INSV[1:0] ECC detection status bits, Address Trap Register EATV[31:0], and ECC Detection Counter ECTV[15:0]. It is not necessary to set the WRPGEN bit before this transaction is executed. The Clear ECC Status Register transaction will be accepted even when the device remains busy with WRPGEN set to 1, as the device does remain busy when either error bit is set. The WRPGEN bit will be unchanged after this command is executed (see “[Transaction table](#)” on page 120).

### 4.9.5 Write any register transaction

The Write Any Register (WRARG\_C\_1 / WRARG\_4\_1) transaction provides a way to write any device register, non-volatile or volatile. The transaction includes the address of the register to be written, followed by one byte of data to write in the addressed register (see “[Transaction table](#)” on page 120).

Before the WRARG\_C\_1 / WRARG\_4\_1 transaction can be accepted by the device, a Write Enable (WRENB\_0\_0) transaction must be issued and decoded, which sets the Write/Program Enable bit (WRPGEN) in the Status Register to enable any write operations. The RDYBSY bit in STR1V[0] can be checked to determine when the operation is completed. The PRGERR and ERSERR bits in STR1V[6:5] can be checked to determine if any error occurred during the operation.

Some registers have a mixture of bit types and individual rules controlling which bits can be modified. Some bits are read only, some are OTP, and some are designated Reserved (DNU).

Read only bits are never modified and the related bits in the WRARG\_C\_1 / WRARG\_4\_1 transaction data byte are ignored without setting a program or erase error indication (PRGERR or ERSERR in STR1V[6:5]). Hence, the value of these bits in the WRARG\_C\_1 / WRARG\_4\_1 data byte do not matter.

OTP bits can only be programmed to the level opposite of their default state. Writing of OTP bits back to their default state is ignored and no error is set.

Non-volatile bits which are changed by the WRARG\_C\_1 / WRARG\_4\_1 data require non-volatile register write time ( $t_{wv}$ ) to be updated. The update process involves an erase and a program operation on the non-volatile register bits. If either the erase or program portion of the update fails, the related error bit and RDYBSY bit in STR1V will be set to 1.

Status Register 1 can be repeatedly read (polled) to monitor the RDYBSY bit (STR1V[0]) and the error bits (STR1V[6,5]) to determine when the register write is completed or failed. If there is a write failure, the CLPEF\_0\_0 transaction is used to clear the error status and enable the device to return to standby state.

The ASP PPB Lock Register (PPLV) register cannot be written by the WRARG\_C\_1 / WRARG\_4\_1 transaction. Only the Write PPB Lock Bit (WRPLB\_0\_0) transaction can write the PPLV Register.

The Data Integrity Check Register cannot be written by the WRARG\_C\_1 / WRARG\_4\_1 transaction. The Data Integrity Check Register is loaded by running the Data Integrity Check transaction (DICHK\_4\_1).

#### 4.9.6 Write PPB lock bit

The Write PPB Lock Bit (WRPLB\_0\_0) transaction clears the PPB Lock Register PPLV[0] to zero. The PPBLCK bit is used to protect the PPB bits. When PPLV[0] = 0, the PPB Program/Erase transaction will be aborted. In Read Password Protection mode, PPBLCK bit is also used to control the high order bits of the address by forcing the address range to be limited to one sector where boot code is stored, until the read password is supplied (see **“Transaction table”** on page 120).

Before the WRPLB\_0\_0 transaction can be accepted by the device, a Write Enable (WRENB\_0\_0) transaction must be issued and decoded by the device, which sets the Write/Program Enable (WRPGEN) in the Status Register 1 to enable any write operations.

While the operation is in progress, the Status Register can still be read to check the value of the RDYBSY bit. The WRPGEN bit is a 1 during the self-timed operation, and is a 0 when it is completed. When the Write PPB Lock transaction is completed, the RDYBSY bit is set to a 0 (see **“Transaction table”** on page 120).

#### 4.9.7 Enter 4 byte address mode

The Enter 4 byte address mode (EN4BA\_0\_0) transaction sets the volatile Address Length bit (CR2V[7]) to 1 to change most 3 byte address commands to require 4 bytes of address. The Read SFDP (RSFDP\_3\_0) transaction is not affected by the Address Length bit. RSFDP\_3\_0 is required by the JEDEC JESD216 standard to always have only 3 bytes of address.

A POR, hardware or software reset will set the address length per the non-volatile Address Length bit (CR2N[7]) definition.

#### 4.9.8 Exit 4 byte address mode

The exit 4 byte address mode (EX4BA\_0\_0) command sets the volatile Address Length bit (CR2V[7]) to 0 to change most 3 byte address commands to require 3 bytes of address. This command will not affect 4-byte only commands which will still continue to expect 4 bytes of address.

#### 4.9.9 Write transactions related registers and transactions

**Table 38 Write transactions related registers and transactions**

| Related registers                                                 | Related SPI transactions<br>(see <b>Table 81</b> )   | Related octal transactions<br>(see <b>Table 82</b> ) |
|-------------------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| Status Register 1 (STR1N, STR1V)<br>(see <b>Table 47</b> )        | Write Enable (WRENB_0_0)                             | Write Enable (WRENB_0_0)                             |
| Configuration Register 5 (CFR5N, CRF5V)<br>(see <b>Table 60</b> ) | Write Disable (WRDIS_0_0)                            | Write Disable (WRDIS_0_0)                            |
| ECC Status Register (ECSV)<br>(see <b>Table 64</b> )              | Clear Program and Erase Failure<br>Flags (CLPEF_0_0) | Clear Program and Erase Failure<br>Flags (CLPEF_0_0) |
| Interrupt Configuration (INCV)<br>(see <b>Table 74</b> )          | Clear ECC Status Register<br>(CLECC_0_0)             | Clear ECC Status Register<br>(CLECC_0_0)             |
| Address Trap Register (EATV)<br>(see <b>Table 65</b> )            | Write Any Register (WRARG_C_1)                       | Write Any Register (WRARG_4_1)                       |
| ECC Detection Counter (ECTV)<br>(see <b>Table 66</b> )            | Write PPB Lock Bit (WRPLB_0_0)                       | Write PPB Lock Bit (WRPLB_0_0)                       |
| Configuration Register 2 (CFR2V)<br>(see <b>Table 51</b> )        | Enter 4 Byte (EN4BA_0_0),<br>Exit 4 Byte (EX4BA_0_0) | –                                                    |

## 4.10 Program

There are program transactions for programming data to the memory array, secure silicon region and persistent protection bits.

These program transactions can use any of these three protocols:

- SPI interface with SDR (1S-1S-1S) protocol, transfers the one byte command one bit per CK rising edge
- Octal interface with SDR (8S-8S-8S) protocol, transfers the two byte command eight bits per CK rising edge
- Octal interface with DDR (8D-8D-8D) protocol, transfers the two byte command eight bits per CK rising and falling edge

Before any program transaction can be accepted by the device, a Write Enable (WRENB\_0\_0) transaction must be issued and decoded by the device. Program transactions can only be executed by the device if the Write/Program Enable (WRPGEN) in the Status Register is set to '1' to enable program operations. When a program transaction is completed, the WRPGEN bit is reset to a '0'.

While the program transaction is in progress, the Status Register 1 may be read to check the value of the Device Ready/Busy (RDYBSY) bit. The RDYBSY bit is a '1' during the self-timed program transaction, and is a '0' when it is completed.

The PGMERR bit in STR1V[6] may be checked to determine if any error occurred during the program transaction.

A program transaction applied to a sector that has been Write Protected through any of the protection schemes will not be executed and will set the PGMERR status fail bit.

The program transactions will be initiated when CS# is driven into the logic HIGH state.

### 4.10.1 Program granularity

The HS/L-T family supports multi-pass programming (bit walking) where programming a '0' over a '1' without performing the sector erase operation. Bit-walking is allowed for the non-AEC-Q100 industrial temperature range (–40°C to +85°C) of this device. It is required to perform only one programming operation (single-pass programming) on each ECC data unit between erase operations for the higher temperature range (–40°C to +105°C) and (–40°C to +125°C) devices and all AEC-Q100 devices.

Multi-pass programming without an erase operation will disable the device's ECC functionality for that data unit. Note that if 2-bit ECC is enabled, multi-pass Programming within the same sector will result in a Program Error.

### 4.10.2 Page programming

Page programming is done by loading a page buffer with data to be programmed and issuing a programming command to move data from the buffer to the memory array. This sets an upper limit on the amount of data that can be programmed with a single programming transaction. Page programming allows up to a page size (either 256- or 512-bytes) to be programmed in one operation. The page size is determined by the Configuration Register 3 bit CFR3V[4]. The page is aligned on the page size address boundary. It is possible to program from one bit up to a page size in each page programming operation. It is recommended that a multiple of 16-byte length and aligned program blocks be written. This ensures that ECC is not disabled. For the very best page program throughput, programming should be done in full pages of 512 bytes aligned on 512-byte boundaries with each page being programmed only once.

#### 4.10.3 Program page transaction

The program page transaction (PRPGE\_4\_1) programs data into the memory array. If data more than a page size (256B or 512B) is sent to the device, then the space between the starting address and the page aligned end boundary, the data loading sequence will wrap from the last byte in the page to the zero byte location of the same page and begin overwriting any data previously loaded in the page. If less than a page of data is sent to the device, then the sent data bytes will be programmed in sequence, starting at the provided address within the page, without having any effect on the other bytes of the same page. The programming process is managed by the device internal control logic. The PRGERR bit indicates if an error has occurred in the programming transaction that prevents successful completion of programming. This includes attempted programming of a protected area (see “[Transaction table](#)” on page 120).

Under Octal SDR mode, this transaction can be used for single byte command and its address can start at an even or odd address. Under DDR mode, this command can only be used for programming multiples of 2-bytes and the address must start at an even address.

#### 4.10.4 Program secure silicon region transaction

The program secure silicon transaction (PRSSR\_4\_1) programs data in the SSR, which is in a different address space from the main array data and is OTP. The SSR is 1024 bytes, so the address bits from A31 to A10 must be zero for this transaction (see “[Transaction table](#)” on page 120). It is required to align start address to 32 bits while programming the SSR space, which means the address bits A1 and A0 should be 0'b and host should deassert CS# to align with 32 bits.

The PRGERR bit in STR1V[6] may be checked to determine if any error occurred during the operation.

To program the OTP array in bit granularity, the rest of the bits within a data byte can be set to 1.

Each SSR memory space can be programmed one or more times, provided that the region is not locked.

Attempting to program zeros in a region that is locked will fail with the PRGERR bit in STR1V[6] set to 1.

Programming once, even in a protected area does not cause an error and does not set PRGERR bit. Subsequent programming can be performed only on the unprogrammed bits (that is, 1 data). Programming more than once within an ECC unit will disable ECC on that data unit.

#### 4.10.5 Program persistent protection bit (PPB)

The program persistent protect bit (PRPPB\_4\_0) transaction programs a bit in the PPB register to protect the sector of the provided address from being programmed or erased (see “[Transaction table](#)” on page 120).

The PRGERR bit in STR1V[6] may be checked to determine if any error occurred during the operation. Program PPB bit transaction will abort when trying to program the PPB bits protected by ASPPPB (ASPO[3]), ASPPRM (ASPO[0]) and PPBLCK (PPLV[0]) bit.

#### 4.10.6 Program related registers and transactions

**Table 39 Program related registers and transactions**

| Related registers                                                          | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|----------------------------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| Status Register 1 (STR1N, STR1V)<br>(see <a href="#">Table 47</a> )        | Write Enable (WRENB_0_0)                                    | Write Enable (WRENB_0_0)                                      |
| Configuration Register 5 (CFR5N, CRF5V)<br>(see <a href="#">Table 60</a> ) | Program Page (PRPGE_4_1)                                    | Program Page (PRPGE_4_1)                                      |
| Advance Sector Protect Register (ASPO)<br>(see <a href="#">Table 67</a> )  | Program Secure Silicon (PRSSR_4_1)                          | Program Secure Silicon (PRSSR_4_1)                            |
| ASP PPB Lock (PPLV)<br>(see <a href="#">Table 69</a> )                     | Program Persistent Protection Bit (PRPPB_4_0)               | Program Persistent Protection Bit (PRPPB_4_0)                 |
| ECC Status Register (ECSV)<br>(see <a href="#">Table 64</a> )              | Clear Program and Erase Failure Flags (CLPEF_0_0)           | Clear Program and Erase Failure Flags (CLPEF_0_0)             |

## 4.11 Erase

There are erase transactions for erasing data bits to 1 (all bytes are FFh) for the memory array and persistent protection bits.

These erase transactions can use any of these three protocols:

- SPI interface with SDR (1S-1S-1S) protocol, transfers the one byte command one bit per CK rising edge
- Octal interface with SDR (8S-8S-8S) protocol, transfers the two byte command eight bits per CK rising edge
- Octal interface with DDR (8D-8D-8D) protocol, transfers the two byte command eight bits per CK rising and falling edge

Before any erase transaction can be accepted by the device, a write enable (WRENB\_0\_0) transaction must be issued and decoded by the device. Erase transactions can only be executed by the device if the Write/Program Enable bit (WRPGEN) in the Status Register is set to '1' to enable erase operations. When an erase transaction is completed, the WRPGEN bit is reset to a '0'.

While the erase transaction is in progress, the Status Register 1 may be read to check the value of the Device Ready/Busy (RDYBSY) bit. The RDYBSY bit is a '1' during the self-timed erase transaction, and is a '0' when it is completed.

The ERSERR bit in STR1V[5] can be checked to determine if any error occurred during the erase transaction.

An erase transaction applied to a sector that has been Write Protected through the Block Protection bits or ASP, will not be executed and will set the ERSERR status fail bit.

Erase transactions will be initiated when CS# is driven into the logic HIGH state.

When the device is shipped from the factory the default erase state is all bytes are FFh.

### 4.11.1 Erase 4KB sector transaction

The erase 4KB sector (ER004\_4\_0) transaction sets all the bits of a 4 KB sector to 1 (all bytes are FFh) (see [“Transaction table”](#) on page 120).

This transaction is ignored when the device is configured for uniform sectors only (CFR3V[3] = 1). If the erase 4 KB sector transaction is issued to a non-4 KB sector address, the device will abort the operation and will not set the ERSERR status fail bit.

### 4.11.2 Erase 256 KB sector transaction

The erase 256 KB Sector (ER256\_4\_0) transaction sets all bits in the addressed sector to 1 (all bytes are FFh) (see [“Transaction table”](#) on page 120).

A device configuration option (CFR3V[3]) determines if the Hybrid Sector Architecture is in use. When CFR3V[3] = 0, 4 KB sectors overlay a portion of the highest or lowest address 128 KB or 64 KB of the device address space. If a sector erase command is applied to a 256 KB sector that is overlaid by 4 KB sectors, the overlaid 4 KB sectors are not affected by the erase. Only the visible (non-overlaid) portion of the 128 KB or 192 KB sector is erased. When CFR3V[3] = 1, there are no 4 KB sectors in the device address space and the Sector Erase command always operates on fully visible 256 KB sectors.

When BLKCHK is enabled an erase transaction first evaluates the erase status of the sector. If the sector is found to be erased, the erase operation is aborted. The erase operation is only executed if programmed bits are found in the sector. Disabling BLKCHK executes an erase operation unconditionally.

### 4.11.3 Erase chip transaction

The erase chip (ERCHP\_0\_0) transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array (see [“Transaction table”](#) on page 120).

An erase chip transaction can be executed only when the block protection (BP2, BP1, BP0) bits are set to 0's. If the BP bits are not zero, the transaction is not executed and ERSERR status fail bit is not set. The transaction will skip any sectors protected by the advance sector protection DYB or PPB and the ERSERR status fail bit will not be set.

#### 4.11.3.1 Erase persistent protection bit (PPB) transaction

The Erase PPB (ERPPB\_0\_0) transaction sets all PPB bits to 1 (see “[Transaction table](#)” on page 120). This transaction will abort if PPB bits are protected by ASPPPB (ASPO[3]), ASPPRM (ASPO[0]) and PPBLCK (PPLV[0]) bit.

#### 4.11.4 Erase status and count

##### 4.11.4.1 Evaluate erase status transaction

The evaluate erase status (EVERS\_4\_0) transaction verifies that the last erase operation on the addressed sector was completed successfully. If the selected sector was successfully erased, then the erase status bit (STR2V[2]) is set to 1. If the selected sector was not completely erased STR2V[2] is 0. The write/program enable transaction (to set the WRPGEN bit) is not required before this transaction. However, the RDYBSY bit is set by the device itself and cleared at the end of the operation, as visible in STR1V[0] when reading status (see “[Transaction table](#)” on page 120).

The evaluate erase status transaction can be used to detect when erase operations that have failed due to loss of power, reset, or failure during the erase operation. The transaction requires  $t_{EES}$  to complete and update the erase status in STR2V. The RDYBSY bit (STR1V[0]) can be read to determine when the evaluate erase status transaction is completed. If a sector is found not erased with STR2V[2] = 0, the sector must be erased again to ensure reliable storage of data in the sector.

##### 4.11.4.2 Sector erase count transaction

The sector erase count (SEERC\_4\_0) transaction outputs the number of erase cycles for the addressed sector. The erase cycle count is stored in the sector erase count (SECV[22:0]) Register, and can be read by using the read any register transaction. The RDYBSY bit is set by the device itself and cleared at the end of the operation, as visible in STR1V[0] when reading status (see “[Transaction table](#)” on page 120).

The transaction requires  $t_{SEC}$  to complete and update the SECV[22:0] Register. The RDYBSY bit (STR1V[0]) may be read to determine when the Sector Erase Count Transaction finished. The SECV[23] bit is used to determine if the reported sector erase count is corrupted and was reset.

#### 4.11.5 Erase related registers and transaction

**Table 40 Erase related registers and transactions**

| Related registers                                                          | Related SPI transactions<br>(see <a href="#">Table 81</a> )   | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|----------------------------------------------------------------------------|---------------------------------------------------------------|---------------------------------------------------------------|
| Status Register 1 (STR1N, STR1V)<br>(see <a href="#">Table 47</a> )        | Write Enable (WRENB_0_0)                                      | Write Enable (WRENB_0_0)                                      |
| Status Register 2 (STR2V)<br>(see <a href="#">Table 50</a> )               | Erase 4KB Sector (ER004_4_0)                                  | Erase 4KB Sector (ER004_4_0)                                  |
| Configuration Register 5 (CFR5N, CFR5V)<br>(see <a href="#">Table 60</a> ) | Erase 256KB Sector (ER256_4_0)                                | Erase 256KB Sector (ER256_4_0)                                |
| ASP PPB Lock (PPLV) (see <a href="#">Table 69</a> )                        | Erase Chip (ERCHP_0_0)                                        | Erase Chip (ERCHP_0_0)                                        |
| ECC Status Register (ECSV)<br>(see <a href="#">Table 64</a> )              | Evaluate Erase Status (EVERS_4_0)                             | Evaluate Erase Status (EVERS_4_0)                             |
| Sector Erase Count Register (SECV)<br>(see <a href="#">Table 73</a> )      | Sector Erase Count (SEERC_4_0)                                | Sector Erase Count (SEERC_4_0)                                |
|                                                                            | Erase Persistent Protection Bit (PPB) Transaction (ERPPB_0_0) | Erase Persistent Protection Bit (PPB) Transaction (ERPPB_0_0) |

## **4.12 Suspend and resume embedded operation**

HL-T/HS-T device can interrupt and suspend the running embedded operations such as erase, program or data Integrity Check. It can also resume the suspended operation once the host finishes the intermediate operation and sends the respective resume transaction to the device.

### **4.12.1 Erase, program or data integrity check suspend**

The suspend transaction allows the system to interrupt a program, erase, or data integrity check operation and then read from any other non erase-suspended sector, non-program-suspended-page, or the array. The Device Ready/Busy Status Flag (RDYBSY) in Status Register 1 (STR1V[0]) must be checked to know when the program, erase, or data integrity check operation has stopped.

#### **4.12.1.1 Program suspend**

- Program suspend is valid only during a programming operation.
- The Program Operation Suspend Status flag (PROGMS) in Status Register-2 (STR2V[0]) can be used to determine if a programming operation has been suspended or was completed at the time RDYBSY changes to 0.
- A program operation can be suspended to allow a read operation.
- Reading at any address within a program-suspended page produces undetermined data.

#### **4.12.1.2 Erase suspend**

- Erase suspend is valid only during a sector erase operation.
- The erase operation Suspend status flag (ERASES) in Status Register-2 (STR2V[1]) can be used to determine if an erase operation has been suspended or was completed at the time RDYBSY changes to 0.
- A chip erase operation cannot be suspended.
- An erase operation can be suspended to allow a program operation or a read operation.
- During an erase suspend, the DIB array can be read to examine sector protection.
- A new erase operation is not allowed with an already suspended erase, program, or data integrity check operation. An erase command is ignored in this situation.
- Reading at any address within an erase-suspended sector produces undetermined data.

#### **4.12.1.3 Data integrity check suspend**

- Data integrity check Suspend is valid only during a Data Integrity Check Calculation operation.
- The memory array data Integrity CRC Suspend Status Flag (DICRCS) in Status Register-2 (STR2V[4]) can be used to determine if a data integrity check operation has been suspended or was completed at the time RDYBSY changes to 0.
- A data integrity check operation can be suspended to allow a read operation.

The write any register or erase persistent protection bit transactions are not allowed during erase, program or data integrity check suspend. It is therefore, not possible to alter the block protection or PPB bits during erase suspend. If there are sectors that may need programming during erase suspend, these sectors should be protected only by DIB bits that can be turned OFF during erase suspend.

The time required for the suspend operation to complete is  $t_{PEDS}$ .

After an erase-suspended program operation is complete, the device returns to the erase-suspend mode. The system can determine the status of the program operation by reading the RDYBSY bit in the Status Register 1, just as in the standard program operation. [Table 41](#) lists the transactions allowed during the suspend operation.

**Table 41 Transactions allowed during suspend**

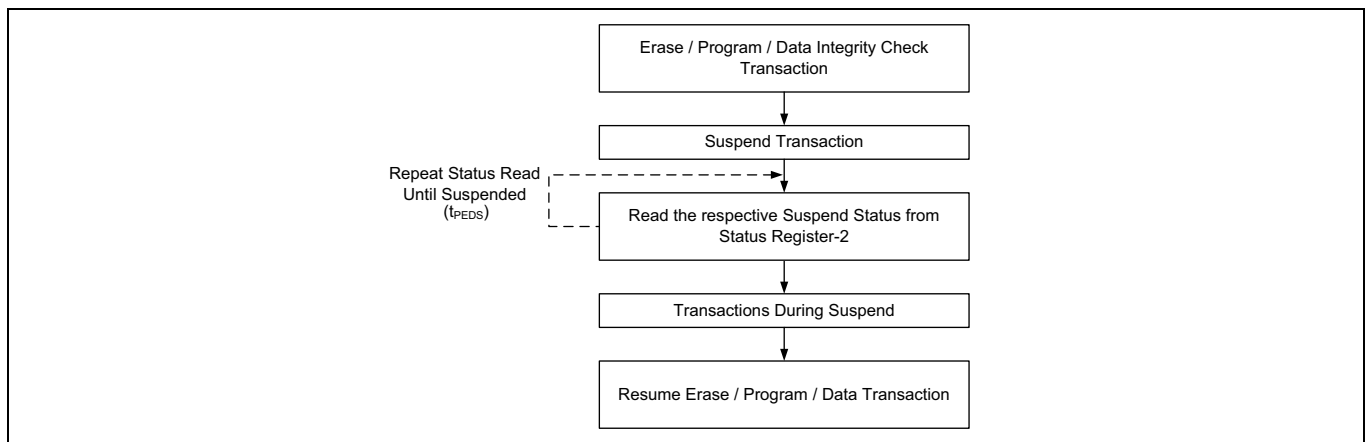
| Transaction name                                                                                  | Allowed during erase suspend | 1. Allowed during program suspend | Allowed during data integrity check suspend |
|---------------------------------------------------------------------------------------------------|------------------------------|-----------------------------------|---------------------------------------------|
| Write Disable (WRDIS_0_0)                                                                         | Yes                          | No                                | No                                          |
| Read Status Register 1 (RDSR1_0_0, RDSR1_4_0)                                                     |                              | Yes                               | Yes                                         |
| Write Enable (WRENB_0_0)                                                                          |                              | No                                | No                                          |
| Read Status Register 2 (RDSR2_0_0, RDSR2_4_0)                                                     |                              | Yes                               | Yes                                         |
| Program Page (PRPGE_4_1)                                                                          |                              | No                                | No                                          |
| Read ECC Status (RDECC_4_0)                                                                       |                              | Yes                               | Yes                                         |
| Clear ECC Status Register (CLECC_0_0)                                                             |                              | Yes                               |                                             |
| Read PPB Lock Bit (RDPLB_0_0, RDPLB_4_0)                                                          |                              |                                   |                                             |
| Resume Program / Erase / Data Integrity Check (RSEPD_0_0)                                         |                              | No                                | No                                          |
| Program SSR (PRSSR_4_1)                                                                           |                              | No                                | No                                          |
| Read SSR (RDSSR_4_0)                                                                              |                              | Yes                               | Yes                                         |
| Read Unique ID (RDUID_0_0, RDUID_4_0)                                                             |                              |                                   |                                             |
| Read SFDP (RSFDP_3_0, RSFDP_4_0)                                                                  |                              |                                   |                                             |
| Read Interface CRC Register (RDCRC_4_0)                                                           |                              |                                   |                                             |
| Read Any Register (RDARG_C_0, RDARG_4_0)                                                          |                              |                                   |                                             |
| Software Reset Enable (SRSTE_0_0)                                                                 |                              |                                   |                                             |
| Clear Program and Erase Failure Flags (CLPEF_0_0)                                                 |                              |                                   |                                             |
| Software Reset (SFRST_0_0)                                                                        |                              |                                   |                                             |
| Read Identification Register (RDIDIN_0_0, RDIDIN_4_0)<br>(manufacturer and device identification) |                              |                                   |                                             |
| Suspend Program / Erase / Data Integrity Check (SPEPD_0_0)                                        |                              | No                                | No                                          |
| Read DYB (RDDYB_4_0)                                                                              |                              | Yes                               | Yes                                         |
| Read PPB (RDPPB_4_0)                                                                              |                              |                                   |                                             |
| Read Octal SDR (RDAY1_4_0)                                                                        |                              |                                   |                                             |
| Read Octal DDR (RDAY2_4_0)                                                                        |                              |                                   |                                             |

#### 4.12.2 Erase, program or data integrity check resume

An Erase, Program or Data Integrity Check Resume transaction must be written to resume a suspended operation. After program or read operations are completed during a Program, Erase, or Data Integrity Check suspend, the Resume transaction is sent to resume the suspended operation.

After an Erase, Program or Data Integrity Check Resume transaction is issued, the RDYBSY bit in Status Register 1 will be set to a 1 and the programming operation will resume if one is suspended. If no program operation is suspended, the suspended erase operation will resume. If there is no suspended program, erase or data integrity check operation, the resume transaction is ignored.

Program, Erase or Data Integrity Check operations may be interrupted as often as necessary. For example, a program suspend transaction could immediately follow a program resume transaction, but for a program or erase operation to progress to completion there must be some period of time between resume and the next suspend transaction greater than or equal to  $t_{PEDRS}$ . **Figure 52** shows the flow of suspend and resume operation.



**Figure 52 Suspend and resume sequence**

#### 4.12.3 Suspend and resume related registers and transactions

**Table 42 Suspend and resume related registers and transactions**

| Related registers                                                   | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|---------------------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| Status Register 1 (STR1N, STR1V)<br>(see <a href="#">Table 47</a> ) | Suspend Erase / Program / Data Integrity Check (SPEPD_0_0)  | Suspend Erase / Program / Data Integrity Check (SPEPD_0_0)    |
| Status Register 2 (STR2V)<br>(see <a href="#">Table 50</a> )        | Resume Erase / Program / Data Integrity Check (RSEPD_0_0)   | Resume Erase / Program / Data Integrity Check (RSEPD_0_0)     |
|                                                                     | Read Any Register (RDARG_C_0)                               | Read Any Register (RDARG_4_0)                                 |
|                                                                     | Read Status Register-1 (RDSR1_0_0)                          | Read Status Register-1 (RDSR1_4_0)                            |
|                                                                     | Read Status Register-2 (RDSR2_0_0)                          | Read Status Register-2 (RDSR2_4_0)                            |

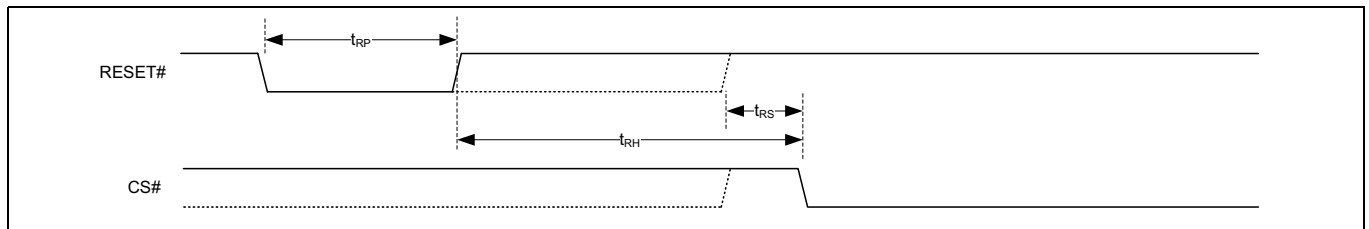
## 4.13 Reset

HL-T/HS-T devices support four types of reset mechanisms.

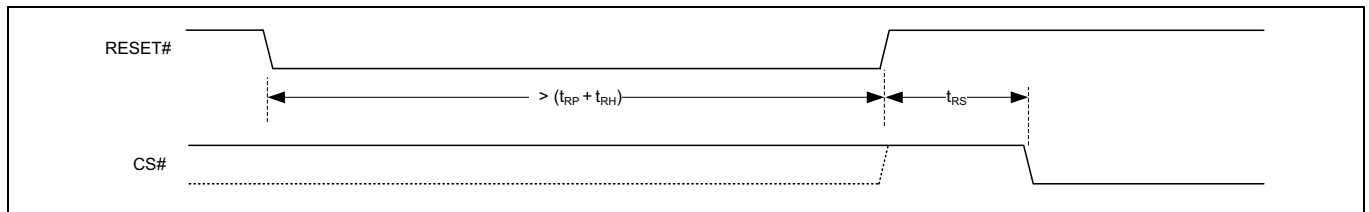
- Hardware reset (using RESET# input pin)
- POR
- CS# signaling reset
- Software reset

### 4.13.1 Hardware reset (using RESET# input pin)

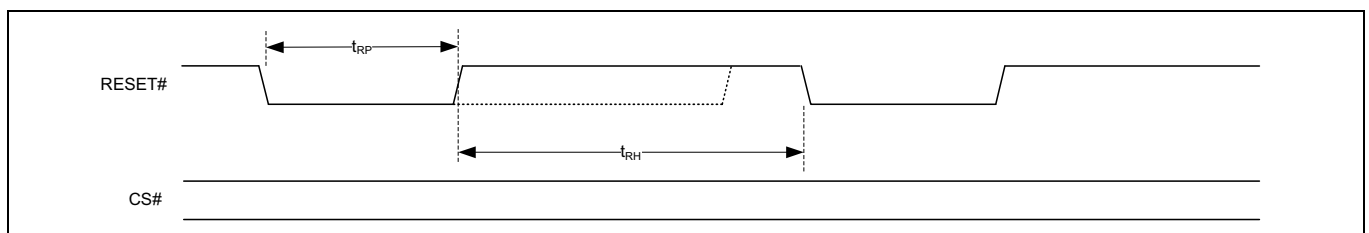
The RESET# input initiates the reset operation with a transition from logic HIGH to logic LOW for  $> t_{RP}$ , and causes the device to perform the full reset process that is performed during POR. The hardware reset process requires a period of  $t_{RH}$  to complete. See [Table 89](#) for timing specifications.



**Figure 53** Hardware reset using RESET# input (reset pulse =  $t_{RP}(\text{Min})$ )



**Figure 54** Hardware reset using RESET# input (reset pulse  $> (t_{RP} + t_{RH})$ )

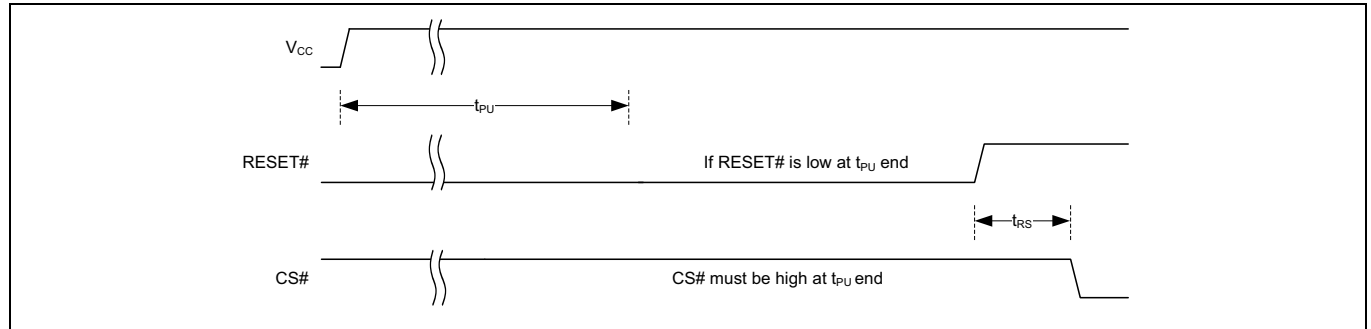


**Figure 55** Hardware reset using RESET# input (back to back hardware reset)

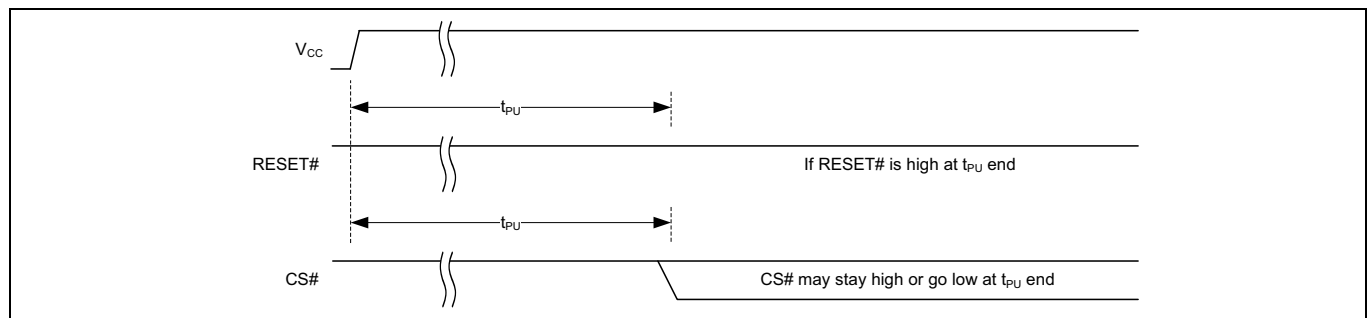
#### 4.13.2 Power-on reset (POR)

The device executes a POR process until a time delay of  $t_{PU}$  has elapsed after the moment that  $V_{CC}$  rises above the minimum  $V_{CC}$  threshold (see [Figure 56](#) and [Figure 57](#)). The device must not be selected during power-up ( $t_{PU}$ ). Therefore, CS# must rise with  $V_{CC}$ . No commands may be sent to the device until the end of  $t_{PU}$ . See [Table 89](#) for timing specifications.

RESET# is ignored during POR. If RESET# is LOW during POR and remains LOW through and beyond the end of  $t_{PU}$ , CS# must remain HIGH until  $t_{RS}$  after RESET# returns HIGH.



**Figure 56** Reset LOW at the end of POR



**Figure 57** Reset HIGH at the end of POR

### 4.13.3 CS# signaling reset

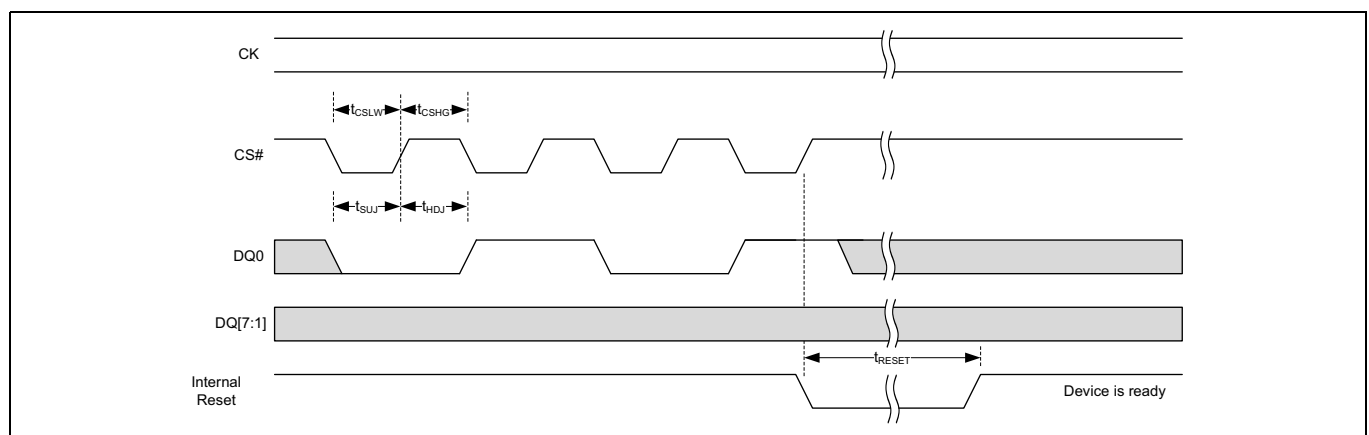
The CS# signaling reset requires CS# and DQ0 signals. This reset method defines a signaling protocol, using existing signals, to initiate an SPI Flash hardware reset, independent of the device operating mode or number of package pins.

The signaling protocol is shown in **Figure 58**. See **Table 89** for timing specifications. The CS# signaling reset steps are as follows:

- CS# is driven active LOW.
- CK remains stable in either HIGH or LOW state.
- CS# and DQ0 are both driven LOW.
- CS# is driven HIGH (inactive).
- Repeat the above four steps, each time alternating the state of DQ0 for a total of four times.
- Reset occurs after the fourth CS# cycle completes and it goes HIGH (inactive).

After the fourth CS# pulse, the slave triggers its internal reset, the device terminates any operation in progress, makes all outputs high impedance, and ignores all read/write transactions for the duration of  $t_{\text{RESET}}$ . Then the device will be in standby state.

This reset sequence is not intended to be used at normal power on, but to be used only when the device is not responding to the system. This reset sequence will be operational from any state that the device may be in. Hence, CS# signaling reset is useful for packages that don't support a RESET# pin to provide behavior identical to Hardware Reset.



**Figure 58** CS# signaling reset protocol

#### 4.13.4 Software reset

Software controlled reset transaction restores the device to its initial power up state, by reloading volatile registers from non-volatile default values except the protection registers. It also terminates the embedded operations. A reset transaction (SFRST\_0\_0) is executed when CS# is brought HIGH at the end of the transaction and requires  $t_{SR}$  time to execute. See [Table 89](#) for timing specifications.

The reset enable (SRSTE\_0\_0) transaction is required immediately before a reset transaction (SFRST\_0\_0) such that a software reset is a sequence of the two transactions. Any transaction other than SFRST\_0\_0 following the SRSTE\_0\_0 transaction will clear the reset enable condition and prevent a later SFRST\_0\_0 transaction from being recognized.

The Reset (SFRST\_0\_0) transaction immediately following a SRSTE\_0\_0 transaction, initiates the software reset process. During software reset, only RDSR1\_4\_0, RDARG\_C\_0, and RDARG\_4\_0 of Status Register 1 are supported operations as long as the volatile and non-volatile configuration states of the device are the same. If the configuration state is changing during software reset, reading Status Register 1 should only be done after the software reset time has elapsed.

The software reset is independent of the state of RESET#. If RESET# is HIGH or Unconnected, and the software reset transactions are issued, the device will perform software reset.

##### 4.13.4.1 Software reset related registers and transactions

**Table 43 Software reset related registers and transactions**

| Related registers | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|-------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| N/A               | Software Reset Enable (SRSTE_0_0)                           | Software Reset Enable (SRSTE_0_0)                             |
|                   | Software Reset (SFRST_0_0)                                  | Software Reset (SFRST_0_0)                                    |

#### 4.13.5 Reset behavior

**Table 44** Reset behavior

| Transaction / register name       | POR                                                                                                                                                                                                                                                                                                                    | Hardware reset and CS# signaling reset                                                                                                                                                                                                                                                                                 | Software reset                                                                                                                                                                                                                                                                 |
|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Summary                           | <ul style="list-style-type: none"> <li>• Device Reset</li> <li>• Status Bits Reset</li> <li>• All Volatile Registers Reset</li> <li>• Configuration Reload to Default</li> <li>• Volatile Protection Reset to Default</li> <li>• Non-volatile Protection unchanged</li> <li>• Reset all Embedded operations</li> </ul> | <ul style="list-style-type: none"> <li>• Device Reset</li> <li>• Status Bits Reset</li> <li>• All Volatile Registers Reset</li> <li>• Configuration Reload to Default</li> <li>• Volatile Protection Reset to Default</li> <li>• Non-volatile Protection unchanged</li> <li>• Reset all Embedded operations</li> </ul> | <ul style="list-style-type: none"> <li>• Device Reset</li> <li>• Status Bits Reset</li> <li>• Configuration Reload to Default</li> <li>• Volatile Protection Reset to Default</li> <li>• Non-volatile Protection unchanged</li> <li>• Reset all Embedded operations</li> </ul> |
| Interface Requirements            | <ul style="list-style-type: none"> <li>• All Inputs - Ignored</li> <li>• All Outputs - Tristated</li> </ul>                                                                                                                                                                                                            | <ul style="list-style-type: none"> <li>• All Inputs - Ignored</li> <li>• All Outputs - Tristated</li> </ul>                                                                                                                                                                                                            | Transactions (SRSTE_0_0, SFRST_0_0)                                                                                                                                                                                                                                            |
| Status Registers                  | Load from Non-volatile Registers                                                                                                                                                                                                                                                                                       | Load from Non-volatile Registers                                                                                                                                                                                                                                                                                       | Load from Non-volatile Registers                                                                                                                                                                                                                                               |
| Configuration Registers           | Load from Non-volatile Registers                                                                                                                                                                                                                                                                                       | Load from Non-volatile Registers                                                                                                                                                                                                                                                                                       | Load from Non-volatile Registers                                                                                                                                                                                                                                               |
| Protection Registers              | PPB Lock Register - Load based on ASPO[2:1]                                                                                                                                                                                                                                                                            | PPB Lock Register - Load based on ASPO[2:1]                                                                                                                                                                                                                                                                            | PPB Lock Register - No Change                                                                                                                                                                                                                                                  |
|                                   | DYB Access Register - Load based on ASPO[4]                                                                                                                                                                                                                                                                            | DYB Access Register - Load based on ASPO[4]                                                                                                                                                                                                                                                                            | DYB Access Register - No Change                                                                                                                                                                                                                                                |
|                                   | Password Register - Load based on ASPO[2] and ASPO[0]                                                                                                                                                                                                                                                                  | Password Register - Load based on ASPO[2] and ASPO[0]                                                                                                                                                                                                                                                                  | Password Register - No Change                                                                                                                                                                                                                                                  |
| ECC Status Register               | Load 0x00                                                                                                                                                                                                                                                                                                              | Load 0x00                                                                                                                                                                                                                                                                                                              | Load 0x00                                                                                                                                                                                                                                                                      |
| AutoBoot Register                 | Load from Non-volatile Registers                                                                                                                                                                                                                                                                                       | Load from Non-volatile Registers                                                                                                                                                                                                                                                                                       | No Change                                                                                                                                                                                                                                                                      |
| Data Integrity Check Register     | Load 0x00                                                                                                                                                                                                                                                                                                              | Load 0x00                                                                                                                                                                                                                                                                                                              | Load 0x00                                                                                                                                                                                                                                                                      |
| Interface CRC Register            | Load 0x00                                                                                                                                                                                                                                                                                                              | Load 0x00                                                                                                                                                                                                                                                                                                              | Load 0x00                                                                                                                                                                                                                                                                      |
| ECC Error Count Register          | Load 0x00                                                                                                                                                                                                                                                                                                              | Load 0x00                                                                                                                                                                                                                                                                                                              | Load 0x00                                                                                                                                                                                                                                                                      |
| Address Trap Register             | Load 0x00                                                                                                                                                                                                                                                                                                              | Load 0x00                                                                                                                                                                                                                                                                                                              | Load 0x00                                                                                                                                                                                                                                                                      |
| Endurance Flex Register           | Load from Non-volatile Registers                                                                                                                                                                                                                                                                                       | Load from Non-volatile Registers                                                                                                                                                                                                                                                                                       | No Change                                                                                                                                                                                                                                                                      |
| I/O Mode                          | Load from Non-volatile Registers                                                                                                                                                                                                                                                                                       | Load from Non-volatile Registers                                                                                                                                                                                                                                                                                       | No Change                                                                                                                                                                                                                                                                      |
| Memory/Register Erase in Progress | Not Applicable                                                                                                                                                                                                                                                                                                         | Abort Erase                                                                                                                                                                                                                                                                                                            | Abort Erase                                                                                                                                                                                                                                                                    |

**Table 44**      **Reset behavior** (Continued)

| Transaction / register name         | POR            | Hardware reset and CS# signaling reset | Software reset |
|-------------------------------------|----------------|----------------------------------------|----------------|
| Memory/Register Program in Progress | Not Applicable | Abort Program                          | Abort Program  |
| Memory/Register Read in Progress    | Not Applicable | Abort Read                             | Not Applicable |
| INT# Pin Configuration Register     | Load 0xFF      | Load 0xFF                              | Load 0xFF      |
| INT# Pin Status Register            | Load 0xFF      | Load 0xFF                              | Load 0xFF      |

## 4.14 Power modes

### 4.14.1 Active power and standby power modes

The device is enabled and in the active power mode when Chip Select (CS#) is LOW. When CS# is HIGH, the device is disabled, but may still be in an active power mode until all program, erase, and write operations have completed. The device then goes into the standby power mode, and power consumption drops to  $I_{SB}$ . See [Table 87](#) for parameter specifications.

### 4.14.2 Deep power down (DPD) mode

Although the standby current during normal operation is relatively low, standby current can be further reduced with the DPD mode. The lower power consumption makes the DPD mode especially useful for battery powered applications.

#### 4.14.2.1 Enter DPD

The device can enter DPD mode in two ways:

1. Enter DPD mode using transaction
2. Enter DPD mode upon power-up or reset

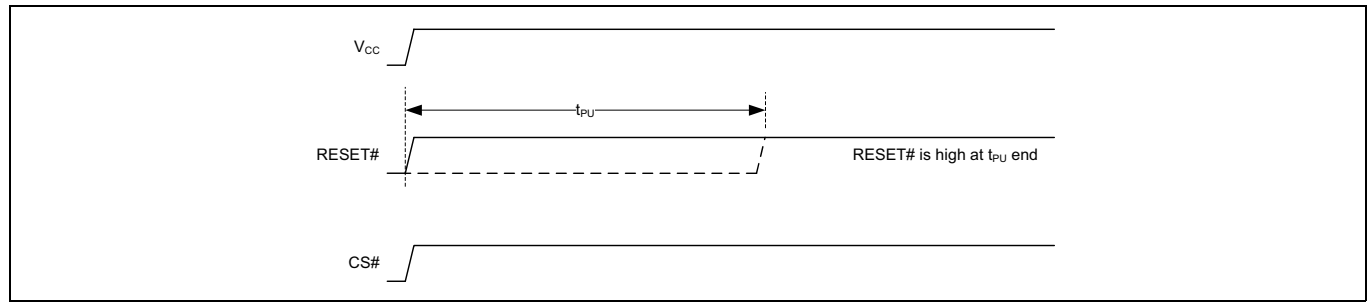
##### Enter DPD mode using the enter deep power down mode transaction

The DPD mode is enabled by sending the Enter Deep Power Down Mode transaction (ENDPD\_0\_0) then waiting for a delay of  $t_{ENTDPD}$ . The CS# pin must be driven HIGH after the command byte has been latched. If this is not done, then the DPD transaction will not be executed. After CS# is driven HIGH, the power-down state will be entered within the time duration of  $t_{ENTDPD}$  (see [Table 89](#) for timing specifications) and power consumption drops to  $I_{DPD}$ . See [Table 87](#) for parameter specifications.

DPD can only be entered from an idle state. The DPD transaction is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register 1 volatile, Device Ready/Busy Status Flag (RDYBSY) bit being cleared to zero (STR1V[0] = RDYBSY = 0). It is not allowed to send any transaction to device during  $t_{ENTDPD}$  time.

##### Enter DPD mode upon power-up or reset

If the DPDPOR configuration bit is enabled (CFR4NV[2] = 1), the device will be in DPD mode after the completion of Power-up, Hardware Reset or CS# Signaling Reset. During POR or Reset the CS# should follow the voltage applied on VCC to enter DPD mode as shown in [Figure 59](#). It is not allowed to send any transaction to device during  $t_{ENTDPD}$  time.



**Figure 59** Enter DPD mode upon power-up or reset

#### 4.14.2.2 Exit DPD

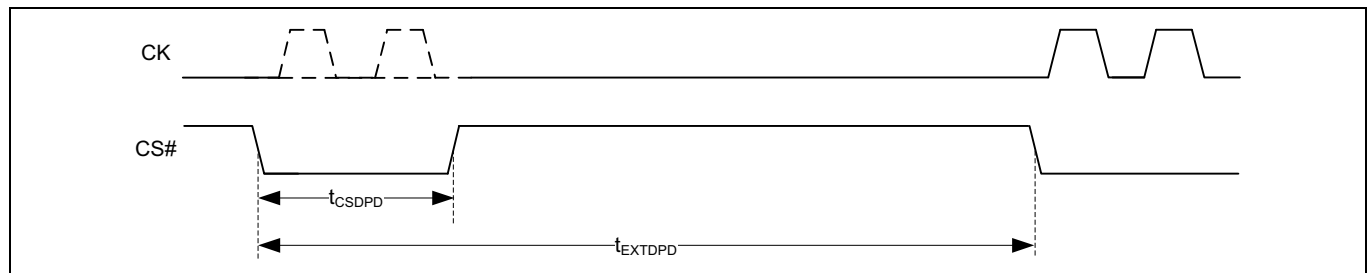
Device leaves DPD mode in one of the following ways:

##### Exit DPD mode upon hardware reset

When the device is in DPD and  $CFR4NV[2] = 0$ , a hardware reset will return the device to standby mode.

##### Exit DPD mode upon CS# pulse

Device exits DPD upon receipt of  $CS\#$  pulse of width  $t_{CSDPD}$ . The  $CS\#$  should be driven HIGH after the pulse. HIGH to LOW transition on  $CS\#$  is required to start a transaction cycle after the DPD exit. It takes  $t_{EXTDPD}$  to come out of DPD mode. The device will not respond until after  $t_{EXTDPD}$ .



**Figure 60** Exit DPD mode

The device maintains its configuration during DPD, meaning the device exits DPD in the same state as it entered. Registers such as the ECC status, ECC error detection counter, address trap, and interrupt status registers will be cleared.

#### 4.14.2.3 DPD related registers and transactions

**Table 45** DPD related registers and transactions

| Related registers                                                       | Related SPI transactions<br>(see <a href="#">Table 81</a> ) | Related octal transactions<br>(see <a href="#">Table 82</a> ) |
|-------------------------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------|
| Configuration Register 4 (CFR4N, CFR4V) (see <a href="#">Table 58</a> ) | Enter Deep Power Down Mode (ENDPD_0_0)                      | Enter Deep Power Down Mode (ENDPD_0_0)                        |

## 4.15 Power up and power down

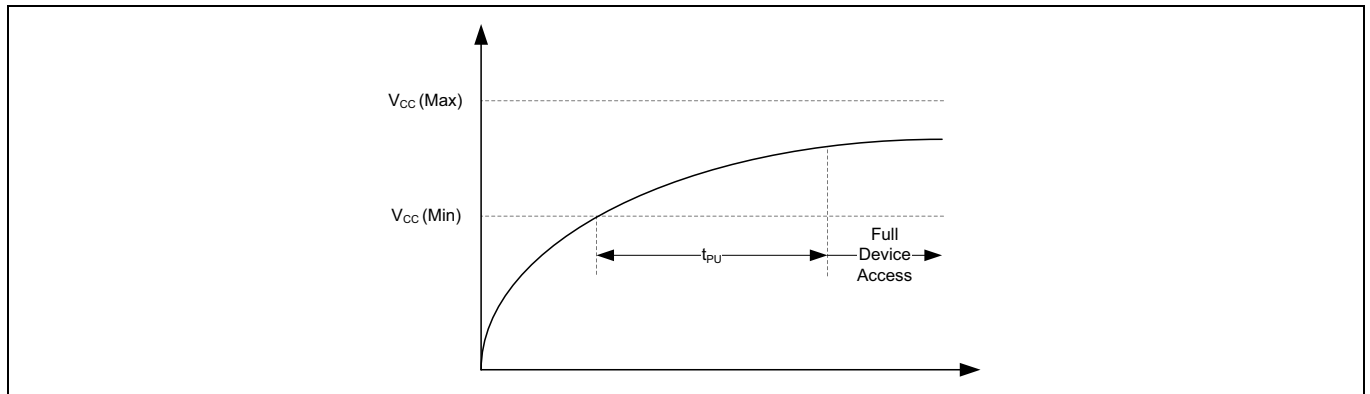
The device must not be selected at power up or power down until  $V_{CC}$  reaches the correct value as follows:

- $V_{CC}$  (min) at power up, and then for a further delay of  $t_{PU}$
- $V_{SS}$  at power down

### 4.15.1 Power up

The device ignores all transactions until a time delay of  $t_{PU}$  has elapsed after the moment that  $V_{CC}$  rises above the minimum  $V_{CC}$  threshold (see [Figure 61](#)). However, correct operation of the device is not guaranteed if  $V_{CC}$  returns below  $V_{CC}$  (min) during  $t_{PU}$ . No command should be sent to the device until the end of  $t_{PU}$ .

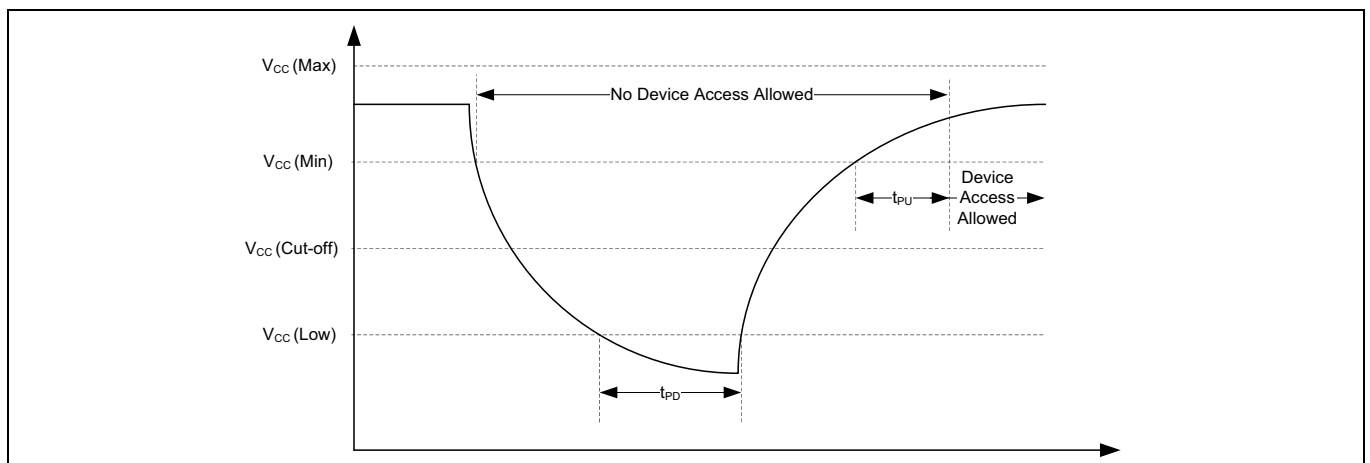
The device draws  $I_{POR}$  current during  $t_{PU}$ . After power up ( $t_{PU}$ ), the WRPGEN bit is reset and there is the option to be in the DPD mode or standby mode. The DPDPOR bit in Configuration Register 4 (CFR4N[2]) controls if the device will be in DPD or standby mode after the completion of POR (see [Table 58](#)). If the DPDPOR bit is enabled (CFR4N[2] = 1) the device is in DPD mode after power up. A hardware reset (RESET#) required to return the device to Standby mode after POR.



**Figure 61** Power up

### 4.15.2 Power down

During power down or voltage drops below  $V_{CC}(\text{cut-off})$ , the voltage must drop below  $V_{CC}(\text{LOW})$  for a period of  $t_{PD}$  for the part to initialize correctly on power up (see [Figure 62](#)). If during a voltage drop the  $V_{CC}$  stays above  $V_{CC}(\text{cut-off})$  the part will stay initialized and will work correctly when  $V_{CC}$  is again above  $V_{CC}(\text{min})$ . In the event POR did not complete correctly after power up, the assertion of the RESET# signal will restart the POR process.

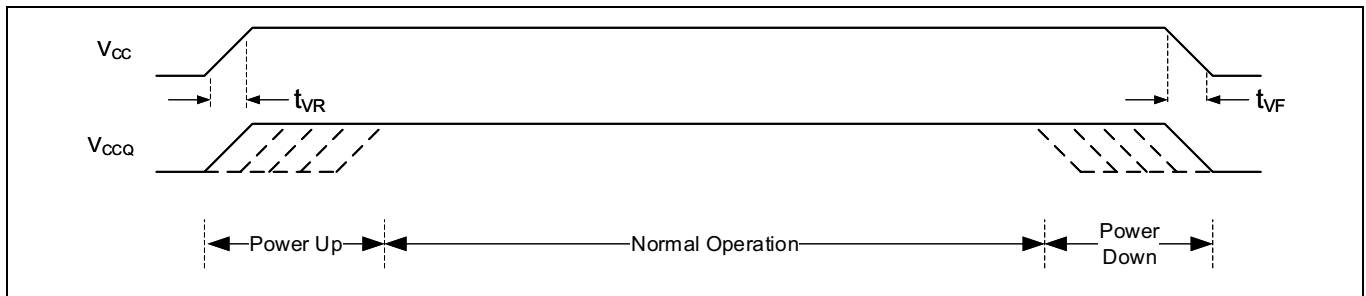


**Figure 62** Power down and voltage drop

### 4.15.3 Power up and power down sequence

The following power sequence needs to be followed for the guaranteed reliable operation of HL-T/HS-T devices:

- Apply  $V_{CC}$  before  $V_{CCQ}$  during power up sequence.  $V_{CC}$  and  $V_{CCQ}$  can be applied simultaneously during power up, as long as  $V_{CCQ}$  does not exceed  $V_{CC}$ .
- During the power down mode, reduce the  $V_{CCQ}$  before  $V_{CC}$ .  $V_{CC}$  and  $V_{CCQ}$  can be reduced simultaneously during power down, as long as  $V_{CCQ}$  does not exceed  $V_{CC}$ .
- It is recommended to keep  $V_{CCQ} \leq V_{CC}$ .



**Figure 63** Power up and power down sequence

## 5 Registers

Registers are small groups of storage cells used to configure as well as report the status of the device operations. HL-T/HS-T family of devices use separate non-volatile and volatile storage groups to implement the different register bit types for legacy compatibility as well as new functionality. Each register is organized as a group of volatile bits with associated non-volatile bits (if permanence is required). During power-up, hardware reset or software reset, the data in the non-volatile bits of the register is transferred to the volatile bits to provide the default state of the volatile bits. When writing new data to non-volatile bits of the register, the volatile bits are also updated with the new data. However, when writing new data to the volatile register bits the non-volatile bits retain the old data. The register structure is shown in [Figure 64](#).

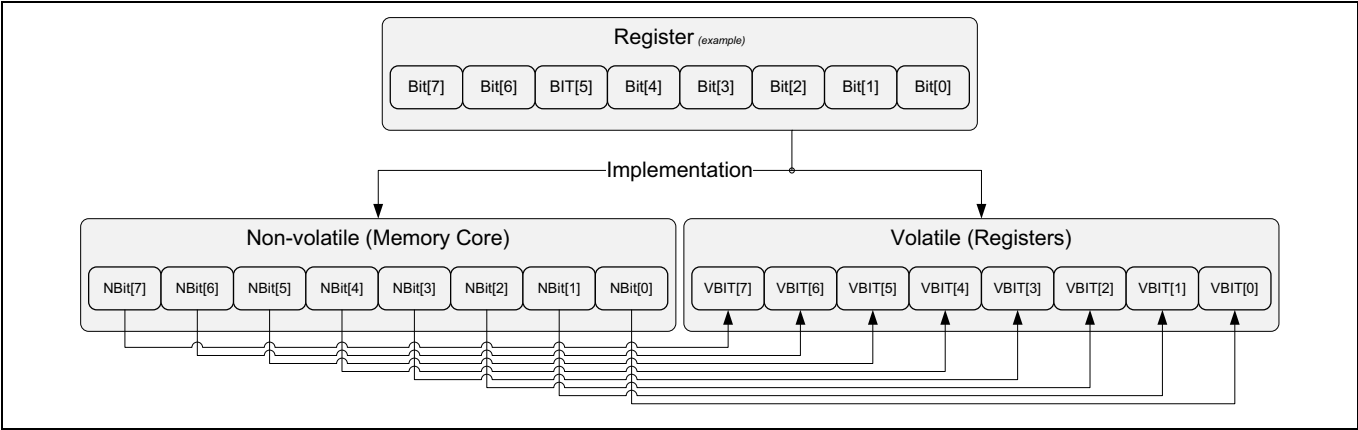


Figure 64 Register structure

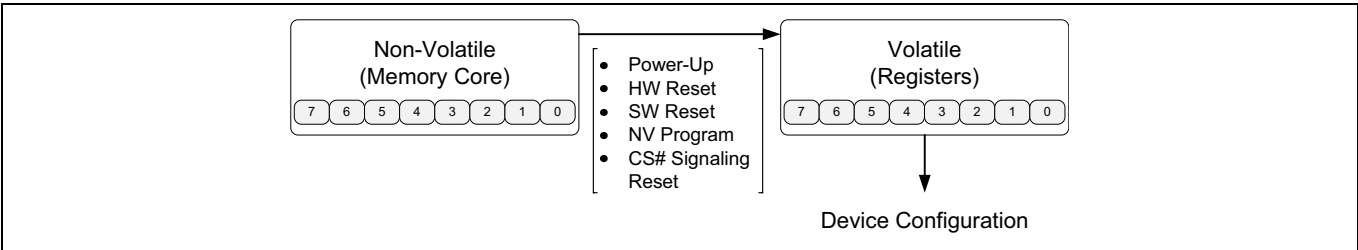


Figure 65 Data movement within register components

## 5.1 Register naming convention

**Table 46** Register bit description convention

| Bit number                                          | Name | Function | Read/write                                                                                                              | Factory default (binary)    | Description                                                                                                                                                                                                                                      |
|-----------------------------------------------------|------|----------|-------------------------------------------------------------------------------------------------------------------------|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REGNAME#T[x]<br>T = N, V, O<br><br>Descending order | –    | –        | Possible options:<br>N/A - Not applicable<br>R - Readable only<br>R/W - Readable and writable<br>R/1 - Readable and OTP | Possible options:<br>0<br>1 | Format:<br>Description of the configuration bit<br><br>Options:<br>0 = Option '0' selection of the bit<br>1 = Option '1' selection of the bit<br><br>Dependency: Is this bit part of a function which requires multiple bits for implementation? |

## 5.2 Status Register 1 (STR1x)

Status Register 1 contains both status and control bits. The functionality of supported Status Register 1 type is described in [Table 47](#).

**Table 47** Status register 1<sup>[22]</sup>

| Bit number           | Name   | Function                      | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------------------|--------|-------------------------------|------------------------------------------------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STR1N[7]<br>STR1V[7] | RESRVD | Reserved for Future Use       | N->R<br>V->R                                   | 0                        | This bit is Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| STR1V[6]             | PRGERR | Programming Error Status Flag | V -> R                                         | 0                        | Description: The PRGERR bit indicates program operation success or failure. When the PRGERR bit is set to a '1', it indicates that there was an error in the last programming operation. PRGERR bit is also set when a program operation is attempted within a protected memory region. When PRGERR is set, it can only be cleared with the Clear Program and Erase Failure Flags (CLPEF_0_0) transaction or a hardware/software reset.<br><b>Note</b> The device will only go to standby mode once the PRGERR flag is cleared.<br>Selection Options:<br>0 = Last programming operation was successful<br>1 = Last programming operation was unsuccessful<br>Dependency: N/A |

**Note**

22.STR1x value during POR, Hardware Reset, Software Reset, DPD Exit, and CS# Signaling Reset is not valid.

Registers

**Table 47**      **Status register 1<sup>[22]</sup>** (Continued)

| Bit number               | Name         | Function                                                  | Read/Write<br>N = Non-volatile<br>V = Volatile                                                            | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------------------------|--------------|-----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STR1V[5]                 | ERSERR       | Erasing Error Status Flag                                 | V -> R                                                                                                    | 0                           | <p>Description: The ERSERR bit indicates erase operation success or failure. When the ERSERR bit is set to a '1', it indicates that there was an error in the last erasing operation. ERSERR bit is also set when a erase operation is attempted within a protected memory sector. When ERSERR is set, it can only be cleared with the Clear Program and Erase Failure Flags (CLPEF_0_0) transaction or a hardware/software reset.</p> <p><b>Note</b> The device will only go to standby mode once the ERSERR flag is cleared.</p> <p>Selection Options:<br/> 0 = Last erase operation was successful<br/> 1 = Last erase operation was unsuccessful<br/> Dependency: N/A</p>                                                                                           |
| STR1N[4:2]<br>STR1V[4:2] | LBPROT [2:0] | Legacy Block Protection based Memory Array size selection | <p>If PLPROT = 0<br/> N -&gt; R/W<br/> V -&gt; R/W</p> <p>If PLPROT = 1<br/> N -&gt; R<br/> V -&gt; R</p> | 000                         | <p>Description: The LBPROT[2:0] bits define the memory array size to be protected against program and erase transactions. Based on the LBPROT[2:0] configuration, either top 1/64, 1/4, 1/2, etc. or bottom 1/64, 1/4, 1/2, etc., or up to the entire array is protected.</p> <p><b>Note</b> If PLPROT bit - Permanent Locking selection of Legacy Block Protection and 4KB Sector Architecture (CFR1x[4]) is set to a '1', the LBPROT[2:0] bits cannot be erased or programmed.</p> <p>Selection Options:<br/> 000 = Protection is disabled<br/> 001 = 1/64th of the (top/bottom) array protection is enabled<br/> 010 = 1/32nd of the (top/bottom) array protection is enabled<br/> .....<br/> 111 = All sectors are protected<br/> Dependency: TBPROT (CFR1x[5])</p> |

**Note**

22.STR1x value during POR, Hardware Reset, Software Reset, DPD Exit, and CS# Signaling Reset is not valid.

**Table 47**      **Status register 1<sup>[22]</sup>** (Continued)

| Bit number | Name   | Function                         | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------|--------|----------------------------------|------------------------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STR1V[1]   | WRPGEN | Write/Program Enable Status Flag | V -> R                                         | 0                           | <p>Description:<br/> The WRPGEN bit must be set to '1' to enable all program, erase or register write operations - it provides protection against inadvertent changes to memory or register values. The Write Enable (WRENB_0_0) transaction set the WRPGEN bit to '1' to allow program, erase or write transactions to execute. The Write Disable (WRDIS_0_0) transaction resets WRPGEN to a '0' to prevent all program, erase, and write transactions from execution. The WRPGEN bit is cleared to '0' at the end of any successful program, erase or register write operation. After a power down / power up sequence or a hardware/software reset, the Deep Power Down WRPGEN bit is cleared to '0'.</p> <p>Selection Options:<br/> 0 = Program, erase or register write is disabled<br/> 1 = Program, erase or register write is enabled<br/> Dependency: N/A</p> |
| STR1V[0]   | RDYBSY | Device Ready/Busy Status Flag    | V -> R                                         | 0                           | <p>Description:<br/> The RDYBSY bit indicates whether the device is performing an embedded operation or is in standby mode ready to receive new transactions.</p> <p><b>Note</b> The PRGERR and ERSERR status bits are updated while RDYBSY is set. If PRGERR or ERSERR are set, the RDYBSY bit will remain set indicating the device is busy and unable to receive new transactions. A Clear Program and Erase Failure Flags (CLPEF_0_0) transaction must be executed to return the device to standby mode.</p> <p>Selection Options:<br/> 0 = Device is in standby mode ready to receive new operation transactions<br/> 1 = Device is busy and unable to receive new operation transactions<br/> Dependency: N/A</p>                                                                                                                                                |

**Note**

22.STR1x value during POR, Hardware Reset, Software Reset, DPD Exit, and CS# Signaling Reset is not valid.

**Table 48 PRGERR summary**

| Error flag    | Symbol | Conditions                                                                                                          |
|---------------|--------|---------------------------------------------------------------------------------------------------------------------|
| Program Error | PRGERR | Bits cannot be programmed '1' to '0'                                                                                |
|               |        | Trying to program in a protected region                                                                             |
|               |        | If ASP0[2] or ASP0[1] is 0, any non-volatile register write attempting to change the value of CFR1N[6:2]/CFR1V[6:2] |
|               |        | After the Password Protection Mode is selected and ASP Password Register update transaction executed                |
|               |        | SafeBoot Failure                                                                                                    |
|               |        | Configuration Failure                                                                                               |

**Table 49 ERSERR summary**

| Error flag  | Symbol | Conditions                                                                                |
|-------------|--------|-------------------------------------------------------------------------------------------|
| Erase Error | ERSERR | Sector Device Erase - All bits cannot be erased to '1's                                   |
|             |        | Trying to erase a protected region                                                        |
|             |        | Register Erase - All bits cannot be erased to '1's during Erase portion of Register Write |
|             |        | SafeBoot Failure                                                                          |

### 5.3 Status Register 2 (STR2x)

Status Register 2 provides device status on operations. The functionality of supported Status Register 2 type is described in [Table 50](#).

**Table 50** Status Register 2<sup>[23]</sup>

| Bit number | Name   | Function                                                                | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------------|--------|-------------------------------------------------------------------------|------------------------------------------------|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STR2V[7:5] | RESRVD | Reserved for Future Use                                                 | V -> R                                         | 0                              | This bit is Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| STR2V[4]   | DICRCS | Memory Array Data Integrity Cyclic Redundancy Check Suspend Status Flag | V -> R                                         | 0                              | Description: The DICRCS bit is used to determine when the device is in Memory Array Data Integrity Cyclic Redundancy Check suspend mode.<br>Selection Options:<br>0 = Memory Array Data Integrity Cyclic Redundancy Check is not in suspend mode<br>1 = Memory Array Data Integrity Cyclic Redundancy Check is in suspend mode<br>Dependency: N/A                                                                                                                                                                                                                                                                |
| STR2V[3]   | DICRCA | Memory Array Data Integrity Cyclic Redundancy Check Abort Status Flag   | V -> R                                         | 0                              | Description: The DICRCA bit indicates that the Memory Array Data Integrity CRC calculation operation was aborted. The abort condition is based on ending address (ENDADD) and starting address (STRADD) relationship. If $ENDADD < STRADD + 3$ , then DICRCA will be set and the device will return to the Standby state. DICRCA flag gets cleared at the next Data Integrity CRC calculation operation when $ENDADD \geq STRADD + 3$ .<br>Selection Options:<br>0 = Memory Array Data Integrity CRC calculation is not aborted<br>1 = Memory Array Data Integrity CRC calculation is aborted<br>Dependency: N/A |
| STR2V[2]   | SESTAT | Sector Erase Success/Failure Status Flag                                | V -> R                                         | 0                              | Description: The SESTAT bit indicates whether the erase operation on the sector completed successfully. Evaluate Erase Status transaction (EVERS_4_0) must be executed prior to reading SESTAT bit which specifies the sector address.<br>Selection Options:<br>1 = Addressed sector (EVERS_4_0) was erased successfully<br>0 = Addressed sector (EVERS_4_0) was not erased successfully<br>Dependency: N/A                                                                                                                                                                                                      |

**Table 50**      **Status Register 2<sup>[23]</sup> (Continued)**

| Bit number | Name   | Function                                    | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                                 |
|------------|--------|---------------------------------------------|------------------------------------------------|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STR2V[1]   | ERASES | Erase operation<br>Suspend Status<br>Flag   | V -> R                                         | 0                              | Description: The ERASES bit is used to indicate if the Erase operation is suspended.<br>Selection Options:<br>0 = Erase operation is not in suspend mode<br>1 = Erase operation is in suspend mode<br>Dependency: N/A       |
| STR2V[0]   | PROGMS | Program operation<br>Suspend Status<br>Flag | V -> R                                         | 0                              | Description: The PROGMS bit is used to indicate if the Program operation is suspended.<br>Selection Options:<br>0 = Program operation is not in suspend mode<br>1 = Program operation is in suspend mode<br>Dependency: N/A |

**Note**

23.STR2x value during POR, Hardware Reset, Software Reset, DPD Exit, and CS# Signaling Reset is not valid.  
STR2x bits are valid only when STR1V[0] / RDYBSY = 0.

## 5.4 Configuration Register 1 (CFR1x)

Configuration Register 1 controls interface and data protection functions.

**Table 51 Configuration Register 1**

| Bit number           | Name   | Function                                                          | Read/Write<br>N = Non-volatile<br>V = Volatile                               | Factory default (binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------------------|--------|-------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFR1N[7]<br>CFR1V[7] | RESRVD | Reserved for Future Use                                           | N -> R/W<br>V -> R/W                                                         | 0                        | This bit is Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| CFR1N[6]<br>CFR1V[6] | SP4KBS | Split 4 KB Sectors selection between top and bottom address space | If PLPROT = 0<br>N -> R/W<br>V -> R<br><br>If PLPROT = 1<br>N -> R<br>V -> R | 0                        | Description: The SP4KBS bit selects whether the 4 KB sectors are grouped together or evenly split between High and LOW address ranges.<br>Selection Options:<br>0 = 4 KB Sectors are grouped together<br>1 = 4 KB Sectors are split between High and Low Addresses<br>Dependency: TB4KBS(CFR1N[2])                                                                                                                                                                                                                                                                                                                                                                |
| CFR1N[5]<br>CFR1V[5] | TBPROT | Top or Bottom Protection selection for Legacy Protection Mode     | If PLPROT = 0<br>N -> R/W<br>V -> R<br><br>If PLPROT = 1<br>N -> R<br>V -> R | 0                        | Description: The TBPROT bit selects the reference point of the Legacy Block Protection bits (LBPROT[2:0]) in the Status Register on whether the protection starts from the top or starts from the bottom of the address range.<br>The bit also selects a memory address range (lowest or highest) to remain readable is available for reading during Read Password Protection mode even before a successful Password entry is completed.<br>Selection Options:<br>0 = Legacy Protection is applicable in the top half of the address range<br>1 = Legacy Protection is applicable in the bottom half of the address range<br>Dependency: LBPROT[2:0] (STR1x[3:1]) |

**Table 51 Configuration Register 1 (Continued)**

| Bit number           | Name   | Function                                                                            | Read/Write<br>N = Non-volatile<br>V = Volatile                               | Factory default (binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------------|--------|-------------------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFR1N[4]<br>CFR1V[4] | PLPROT | Permanent Locking selection of Legacy Block Protection and 4 KB Sector Architecture | N -> R/1<br>V -> R                                                           | 0                        | Description: The PLPROT bit permanently protects the Legacy Block Protection and 4 KB Sector location. It thereby permanently protects the memory array protection scheme and sector architecture.<br><b>Note</b> PLPROT protects LBPROT[2:0], SP4KBS, TBPROT, and TB4KBS bits from program and erase, and it is recommended to configure these bits before configuring the PLPROT bit.<br>Selection Options:<br>0 = Legacy Block Protection and 4 KB Sector Location are not protected<br>1 = Legacy Block Protection and 4 KB Sector Location are protected<br>Dependency: N/A |
| CFR1N[3]<br>CFR1V[3] | RESRVD | Reserved for Future Use                                                             | N -> R/W<br>V -> R/W                                                         | 0                        | This bit is Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| CFR1N[2]<br>CFR1V[2] | TB4KBS | Top or Bottom Address Range selection for 4 KB Sector Block                         | If PLPROT = 0<br>N -> R/W<br>V -> R<br><br>If PLPROT = 1<br>N -> R<br>V -> R | 0                        | Description:<br>The TB4KBS bit defines the logical address location of the 4 KB sector block. The 4 KB sector block replaces the fitting portion of the highest or lowest address sector.<br>Selection Options:<br>0 = 4 KB Sector Block is in the bottom of the memory address space<br>1 = 4 KB Sector Block is in the top of the memory address space<br>Dependency: SP4KBS (CFR1x[6])                                                                                                                                                                                        |

**Table 51 Configuration Register 1 (Continued)**

| Bit number           | Name   | Function                                                                       | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------------------|--------|--------------------------------------------------------------------------------|------------------------------------------------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFR1N[1]<br>CFR1V[1] | RESRVD | Reserved for Future Use                                                        | N -> R/W<br>V -> R/W                           | 0                        | This bit is Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| CFR1N[0]<br>CFR1V[0] | TLPROT | Temporary Locking selection of Legacy Block Protection and Sector Architecture | N -> R<br>V -> R/W                             | 0                        | <p>Description:<br/> The TLPROT bit temporarily protects the Legacy Block Protection and 4 KB Sector location. Upon power-up or a hardware reset, TLPROT is set to its default state. When selected, it protects the memory array protection scheme and sector architecture from any changes.</p> <p><b>Note</b> TLPROT protects LBPROT[2:0], SP4KBS, TBPROT, and TB4KBS bits from program and erase.</p> <p>Selection Options:<br/> 0 = Legacy Block Protection and 4 KB Sector Location are not protected<br/> 1 = Legacy Block Protection and 4 KB Sector Location are temporarily protected</p> <p>Dependency: N/A</p> |

**Table 52 4KB parameter sector location selection**

| SP4KBS | TB4KBS | 4 KB location                                                                       |
|--------|--------|-------------------------------------------------------------------------------------|
| 0      | 0      | 4KB physical sectors at bottom (Low address)                                        |
| 0      | 1      | 4KB physical sectors at top, (High address)                                         |
| 1      | X      | 4KB Parameter sectors are split between top (High Address) and bottom (Low Address) |

**Table 53 PLPROT and TLPROT protection**

| PLPROT | TLPROT | Array protection and 4K sector                                            |
|--------|--------|---------------------------------------------------------------------------|
| 0      | 0      | Unprotected (Unlocked)                                                    |
| 1      | X      | TBPROT, LBPROTx, SP4KBS, TB4KBS - Permanently Protected (Locked)          |
| 0      | 1      | TBPROT, LBPROTx, SP4KBS, TB4KBS - Protected (Locked) till next Power-down |

## 5.5 Configuration register 2 (CFR2x)

Configuration Register 2 controls memory read latency and address byte length selection.

**Table 54 Configuration register 2**

| Bit number               | Name        | Function                                                                            | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------------------------|-------------|-------------------------------------------------------------------------------------|------------------------------------------------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFR2N[7]<br>CFR2V[7]     | ADRBYT      | Address Byte Length selection between 3 or 4 bytes for Instructions                 | N -> R/W<br>V -> R/W                           | 0                           | <p>Description:<br/>The ADRBYT bit controls the expected address length for all instructions that require address and is selectable between 3 Bytes or 4 Bytes.</p> <p>Selection Options:<br/>0 = Instructions will use 3 Bytes for address<br/>1 = Instructions will use 4 Bytes for address</p> <p>Dependency: N/A</p>                                                                                                                                                                                              |
| CFR2N[6:4]<br>CFR2V[6:4] | RESRVD      | Reserved for Future Use                                                             | N -> R/W<br>V -> R/W                           | 000                         | These bits are Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                                                                                                                                                                                  |
| CFR2N[3:0]<br>CFR2V[3:0] | MEMLAT[3:0] | Memory Array Read Latency selection - Dummy cycles required for initial data access | N -> R/W<br>V -> R/W                           | 1000                        | <p>Description: The MEMLAT[3:0] bits control the read latency (dummy cycles) delay in all variable latency memory array and non-volatile register read transactions. MEMLAT selection allows the user to adjust the read latency during normal operation based on different operating frequencies.</p> <p>Selection Options:<br/>0000 = 0/5 Latency Cycles<br/>Selection based on transaction opcodes<br/>.....<br/>1111 = 15/28 Latency Cycles<br/>Selection based on transaction opcodes</p> <p>Dependency: N/A</p> |

**Table 55** Latency code (cycles) versus frequency<sup>[24, 25, 27]</sup>

| Latency code | Number of cycles<br>(1-1-1, 1-1-8 / 8-8-8) | SDR SPI read transactions (MHz)<br>(1S-1S-1S / 1S-1S-8S)                                   | SDR octal read transactions (MHz)<br>(8S-8S-8S)                               | DDR octal read transactions (MHz)<br>(8D-8D-8D)                               |
|--------------|--------------------------------------------|--------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|              |                                            | RDAY2_C_0<br>RDSSR_4_0<br>RDARG_C_0 <sup>[26]</sup><br>RDECC_4_0<br>RDPPB_4_0<br>RDAY3_4_0 | RDAY1_4_0<br>RDSSR_4_0<br>RDARG_4_0 <sup>[26]</sup><br>RDECC_4_0<br>RDPPB_4_0 | RDAY2_4_0<br>RDSSR_4_0<br>RDARG_4_0 <sup>[26]</sup><br>RDECC_4_0<br>RDPPB_4_0 |
| 0000         | 0 / 5                                      | 50                                                                                         | 50                                                                            | 42                                                                            |
| 0001         | 1 / 6                                      | 68                                                                                         | 64                                                                            | 57                                                                            |
| 0010         | 2 / 8                                      | 81                                                                                         | 92                                                                            | 85                                                                            |
| 0011         | 3 / 10                                     | 93                                                                                         | 121                                                                           | 107                                                                           |
| 0100         | 4 / 12                                     | 106                                                                                        | 150                                                                           | 121                                                                           |
| 0101         | 5 / 14                                     | 118                                                                                        | 166 (HL-T) / 178 (HS-T)                                                       | 135                                                                           |
| 0110         | 6 / 16                                     | 131                                                                                        | 200                                                                           | 150                                                                           |
| 0111         | 7 / 18                                     | 143                                                                                        | 200                                                                           | 164                                                                           |
| 1000         | 8 / 20                                     | 156                                                                                        | 200                                                                           | 166 (HL-T) / 178 (HS-T)                                                       |
| 1001         | 9 / 22                                     | 166                                                                                        | 200                                                                           | 192                                                                           |
| 1010         | 10 / 23                                    | 166                                                                                        | 200                                                                           | 200                                                                           |
| 1011         | 11 / 24                                    | 166                                                                                        | 200                                                                           | 200                                                                           |
| 1100         | 12 / 25                                    | 166                                                                                        | 200                                                                           | 200                                                                           |
| 1101         | 13 / 26                                    | 166                                                                                        | 200                                                                           | 200                                                                           |
| 1110         | 14 / 27                                    | 166                                                                                        | 200                                                                           | 200                                                                           |
| 1111         | 15 / 28                                    | 166                                                                                        | 200                                                                           | 200                                                                           |

**Notes**

24. When using the ECC error reporting mechanisms, the read output data must be at least 2 bytes for correct ECC reporting.
25. CK frequency > 200 MHz SDR, or > 200 MHz DDR is not supported by HS-T family of devices and CK frequency > 166 MHz SDR, or > 166 MHz DDR is not supported by HL-T family of devices.
26. RDARG\_C\_0 and RDARG\_4\_0 uses these latency cycles for reading non-volatile registers.
27. RSFDP\_3\_0 always have a dummy cycle of eight and the maximum frequencies for different interfaces related to eight dummy cycles.

## 5.6 Configuration Register 3 (CFR3x)

Configuration Register 3 controls transaction behavior.

**Table 56 Configuration Register 3**

| Bit number               | Name        | Function                                                                                 | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------------------|-------------|------------------------------------------------------------------------------------------|------------------------------------------------|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFR3N[7:6]<br>CFR3V[7:6] | VRGLAT[1:0] | Volatile Register Read Latency selection - Dummy cycles required for initial data access | N -> R/W<br>V -> R/W                           | 00                          | Description: The VRGLAT[1:0] bits control the read latency (dummy cycles) delay in all variable latency register read transactions. VRGLAT[1:0] selection allows the user to adjust the read latency during normal operation based on different operating frequencies.<br><br>Selection Options:<br>00, 01, 10, 11 Latency Cycles<br>Selection based on transaction opcodes<br><br>Dependency: N/A                                                                                                                                               |
| CFR3N[5]<br>CFR3V[5]     | BLKCHK      | Blank Check selection during Erase operation for better endurance                        | N -> R/W<br>V -> R/W                           | 0                           | Description: When this feature is enabled an erase transaction first evaluates the erase status of the sector. If the sector is found to erased, the erase operation is aborted. In other words, the erase operation is only executed if programmed bits are found in the sector. Disabling BLKCHK executes an erase operation unconditionally.<br><br>Selection Options:<br>0 = Blank Check is disabled before executing an erase operation<br>1 = Blank Check evaluation is enabled before executing an erase operation<br><br>Dependency: N/A |
| CFR3N[4]<br>CFR3V[4]     | PGMBUF      | Program Buffer Size selection                                                            | N -> R/W<br>V -> R/W                           | 0                           | Description: The PGMBUF bit selects the Programming Buffer size which is used for page programming. Program buffer size affects the device programming time.<br><b>Note</b> If programming data exceeds the program buffer size, data gets wrapped.<br><br>Selection Options:<br>0 = 256 Byte Write Buffer Size<br>1 = 512 Byte Write Buffer Size<br><br>Dependency: N/A                                                                                                                                                                         |

**Table 56 Configuration Register 3 (Continued)**

| Bit number           | Name   | Function                                        | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------------------|--------|-------------------------------------------------|------------------------------------------------|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFR3N[3]<br>CFR3V[3] | UNHYSA | Uniform or Hybrid Sector Architecture Selection | N -> R/W<br>V -> R                             | 0                        | <p>Description: The UNHYSA bit selects between uniform (all 256 KB sectors) or hybrid (4 KB sectors and 256 KB sectors) sector architecture. If hybrid sector architecture is selected, 4 KB sector block is made part of the main Flash array address map. The 4 KB sector block can overlay at either the highest or the lowest address range of the device. If uniform sector architecture is selected, 4KB sector block is removed from the address map and all sectors are of uniform size.</p> <p><b>Note</b> Hybrid sector architecture also enables 4 KB Sector Erase transaction (20h). Otherwise, 4 KB Sector Erase transaction, if issued, is ignored by the device.</p> <p>Selection Options:<br/> 0 = Hybrid Sector Architecture (combination of 4 KB sectors and 256 KB sectors)<br/> 1 = Uniform Sector Architecture (all 256 KB sectors)</p> <p>Dependency: SP4KBS(CFR1N[6]), TB4KBS(CFR1N[2])</p> |
| CFR3N[2]<br>CFR3V[2] | RESRVD | Reserved for Future Use                         | N -> R/W<br>V -> R/W                           | 0                        | <p>This bit is Reserved for future use. This bit must always be written/loaded to its default state.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| CFR3N[1]<br>CFR3V[1] | RESRVD | Reserved for Future Use                         | N -> R/W<br>V -> R/W                           | 0                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| CFR3N[0]<br>CFR3V[0] | RESRVD | Reserved for Future Use                         | N -> R/W<br>V -> R/W                           | 0                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

**Table 57** Register latency code (cycles) versus frequency<sup>[28, 29]</sup>

| Latency code | SDR SPI register transaction latency dummy cycles (1S-1S-1S) <sup>[30]</sup> |                                        |                                                  | SDR octal register transactions latency dummy cycle (8S-8S-8S) |                                                                                            | DDR octal register transactions latency dummy cycle (8D-8D-8D) |                                                                                            |
|--------------|------------------------------------------------------------------------------|----------------------------------------|--------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------------------------|----------------------------------------------------------------|--------------------------------------------------------------------------------------------|
|              | Frequency                                                                    | RDARG_C_0 <sup>[31]</sup><br>RDDYB_4_0 | RDPLB_0_0<br>RDIDN_0_0<br>RDSR1_0_0<br>RDSR2_0_0 | Frequency                                                      | RDARG_4_0 <sup>[31]</sup><br>RDPLB_4_0<br>RDDYB_4_0<br>RDIDN_4_0<br>RDSR1_4_0<br>RDSR2_4_0 | Frequency                                                      | RDARG_4_0 <sup>[31]</sup><br>RDPLB_4_0<br>RDDYB_4_0<br>RDIDN_4_0<br>RDSR1_4_0<br>RDSR2_4_0 |
| 00           | 50 MHz                                                                       | 0                                      | 0                                                | 50 MHz                                                         | 3                                                                                          | 25 MHz                                                         | 3                                                                                          |
| 01           | 133 MHz                                                                      | 1                                      | 0                                                | 133 MHz                                                        | 4                                                                                          | 66 MHz                                                         | 4                                                                                          |
| 10           | 133 MHz                                                                      | 1                                      | 1                                                | 166 MHz                                                        | 5                                                                                          | 166 MHz (HL-T) /<br>200 MHz (HS-T)                             | 5                                                                                          |
| 11           | 166 MHz                                                                      | 2                                      | 2                                                | 200 MHz                                                        | 6                                                                                          | 200 MHz                                                        | 6                                                                                          |

**Notes**

- 28.RDUID\_4\_0 and RDUID\_0\_0 always has 32 cycles of latency. Maximum frequency under SDR SPI is 166 MHz, under HS-T SDR/DDR Octal is 200 MHz and under HL-T SDR/DDR Octal is 166 MHz.  
29.RDCRC\_4\_0 alway has 8 cycles of latency. Maximum frequency under SDR SPI is 166 MHz, under HS-T SDR/DDR Octal is 200 MHz and under HL-T SDR/DDR Octal is 166 MHz.  
30.CK frequency > 166 MHz SDR, is not supported.  
31.RDARG\_C\_0 and RDARG\_4\_0 uses these dummy cycles for reading volatile registers.

## 5.7 Configuration Register 4 (CFR4x)

Configuration Register 4 controls the main Flash array read transactions burst wrap behavior and output driver impedance.

**Table 58 Configuration Register 4**

| Bit number               | Name             | Function                              | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------------------------|------------------|---------------------------------------|------------------------------------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFR4N[7:5]<br>CFR4V[7:5] | IOIMPD[2:0]<br>] | I/O Driver Output Impedance selection | N -> R/W<br>V -> R/W                           | 101                         | <p>Description: The IOIMPD[2:0] bits select the IO driver output impedance (drive strength). The output impedance configuration bits adjust the drive strength during normal device operation to meet system signal integrity requirements.</p> <p>Selection Options:<br/>           000 = 45 <math>\Omega</math><br/>           001 = 120 <math>\Omega</math><br/>           010 = 90 <math>\Omega</math><br/>           011 = 60 <math>\Omega</math><br/>           100 = 45 <math>\Omega</math><br/>           101 = 30 <math>\Omega</math> (Factory Default)<br/>           110 = 20 <math>\Omega</math><br/>           111 = 15 <math>\Omega</math></p> <p>Dependency: N/A</p> |
| CFR4N[4]<br>CFR4V[4]     | RBSTWP           | Read Burst Wrap Enable selection      | N -> R/W<br>V -> R/W                           | 0                           | <p>Description: The RBSTWP bit selects the read burst wrap feature. It allows the device to enter and exit burst wrapped read mode during normal operation. The wrap length is selected by RBSTWL[1:0] bits.</p> <p>Selection Options:<br/>           0 = Read Wrapped Burst disabled<br/>           1 = Read Wrapped Burst enabled</p> <p>Dependency: RBSTWL[1:0] (CFR4x[1:0])</p>                                                                                                                                                                                                                                                                                                 |

**Table 58 Configuration Register 4 (Continued)**

| Bit number           | Name   | Function                                                                    | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------|--------|-----------------------------------------------------------------------------|------------------------------------------------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFR4N[3]<br>CFR4V[3] | ECC12S | Error Correction Code (ECC) 1-bit or 1-bit/2-bit error correction selection | N -> R/W<br>V -> R/W                           | 1                              | <p>Description: The ECC12S bit selects between 1-bit ECC error detection/correction or both 1-bit ECC error detection and correction and 2-bit ECC error detection. This configuration option affects Address Trap Register and ECC Counter Register functionalities as well. The host needs to erase and reprogram the data in the SEMPER™ Flash memory upon ECC configuration change (1-bit correction to 1-bit correction and 2-bit detection or vice versa).</p> <p>Selection Options:<br/> 0 = 1-bit ECC Error Detection/Correction<br/> 1 = 1-bit ECC Error Detection/Correction and 2-bit ECC error detection</p> <p>Dependency: N/A</p> |
| CFR4N[2]<br>CFR4V[2] | DPDPOR | Deep Power Down power saving mode entry selection upon POR                  | N -> R/W<br>V -> R                             | 0                              | <p>Description: The DPDPOR bit selects if the device will be in either Deep Power Down (DPD) mode or the Standby mode after the completion of POR. If enabled, DPDPOR configures the device to start in DPD mode to reduce current consumption until the device is needed. If the device is in DPD, a pulse on CS# or a Hardware reset will return the device to Standby mode.</p> <p>Selection Options:<br/> 0 = Standby mode is entered upon the completion of POR<br/> 1 = Deep Power Down Power mode is entered upon the completion of POR</p> <p>Dependency: N/A</p>                                                                       |

**Table 58 Configuration Register 4 (Continued)**

| Bit number               | Name        | Function                         | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                         |
|--------------------------|-------------|----------------------------------|------------------------------------------------|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFR4N[1:0]<br>CFR4V[1:0] | RBSTWL[1:0] | Read Burst Wrap Length selection | N -> R/W<br>V -> R/W                           | 00                             | <p>Description: The RBSTWL[1:0] bits select the read burst wrap length and alignment during normal operation. It selects the fixed length/aligned group of 8-, 16-, 32-, or 64-bytes.</p> <p>Selection Options:<br/> 00 = 8 Bytes Wrap length<br/> 01 = 16 Bytes Wrap length<br/> 10 = 32 Bytes Wrap length<br/> 11 = 64 Bytes Wrap length</p> <p>Dependency: RBSTWP (CFR4x[4])</p> |

**Table 59 Output data wrap sequence**

| Wrap boundary (bytes) | Start address (Hex) | Address sequence (Hex)                                                                                                                                                                                                                                          |
|-----------------------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Sequential            | XXXXXX03            | 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18.                                                                                                                                                                         |
| 8                     | XXXXXX00            | 00, 01, 02, 03, 04, 05, 06, 07, 00, 01, 02.                                                                                                                                                                                                                     |
| 8                     | XXXXXX07            | 07, 00, 01, 02, 03, 04, 05, 06, 07, 00, 01.                                                                                                                                                                                                                     |
| 16                    | XXXXXX02            | 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03.                                                                                                                                                                                         |
| 16                    | XXXXXX0C            | 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E.                                                                                                                                                                                     |
| 32                    | XXXXXX0A            | 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F.                                                                                                         |
| 32                    | XXXXXX1E            | 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00.                                                                                                                     |
| 64                    | XXXXXX03            | 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F 00, 01, 02.  |
| 64                    | XXXXXX2E            | 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D. |

## 5.8 Configuration Register 5 (CFR5x)

Configuration Register 5 controls the Octal interface device behavior.

**Table 60 Configuration Register 5**

| Bit number               | Name   | Function                                                                 | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------|--------|--------------------------------------------------------------------------|------------------------------------------------|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFR5N[7]<br>CFR5V[7]     | RESRVD | Reserved for Future Use                                                  | N -> R/W<br>V -> R/W                           | 0                           | These bits are Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                                                                                 |
| CFR5N[6]<br>CFR5V[6]     | RESRVD | Reserved for Future Use                                                  | N -> R/W<br>V -> R/W                           | 1                           |                                                                                                                                                                                                                                                                                                                                                                                                                      |
| CFR5N[5:2]<br>CFR5V[5:2] | RESRVD | Reserved for Future Use                                                  | N -> R/W<br>V -> R/W                           | 0000                        |                                                                                                                                                                                                                                                                                                                                                                                                                      |
| CFR5N[1]<br>CFR5V[1]     | SDRDDR | Octal SPI SDR or DDR selection                                           | N -> R/W<br>V -> R/W                           | 0                           | <p>Description: The SDRDDR bit selects between SDR or DDR for all data transfers to the device. Based on SDRDDR selection, all transactions either are SDR or DDR.</p> <p><b>Note</b> SDRDDR bit only controls the interface for Octal mode (8-8-8).</p> <p>Selection Options:<br/> 0 = SDR enabled<br/> 1 = DDR enabled</p> <p>Dependency: N/A</p>                                                                  |
| CFR5N[0]<br>CFR5V[0]     | OPI-IT | Octal Interface and Protocol Selection - I/O width set to 8 bits (8-8-8) | N -> R/W<br>V -> R/W                           | 0                           | <p>Description: The OPI-IT bit selects the I/O width of the device to be 8-bits wide. When configured to 8-bits (OPI-IT) all transactions require Opcode, Address and Data always sent on all eight I/Os.</p> <p>Selection Options:<br/> 0 = Data Width set to 1 bit wide (1S-1S-1S) - Legacy Single SPI Protocol<br/> 1 = Data Width set to 8 wide (8S-8S-8S, 8D-8D-8D) - Octal Protocol</p> <p>Dependency: N/A</p> |

## 5.9 Interface CRC Enable Register (ICEV)

Interface CRC Enable Register controls the enabling/disabling of the Interface CRC function.

**Table 61** Interface CRC enable register

| Bit number | Name   | Function                | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                    |
|------------|--------|-------------------------|------------------------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ICEV[7:1]  | RESVRD | Reserved for Future Use | V -> R                                         | 0000000                     | This bit is Reserved for future use. This bit must always be written/loaded to its default state.                                                                                              |
| ICEV[0]    | ITCRCE | Interface CRC Selection | V -> R/W                                       | 0                           | Description: The ITCRCE bit controls enabling/disabling of the Interface CRC function.<br><br>Selection Options:<br>0 = Interface CRC Enabled<br>1 = Interface CRC Disabled<br>Dependency: N/A |

## 5.10 Interface CRC Check-value Register (ICRV)

The Interface CRC Check-value Register (ICRV) stores the results of the CRC calculation on the command and data content over the interface for protection.

**Table 62** Interface CRC check-value register

| Bit number | Name         | Function                     | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                    |
|------------|--------------|------------------------------|------------------------------------------------|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ICRV[31:0] | ITCRCV[31:0] | Interface CRC Checksum Value | V -> R                                         | 0xFFFFFFFF                  | Description: The ITCRCV[31:0] bits store the check-value of the CRC process on the memory array data contained within the starting address and the ending address.<br><br>Selection Options: Checksum Value<br>Dependency: N/A |

### 5.11 Memory Array Data Integrity Check CRC Register (DCRV)

The memory array Data Integrity Check CRC Register (DCRV) stores the results of the CRC calculation on the data contained between the specified starting and ending addresses.

**Table 63 Memory array data integrity check CRC register**

| Bit number | Name         | Function                             | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                           |
|------------|--------------|--------------------------------------|------------------------------------------------|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DCRV[31:0] | DTCRCV[31:0] | Memory Array Data CRC Checksum Value | V -> R                                         | 0x00000000                  | Description: The DTCRCV[31:0] bits store the checksum value of the CRC process on the memory array data contained within the starting address and the ending address.<br><br>Selection Options: Checksum Value<br><br>Dependency: N/A |

### 5.12 ECC Status Register (ESCV)

The ECC Status Register (ESCV) contains the ECC status of any error correction action performed on the unit data whose byte was addressed during last read.

**Note** Unit data is defined as the number of bytes over which the ECC is calculated. HL-T/HS-T family devices have a 16 bytes (128 bits) unit data.

**Table 64 ECC Status Register**

| Bit number | Name   | Function                             | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------------|--------|--------------------------------------|------------------------------------------------|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ESCV[7:5]  | RESRVD | Reserved for Future Use              | V -> R                                         | 000                         | This bit is Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| ESCV[4]    | ECC2BT | ECC Error 2-bit Error Detection Flag | V -> R                                         | 0                           | Description: The ECC2BT bit indicates that a 2-bit ECC Error was detected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC2BT.<br><b>Note</b> ECC2BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC2BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed.<br><b>Note</b> ECC1BT is not valid if ECC2BT status flag is set.<br><br>Selection Options:<br>0 = No 2-Bit ECC Error was detected in the data unit (16 bytes)<br>1 = 2-bit ECC Error was detected in the data unit (16 bytes)<br><br>Dependency: CFR4x[3] |

**Table 64**      **ECC Status Register** (Continued)

| Bit number | Name   | Function                                            | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------------|--------|-----------------------------------------------------|------------------------------------------------|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ECSV[3]    | ECC1BT | ECC Error 1-bit Error Detection and Correction Flag | V -> R                                         | 0                           | <p>Description: The ECC1BT bit indicates that a 1-bit ECC Error was detected and corrected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC1BT.</p> <p><b>Note</b> ECC1BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC1BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed.</p> <p>Selection Options:<br/> 0 = No 1-Bit ECC Error was detected in the data unit (16 bytes)<br/> 1 = 1-bit ECC Error was detected in the data unit (16 bytes)</p> <p>Dependency: N/A</p> |
| ECSV[2:0]  | RESRVD | Reserved for Future Use                             | V -> R                                         | 000                         | <p>This bit is Reserved for future use. This bit must always be written/loaded to its default state.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

### 5.13 ECC Address Trap Register (EATV)

The ECC Address Trap Register (EATV) stores the address of the ECC unit data where either a 1-Bit/2-Bit error or only a 1-Bit error occurred during a read operation. It stores the ECC unit address of the first ECC error captured during a memory read operation since the last Clear ECC transaction.

**Table 65**      **ECC Address Trap Register**

| Bit number | Name         | Function                                        | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------------|--------------|-------------------------------------------------|------------------------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EATV[31:0] | ECCATP[31:0] | ECC 1-bit and 2-bit Error Address Trap Register | V -> R                                         | 0x00000000                  | <p>Description: The Address Trap Register (ECCATP[31:0]) stores the ECC unit data address where a 1-Bit/2-Bit error occurred during a read operation. ECCATP[31:0] stores the ECC unit address of the first ECC error captured during a memory read operation since the last Clear ECC Status Register transaction (CLECC_0_0).</p> <p><b>Note</b> ECCATP[31:0] is only updated during Read Instruction.</p> <p><b>Note</b> Mask non-valid upper ECCATP address bits from ECC unit address.</p> <p><b>Note</b> Clear ECC Status Register transaction (CLECC_0_0), POR or Hardware/Software reset clears the EATV[31:0] to 0x00000000.</p> <p>Selection Options: ECC Error Data Unit Address</p> <p>Dependency: N/A</p> |

## 5.14 ECC Error Detection Count Register (ECTV)

The ECC Error Detection Counter Register (ECTV) stores the number of either 1-Bit/2-Bit or only 1-Bit ECC errors have occurred during read operations since the last POR or hardware/software reset.

**Table 66** ECC Count Register

| Bit number | Name         | Function                                 | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------------|--------------|------------------------------------------|------------------------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ECTV[15:0] | ECCCNT[15:0] | ECC 1-bit and 2-bit Error Count Register | V -> R                                         | 0x0000                      | <p>Description: The ECCCNT[15:0] stores the number of 1-bit/2-bit ECC errors occurred during read operations since the last POR or hardware/software reset.</p> <p><b>Note</b> ECCCNT[15:0] is only updated during Read Instruction.</p> <p><b>Note</b> Only one ECC error is counted for each data unit. If multiple read transactions access the same unit data containing an ECC error, the ECCCNT[15:0] will increment each time the unit data is read.</p> <p><b>Note</b> Once the count reaches 0xFFFF, the ECCCNT[15:0] will stop incrementing.</p> <p><b>Note</b> POR or Hardware/Software reset clears the ECCCNT[15:0] to 0x0000.</p> <p>Selection Options: ECC Error Count</p> <p>Dependency: N/A</p> |

## 5.15 Advanced Sector Protection register (ASPO)

The ASP Register (ASPO) configures the behavior of advanced sector protection scheme.

**Table 67 Advanced Sector Protection Register**

| Bit number | Name   | Function                                                                  | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------|--------|---------------------------------------------------------------------------|------------------------------------------------|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ASPO[15:6] | RESRVD | Reserved for Future Use                                                   | N -> R/1                                       | 111111111                      | This bit is Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                                                                                                                                            |
| ASPO[5]    | ASPRDP | Read Password Based Protection Selection                                  | N -> R/1                                       | 1                              | Description: The ASPRDP bit selects the Read Password Mode Protection mode. Read Password Protection mode works in conjunction with Password Protection mode to protect all sectors from Read/Erase/Program. Based on TBPROT configuration bit (CFR1x[5]), either the top or bottom sector is available for reading.<br>Selection Options:<br>0 = Read Password Protection Mode is enabled<br>1 = Read Password Protection Mode is disabled<br>Dependency: TBPROT (CFR1x[5]) |
| ASPO[4]    | ASPDYB | Dynamic Protection (DYB) for all sectors at power-up Selection            | N -> R/1                                       | 1                              | Description: The ASPDYB bit selects whether all DYB bits (sectors) are in the protected state following power-up or hardware reset. DYB bits will individually need to be reset to change sector protections.<br>Selection Options:<br>0 = DYB based sector protection enabled at power-up or hardware reset<br>1 = DYB based sector protection disabled at power-up or hardware reset<br>Dependency: N/A                                                                    |
| ASPO[3]    | ASPPPB | Permanent Protection (PPB) bits for all sectors programmability Selection | N -> R/1                                       | 1                              | Description: The ASPPPB bit selects whether all PPB bits are one-time programmable making PPB sector protection permanent.<br><b>Note</b> ASPPPB disables PPB erase transaction (ERPPB_0_0).<br>Selection Options:<br>0 = PPB bits are one-time programmable<br>1 = PPB bits can be erased and programmed as desired<br>Dependency: N/A                                                                                                                                      |

**Table 67 Advanced Sector Protection Register (Continued)**

| Bit number | Name   | Function                            | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------|--------|-------------------------------------|------------------------------------------------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ASPO[2]    | ASPPWD | Password Based Protection Selection | N -> R/1                                       | 1                              | <p>Description: The ASPPWD bit selects the Password Protection Mode. Password Protection mode protects all PPB bits till the correct password is entered. The ASPPWD can also be used in combination with the ASPRDP to protect all registers and all memory from erase/program and to protect sectors from being read as well till the correct password is provided - except for top or bottom sector which is available for reading based on TBPROT configuration bit (CFR1x[5]).</p> <p><b>Note</b> When ASPPWD is selected, ASPO[15:0], CFR1N[7:2] and PWDO[63:0] are protected against Write operations.</p> <p>Selection Options:<br/> 0 = Password Protection Mode is enabled<br/> 1 = Password Protection Mode is disabled</p> <p>Dependency: N/A</p> |

**Table 67 Advanced Sector Protection Register (Continued)**

| Bit number | Name   | Function                                                        | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------------|--------|-----------------------------------------------------------------|------------------------------------------------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ASPO[1]    | ASPPER | Persistent Protection Selection (Register Protection Selection) | N -> R/1                                       | 1                              | Description: The ASPPER bit selects the Persistent Protection Mode. The Persistent Protection mode (ASPPER) protects the ASPO[15:0], CFR1x[6, 5, 4, 2] and CFR3x[3] registers from erase or program.<br>Selection Options:<br>0 = Persistent Protection Mode is enabled<br>1 = Persistent Protection Mode is disabled<br>Dependency: N/A                                                                                                                             |
| ASPO[0]    | ASPPRM | Permanent Protection Selection                                  | N -> R/1                                       | 1                              | Description: The ASPPRM bit selects the Permanent Protection Mode. The Permanent Protection mode (ASPPRM) permanently protects the PPB bits from erase or program. ASPPRM bit should be programmed once all the PPB based sector protections are finalized.<br><b>Note</b> Permanent protection is independent of the PPBLOCK bit.<br>Selection Options:<br>0 = Permanent Protection Mode is enabled<br>1 = Permanent Protection Mode is disabled<br>Dependency: N/A |

## 5.16 ASP Password Register (PWDO)

The ASP Password Register (PWDO) is used to permanently define a password.

**Table 68 Password Register**

| Bit number | Name         | Function          | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                                                                                             |
|------------|--------------|-------------------|------------------------------------------------|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PWDO[63:0] | PASWRD[63:0] | Password Register | N -> R/1                                       | 0xFFFFFFFF<br>FFFFFFF          | Description: The PASWRD[63:0] permanently stores a password used in password protected modes of operation. When the Password Protection Mode is enabled, this register will output the undefined data upon read password request.<br><br>Selection Options: Password<br>Dependency: N/A |

## 5.17 ASP PPB Lock Register (PPLV)

The PPBLCK bit in the ASP PPB Lock Register (PPLV) is used to protect the PPB bits.

**Table 69 ASP PPB lock register**

| Bit number | Name   | Function                           | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                                                                      |
|------------|--------|------------------------------------|------------------------------------------------|--------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PPLV[7:1]  | RESVRD | Reserved for Future Use            | V -> R                                         | 0000000                        | This bit is Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                |
| PPLV[0]    | PPBLCK | PPB Temporary Protection Selection | V -> R/W                                       | 1, ASPO[2:1]                   | Description: The PPBLCK bit is used to temporarily protect all the PPB bits.<br><br>Selection Options:<br>1 = PPB Bits can be erased or programmed<br>0 = PPB bits are protected against erase or program till the next POR or hardware reset<br>Dependency: N/A |

## 5.18 ASP PPB Access Register (PPAV)

The ASP PPB Access Register (PPAV) is used to provide the state of each sector's PPB protection bit.

**Table 70 ASP PPB Access Register**

| Bit number | Name        | Function                           | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------|-------------|------------------------------------|------------------------------------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PPAV[7:0]  | PPBACS[7:0] | Sector Based PPB Protection Status | N -> R/W                                       | 11111111                    | <p>Description: The PPBACS[7:0] bits are used to provide the state of the individual sector's PPB bit.</p> <p>Selection Options:<br/>           FF = PPB for the sector addressed by the Read PPB transaction (RDPPB_4_0) is 1, not protecting that sector from program or erase operations<br/>           00 = PPB for the sector addressed by the Read PPB transaction (RDPPB_4_0) is 0, protecting that sector from program or erase operations</p> <p>Dependency: N/A</p> |

## 5.19 ASP Dynamic Block Access Register (DYAV)

The ASP DYB Access Register (DYAV) is used to provide the state of each sector's DYB protection bit.

**Table 71 ASP DYB Access Register**

| Bit number | Name        | Function                           | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------|-------------|------------------------------------|------------------------------------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DYAV[7:0]  | DYBACS[7:0] | Sector Based DYB Protection Status | V -> R/W                                       | 11111111                    | <p>Description: The DYBACS[7:0] bits are used to provide the state of the individual sector's DYB bit.</p> <p>Selection Options:<br/>           FF = DYB for the sector addressed by the Read DYB transaction (RDDYB_4_0) is 1, not protecting that sector from program or erase operations<br/>           00 = DYB for the sector addressed by the Read DYB transaction (RDDYB_4_0) is 0, protecting that sector from program or erase operations</p> <p>Dependency: N/A</p> |

## 5.20 AutoBoot Register (ATBN)

The AutoBoot Register (ATBN) provides a means to automatically read boot code as part of the power-on reset, or hardware reset process.

**Table 72 AutoBoot Register**

| Bit number | Name        | Function                                                               | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary)  | Description                                                                                                                                                                                                                                                                                                                                                                                                       |
|------------|-------------|------------------------------------------------------------------------|------------------------------------------------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ATBN[31:9] | STADR[22:0] | Starting Address Selection where AutoBoot will start reading data from | N -> R/W                                       | 00000000000000<br>0000000000 | Description: The STADR[22:0] bits set the starting address from which the device will output the read data.<br><br>Selection Options: Address Bits<br><br>Dependency: N/A                                                                                                                                                                                                                                         |
| ATBN[8:1]  | STDLY[7:0]  | AutoBoot Read Starting Delay Selection                                 | N -> R/W                                       | 00000000                     | Description: The STDLY[7:0] bits specify the initial delay (clock cycles) needed by the host before it can accept data.<br><b>Note</b> STDLY[7:0] = 0x00 is valid for SPI up to 50 MHz. STDLY[7:0] = 0x01 or higher is valid for SPI up to 166 MHz. STDLY[7:0] = 0x05 or higher is valid for HL-T Octal up to 166 MHz and HS-T Octal up to 200 MHz.<br><br>Selection Options: Address Bits<br><br>Dependency: N/A |
| ATBN[0]    | ATBTEN      | AutoBoot Feature Selection                                             | N -> R/W                                       | 0                            | Description: The ATBTEN bit enables or disables the AutoBoot feature.<br><br>Selection Options:<br>0 = AutoBoot feature disabled<br>1 = AutoBoot feature enabled<br><br>Dependency: N/A                                                                                                                                                                                                                           |

## 5.21 Sector Erase Count Register (SECV)

The Sector Erase Count Register (SECV) contains the number of times the addressed sector has been erased.

**Table 73 Sector Erase Count Register**

| Bit number | Name         | Function                                  | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------|--------------|-------------------------------------------|------------------------------------------------|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SECV[23]   | SECCPT       | Sector Erase Count Corruption Status Flag | V -> R                                         | 0x0                         | <p>Description: The SECCPT bit is used to determine if the reported sector erase count is corrupted and was reset.</p> <p><b>Note</b> If SECCPT is set due to count corruption, it will reset to 0 on the next successful erase operation on the selected sector.</p> <p>Selection Options:<br/>           0 = Sector Erase Count is not corrupted and is valid<br/>           1 = Sector Erase Count is corrupted and is not valid</p> <p>Dependency: N/A</p> |
| SECV[22:0] | SECVAL[22:0] | Sector Erase Count Value                  | V -> R                                         | 0x000000                    | <p>Description: The SECVAL[22:0] bits store the number of times a sector has been erased</p> <p>Selection Options: Value</p> <p>Dependency: N/A</p>                                                                                                                                                                                                                                                                                                            |

## 5.22 INT# Pin Configuration Register (INCV) - octal only

The INT# pin Configuration Register (INCV) configures which internal event will trigger a HIGH to LOW transition on the INT# output pin.

### Notes

- When INCV disables a particular feature from driving the INT# pin, it will prevent the corresponding INSV bit(s) from being updated.
- Clearing a bit within INCV has no effect on INSV, and it is a system responsibility to independently clear the INSV as required.

**Table 74 Interrupt Configuration Register**

| Bit number | Name   | Function                             | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description                                                                                                                                                                                                                                                                                                                                               |
|------------|--------|--------------------------------------|------------------------------------------------|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INCV[7]    | INTBEN | INT# pin Enable Selection            | V -> R/W                                       | 1                        | Description: The INT# pin is an open-drain output used to indicate to the host system that an event has occurred within the memory device. The INTBEN bit enables or disables the functionality controlling INT# pin.<br><br>Selection Options:<br>0 = INT# pin functionality is enabled<br>1 = INT# pin functionality is disabled<br><br>Dependency: N/A |
| INCV[6:5]  | RESRVD | Reserved for Future Use              | V -> R/W                                       | 11                       | These bits are Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                      |
| INCV[4]    | REYBSY | Ready/Busy Transition Selection      | V -> R/W                                       | 1                        | Description: The REYBSY bit enables or disables whether device ready/busy state will transition INT#.<br><br>Selection Options:<br>0 = A Busy to Ready transition will cause a HIGH to LOW transition on the INT# output<br>1 = Ready/Busy transitions will not transition the INT# output<br><br>Dependency: N/A                                         |
| INCV[3:2]  | RESRVD | Reserved for Future Use              | V -> R/W                                       | 11                       | These bits are Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                                                                                                                      |
| INCV[1]    | ECC2BT | ECC 2-bit Error Detection Selection0 | V -> R/W                                       | 1                        | Description: The ECC2BT bit enables or disables whether a 2-bit ECC detection error will transition INT#.<br><br>Selection Options:<br>0 = 2-bit ECC detection will cause a HIGH to LOW transition the INT# output<br>1 = 2-bit ECC detection will not transition the INT# output<br><br>Dependency: N/A                                                  |

**Table 74**      **Interrupt Configuration Register (Continued)**

| Bit number | Name   | Function                                           | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                      |
|------------|--------|----------------------------------------------------|------------------------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INCV[0]    | ECC1BT | ECC 1-bit Error Detection and Correction Selection | V -> R/W                                       | 1                           | <p>Description: The ECC1BT bit enables or disables whether a 1-bit ECC detection and correction error will transition INT#.</p> <p>Selection Options:<br/> 0 = 1-bit ECC detection and correction will cause a HIGH to LOW transition the INT# output<br/> 1 = 1-bit ECC detection and correction will not transition the INT# output</p> <p>Dependency: N/A</p> |

## 5.23 INT# Pin Status Register (INSV) - Octal only

The INT# Pin Status Register (INSV) indicates which internal event(s) has occurred since the last time the ISR was cleared.

**Table 75 Interrupt status register**

| Bit number | Name   | Function                                 | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default (binary) | Description                                                                                                                                                                                                                                                      |
|------------|--------|------------------------------------------|------------------------------------------------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INSV[7:5]  | RESRVD | Reserved for Future Use                  | V -> R/W                                       | 111                      | These bits are Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                             |
| INSV[4]    | REYBSY | Ready/Busy Transition                    | V -> R/W                                       | 1                        | Description: The REYBSY bit indicates whether the device's ready/busy status has caused a transition on INT#.<br><br>Selection Options:<br>0 = A Busy to Ready transition has occurred<br>1 = A Busy to Ready transition has not occurred<br><br>Dependency: N/A |
| INSV[3:2]  | RESRVD | Reserved for Future Use                  | V -> R/W                                       | 11                       | These bits are Reserved for future use. This bit must always be written/loaded to its default state.                                                                                                                                                             |
| INSV[1]    | ECC2BT | ECC 2-bit Error Detection                | V -> R/W                                       | 1                        | Description: The ECC2BT bit indicates whether a 2-bit ECC detection error has caused a transition on INT#.<br><br>Selection Options:<br>0 = 2-bit error detection has occurred<br>1 = 2-bit error detection has not occurred<br><br>Dependency: N/A              |
| INSV[0]    | ECC1BT | ECC 1-bit Error Detection and Correction | V -> R/W                                       | 1                        | Description: The ECC1BT bit indicates whether a 1-bit ECC correction error has caused a transition on INT#.<br><br>Selection Options:<br>0 = 1-bit error correction has occurred<br>1 = 1-bit error correction has not occurred<br><br>Dependency: N/A           |

## 5.24 Endurance Flex Architecture Selection Register (EFXx)

The Endurance Flex Architecture Selection Registers (EFXx) define the long retention / high endurance regions based on a four pointer based architecture.

**Table 76 Endurance Flex Architecture Selection Register (pointer 4)**

| Bit number  | Name        | Function                                             | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                       |
|-------------|-------------|------------------------------------------------------|------------------------------------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EFX40[10:2] | EPTAD4[8:0] | Endurance Flex Pointer 4 Address Selection           | N -> R/1                                       | 11111111                    | Description: The EPTAD4[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined.<br><br>Selection Options: Pointer Address<br>Dependency: N/A |
| EFX40[1]    | ERGNT4      | Endurance Flex Pointer 4 based Region Type Selection | N -> R/1                                       | 1                           | Description: The ERGNT4 bit defines whether the region is long retention or high endurance.<br><br>Selection Options:<br>0 = Long Retention Sectors<br>1 = High Endurance Sectors<br>Dependency: N/A              |
| EFX40[0]    | EPTEB4      | Endurance Flex Pointer 4 Enable# Selection           | N -> R/1                                       | 1                           | Description: The EPTEN4 bit define whether the wear leveling pointer is enabled/disabled.<br><br>Selection Options:<br>0 = Pointer Address Enabled<br>1 = Pointer Address Disabled<br>Dependency: N/A             |

**Table 77 Endurance Flex Architecture Selection Register (pointer 3)**

| Bit number  | Name        | Function                                   | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                                       |
|-------------|-------------|--------------------------------------------|------------------------------------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EFX30[10:2] | EPTAD3[8:0] | Endurance Flex Pointer 3 Address Selection | N -> R/1                                       | 11111111                    | Description: The EPTAD3[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined.<br><br>Selection Options: Pointer Address<br>Dependency: N/A |

Registers

**Table 77**      **Endurance Flex Architecture Selection Register (pointer 3) (Continued)**

| Bit number | Name   | Function                                             | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory default<br>(binary) | Description                                                                                                                                                                                               |
|------------|--------|------------------------------------------------------|------------------------------------------------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EFX3O[1]   | ERGNT3 | Endurance Flex Pointer 3 based Region Type Selection | N -> R/1                                       | 1                           | Description: The ERGNT3 bit defines whether the region is long retention or high endurance.<br><br>Selection Options:<br>0 = Long Retention Sectors<br>1 = High Endurance Sectors<br><br>Dependency: N/A  |
| EFX3O[0]   | EPTEB3 | Endurance Flex Pointer 3 Enable# Selection           | N -> R/1                                       | 1                           | Description: The EPTEN3 bit define whether the wear leveling pointer is enabled/disabled.<br><br>Selection Options:<br>0 = Pointer Address Enabled<br>1 = Pointer Address Disabled<br><br>Dependency: N/A |

**Table 78 Endurance Flex Architecture Selection Register (pointer 2)**

| Bit number  | Name        | Function                                             | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                           |
|-------------|-------------|------------------------------------------------------|------------------------------------------------|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EFX2O[10:2] | EPTAD2[8:0] | Endurance Flex Pointer 2 Address Selection           | N -> R/1                                       | 11111111                       | Description: The EPTAD2[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined.<br><br>Selection Options: Pointer Address<br><br>Dependency: N/A |
| EFX2O[1]    | ERGNT2      | Endurance Flex Pointer 2 based Region Type Selection | N -> R/1                                       | 1                              | Description: The ERGNT2 bit defines whether the region is long retention or high endurance.<br><br>Selection Options:<br>0 = Long Retention Sectors<br>1 = High Endurance Sectors<br><br>Dependency: N/A              |
| EFX2O[0]    | EPTEB2      | Endurance Flex Pointer 2 Enable# Selection           | N -> R/1                                       | 1                              | Description: EPTEN2 bit define whether the wear leveling pointer is enabled/disabled.<br><br>Selection Options:<br>0 = Pointer Address Enabled<br>1 = Pointer Address Disabled<br><br>Dependency: N/A                 |

**Table 79 Endurance Flex Architecture Selection Register (pointer 1)**

| Bit number  | Name        | Function                                             | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                           |
|-------------|-------------|------------------------------------------------------|------------------------------------------------|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EFX1O[10:2] | EPTAD1[8:0] | Endurance Flex Pointer 1 Address Selection           | N -> R/1                                       | 11111111                       | Description: The EPTAD1[8:0] bits define the 9-bit address of the beginning sector from where the long retention / high endurance region is defined.<br><br>Selection Options: Pointer Address<br><br>Dependency: N/A |
| EFX1O[1]    | ERGNT1      | Endurance Flex Pointer 1 based Region Type Selection | N -> R/1                                       | 1                              | Description: The ERGNT1 bit defines whether the region is long retention or high endurance.<br><br>Selection Options:<br>0 = Long Retention Sectors<br>1 = High Endurance Sectors<br><br>Dependency: N/A              |

**Table 79**      **Endurance Flex Architecture Selection Register (pointer 1) (Continued)**

| Bit number | Name   | Function                                            | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                     |
|------------|--------|-----------------------------------------------------|------------------------------------------------|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EFX10[0]   | EPTEB1 | Endurance Flex<br>Pointer 1<br>Enable#<br>Selection | N -> R/1                                       | 1                              | Description: The EPTEN1 bit<br>define whether the wear leveling<br>pointer is enabled/disabled.<br><br>Selection Options:<br>0 = Pointer Address Enabled<br>1 = Pointer Address Disabled<br><br>Dependency: N/A |

**Table 80**      **Endurance Flex Architecture Selection Register (pointer 0)**

| Bit<br>number | Name   | Function                                      | Read/Write<br>N = Non-volatile<br>V = Volatile | Factory<br>default<br>(binary) | Description                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------|--------|-----------------------------------------------|------------------------------------------------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EFX00[1]      | GBLSEL | All Sectors based<br>Region type<br>Selection | N -> R/1                                       | 1                              | Description: The MBLSEL bit<br>defines whether all sectors are<br>defined as long retention region or<br>high endurance region.<br><b>Note</b> If all other pointer registers<br>are disabled, this bit defines the<br>behavior of the entire memory<br>space and is hardwired to start at<br>Sector 0.<br><br>Selection Options:<br>0 = Long Retention Sectors<br>1 = High Endurance Sectors<br><br>Dependency: N/A |
| EFX00[0]      | WRLVEN | Wear Leveling<br>Enable Selection             | N -> R/1                                       | 1                              | Description: The WRLVEN bit<br>enables/disables the wear leveling<br>feature.<br><br>Selection Options:<br>0 = Wear Leveling Disabled<br>1 = Wear Leveling Enabled<br><br>Dependency: N/A                                                                                                                                                                                                                            |

## 6 Transaction table

### 6.1 SPI (1S-1S-1S) transaction table

**Table 81** SPI (1S-1S-1S) transaction table

| Function        | Transaction name | Description                                                                                                                                    | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex)     | Byte 6 (Hex) | Byte 7 (Hex) | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max frequency (MHz) | Address length |     |
|-----------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|--------------|--------------|--------------|--------------|------------------|--------------|--------------|--------------|--------------|--------------------|---------------------|----------------|-----|
| Read device ID  | RDIDN_0_0        | <b>Read manufacturer and device identification</b> transaction provides read access to manufacturer and device identification.                 | -                        | 9F (CMD)     | -            | -            | -            | -                | -            | -            | -            | -            | Figure 11          | 166                 | N/A            |     |
|                 | RSFDP_3_0        | <b>Read JEDEC Serial Flash Discoverable Parameters</b> transaction sequentially accesses the Serial Flash Discovery Parameters (SFDP).         | -                        | 5A (CMD)     | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | -                | -            | -            | -            | -            | Figure 12          |                     | 3              |     |
|                 | RDUID_0_0        | <b>Read Unique ID</b> accesses a factory programmed 64-bit number which is unique to each device.                                              | -                        | 4C (CMD)     | -            | -            | -            | -                | -            | -            | -            | -            | Figure 11          |                     | N/A            |     |
| Register access | RDSR1_0_0        | <b>Read Status Register 1</b> transaction allows the Status Register 1 contents to be read from DQ1/SO.                                        | -                        | 05 (CMD)     | -            | -            | -            | -                | -            | -            | -            | -            |                    |                     | Figure 11      | N/A |
|                 | RDSR2_0_0        | <b>Read Status Register-2</b> transaction allows the Status Register-2 contents to be read from DQ1/SO.                                        | -                        | 07 (CMD)     | -            | -            | -            | -                | -            | -            | -            | -            | Figure 12          |                     |                | 3   |
|                 | RDARG_C_0        | <b>Read Any Register</b> transaction provides a way to read all addressed non-volatile and volatile device registers.                          | -                        | 65 (CMD)     | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | -                | -            | -            | -            | -            |                    |                     | Figure 12      | 4   |
|                 |                  |                                                                                                                                                | -                        |              | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]       | -            | -            | -            | -            | Figure 6           |                     |                | N/A |
|                 | WRENB_0_0        | <b>Write Enable</b> sets the Write Enable Latch bit of the Status Register 1 to 1 to enable write, program and erase transactions.             | -                        | 06 (CMD)     | -            | -            | -            | -                | -            | -            | -            | -            |                    |                     | Figure 9       | 3   |
|                 | WRDIS_0_0        | <b>Write Disable</b> sets the Write Enable Latch bit of the Status Register 1 to 0 to disable write, program and erase transactions execution. | -                        | 04 (CMD)     | -            | -            | -            | -                | -            | -            | -            | -            |                    |                     |                |     |
|                 | WRARG_C_1        | <b>Write Any Register</b> transaction provides a way to write all addressed non-volatile and volatile device registers.                        | WRENB_0_0                | 71 (CMD)     | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | Input Data [7:0] | -            | -            | -            | -            |                    |                     |                |     |
| ADDR [31:24]    |                  |                                                                                                                                                |                          |              | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | Input Data [7:0] | -            | -            | -            |              |                    |                     |                |     |

**Table 81 SPI (1S-1S-1S) transaction table (Continued)**

| Function            | Transaction name | Description                                                                                                                                                                                               | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex)       | Byte 3 (Hex)       | Byte 4 (Hex)      | Byte 5 (Hex)     | Byte 6 (Hex)       | Byte 7 (Hex)       | Byte 8 (Hex)    | Byte 9 (Hex)   | Transaction format | Max frequency (MHz) | Address length |
|---------------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|--------------|--------------------|--------------------|-------------------|------------------|--------------------|--------------------|-----------------|----------------|--------------------|---------------------|----------------|
| Register access     | CLPEF_0_0        | <b>Clear Program and Erase Failure Flags</b> transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag).                                                                        | -                        | 82 (CMD)     | -                  | -                  | -                 | -                | -                  | -                  | -               | -              | Figure 6           | 166                 | N/A            |
|                     | EN4BA_0_0        | <b>Enter 4 Byte Address Mode</b> transaction sets the Address Length bit CFR2V[7] to 1                                                                                                                    |                          | B7 (CMD)     |                    |                    |                   |                  |                    |                    |                 |                |                    |                     |                |
|                     | EX4BA_0_0        | Exit 4 Byte Address Mode transaction sets the Address Length bit CFR2V[7] to 0                                                                                                                            |                          | B8 (CMD)     |                    |                    |                   |                  |                    |                    |                 |                |                    |                     |                |
| ECC                 | RDECC_4_0        | <b>Read ECC Status</b> is used to determine the ECC status of the addressed data unit.                                                                                                                    | -                        | 19 (CMD)     | ADDR [31:24]       | ADDR [23:16]       | ADDR [15:8]       | ADDR [7:0]       | -                  | -                  | -               | -              | Figure 12          | 166                 | 4              |
|                     | CLECC_0_0        | <b>Clear ECC Status Register</b> transaction resets ECC Status Register bit[4] (2-bit ECC Detection), ECC Status Register bit[3] (1-bit ECC Correction), Address Trap Register and ECC Detection Counter. | -                        | 1B (CMD)     | -                  | -                  | -                 | -                | -                  | -                  | -               | -              | Figure 6           |                     | N/A            |
| CRC                 | DICHK_4_1        | <b>Data Integrity Check</b> transaction causes the device to perform a Data Integrity Check over a user defined address range.                                                                            | -                        | 5B (CMD)     | Start ADDR [31:24] | Start ADDR [23:16] | Start ADDR [15:8] | Start ADDR [7:0] | End ADDR [31:24]   | End ADDR [23:16]   | End ADDR [15:8] | End ADDR [7:0] | Figure 8           |                     |                |
| Read flash array    | RDAY1_C_0        | <b>Read</b> transaction reads out the memory contents at the given address. The maximum CK frequency for this transaction is 50MHz frequency.                                                             | -                        | 03 (CMD)     | ADDR [23:16]       | ADDR [15:8]        | ADDR [7:0]        | -                | -                  | -                  | -               | -              | Figure 13          | 50                  | 3              |
|                     |                  |                                                                                                                                                                                                           | -                        |              | ADDR [31:24]       | ADDR [23:16]       | ADDR [15:8]       | ADDR [7:0]       | -                  | -                  | -               | -              |                    |                     | 4              |
|                     | RDAY1_4_0        |                                                                                                                                                                                                           | -                        | 13 (CMD)     | ADDR [31:24]       | ADDR [23:16]       | ADDR [15:8]       | ADDR [7:0]       | -                  | -                  | -               | -              |                    |                     |                |
|                     | RDAY2_C_0        | <b>Read Fast</b> transaction reads out the memory contents at the given address. The maximum CK frequency for this transaction is 166MHz frequency.                                                       | -                        | 0B (CMD)     | ADDR [23:16]       | ADDR [15:8]        | ADDR [7:0]        | -                | -                  | -                  | -               | -              | Figure 12          | 166                 | 3              |
|                     |                  |                                                                                                                                                                                                           | -                        |              | ADDR [31:24]       | ADDR [23:16]       | ADDR [15:8]       | ADDR [7:0]       | -                  | -                  | -               | -              |                    |                     | 4              |
| Program flash array | PRPGE_4_1        | <b>Program Page</b> programs 256B or 512B data to the memory array in one transaction.                                                                                                                    | WRENB_0_0                | 12 (CMD)     | ADDR [31:24]       | ADDR [23:16]       | ADDR [15:8]       | ADDR [7:0]       | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue)      | -              | Figure 9           |                     |                |

**Table 81 SPI (1S-1S-1S) transaction table (Continued)**

| Function                   | Transaction name | Description                                                                                                                                              | Prerequisite transaction | Byte 1 (Hex)   | Byte 2 (Hex) | Byte 3 (Hex) | Byte 4 (Hex) | Byte 5 (Hex) | Byte 6 (Hex)       | Byte 7 (Hex)       | Byte 8 (Hex) | Byte 9 (Hex) | Transaction format | Max frequency (MHz) | Address length |
|----------------------------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------|--------------|--------------|--------------|--------------|--------------------|--------------------|--------------|--------------|--------------------|---------------------|----------------|
| Erase flash array          | ER004_4_0        | <b>Erase 4-KB Sector</b> transaction sets all the bits of a 4KB sector to 1 (all bytes are FFh).                                                         | WRENB_0_0                | 21 (CMD)       | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | -                  | -                  | -            | -            | Figure 7           | 166                 | 4              |
|                            | ER256_4_0        | <b>Erase 256-KB Sector</b> transaction sets all the bits of a 256KB sector to 1 (all bytes are FFh).                                                     | WRENB_0_0                | DC (CMD)       | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | -                  | -                  | -            | -            |                    |                     | 4              |
|                            | ERCHP_0_0        | <b>Erase Chip</b> transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array.                                               | WRENB_0_0                | 60 or C7 (CMD) | -            | -            | -            | -            | -                  | -                  | -            | -            | Figure 6           |                     | N/A            |
|                            | EVERS_4_0        | <b>Evaluate Erase Status</b> transaction verifies that the last erase operation on the addressed sector was completed successfully.                      | -                        | D0 (CMD)       | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | -                  | -                  | -            | -            | Figure 7           |                     | 4              |
|                            | SEERC_4_0        | <b>Sector Erase Count</b> transaction outputs the number of erase cycles for the sector of the inputted address from the Sector Erase Count Register.    | -                        | 5D (CMD)       | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | -                  | -                  | -            | -            | Figure 12          |                     | 4              |
| Suspend / resume           | SPEPD_0_0        | <b>Suspend Erase / Program / Data Integrity Check</b> transaction allows the system to interrupt a programming, erase or data integrity check operation. | -                        | B0 (CMD)       | -            | -            | -            | -            | -                  | -                  | -            | -            | Figure 6           | 166                 | N/A            |
|                            | RSEPD_0_0        | <b>Resume Erase / Program / Data Integrity Check</b> transaction allows the system to resume a programming, erase or data integrity check operation.     | -                        | 7A (CMD)       | -            | -            | -            | -            | -                  | -                  | -            | -            |                    |                     |                |
| Secure silicon region      | PRSSR_4_1        | <b>Program Secure Silicon Region</b> transaction programs data in 1024 bytes of Secure Silicon Region.                                                   | WRENB_0_0                | 42 (CMD)       | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue)   | -            | Figure 9           | 166                 | 4              |
|                            | RDSSR_4_0        | <b>Read Secure Silicon Region</b> transaction reads data from the SSR.                                                                                   | -                        | 4B (CMD)       | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | -                  | -                  | -            | -            | Figure 12          |                     |                |
| Advanced sector protection | RDDYB_4_0        | <b>Read Dynamic Protection Bit</b> transaction reads the contents of the DYB Access Register.                                                            | -                        | E0 (CMD)       | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | -                  | -                  | -            | -            | Figure 12          | 166                 | 4              |
|                            | WRDYB_4_1        | <b>Write Dynamic Protection Bit</b> transaction writes to the DYB Access Register.                                                                       | WRENB_0_0                | E1 (CMD)       | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | Input Data [7:0]   | -                  | -            | -            | Figure 9           |                     |                |
|                            | RDPPB_4_0        | <b>Read Persistent Protection Bit</b> transaction reads the contents of the PPB Access Register.                                                         | -                        | E2 (CMD)       | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | -                  | -                  | -            | -            | Figure 12          |                     |                |
|                            | PRPPB_4_0        | <b>Program Persistent Protection Bit</b> transaction programs / writes the PPB Register to enable the sector protection.                                 | WRENB_0_0                | E3 (CMD)       | ADDR [31:24] | ADDR [23:16] | ADDR [15:8]  | ADDR [7:0]   | -                  | -                  | -            | -            | Figure 7           |                     |                |
|                            | ERPPB_0_0        | <b>Erase Persistent Protection Bit</b> transaction sets all persistent protection bits to 1.                                                             | WRENB_0_0                | E4 (CMD)       | -            | -            | -            | -            | -                  | -                  | -            | -            | Figure 6           |                     | N/A            |

**Table 81 SPI (1S-1S-1S) transaction table (Continued)**

| Function                   | Transaction name | Description                                                                                                                                                                                                                                                                                                                                                                               | Prerequisite transaction | Byte 1 (Hex) | Byte 2 (Hex)    | Byte 3 (Hex)     | Byte 4 (Hex)      | Byte 5 (Hex)      | Byte 6 (Hex)      | Byte 7 (Hex)      | Byte 8 (Hex)      | Byte 9 (Hex)      | Transaction format | Max frequency (MHz) | Address length |
|----------------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|--------------|-----------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--------------------|---------------------|----------------|
| Advanced sector protection | WRPLB_0_0        | <b>Write PPB Protection Lock Bit</b> transaction clears the PPB Lock to 0.                                                                                                                                                                                                                                                                                                                | WRENB_0_0                | A6 (CMD)     | -               | -                | -                 | -                 | -                 | -                 | -                 | -                 |                    | 166                 | 4              |
|                            | RDPLB_0_0        | <b>Read Password Protection Mode Lock Bit</b> transaction shifts out the 8-bit PPB Lock Register contents with MSb first.                                                                                                                                                                                                                                                                 | -                        | A7 (CMD)     | -               | -                | -                 | -                 | -                 | -                 | -                 | -                 | Figure 11          |                     |                |
|                            | PWDUL_0_1        | <b>Password Unlock</b> transaction sends the 64-bit password to flash device. If the supplied password does not match the hidden password in the Password Register, the device is locked and only a hardware reset or POR will return the device to standby state, ready for new transactions such as a retry of the PWDUL_0_1. If the password does match, the PPB Lock bit is set to 1. | -                        | E9 (CMD)     | Passw ord [7:0] | Passw ord [15:8] | Passw ord [23:16] | Passw ord [31:24] | Passw ord [39:32] | Passw ord [47:40] | Passwo rd [55:48] | Passw ord [63:56] | Figure 10          |                     |                |
| Reset                      | SRSTE_0_0        | <b>Software Reset Enable</b> command is required immediately before a SFRST_0_0 transaction.                                                                                                                                                                                                                                                                                              | -                        | 66 (CMD)     | -               | -                | -                 | -                 | -                 | -                 | -                 | -                 |                    | 166                 | N/A            |
|                            | SFRST_0_0        | <b>Software Reset</b> transaction restores the device to its initial power up state, by reloading volatile registers from non-volatile default values.                                                                                                                                                                                                                                    | SRSTE_0_0                | 99 (CMD)     | -               | -                | -                 | -                 | -                 | -                 | -                 | -                 | Figure 6           |                     |                |
|                            | ENDPD_0_0        | <b>Enter Deep Power Down Mode</b> transaction shifts device in the lowest power consumption mode.                                                                                                                                                                                                                                                                                         | -                        | B9 (CMD)     | -               | -                | -                 | -                 | -                 | -                 | -                 | -                 |                    |                     |                |

## 6.2 Octal (8S-8S-8S, 8D-8D-8D) transaction table

**Table 82** Octal (8S-8S-8S, 8D-8D-8D) transaction table

| Function           | Transaction name | Description                                                                                                                                    | Prerequisite transaction | Byte 1 (Hex)         | Byte 2 (Hex)         | Byte 3 (Hex)         | Byte 4 (Hex)         | Byte 5 (Hex)         | Byte 6 (Hex)         | Byte 7 (Hex)         | Byte 8 (Hex)         | Byte 9 (Hex)         | Byte 10 (Hex)        | Byte 11 (Hex)        | Byte 12 (Hex)        | Byte 13 (Hex)        | Byte 14 (Hex)        | Trans-<br>action<br>format<br>(SDR/DDR) | HL-T / HS-T<br>max<br>frequency<br>(MHz) | Address<br>length |     |
|--------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|-----------------------------------------|------------------------------------------|-------------------|-----|
|                    |                  |                                                                                                                                                |                          | CK ↑<br>edge<br>[32] | CK ↓<br>edge<br>[32] | CK ↑<br>edge<br>[32] | CK ↓<br>edge<br>[32] | CK ↑<br>edge<br>[32] | CK ↓<br>edge<br>[32] | CK ↑<br>edge<br>[32] | CK ↓<br>edge<br>[32] | CK ↑<br>edge<br>[32] | CK ↓<br>edge<br>[32] | CK ↑<br>edge<br>[32] | CK ↓<br>edge<br>[32] | CK ↑<br>edge<br>[32] | CK ↓<br>edge<br>[32] |                                         |                                          |                   |     |
| Read<br>device ID  | RDIDN_4_0        | <b>Read manufacturer and device identification</b> transaction provides read access to manufacturer and device identification.                 | -                        | 9F (CMD)             | 9F (CMD)             | 00 (ADDR)            | 00 (ADDR)            | 00 (ADDR)            | 00 (ADDR)            | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | Figure 24<br>/<br>Figure 25             | 166/200                                  | 4                 |     |
|                    | RSFDP_4_0        | <b>Read JEDEC Serial Flash Discoverable Parameters</b> transaction sequentially accesses the Serial Flash Discovery Parameters (SFDP).         | -                        | 5A (CMD)             | 5A (CMD)             | ADDR [31:24]         | ADDR [23:16]         | ADDR [15:8]          | ADDR [7:0]           | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    |                                         | 92 (SDR) /<br>85 (DDR)                   |                   |     |
|                    | RDUID_4_0        | <b>Read Unique ID</b> accesses a factory programmed 64-bit number which is unique to each device.                                              | -                        | 4C (CMD)             | 4C (CMD)             | 00 (ADDR)            | 00 (ADDR)            | 00 (ADDR)            | 00 (ADDR)            | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    |                                         |                                          |                   |     |
| Register<br>access | RDSR1_4_0        | <b>Read Status Register 1</b> transaction allows the Status Register 1 contents to be read from DQ[7:0]                                        | -                        | 05 (CMD)             | 05 (CMD)             | 00 (ADDR)            | 00 (ADDR)            | 00 (ADDR)            | 00 (ADDR)            | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | Figure 24<br>/<br>Figure 26             | 166 / 200                                |                   | N/A |
|                    | RDSR2_4_0        | <b>Read Status Register-2</b> transaction allows the Status Register-2 contents to be read from DQ[7:0]                                        | -                        | 07 (CMD)             | 07 (CMD)             | 00 (ADDR)            | 00 (ADDR)            | 00 (ADDR)            | 00 (ADDR)            | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    |                                         |                                          |                   |     |
|                    | RDARG_4_0        | <b>Read Any Register</b> transaction provides a way to read all addressed non-volatile and volatile device registers.                          | -                        | 65 (CMD)             | 65 (CMD)             | ADDR [31:24]         | ADDR [23:16]         | ADDR [15:8]          | ADDR [7:0]           | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    |                                         |                                          |                   |     |
|                    | WRENB_0_0        | <b>Write Enable</b> sets the Write Enable Latch bit of the Status Register 1 to 1 to enable write, program and erase transactions.             | -                        | 06 (CMD)             | 06 (CMD)             | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | Figure 15<br>/<br>Figure 16             |                                          |                   |     |
|                    | WRDIS_0_0        | <b>Write Disable</b> sets the Write Enable Latch bit of the Status Register 1 to 0 to disable write, program and erase transactions execution. | -                        | 04 (CMD)             | 04 (CMD)             | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    | -                    |                                         |                                          |                   |     |
|                    | WRARG_4_1        | <b>Write Any Register</b> transaction provides a way to write all addressed non-volatile and volatile device registers.                        | WRENB_0_0                | 71 (CMD)             | 71 (CMD)             | ADDR [31:24]         | ADDR [23:16]         | ADDR [15:8]          | ADDR [7:0]           | Input Data [7:0]     | -                    | -                    | -                    | -                    | -                    | -                    | -                    |                                         | Figure 21<br>/<br>Figure 22              | 4                 |     |

**Note**  
32. In case of Octal DDR protocol.

**Table 82 Octal (8S-8S-8S, 8D-8D-8D) transaction table (Continued)**

| Function            | Transaction name | Description                                                                                                                                                                                               | Prerequisite transaction | Byte 1 (Hex)   | Byte 2 (Hex)   | Byte 3 (Hex)   | Byte 4 (Hex)   | Byte 5 (Hex)   | Byte 6 (Hex)   | Byte 7 (Hex)       | Byte 8 (Hex)       | Byte 9 (Hex)      | Byte 10 (Hex)    | Byte 11 (Hex)    | Byte 12 (Hex)    | Byte 13 (Hex)   | Byte 14 (Hex)  | Transaction format (SDR/DDR) | HL-T / HS-T max frequency (MHz) | Address length |
|---------------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------|----------------|----------------|----------------|----------------|----------------|--------------------|--------------------|-------------------|------------------|------------------|------------------|-----------------|----------------|------------------------------|---------------------------------|----------------|
|                     |                  |                                                                                                                                                                                                           |                          | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32]     | CK ↓ edge [32]     | CK ↑ edge [32]    | CK ↓ edge [32]   | CK ↑ edge [32]   | CK ↓ edge [32]   | CK ↑ edge [32]  | CK ↓ edge [32] |                              |                                 |                |
| Register access     | CLPEF_0_0        | <b>Clear Program and Erase Failure Flags</b> transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag)                                                                         | -                        | 82 (CMD)       | 82 (CMD)       | -              | -              | -              | -              | -                  | -                  | -                 | -                | -                | -                | -               | -              | Figure 15 / Figure 16        | 166 / 200                       | N/A            |
| ECC                 | RDECC_4_0        | <b>Read ECC Status</b> is used to determine the ECC status of the addressed data unit.                                                                                                                    | -                        | 19 (CMD)       | 19 (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                  | -                  | -                 | -                | -                | -                | -               | -              | Figure 24 / Figure 26        |                                 | 4              |
|                     | CLECC_0_0        | <b>Clear ECC Status Register</b> transaction resets ECC Status Register bit[4] (2-bit ECC Detection), ECC Status Register bit[3] (1-bit ECC Correction), Address Trap Register and ECC Detection Counter. | -                        | 1B (CMD)       | 1B (CMD)       | -              | -              | -              | -              | -                  | -                  | -                 | -                | -                | -                | -               | -              | Figure 15 / Figure 16        |                                 | N/A            |
| CRC                 | RDCRC_4_0        | <b>Read Interface CRC Register</b> transaction allows the volatile Interface CRC Register contents to be read                                                                                             | -                        | 64 (CMD)       | 64 (CMD)       | 00 (ADDR)      | 00 (ADDR)      | 00 (ADDR)      | 00 (ADDR)      | -                  | -                  | -                 | -                | -                | -                | -               | -              | Figure 24 / Figure 25        |                                 |                |
|                     | DICLK_4_1        | <b>Data Integrity Check</b> transaction causes the device to perform a Data Integrity Check over a user defined address range.                                                                            | -                        | 5B (CMD)       | 5B (CMD)       | 00 (ADDR)      | 00 (ADDR)      | 00 (ADDR)      | 00 (ADDR)      | Start ADDR [31:24] | Start ADDR [23:16] | Start ADDR [15:8] | Start ADDR [7:0] | End ADDR [31:24] | End ADDR [23:16] | End ADDR [15:8] | End ADDR [7:0] | Figure 19 / Figure 20        |                                 |                |
| Read flash array    | RDAY1_4_0        | <b>Read Octal SDR</b> transaction reads out the memory contents at the given address on DQ[7:0]. The maximum CK frequency for this SDR transaction is 200-MHz frequency                                   | -                        | EC (CMD)       | EC (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                  | -                  | -                 | -                | -                | -                | -               | -              | Figure 24                    | 4                               |                |
|                     | RDAY2_4_0        | <b>Read Octal DDR</b> transaction reads out the memory contents at the given address on DQ[7:0]. The maximum CK frequency for this DDR transaction is 200-MHz frequency                                   | -                        | EE (CMD)       | EE (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                  | -                  | -                 | -                | -                | -                | -               | -              | Figure 25                    |                                 |                |
| Program flash array | PRPGE_4_1        | <b>Program Page</b> programs 256B or 512B data to the memory array in one transaction.                                                                                                                    | WRENB_0_0                | 12 (CMD)       | 12 (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue)        | -                | -                | -                | -               | -              | Figure 21 / Figure 22        |                                 |                |

**Note**  
32. In case of Octal DDR protocol.

**Table 82 Octal (8S-8S-8S, 8D-8D-8D) transaction table (Continued)**

| Function              | Transaction name | Description                                                                                                                                             | Prerequisite transaction | Byte 1 (Hex)   | Byte 2 (Hex)   | Byte 3 (Hex)   | Byte 4 (Hex)   | Byte 5 (Hex)   | Byte 6 (Hex)   | Byte 7 (Hex)       | Byte 8 (Hex)       | Byte 9 (Hex)   | Byte 10 (Hex)  | Byte 11 (Hex)  | Byte 12 (Hex)  | Byte 13 (Hex)  | Byte 14 (Hex)  | Transaction format (SDR/DDR) | HL-T / HS-T max frequency (MHz) | Address length |
|-----------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------|----------------|----------------|----------------|----------------|----------------|--------------------|--------------------|----------------|----------------|----------------|----------------|----------------|----------------|------------------------------|---------------------------------|----------------|
|                       |                  |                                                                                                                                                         |                          | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32]     | CK ↓ edge [32]     | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] |                              |                                 |                |
| Erase flash array     | ER004_4_0        | <b>Erase 4-KB Sector</b> transaction sets all the bits of a 4KB sector to 1 (all bytes are FFh).                                                        | WRENB_0_0                | 21 (CMD)       | 21 (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                  | -                  | -              | -              | -              | -              | -              | -              | Figure 17 / Figure 18        | 166 / 200                       | 4              |
|                       | ER256_4_0        | <b>Erase 256-KB Sector</b> transaction sets all the bits of a 256KB sector to 1 (all bytes are FFh).                                                    | WRENB_0_0                | DC (CMD)       | DC (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                  | -                  | -              | -              | -              | -              | -              | -              |                              |                                 |                |
|                       | ERCHP_0_0        | <b>Erase Chip</b> transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array.                                              | WRENB_0_0                | 60 or C7 (CMD) | 60 or C7 (CMD) | -              | -              | -              | -              | -                  | -                  | -              | -              | -              | -              | -              | -              | Figure 15 / Figure 16        |                                 | N/A            |
|                       | EVERS_4_0        | <b>Evaluate Erase Status</b> transaction verifies that the last erase operation on the addressed sector was completed successfully.                     | -                        | D0 (CMD)       | D0 (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                  | -                  | -              | -              | -              | -              | -              | -              | Figure 17 / Figure 18        |                                 | 4              |
|                       | SEERC_4_0        | <b>Sector Erase Count</b> transaction outputs the number of erase cycles for the sector of the inputted address from the Sector Erase Count Register.   | -                        | 5D (CMD)       | 5D (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                  | -                  | -              | -              | -              | -              | -              | -              |                              |                                 |                |
| Suspend / resume      | SPEPD_0_0        | <b>Suspend Erase / Program / Data Integrity Check</b> transaction allows the system to interrupt a programming, erase or data integrity check operation | -                        | B0 (CMD)       | B0 (CMD)       | -              | -              | -              | -              | -                  | -                  | -              | -              | -              | -              | -              | -              | Figure 15 / Figure 16        | N/A                             |                |
|                       | RSEPD_0_0        | <b>Resume Erase / Program / Data Integrity Check</b> transaction allows the system to resume a programming, erase or data integrity check operation     | -                        | 30 (CMD)       | 30 (CMD)       | -              | -              | -              | -              | -                  | -                  | -              | -              | -              | -              | -              | -              |                              |                                 |                |
| Secure silicon region | PRSSR_4_1        | <b>Program Secure Silicon Region</b> transaction programs data in 1024 bytes of Secure Silicon Region                                                   | WRENB_0_0                | 42 (CMD)       | 42 (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | Input Data 1 [7:0] | Input Data 2 [7:0] | (Continue)     | -              | -              | -              | -              | -              | Figure 21 / Figure 22        | 4                               |                |
|                       | RDSSR_4_0        | <b>Read Secure Silicon Region</b> transaction reads data from the SSR.                                                                                  | -                        | 4B (CMD)       | 4B (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                  | -                  | -              | -              | -              | -              | -              | -              | Figure 24 / Figure 25        |                                 |                |

**Note**  
32. In case of Octal DDR protocol.

**Table 82** Octal (8S-8S-8S, 8D-8D-8D) transaction table (Continued)

| Function                   | Transaction name | Description                                                                                                                                                                                                                                                                                                                                                                               | Prerequisite transaction | Byte 1 (Hex)   | Byte 2 (Hex)   | Byte 3 (Hex)   | Byte 4 (Hex)   | Byte 5 (Hex)   | Byte 6 (Hex)   | Byte 7 (Hex)     | Byte 8 (Hex)     | Byte 9 (Hex)      | Byte 10 (Hex)     | Byte 11 (Hex)     | Byte 12 (Hex)     | Byte 13 (Hex)     | Byte 14 (Hex)     | Transaction format (SDR/DDR) | HL-T / HS-T max frequency (MHz) | Address length |
|----------------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------------------------------|---------------------------------|----------------|
|                            |                  |                                                                                                                                                                                                                                                                                                                                                                                           |                          | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32]   | CK ↓ edge [32]   | CK ↑ edge [32]    | CK ↓ edge [32]    | CK ↑ edge [32]    | CK ↓ edge [32]    | CK ↑ edge [32]    | CK ↓ edge [32]    |                              |                                 |                |
| Advanced sector protection | RDDYB_4_0        | <b>Read Dynamic Protection Bit</b> transaction reads the contents of the DYB Access Register.                                                                                                                                                                                                                                                                                             | -                        | E0 (CMD)       | E0 (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                | -                | -                 | -                 | -                 | -                 | -                 | -                 | Figure 24 / Figure 26        | 166 / 200                       | 4              |
|                            | WRDYB_4_1        | <b>Write Dynamic Protection Bit</b> transaction writes to the DYB Access Register                                                                                                                                                                                                                                                                                                         | WRENB_0_0                | E1 (CMD)       | E1 (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | Input Data [7:0] | -                | -                 | -                 | -                 | -                 | -                 | -                 | Figure 21 / Figure 23        |                                 | N/A            |
|                            | RDPPB_4_0        | <b>Read Persistent Protection Bit</b> transaction reads the contents of the PPB Access Register                                                                                                                                                                                                                                                                                           | -                        | E2 (CMD)       | E2 (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                | -                | -                 | -                 | -                 | -                 | -                 | -                 | Figure 24 / Figure 26        |                                 | 4              |
|                            | PRPPB_4_0        | <b>Program Persistent Protection Bit</b> transaction programs / writes the PPB Register to enable the sector protection.                                                                                                                                                                                                                                                                  | WRENB_0_0                | E3 (CMD)       | E3 (CMD)       | ADDR [31:24]   | ADDR [23:16]   | ADDR [15:8]    | ADDR [7:0]     | -                | -                | -                 | -                 | -                 | -                 | -                 | -                 | Figure 17 / Figure 18        |                                 | N/A            |
|                            | ERPPB_0_0        | <b>Erase Persistent Protection Bit</b> transaction sets all persistent protection bits to 1.                                                                                                                                                                                                                                                                                              | WRENB_0_0                | E4 (CMD)       | E4 (CMD)       | -              | -              | -              | -              | -                | -                | -                 | -                 | -                 | -                 | -                 | -                 | Figure 15 / Figure 16        |                                 | N/A            |
|                            | WRPLB_0_0        | <b>Write PPB Protection Lock Bit</b> transaction clears the PPB Lock to 0                                                                                                                                                                                                                                                                                                                 | WRENB_0_0                | 2C (CMD)       | 2C (CMD)       | -              | -              | -              | -              | -                | -                | -                 | -                 | -                 | -                 | -                 | -                 | -                            |                                 | 4              |
|                            | RDPLB_4_0        | <b>Read Password Protection Mode Lock Bit</b> transaction shifts out the 8-bit PPB Lock Register contents with MSb first.                                                                                                                                                                                                                                                                 | -                        | 2D (CMD)       | 2D (CMD)       | 00 (ADDR)      | 00 (ADDR)      | 00 (ADDR)      | 00 (ADDR)      | -                | -                | -                 | -                 | -                 | -                 | -                 | -                 | Figure 24 / Figure 26        |                                 | 4              |
|                            | PWDUL_4_1        | <b>Password Unlock</b> transaction sends the 64-bit password to flash device. If the supplied password does not match the hidden password in the Password Register, the device is locked and only a hardware reset or POR will return the device to standby state, ready for new transactions such as a retry of the PWDUL_0_1. If the password does match, the PPB Lock bit is set to 1. | -                        | E9 (CMD)       | E9 (CMD)       | 00 (ADDR)      | 00 (ADDR)      | 00 (ADDR)      | 00 (ADDR)      | Passw ord [7:0]  | Passw ord [15:8] | Passw ord [23:16] | Passw ord [31:24] | Passw ord [39:32] | Passw ord [47:40] | Passw ord [55:48] | Passw ord [63:56] | Figure 21 / Figure 22        | N/A                             |                |

**Note**  
32. In case of Octal DDR protocol.

Transaction table

Table 82 Octal (8S-8S-8S, 8D-8D-8D) transaction table (Continued)

| Function        | Transaction name | Description                                                                                                                                           | Prerequisite transaction | Byte 1 (Hex)   | Byte 2 (Hex)   | Byte 3 (Hex)   | Byte 4 (Hex)   | Byte 5 (Hex)   | Byte 6 (Hex)   | Byte 7 (Hex)   | Byte 8 (Hex)   | Byte 9 (Hex)   | Byte 10 (Hex)  | Byte 11 (Hex)  | Byte 12 (Hex)  | Byte 13 (Hex)  | Byte 14 (Hex)  | Transaction format (SDR/DDR) | HL-T / HS-T max frequency (MHz) | Address length |
|-----------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|------------------------------|---------------------------------|----------------|
|                 |                  |                                                                                                                                                       |                          | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] | CK ↑ edge [32] | CK ↓ edge [32] |                              |                                 |                |
| Reset           | SRSTE_0_0        | <b>Software Reset Enable</b> command is required immediately before a SFRST_0_0 transaction                                                           | -                        | 66 (CMD)       | 66 (CMD)       | -              | -              | -              | -              | -              | -              | -              | -              | -              | -              | -              | -              | Figure 15 / Figure 16        | 166 / 200                       | N/A            |
|                 | SFRST_0_0        | <b>Software Reset</b> transaction restores the device to its initial power up state, by reloading volatile registers from non-volatile default values | SFRSE_0_0                | 99 (CMD)       | 99 (CMD)       | -              | -              | -              | -              | -              | -              | -              | -              | -              | -              | -              | -              |                              |                                 |                |
| Deep power down | ENDPD_0_0        | <b>Enter Deep Power Down Mode</b> transaction shifts device in the lowest power consumption mode                                                      | -                        | B9 (CMD)       | B9 (CMD)       | -              | -              | -              | -              | -              | -              | -              | -              | -              | -              | -              | -              |                              |                                 |                |

**Note**  
32. In case of Octal DDR protocol.

## 7 Electrical characteristics

### 7.1 Absolute maximum ratings<sup>[35]</sup>

|                                                                         |                                   |
|-------------------------------------------------------------------------|-----------------------------------|
| Storage temperature plastic packages                                    | –65°C to +150°C                   |
| Ambient temperature with power applied                                  | –65°C to +125°C                   |
| V <sub>CC</sub> (HL-T)                                                  | –0.5 V to +4.0 V                  |
| V <sub>CC</sub> (HS-T)                                                  | –0.5 V to +2.5 V                  |
| Input voltage with respect to ground (V <sub>SS</sub> ) <sup>[33]</sup> | –0.5 V to V <sub>CC</sub> + 0.5 V |
| Output short circuit current <sup>[34]</sup>                            | 100 mA                            |

#### Notes

33. See “**Input signal overshoot**” on page 131 for allowed maximums during signal transition.

34. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

35. Stresses above those listed under “**Absolute maximum ratings[35]**” on page 129 may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

### 7.2 Operating range

Operating ranges define those limits between which the functionality of the device is guaranteed.

#### 7.2.1 Power supply voltages

|                                                   |                |
|---------------------------------------------------|----------------|
| V <sub>CC</sub> / V <sub>CCQ</sub> (HL-T devices) | 2.7 V to 3.6 V |
| V <sub>CC</sub> / V <sub>CCQ</sub> (HS-T devices) | 1.7 V to 2.0 V |

#### 7.2.2 Temperature ranges

**Table 83** Temperature range

| Parameter           | Symbol         | Devices                                                       | Spec |      | Unit |
|---------------------|----------------|---------------------------------------------------------------|------|------|------|
|                     |                |                                                               | Min  | Max  |      |
| Ambient temperature | T <sub>A</sub> | Industrial / automotive AEC-Q100 grade 3                      | –40  | +85  | °C   |
|                     |                | Industrial plus / automotive AEC-Q100 grade 2 <sup>[36]</sup> |      | +105 |      |
|                     |                | Automotive AEC-Q100 grade 1 <sup>[36]</sup>                   |      | +125 |      |

#### Note

36. Industrial plus, automotive grade-2 and automotive grade-1 operating and performance parameters will be determined by device characterization and may vary from standard industrial or automotive grade-3 temperature range devices as currently shown in this specification.

## 7.3 Thermal resistance

**Table 84 Thermal resistance**

| Parameter | Description                              | Test Condition                                                                                                                                    | Device | 24-ball BGA | Unit |
|-----------|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|------|
| Theta JA  | Thermal resistance (Junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance in accordance with EIA/JESD51. With Still Air (0 m/s) | 512T   | 40.4        | °C/W |
|           |                                          |                                                                                                                                                   | 01GT   | 37          |      |
| Theta JB  | Thermal resistance (Junction to board)   |                                                                                                                                                   | 512T   | 14.5        |      |
|           |                                          |                                                                                                                                                   | 01GT   | 9.7         |      |
| Theta JC  | Thermal resistance (Junction to case)    |                                                                                                                                                   | 512T   | 8           |      |
|           |                                          |                                                                                                                                                   | 01GT   | 7.5         |      |

## 7.4 Capacitance characteristics

**Table 85 Capacitance**

| Symbol           | Parameter                                      | Test conditions | Typ  | Max  | Unit |
|------------------|------------------------------------------------|-----------------|------|------|------|
| C <sub>IN</sub>  | Input capacitance (applies to CK, CS#, RESET#) | 1 MHz           | 3.0  | 7.50 | pF   |
| C <sub>OUT</sub> | Output capacitance (applies to all I/O)        |                 | 6.50 |      |      |

## 7.5 Latchup characteristics

**Table 86 Latchup specifications<sup>[37]</sup>**

| Description                                                                        | Min         | Max                          | Unit      |
|------------------------------------------------------------------------------------|-------------|------------------------------|-----------|
| <b>Input voltage with respect to V<sub>SSQ</sub> on all input only connections</b> | <b>-1.0</b> | <b>V<sub>CCQ</sub> + 1.0</b> | <b>V</b>  |
| <b>Input voltage with respect to V<sub>SSQ</sub> on all I/O connections</b>        |             |                              |           |
| <b>V<sub>CCQ</sub> current</b>                                                     | <b>-100</b> | <b>+100</b>                  | <b>mA</b> |

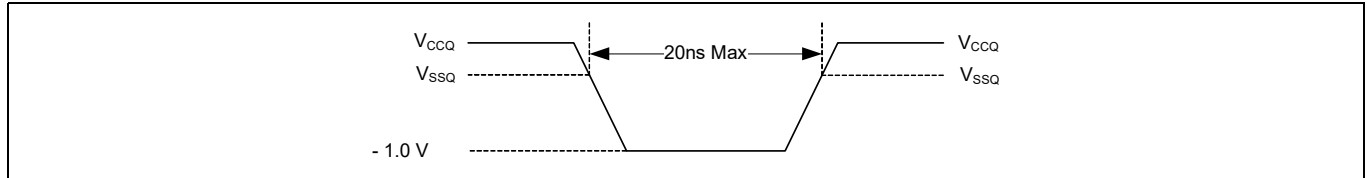
### Note

37.Excludes power supply V<sub>CC</sub>. Test conditions: V<sub>CC</sub> = 1.8 V / 3.0 V, one connection at a time tested, connections not being tested are at V<sub>SS</sub>.

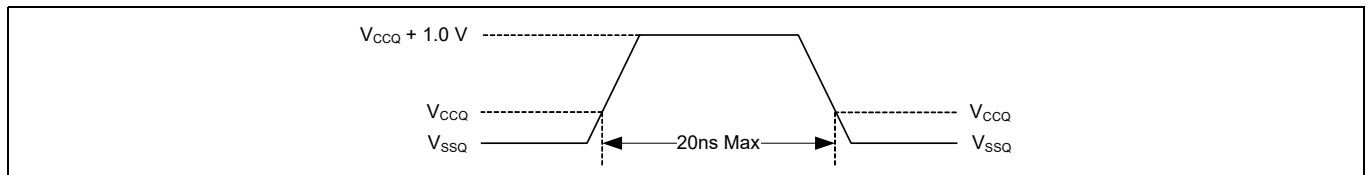
## 7.6 DC characteristics

### 7.6.1 Input signal overshoot

During DC conditions, input or I/O signals should remain equal to or between  $V_{SSQ}$  and  $V_{CCQ}$ . During voltage transitions, inputs or I/Os may overshoot  $V_{SSQ}$  to  $-1.0\text{ V}$  or overshoot to  $V_{CCQ} + 1.0\text{ V}$ , for periods up to 20 ns.



**Figure 66** Maximum negative overshoot waveform



**Figure 67** Maximum positive overshoot waveform

### 7.6.2 DC characteristics (all temperature ranges)

**Table 87** DC Characteristics<sup>[38, 40]</sup>

| Symbol   | Parameter                           | Test conditions                                                                                    | Min                    | Typ | Max                   | Unit          | Reference figure |
|----------|-------------------------------------|----------------------------------------------------------------------------------------------------|------------------------|-----|-----------------------|---------------|------------------|
| $V_{IL}$ | Input low voltage (all $V_{CC}$ )   | –                                                                                                  | $V_{CCQ} \times -0.15$ | –   | $V_{CCQ} \times 0.35$ | V             | –                |
| $V_{IH}$ | Input high voltage (all $V_{CC}$ )  | –                                                                                                  | $V_{CCQ} \times 0.65$  |     | $V_{CCQ} \times 1.15$ |               |                  |
| $V_{OL}$ | Output low voltage (all $V_{CC}$ )  | At 0.1 mA                                                                                          | –                      |     | 0.2                   |               |                  |
| $V_{OH}$ | Output high voltage (all $V_{CC}$ ) | At $-0.1\text{ mA}$                                                                                | $V_{CCQ} - 0.20$       |     |                       |               |                  |
| $I_{LI}$ | Input leakage current               | $V_{CC} = V_{CC}\text{ Max}$ ,<br>$V_{IN} = V_{IH}\text{ or }V_{SS}$ ,<br>$CS\# = V_{IH}$ , 85 °C  | –                      | –   | $\pm 2$               | $\mu\text{A}$ | –                |
|          |                                     | $V_{CC} = V_{CC}\text{ Max}$ ,<br>$V_{IN} = V_{IH}\text{ or }V_{SS}$ ,<br>$CS\# = V_{IH}$ , 105 °C |                        |     | $\pm 3$               |               |                  |
|          |                                     | $V_{CC} = V_{CC}\text{ Max}$ ,<br>$V_{IN} = V_{IH}\text{ or }V_{SS}$ ,<br>$CS\# = V_{IH}$ , 125 °C |                        |     | $\pm 4$               |               |                  |

#### Notes

38. Typical values are at  $T_{AI} = 25\text{ °C}$  and  $V_{CC} = 1.8\text{ V}/3.0\text{ V}$ .

39. Outputs unconnected during read data return. Output switching current is not included.

40. The recommended pull-up resistor for the INT# outputs is 5 k $\Omega$  to 10 k $\Omega$ .

**Table 87 DC Characteristics**<sup>[38, 40]</sup> (Continued)

| Symbol    | Parameter                                                         | Test conditions                                                                                       | Min | Typ                    | Max                    | Unit | Reference figure |
|-----------|-------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|-----|------------------------|------------------------|------|------------------|
| $I_{LO}$  | Output leakage current                                            | $V_{CC} = V_{CC} \text{ Max}$ ,<br>$V_{IN} = V_{IH} \text{ or } V_{SS}$ ,<br>$CS\# = V_{IH}$ , 85 °C  | –   | –                      | ±2                     | μA   | –                |
|           |                                                                   | $V_{CC} = V_{CC} \text{ Max}$ ,<br>$V_{IN} = V_{IH} \text{ or } V_{SS}$ ,<br>$CS\# = V_{IH}$ , 105 °C |     |                        | ±3                     |      |                  |
|           |                                                                   | $V_{CC} = V_{CC} \text{ Max}$ ,<br>$V_{IN} = V_{IH} \text{ or } V_{SS}$ ,<br>$CS\# = V_{IH}$ , 125 °C |     |                        | ±4                     |      |                  |
| $I_{CC1}$ | Active power supply current (READ) <sup>[39]</sup>                | SDR @ 50MHz<br>(HL512T /<br>HS512T)<br>(HL01GT /<br>HS01GT)                                           | –   | 10 / 10<br>18 / 14     | 21 / 18<br>25 / 25     | mA   | –                |
|           |                                                                   | SDR @ 166MHz<br>(HL512T /<br>HS512T)<br>(HL01GT /<br>HS01GT)                                          |     | 75 / 75<br>75 / 80     | 100 / 100<br>100 / 100 |      |                  |
|           |                                                                   | DDR @ 200MHz<br>(HL512T /<br>HS512T)<br>(HL01GT /<br>HS01GT)                                          |     | 156 / 156<br>156 / 156 | 173 / 173<br>173 / 173 |      |                  |
| $I_{CC2}$ | Active power supply current (page program)<br>(512T / 01GT)       | $V_{CC} = V_{CC} \text{ Max}$ ,<br>$CS\# = V_{IH}$                                                    | –   | 50                     | 58 / 66                | mA   | –                |
| $I_{CC3}$ | Active power supply current (write any register)<br>(512T / 01GT) | $V_{CC} = V_{CC} \text{ Max}$ ,<br>$CS\# = V_{IH}$                                                    | –   | 50                     | 55 / 66                | mA   | –                |
| $I_{CC4}$ | Active power supply current (sector erase)<br>(512T / 01GT)       | $V_{CC} = V_{CC} \text{ Max}$ ,<br>$CS\# = V_{IH}$                                                    | –   | 50                     | 55 / 66                | mA   | –                |
| $I_{CC5}$ | Active power supply current (chip erase)<br>(512T / 01GT)         | $V_{CC} = V_{CC} \text{ Max}$ ,<br>$CS\# = V_{IH}$                                                    | –   | 50                     | 55 / 66                | mA   | –                |

**Notes**

38. Typical values are at  $T_{AI} = 25 \text{ °C}$  and  $V_{CC} = 1.8 \text{ V}/3.0 \text{ V}$ .

39. Outputs unconnected during read data return. Output switching current is not included.

40. The recommended pull-up resistor for the INT# outputs is 5 kΩ to 10 kΩ.

**Table 87** DC Characteristics<sup>[38, 40]</sup> (Continued)

| Symbol   | Parameter                                            | Test conditions                                                              | Min | Typ | Max                | Unit    | Reference figure |
|----------|------------------------------------------------------|------------------------------------------------------------------------------|-----|-----|--------------------|---------|------------------|
| $I_{SB}$ | Standby current<br>(HS512T / HS01GTxx<br>/ HS01GTGZ) | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 85°C  | –   | 11  | 113 / 160 /<br>180 | $\mu A$ | –                |
|          |                                                      | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 105°C | –   |     | 188 / 320 /<br>350 |         |                  |
|          |                                                      | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 125°C | –   |     | 340 / 490 /<br>650 |         |                  |
|          | Standby current<br>(HL512T / HL01GT)                 | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 85°C  | –   | 14  | 126 / 160          |         |                  |
|          |                                                      | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 105°C | –   |     | 188 / 320          |         |                  |
|          |                                                      | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 125°C | –   |     | 340 / 490          |         |                  |

**Notes**38. Typical values are at  $T_{AI} = 25^\circ C$  and  $V_{CC} = 1.8 V/3.0 V$ .

39. Outputs unconnected during read data return. Output switching current is not included.

40. The recommended pull-up resistor for the INT# outputs is 5 k $\Omega$  to 10 k $\Omega$ .

**Table 87** DC Characteristics<sup>[38, 40]</sup> (Continued)

| Symbol                        | Parameter                                        | Test conditions                                                              | Min | Typ             | Max          | Unit    | Reference figure        |
|-------------------------------|--------------------------------------------------|------------------------------------------------------------------------------|-----|-----------------|--------------|---------|-------------------------|
| $I_{DPD}$                     | DPD current<br>(HS512T / HS01GTxx<br>/ HS01GTGZ) | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 85°C  | –   | 1.3 / 1.3 / 1.3 | 18 / 24 / 24 | $\mu A$ | –                       |
|                               |                                                  | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 105°C | –   |                 | 18 / 26 / 46 |         |                         |
|                               |                                                  | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 125°C | –   |                 | 31 / 52 / 80 |         |                         |
|                               | DPD current<br>(HL512T / HL01GT)                 | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 85°C  | –   | 2.2 / 2.2       | 18 / 26      |         |                         |
|                               |                                                  | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 105°C | –   |                 | 18 / 26      |         |                         |
|                               |                                                  | RESET#, CS# =<br>$V_{CCQ}$ ;<br>All I/Os = $V_{CCQ}$ or<br>$V_{SSQ}$ , 125°C | –   |                 | 31 / 52      |         |                         |
| $I_{POR}$                     | POR current                                      | RESET#, CS# =<br>$V_{CCQ}$ ; All I/Os =<br>$V_{CCQ}$ or $V_{SSQ}$            | –   | –               | 80           | mA      | –                       |
| Power up / Power down voltage |                                                  |                                                                              |     |                 |              |         |                         |
| $V_{CC}$<br>(min)             | $V_{CC}$ (minimum<br>operation voltage,<br>HL-T) | –                                                                            | 2.7 | –               | –            | V       | Figure 61/<br>Figure 63 |
|                               | $V_{CC}$ (minimum<br>operation voltage,<br>HS-T) | –                                                                            | 1.7 |                 |              |         |                         |

**Notes**38. Typical values are at  $T_{AI} = 25^\circ C$  and  $V_{CC} = 1.8 V/3.0 V$ .

39. Outputs unconnected during read data return. Output switching current is not included.

40. The recommended pull-up resistor for the INT# outputs is 5 k $\Omega$  to 10 k $\Omega$ .

**Table 87** DC Characteristics<sup>[38, 40]</sup> (Continued)

| Symbol                       | Parameter                                                         | Test conditions | Min  | Typ | Max | Unit | Reference figure |
|------------------------------|-------------------------------------------------------------------|-----------------|------|-----|-----|------|------------------|
| V <sub>CC</sub><br>(cut-off) | V <sub>CC</sub> (cut off where re-initialization is needed, HL-T) | –               | 2.4  | –   | –   | V    | Figure 62        |
|                              | V <sub>CC</sub> (cut off where re-initialization is needed, HS-T) | –               | 1.55 |     |     |      |                  |
| V <sub>CC</sub><br>(Low)     | V <sub>CC</sub> (low voltage for initialization to occur, HL-T)   | –               | 0.7  | –   | –   | V    |                  |
|                              | V <sub>CC</sub> (low voltage for initialization to occur, HS-T)   | –               | 0.7  |     |     |      |                  |

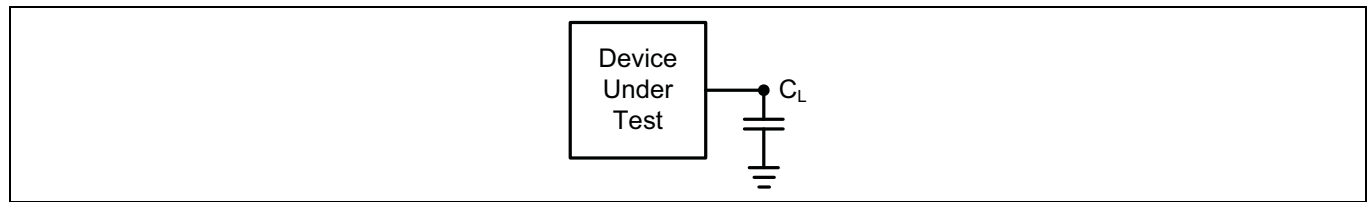
**Notes**

38. Typical values are at T<sub>AI</sub> = 25 °C and V<sub>CC</sub> = 1.8 V/3.0 V.

39. Outputs unconnected during read data return. Output switching current is not included.

40. The recommended pull-up resistor for the INT# outputs is 5 kΩ to 10 kΩ.

## 7.7 AC test conditions



**Figure 68** Test setup

**Table 88** AC measurement conditions<sup>[42]</sup>

| Parameter                                                                                     | Min                    | Max                   | Unit | Reference Figure      |
|-----------------------------------------------------------------------------------------------|------------------------|-----------------------|------|-----------------------|
| Load capacitance ( $C_L$ )                                                                    | -                      | 15                    | pF   | Figure 68             |
| Input pulse voltage                                                                           | 0                      | $V_{CCQ}$             | V    | Figure 70             |
| CK rise ( $t_{CRT1}$ ) and fall ( $t_{CFT1}$ ) slew rates at 200 MHz (HS-T) <sup>[41]</sup>   | 1.13                   | -                     | V/ns | Figure 73             |
| CK rise ( $t_{CRT2}$ ) and fall ( $t_{CFT2}$ ) slew rates at 166 MHz (HL-T) <sup>[41]</sup>   | 1.72                   |                       |      |                       |
| Data rise ( $t_{DRT1}$ ) and fall ( $t_{DFT1}$ ) slew rates at 200 MHz (HS-T) <sup>[41]</sup> | 1.13                   |                       |      |                       |
| Data rise ( $t_{DRT2}$ ) and fall ( $t_{DFT2}$ ) slew rates at 166 MHz (HL-T) <sup>[41]</sup> | 1.72                   |                       |      |                       |
| $V_{IL(ac)}$                                                                                  | $-0.30 \times V_{CCQ}$ | $0.30 \times V_{CCQ}$ | V    | Figure 70             |
| $V_{IH(ac)}$                                                                                  | $0.7 \times V_{CCQ}$   | $1.30 \times V_{CCQ}$ |      |                       |
| $V_{OH(ac)}$                                                                                  | $0.75 \times V_{CCQ}$  | -                     |      |                       |
| $V_{OL(ac)}$                                                                                  | -                      | $0.25 \times V_{CCQ}$ |      |                       |
| Input timing ref voltage                                                                      | $0.5 \times V_{CC}$    |                       |      | Figure 71 / Figure 72 |
| Output timing ref voltage                                                                     | $0.5 \times V_{CC}$    |                       |      |                       |

### Notes

41. Input slew rate measured from input pulse min to max at  $V_{CC}$  max.

42. AC characteristics tables assume clock and data signals have the same slew rate (slope).

## 8 Timing characteristics

**Table 89** Timing characteristics<sup>[45]</sup>

| Symbol            | Parameter                                                                                | Min                 | Typ | Max             | Unit | Reference figure         |
|-------------------|------------------------------------------------------------------------------------------|---------------------|-----|-----------------|------|--------------------------|
| Octal SDR/DDR     |                                                                                          |                     |     |                 |      |                          |
| f <sub>CK</sub>   | CK clock frequency for octal mode transactions using DS (HS-T)                           | 0                   | –   | 200             | MHz  | –                        |
|                   | CK clock frequency for octal mode transactions using DS (HL-T)                           | 0                   | –   | 166             |      |                          |
| p <sub>CK</sub>   | CK clock period                                                                          | 1/f <sub>CK</sub>   | –   | ∞               | ns   | Figure 70                |
| t <sub>CH</sub>   | Clock high time                                                                          | 45% p <sub>CK</sub> | –   | 55%             | ns   | Figure 73                |
| t <sub>CL</sub>   | Clock low time                                                                           |                     | –   | p <sub>CK</sub> | ns   |                          |
| t <sub>CS</sub>   | CS# high time (read transactions)                                                        | 10                  | –   | –               | ns   | Figure 76 /<br>Figure 77 |
|                   | CS# high time between transactions (interface CRC Read Register and aborted transaction) | 50                  | –   | –               |      |                          |
|                   | CS# high time (program / erase transactions)                                             | 50                  | –   | –               |      |                          |
| t <sub>CSS</sub>  | CS# active setup time (relative to CK)                                                   | 4                   | –   | –               | ns   |                          |
| t <sub>CSH0</sub> | CS# active hold time (relative to CK in Mode 0)                                          | 4                   | –   | –               | ns   |                          |
| t <sub>CSH3</sub> | CS# active hold time (relative to CK in Mode 3)                                          | 6.5                 | –   | –               | ns   |                          |
| t <sub>SU</sub>   | HS-T data setup time (all V <sub>CC</sub> )                                              | 0.5                 | –   | –               | ns   |                          |
|                   | HL-T data setup time (all V <sub>CC</sub> )                                              | 0.6                 | –   | –               |      |                          |
| t <sub>HD</sub>   | HL-T data hold time (all V <sub>CC</sub> )                                               | 0.6                 | –   | –               | ns   |                          |
|                   | HS-T data hold time (all V <sub>CC</sub> )                                               | 0.5                 | –   | –               |      |                          |

### Notes

43. Full  $V_{CC}$  range and  $CL = 15$  pF.
44. Output HI-Z is defined as the point where data is no longer driven.
45. Applicable across all operating temperature options.
46. If Reset# is asserted during the end of  $t_{PU}$ , the device will remain in the reset state and  $t_{RH}$  will determine when CS# may go Low.
47. Sum of  $t_{RP}$  and  $t_{RH}$  must be equal to or greater than  $t_{RPH}$ .
48. Typical program and erase times assume the following conditions: 25°C,  $V_{CC} = 1.8$  V and 3.0 V; checkerboard data pattern.
49. The programming time for any OTP programming transaction is the same as  $t_{pp}$ . This includes PRSSR\_4\_1.
50. The programming time for the PRPPB\_4\_0 transaction is the same as  $t_{pp}$ . The erase time for ERPPB\_0\_0 transaction is the same as  $t_{SE}$ .
51. Values are guaranteed by characterization and not 100% tested in production.
52. Guaranteed by design.
53. The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

**Table 89** Timing characteristics<sup>[45]</sup> (Continued)

| Symbol                | Parameter                                                                                                        | Min          | Typ | Max                 | Unit | Reference figure         |
|-----------------------|------------------------------------------------------------------------------------------------------------------|--------------|-----|---------------------|------|--------------------------|
| $t_V^{[43]}$          | Clock low to output valid (15 pF loading) (HS-T)                                                                 | 2            | –   | 5.45                | ns   | Figure 76 /<br>Figure 78 |
|                       | Clock low to output valid (15 pF loading) (HL-T)                                                                 |              |     | 7.25                |      |                          |
| $t_{CKDS}$            | DS valid (HS-T)                                                                                                  | –            | –   | 5.45                | ns   |                          |
|                       | DS valid (HL-T)                                                                                                  | –            | –   | 7.25                |      |                          |
| $t_{DSS}^{[51]}$      | DS transition to data valid                                                                                      | –0.4         | –   | 0.4                 | ns   |                          |
| $t_{DSH}^{[51]}$      | DS transition to data invalid                                                                                    | –0.4         | –   | 0.4                 | ns   |                          |
| $t_{HO}$              | Output hold time                                                                                                 | 0.4          | –   | –                   | ns   | Figure 76                |
| $t_{DIS}^{[44]}$      | CS# inactive to output disable time (HL-T/HS-T) (SDR)                                                            | –            | –   | 6.5 / 7.5           | ns   | Figure 76 /<br>Figure 78 |
|                       | CS# inactive to output disable time (HL-T/HS-T) (DDR)                                                            | –            | –   | 6.0 / 7.5           |      |                          |
| $t_{DSZ}$             | CS# inactive to DS disable time (HS-T) (SDR / DDR)                                                               | –            | –   | 6.50 / 6.0          | ns   |                          |
|                       | CS# inactive to DS disable time (HL-T)                                                                           | –            | –   | 7.50                |      |                          |
| $t_{IO\_SKEW}^{[51]}$ | Data skew (first data bit to last data bit)                                                                      | –            | –   | 0.5                 | ns   | –                        |
| $t_{PS}$              | Program/erase transaction CS# invalid to program suspend / erase suspend transaction CS# invalid (interface CRC) | –            | –   | 15                  | μs   | Figure 39                |
| $t_{CSDS}$            | CS# low to DS low                                                                                                | –            | –   | 10                  | ns   | Figure 27 /<br>Figure 28 |
| SPI SDR               |                                                                                                                  |              |     |                     |      |                          |
| $f_{CK}$              | CK clock frequency                                                                                               | 0            | –   | 166 <sup>[53]</sup> | MHz  | –                        |
| $p_{CK}$              | CK clock period                                                                                                  | 1/ $f_{CK}$  | –   | ∞                   | ns   | Figure 70                |
| $t_{CH}$              | Clock high time                                                                                                  | 45% $p_{CK}$ | –   | 55%                 | ns   | Figure 73                |
| $t_{CL}$              | Clock low time                                                                                                   |              | –   | $p_{CK}$            |      |                          |

**Notes**

- 43.Full  $V_{CC}$  range and  $CL = 15$  pF.
- 44.Output HI-Z is defined as the point where data is no longer driven.
- 45.Applicable across all operating temperature options.
- 46.If Reset# is asserted during the end of  $t_{PU}$ , the device will remain in the reset state and  $t_{RH}$  will determine when CS# may go Low.
- 47.Sum of  $t_{RP}$  and  $t_{RH}$  must be equal to or greater than  $t_{RPH}$ .
- 48.Typical program and erase times assume the following conditions: 25°C,  $V_{CC} = 1.8$  V and 3.0 V; checkerboard data pattern.
- 49.The programming time for any OTP programming transaction is the same as  $t_{pp}$ . This includes PRSSR\_4\_1.
- 50.The programming time for the PRPPB\_4\_0 transaction is the same as  $t_{pp}$ . The erase time for ERPPB\_0\_0 transaction is the same as  $t_{SE}$ .
- 51.Values are guaranteed by characterization and not 100% tested in production.
- 52.Guaranteed by design.
- 53.The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

**Table 89**      **Timing characteristics**<sup>[45]</sup> (Continued)

| Symbol     | Parameter                                                                        | Min   | Typ | Max | Unit | Reference figure         |
|------------|----------------------------------------------------------------------------------|-------|-----|-----|------|--------------------------|
| $t_{CS}$   | CS# high time (read transactions)                                                | 10    | –   | –   | ns   | Figure 74 /<br>Figure 75 |
|            | CS# high time between transactions (aborted commands)                            | 20    | –   | –   |      |                          |
|            | CS# high time (program / erase transactions)                                     | 50    | –   | –   |      |                          |
| $t_{CSS}$  | CS# active setup time relative to CK ( $f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz) | 5 / 4 | –   | –   | ns   | Figure 74                |
| $t_{CSH0}$ | CS# active hold time (relative to CK in Mode 0)                                  | 4     | –   | –   | ns   |                          |
| $t_{CSH3}$ | CS# active hold time (relative to CK in Mode 3)                                  | 6     | –   | –   | ns   |                          |
| $t_{SU}$   | Data setup time (all $V_{CC}$ ) ( $f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)      | 5 / 2 | –   | –   | ns   |                          |
| $t_{HD}$   | Data hold time (all $V_{CC}$ ) ( $f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)       | 5 / 2 | –   | –   | ns   |                          |

**Notes**

43. Full  $V_{CC}$  range and  $CL = 15$  pF.
44. Output HI-Z is defined as the point where data is no longer driven.
45. Applicable across all operating temperature options.
46. If Reset# is asserted during the end of  $t_{PU}$ , the device will remain in the reset state and  $t_{RH}$  will determine when CS# may go Low.
47. Sum of  $t_{RP}$  and  $t_{RH}$  must be equal to or greater than  $t_{RPH}$ .
48. Typical program and erase times assume the following conditions: 25°C,  $V_{CC} = 1.8$  V and 3.0 V; checkerboard data pattern.
49. The programming time for any OTP programming transaction is the same as  $t_{pp}$ . This includes PRSSR\_4\_1.
50. The programming time for the PRPPB\_4\_0 transaction is the same as  $t_{pp}$ . The erase time for ERPPB\_0\_0 transaction is the same as  $t_{SE}$ .
51. Values are guaranteed by characterization and not 100% tested in production.
52. Guaranteed by design.
53. The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

Timing characteristics

**Table 89** Timing characteristics<sup>[45]</sup> (Continued)

| Symbol    | Parameter                                                                                   | Min       | Typ    | Max                | Unit | Reference figure |
|-----------|---------------------------------------------------------------------------------------------|-----------|--------|--------------------|------|------------------|
| $t_V$     | Clock low to output valid (15 pF loading, 3.0 V–3.6 V, 30 $\Omega$ output Impedance) (HL-T) | 2         | –      | 6.5                | ns   | <b>Figure 75</b> |
|           | Clock low to output valid (30pF Loading) (HS-T) (512T / 01GT)                               | 2 / 2     | –      | 8 / 8              |      |                  |
|           | Clock low to output valid (30pF Loading) (HL-T)                                             | 2         | –      | 9                  |      |                  |
|           | Clock low to output valid (15pF Loading) (HS-T) (512T / 01GT)                               | 2 / 2     | –      | 6 / 6              |      |                  |
|           | Clock low to output valid (15pF Loading) (HL-T)                                             | 2         | –      | 8                  |      |                  |
| $t_{HO}$  | Output hold time                                                                            | 1.5 / 1.5 | –      | –                  | ns   |                  |
| $t_{DIS}$ | Output disable time (HL512T / HS512T) (HL01GT / HS01GT)                                     | –         | –<br>– | 7.5 / 6<br>7.4 / 6 | ns   |                  |

**Power up / power down timing**

|                 |                                                                            |         |   |                        |                 |                  |
|-----------------|----------------------------------------------------------------------------|---------|---|------------------------|-----------------|------------------|
| $t_{PU}$        | $V_{CC}(\text{min})$ to read operation (HL512T / HS512T) (HL01GT / HS01GT) | –       | – | 450 / 500<br>500 / 500 | $\mu\text{s}$   | <b>Figure 61</b> |
| $t_{PD}$        | $V_{CC}(\text{low})$ time                                                  | 25      | – | –                      |                 | <b>Figure 62</b> |
| $t_{VR}^{[52]}$ | $V_{CC} / V_{CCQ}$ power up ramp rate                                      | 1       | – | –                      | $\mu\text{s/V}$ | <b>Figure 63</b> |
| $t_{VF}$        | $V_{CC} / V_{CCQ}$ power down ramp rate (512T / 01GT)                      | 30 / 30 | – | –                      |                 |                  |

**Deep power down mode timing**

|                     |                        |   |   |   |               |   |
|---------------------|------------------------|---|---|---|---------------|---|
| $t_{ENTDPD}^{[52]}$ | Time to enter DPD mode | – | – | 3 | $\mu\text{s}$ | – |
|---------------------|------------------------|---|---|---|---------------|---|

**Notes**

- 43.Full  $V_{CC}$  range and  $CL = 15 \text{ pF}$ .
- 44.Output HI-Z is defined as the point where data is no longer driven.
- 45.Applicable across all operating temperature options.
- 46.If Reset# is asserted during the end of  $t_{PU}$ , the device will remain in the reset state and  $t_{RH}$  will determine when CS# may go Low.
- 47.Sum of  $t_{RP}$  and  $t_{RH}$  must be equal to or greater than  $t_{RPH}$ .
- 48.Typical program and erase times assume the following conditions: 25°C,  $V_{CC} = 1.8 \text{ V}$  and 3.0 V; checkerboard data pattern.
- 49.The programming time for any OTP programming transaction is the same as  $t_{pp}$ . This includes PRSSR\_4\_1.
- 50.The programming time for the PRPPB\_4\_0 transaction is the same as  $t_{pp}$ . The erase time for ERPPB\_0\_0 transaction is the same as  $t_{SE}$ .
- 51.Values are guaranteed by characterization and not 100% tested in production.
- 52.Guaranteed by design.
- 53.The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

Timing characteristics

**Table 89** Timing characteristics<sup>[45]</sup> (Continued)

| Symbol              | Parameter                                                       | Min  | Typ | Max                          | Unit | Reference figure |
|---------------------|-----------------------------------------------------------------|------|-----|------------------------------|------|------------------|
| $t_{\text{EXTDPD}}$ | Time to exit DPD mode<br>(HL512T / HS512T)<br>(HL01GT / HS01GT) | –    | –   | 380 /<br>430<br>430 /<br>430 | μs   | Figure 60        |
| $t_{\text{CSDPD}}$  | Chip select pulse width to exit DPD                             | 0.02 | –   | 3                            | μs   |                  |

**Reset timing**<sup>[46, 47]</sup>

|                 |                                                                                    |                        |   |         |    |           |
|-----------------|------------------------------------------------------------------------------------|------------------------|---|---------|----|-----------|
| $t_{\text{RS}}$ | Reset setup - RESET# high before CS# low                                           | 50                     | – | –       | ns | Figure 53 |
| $t_{\text{RH}}$ | Reset pulse hold - RESET# low to CS# low<br>(HL512T / HS512T)<br>(HL01GT / HS01GT) | 450 / 500<br>500 / 500 | – | –       | μs |           |
| $t_{\text{RP}}$ | RESET# pulse width                                                                 | 200                    | – | –       | ns |           |
| $t_{\text{SR}}$ | Internal device reset from software reset transaction (512T / 01GT)                | –                      | – | 83 / 83 | μs | –         |

**CS# signaling reset timing**

|                    |                                                                 |     |   |                              |    |           |
|--------------------|-----------------------------------------------------------------|-----|---|------------------------------|----|-----------|
| $t_{\text{CSLW}}$  | Chip select low                                                 | 500 | – | –                            | ns | Figure 58 |
| $t_{\text{CSHG}}$  | Chip select high                                                | 500 | – | –                            | ns |           |
| $t_{\text{RESET}}$ | Internal device reset<br>(HL512T / HS512T)<br>(HL01GT / HS01GT) | –   | – | 450 /<br>500<br>500 /<br>500 | μs |           |
| $t_{\text{SUJ}}$   | Data in setup time (w.r.t CS#)                                  | 50  | – | –                            | ns |           |
| $t_{\text{HDJ}}$   | Data in hold time (w.r.t CS#)                                   | 50  | – | –                            | ns |           |

**Notes**

43. Full  $V_{\text{CC}}$  range and  $CL = 15 \text{ pF}$ .
44. Output HI-Z is defined as the point where data is no longer driven.
45. Applicable across all operating temperature options.
46. If Reset# is asserted during the end of  $t_{\text{PU}}$ , the device will remain in the reset state and  $t_{\text{RH}}$  will determine when CS# may go Low.
47. Sum of  $t_{\text{RP}}$  and  $t_{\text{RH}}$  must be equal to or greater than  $t_{\text{RPH}}$ .
48. Typical program and erase times assume the following conditions: 25°C,  $V_{\text{CC}} = 1.8 \text{ V}$  and 3.0 V; checkerboard data pattern.
49. The programming time for any OTP programming transaction is the same as  $t_{\text{pp}}$ . This includes PRSSR\_4\_1.
50. The programming time for the PRPPB\_4\_0 transaction is the same as  $t_{\text{pp}}$ . The erase time for ERPPB\_0\_0 transaction is the same as  $t_{\text{SE}}$ .
51. Values are guaranteed by characterization and not 100% tested in production.
52. Guaranteed by design.
53. The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

**Table 89**      **Timing characteristics**<sup>[45]</sup> (Continued)

| Symbol                                                                                                      | Parameter                                                                                  | Min | Typ               | Max                | Unit    | Reference figure |
|-------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|-----|-------------------|--------------------|---------|------------------|
| <b>Embedded algorithm (erase, program and data integrity check) performance</b> <sup>[48, 49, 50, 53]</sup> |                                                                                            |     |                   |                    |         |                  |
| $t_W$                                                                                                       | Non-volatile register write time (512T / 01GT)                                             | –   | 44 / 44           | 357.5              | ms      | –                |
| $t_{PP}$                                                                                                    | 256B page programming 4KB Sector (512T / 01GT)                                             | –   | 430 / 480         | 2175               | $\mu$ s | –                |
|                                                                                                             | 256B page programming 256KB Sector                                                         | –   | 430               | 1700               |         |                  |
|                                                                                                             | 512B Page Programming 4KB Sector                                                           | –   | 680               | 2175               |         |                  |
|                                                                                                             | 512B Page Programming 256KB Sector)                                                        | –   | 570               | 1700               |         |                  |
| $t_{SE}$                                                                                                    | Sector Erase Time (4 KB physical sectors)                                                  | –   | 42                | 335                | ms      | –                |
|                                                                                                             | Sector Erase Time (256 KB Infineon Endurance Flex architecture disabled)                   | –   | 773               | 2677               |         |                  |
|                                                                                                             | Sector Erase Time (256 KB Infineon Endurance Flex architecture enabled)                    | –   | 773               | 5869               |         |                  |
| $t_{BE}$                                                                                                    | Chip Erase Time (512 Mb)                                                                   | –   | 201               | 696                | sec     | –                |
|                                                                                                             | Chip Erase Time (1 Gb)                                                                     | –   | 398               | 1381               | sec     | –                |
| $t_{EES}$                                                                                                   | Evaluate Erase Status Time for 4 KB physical sectors (HL512T / HS512T) (HL01GT / HS01GT)   | –   | 45/ 45<br>45 / 45 | 51 / 51<br>53 / 56 | $\mu$ s | –                |
|                                                                                                             | Evaluate Erase Status Time for 256 KB physical sectors (HL512T / HS512T) (HL01GT / HS01GT) | –   |                   |                    |         |                  |
| $t_{DIC\_SETUP}$                                                                                            | Data Integrity Check Calculation Setup Time (512T / 01GT)                                  | –   | 50 / 17           | –                  | MBps    | –                |

**Notes**

- 43.Full  $V_{CC}$  range and  $CL = 15$  pF.
- 44.Output HI-Z is defined as the point where data is no longer driven.
- 45.Applicable across all operating temperature options.
- 46.If Reset# is asserted during the end of  $t_{PU}$ , the device will remain in the reset state and  $t_{RH}$  will determine when CS# may go Low.
- 47.Sum of  $t_{RP}$  and  $t_{RH}$  must be equal to or greater than  $t_{RPH}$ .
- 48.Typical program and erase times assume the following conditions: 25°C,  $V_{CC} = 1.8$  V and 3.0 V; checkerboard data pattern.
- 49.The programming time for any OTP programming transaction is the same as  $t_{pp}$ . This includes PRSSR\_4\_1.
- 50.The programming time for the PRPPB\_4\_0 transaction is the same as  $t_{pp}$ . The erase time for ERPPB\_0\_0 transaction is the same as  $t_{SE}$ .
- 51.Values are guaranteed by characterization and not 100% tested in production.
- 52.Guaranteed by design.
- 53.The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

**Table 89**      **Timing characteristics<sup>[45]</sup>** (Continued)

| Symbol                                                               | Parameter                                                                                                            | Min     | Typ                | Max                | Unit    | Reference figure |
|----------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|---------|--------------------|--------------------|---------|------------------|
| $t_{DIC\_RATES}$                                                     | Data Integrity Check Calculation Rate<br>(Calculation rate over a large<br>(>1024-byte) block of data) (512T / 01GT) | 55 / 56 | 65 / 65            | –                  | MBps    | –                |
| $t_{SEC}$                                                            | Sector Erase Count Time<br>(HL512T / HS512T)<br>(HL01GT / HS01GT)                                                    | –       | 55 / 55<br>55 / 55 | 63 / 63<br>70 / 70 | $\mu s$ | –                |
| $t_{BEC1}$                                                           | Blank Check single 256 KB sector                                                                                     | –       | 15                 | 17                 | ms      | –                |
| $t_{BEC2}$                                                           | Blank Check single 4 KB sector                                                                                       | –       | 1                  | 2                  |         | –                |
| $t_{PASSWORD}$                                                       | Password Comparison Time                                                                                             | 80      | 100                | 120                | $\mu s$ | –                |
| <b>Program, Erase, or Data Integrity Check Suspend/Resume Timing</b> |                                                                                                                      |         |                    |                    |         |                  |
| $t_{PEDS}$                                                           | Program/Erase/Data Integrity Check<br>Suspend                                                                        | –       | –                  | 100                | $\mu s$ | –                |
| $t_{PEDRS}$                                                          | Program/Erase/Data Integrity Check<br>Resume to next Program/Erase/Data<br>Integrity Check Suspend                   | –       | 100                | –                  |         | –                |

**Notes**

- 43.Full  $V_{CC}$  range and  $CL = 15$  pF.
- 44.Output HI-Z is defined as the point where data is no longer driven.
- 45.Applicable across all operating temperature options.
- 46.If Reset# is asserted during the end of  $t_{PU}$ , the device will remain in the reset state and  $t_{RH}$  will determine when CS# may go Low.
- 47.Sum of  $t_{RP}$  and  $t_{RH}$  must be equal to or greater than  $t_{RPH}$ .
- 48.Typical program and erase times assume the following conditions: 25°C,  $V_{CC} = 1.8$  V and 3.0 V; checkerboard data pattern.
- 49.The programming time for any OTP programming transaction is the same as  $t_{pp}$ . This includes PRSSR\_4\_1.
- 50.The programming time for the PRPPB\_4\_0 transaction is the same as  $t_{pp}$ . The erase time for ERPPB\_0\_0 transaction is the same as  $t_{SE}$ .
- 51.Values are guaranteed by characterization and not 100% tested in production.
- 52.Guaranteed by design.
- 53.The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

## 8.1 Timing waveforms

### 8.1.1 Key to timing waveform

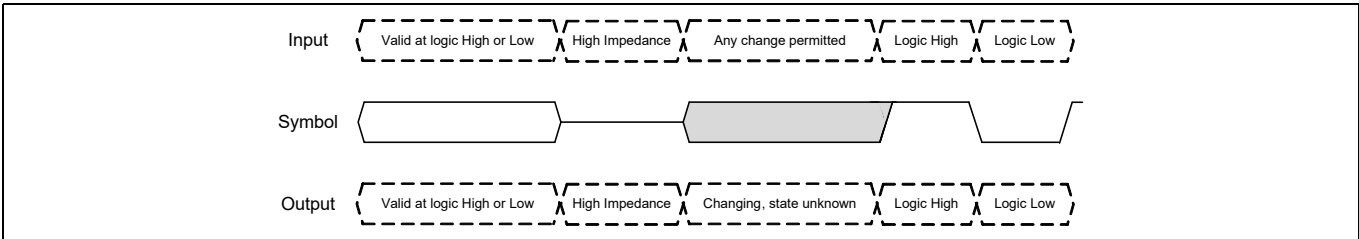


Figure 69 Waveform element meaning

### 8.1.2 Timing reference levels

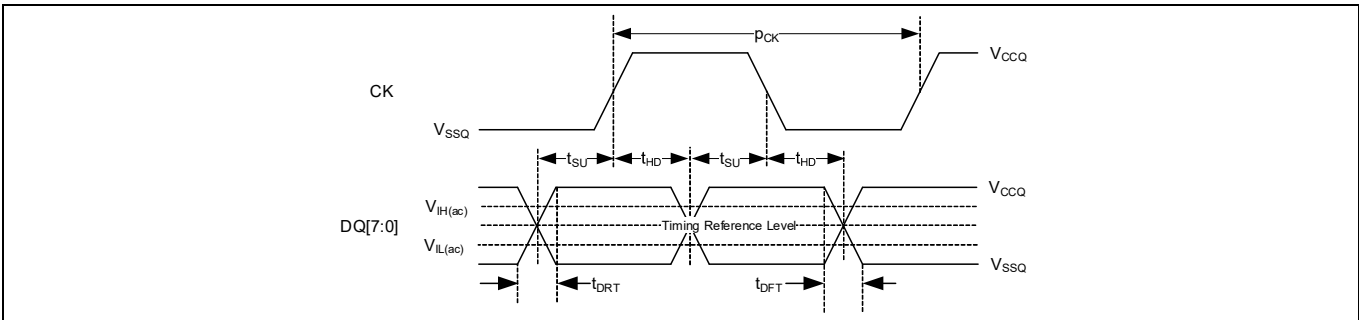


Figure 70 Input timing reference level

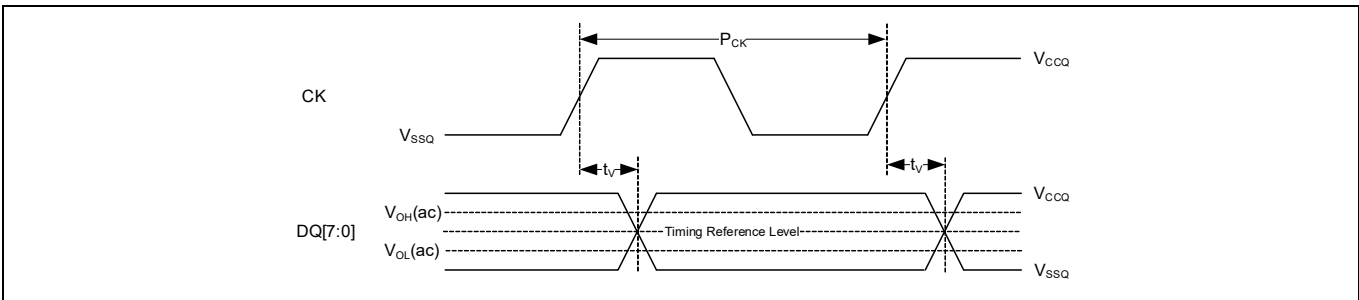


Figure 71 SDR output reference levels

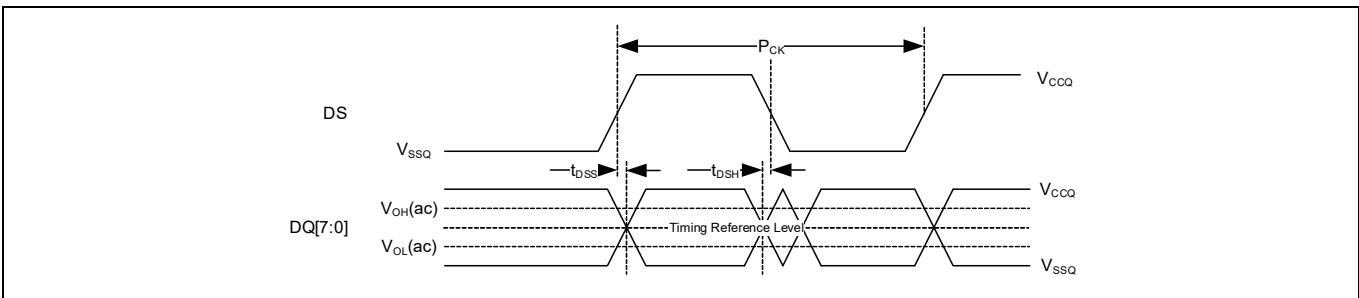


Figure 72 DDR output reference level

### 8.1.3 Clock timing

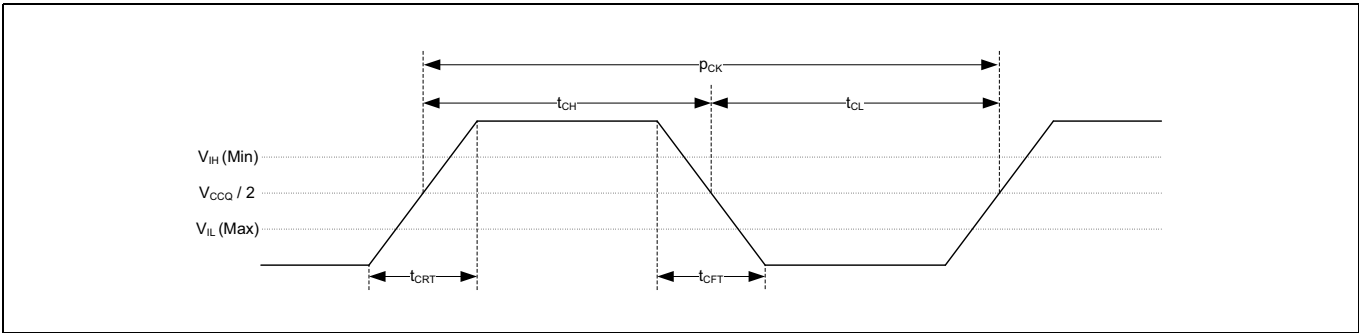


Figure 73 Clock timing

### 8.1.4 Input / output timing

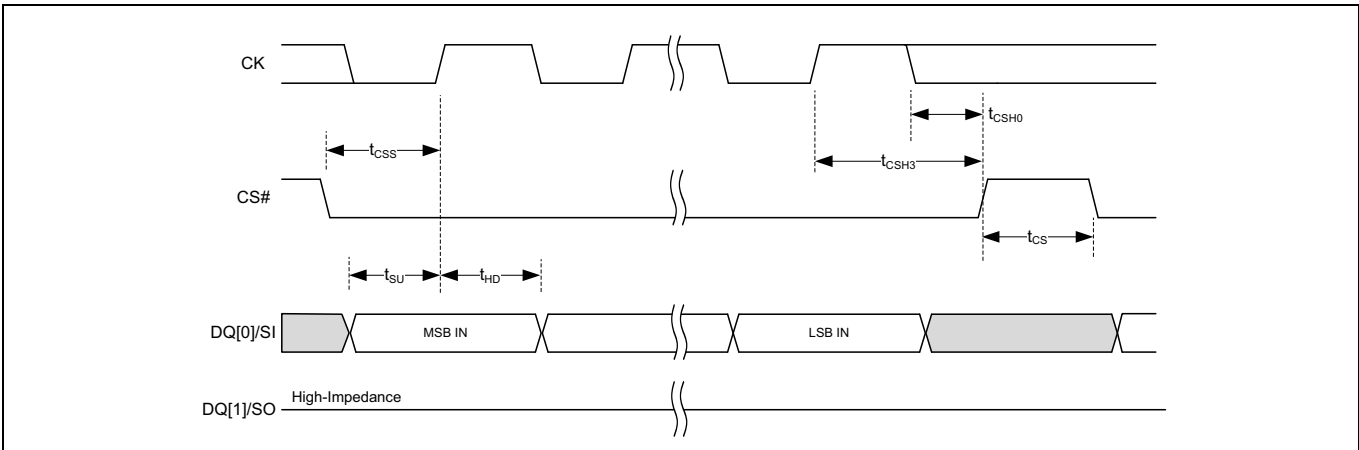


Figure 74 SPI input timing

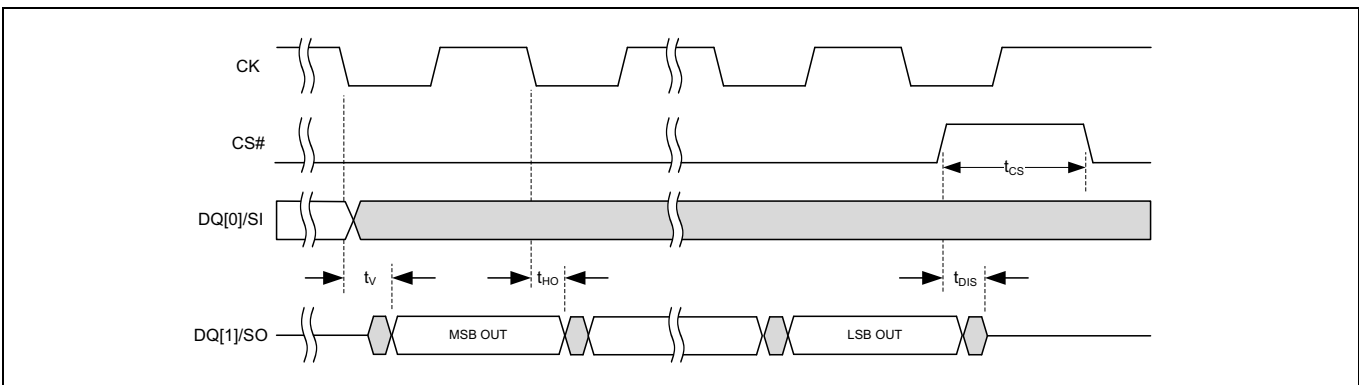


Figure 75 SPI output timing

Timing characteristics

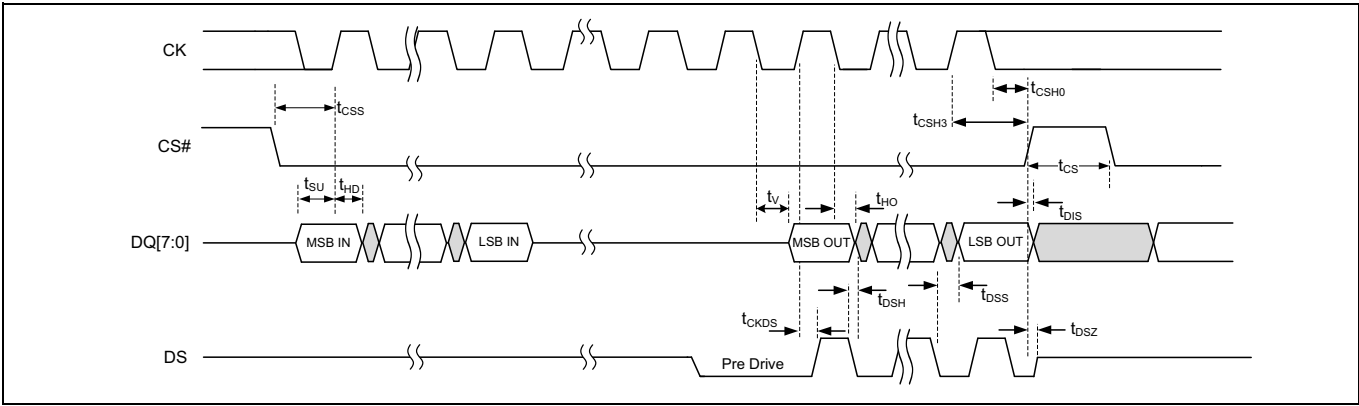


Figure 76 Octal SDR input and output timing

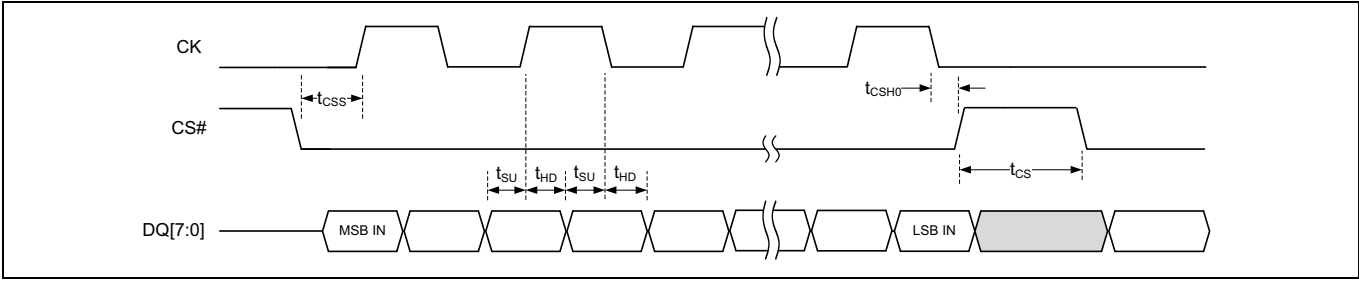


Figure 77 Octal DDR input timing

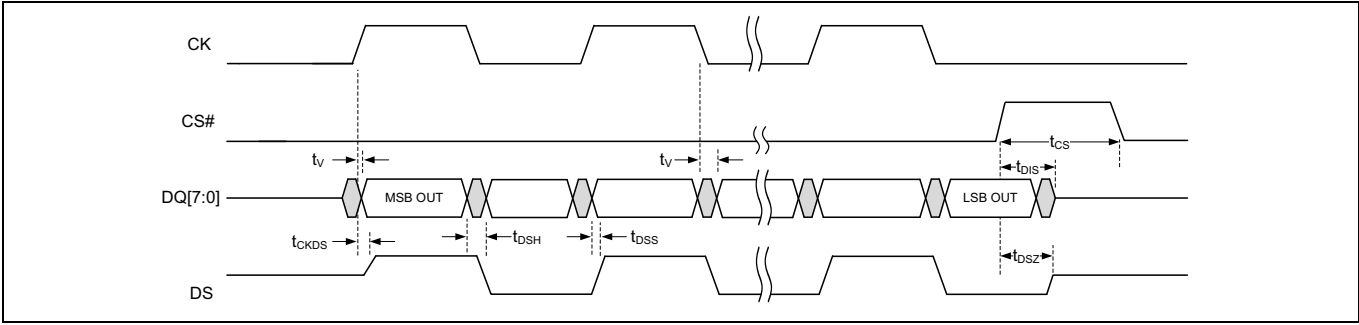


Figure 78 Octal DDR output timing

## 9 Device identification

### 9.1 JEDEC SFDP Rev D

#### 9.1.1 JEDEC SFDP Rev D header table

**Table 90** JEDEC SFDP Rev D header table

| SFDP byte address | SFDP DWORD name      | Data | Description                                                                                                                       |
|-------------------|----------------------|------|-----------------------------------------------------------------------------------------------------------------------------------|
| 00h               | SFDP Header          | 53h  | This is the entry point for Read SFDP (5Ah) command i.e., location zero within SFDP space ASCII "S"                               |
| 01h               |                      | 46h  | ASCII "F"                                                                                                                         |
| 02h               |                      | 44h  | ASCII "D"                                                                                                                         |
| 03h               |                      | 50h  | ASCII "P"                                                                                                                         |
| 04h               |                      | 08h  | SFDP Minor Revision (08h = JEDEC JESD216 Revision D)                                                                              |
| 05h               |                      | 01h  | SFDP Major Revision (01h = JEDEC JESD216 Revision D)                                                                              |
| 06h               |                      | 05h  | Number of Parameter Headers (zero based, 05h = 6 parameters)                                                                      |
| 07h               |                      | FEh  | xSPI NOR Profile 1 Octal, (8D, 8D, 8D) operation, 4-byte addressing for SFDP command, 8 WAIT states (Booting up in 1S-1S-1S mode) |
| 08h               | 1st Parameter Header | 00h  | Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)                                                                     |
| 09h               |                      | 00h  | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)                                                                   |
| 0Ah               |                      | 01h  | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)                                                                   |
| 0Bh               |                      | 14h  | Parameter Table Length (14h = 20 DWORDs are in the Parameter table)                                                               |
| 0Ch               |                      | 00h  | Parameter Table Pointer Byte 0 (DWORD = 4 byte aligned)<br>JEDEC Basic SPI Flash parameter byte offset = 0100h address            |
| 0Dh               |                      | 01h  | Parameter Table Pointer Byte 1                                                                                                    |
| 0Eh               |                      | 00h  | Parameter Table Pointer Byte 2                                                                                                    |
| 0Fh               |                      | FFh  | Parameter ID MSB (FFh = JEDEC defined Parameter)                                                                                  |
| 10h               | 2nd Parameter Header | 84h  | Parameter ID LSB (84h = 4-Byte Address Instruction Table)                                                                         |
| 11h               |                      | 00h  | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)                                                                   |
| 12h               |                      | 01h  | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)                                                                   |
| 13h               |                      | 02h  | Parameter Table Length (2h = 2 DWORDs are in the Parameter table)                                                                 |
| 14h               |                      | 50h  | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned)<br>4-Byte Address Instruction Table byte offset = 0150h address           |
| 15h               |                      | 01h  | Parameter Table Pointer Byte 1                                                                                                    |
| 16h               |                      | 00h  | Parameter Table Pointer Byte 2                                                                                                    |
| 17h               |                      | FFh  | Parameter ID MSB (FFh = JEDEC defined Parameter)                                                                                  |

**Table 90**      **JEDEC SFDP Rev D header table** (Continued)

| SFDP byte address | SFDP DWORD name      | Data | Description                                                                                                                     |
|-------------------|----------------------|------|---------------------------------------------------------------------------------------------------------------------------------|
| 18h               | 3rd Parameter Header | 05h  | Parameter ID LSB (05h = JEDEC xSPI Profile 1.0)                                                                                 |
| 19h               |                      | 00h  | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)                                                                 |
| 1Ah               |                      | 01h  | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)                                                                 |
| 1Bh               |                      | 05h  | Parameter Table Length (5h = 5 DWORDs are in the Parameter table)                                                               |
| 1Ch               |                      | 58h  | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) JEDEC xSPI Profile 1.0 = 0158h address                                  |
| 1Dh               |                      | 01h  | Parameter Table Pointer Byte 1                                                                                                  |
| 1Eh               |                      | 00h  | Parameter Table Pointer Byte 2                                                                                                  |
| 1Fh               |                      | FFh  | Parameter ID MSB (FFh = JEDEC defined Parameter)                                                                                |
| 20h               | 4th Parameter Header | 87h  | Parameter ID LSB (87h = JEDEC Status, Control and Configuration Register Map)                                                   |
| 21h               |                      | 00h  | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)                                                                 |
| 22h               |                      | 01h  | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)                                                                 |
| 23h               |                      | 1Ch  | Parameter Table Length (1Ch = 28 DWORDs are in the Parameter table)                                                             |
| 24h               |                      | 6Ch  | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) JEDEC Status, Control and Configuration Register Map = 016Ch address    |
| 25h               |                      | 01h  | Parameter Table Pointer Byte 1                                                                                                  |
| 26h               |                      | 00h  | Parameter Table Pointer Byte 2                                                                                                  |
| 27h               |                      | FFh  | Parameter ID MSB (FFh = JEDEC defined Parameter)                                                                                |
| 28h               | 5th Parameter Header | 0Ah  | Parameter ID LSB (0Ah = Command Sequences to change to Octal DDR (8D-8D-8D) mode)                                               |
| 29h               |                      | 00h  | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)                                                                 |
| 2Ah               |                      | 01h  | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)                                                                 |
| 2Bh               |                      | 04h  | Parameter Table Length (4h = 4 DWORDs are in the Parameter table)                                                               |
| 2Ch               |                      | DCh  | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) Command Sequences to Change to Octal DDR (8D-8D-8D) Mode = 1DCh address |
| 2Dh               |                      | 01h  | Parameter Table Pointer Byte 1                                                                                                  |
| 2Eh               |                      | 00h  | Parameter Table Pointer Byte 2                                                                                                  |
| 2Fh               |                      | FFh  | Parameter ID MSB (FFh = JEDEC defined Parameter)                                                                                |

**Table 90**      **JEDEC SFDP Rev D header table** (Continued)

| SFDP byte address | SFDP DWORD name      | Data | Description                                                                                |
|-------------------|----------------------|------|--------------------------------------------------------------------------------------------|
| 30h               | 6th Parameter Header | 81h  | Parameter ID LSB (81h = JEDEC Sector Map)                                                  |
| 31h               |                      | 00h  | Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)                            |
| 32h               |                      | 01h  | Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)                            |
| 33h               |                      | 16h  | Parameter Table Length (16h = 22 DWORDs are in the Parameter table)                        |
| 34h               |                      | ECh  | Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned)<br>JEDEC Sector Map = 1ECh address |
| 35h               |                      | 01h  | Parameter Table Pointer Byte 1                                                             |
| 36h               |                      | 00h  | Parameter Table Pointer Byte 2                                                             |
| 37h               |                      | FFh  | Parameter ID MSB (FFh = JEDEC defined Parameter)                                           |

**Table 91 JEDEC SFDP Rev D parameter table**

| SFDP byte address | SFDP DWORD name                     | Data                         | Description                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------|-------------------------------------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 100h              | JEDEC Basic Flash Parameter DWORD-1 | F7h                          | Bits 7:5 = unused = 111b<br>Bit 4 = 1b<br>Bit 3 = Block Protect Bits are non-volatile / volatile = 0b<br>Bit 2 = Program Buffer > 64 Bytes = 1b<br>Bits 1:0 = Uniform 4KB erase is unavailable = 11b                                                                                                                                                                          |
| 101h              |                                     | 21h                          | Bits 15:8 = 4KB erase instruction = 21h                                                                                                                                                                                                                                                                                                                                       |
| 102h              |                                     | 8Ah                          | Bit 23 = Unused = 1b<br>Bit 22 = (1-1-4) Fast Read NOT supported = 0b<br>Bit 21 = (1-4-4) Fast Read NOT supported = 0b<br>Bit 20 = (1-2-2) Fast Read NOT supported = 0b<br>Bit19 = Supports DDR, Yes = 1b<br>Bit 18:17 = 3- or 4-Byte addressing (for example, defaults to 3-Byte mode; enters 4-Byte mode on command) = 01b<br>Bit 16 = (1-1-2) Fast Read NOT supported = 0b |
| 103h              |                                     | FFh                          | Bits 31:24 = Unused = FFh                                                                                                                                                                                                                                                                                                                                                     |
| 104h              | JEDEC Basic Flash Parameter DWORD-2 | FFh                          | Density in bits, zero based, 512Mb = 1FFFFFFFh<br>Density in bits, zero based, 1Gb = 3FFFFFFFh                                                                                                                                                                                                                                                                                |
| 105h              |                                     | FFh                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 106h              |                                     | FFh                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 107h              |                                     | 1Fh for 512Mb<br>3Fh for 1Gb |                                                                                                                                                                                                                                                                                                                                                                               |
| 108h              | JEDEC Basic Flash Parameter DWORD-3 | 00h                          | Not Supported                                                                                                                                                                                                                                                                                                                                                                 |
| 109h              |                                     | 00h                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 10Ah              |                                     | 00h                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 10Bh              |                                     | 00h                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 10Ch              | JEDEC Basic Flash Parameter DWORD-4 | 00h                          | Not Supported                                                                                                                                                                                                                                                                                                                                                                 |
| 10Dh              |                                     | 00h                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 10Eh              |                                     | 00h                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 10Fh              |                                     | 00h                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 110h              | JEDEC Basic Flash Parameter DWORD-5 | EEh                          | Bits 7:5 = Reserved = 111b<br>Bit 4 = Not Supported = 0b<br>Bit 3:1 = Reserved = 111b<br>Bits 0 = Not Supported = 0b                                                                                                                                                                                                                                                          |
| 111h              |                                     | FFh                          | Reserved                                                                                                                                                                                                                                                                                                                                                                      |
| 112h              |                                     | FFh                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 113h              |                                     | FFh                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 114h              | JEDEC Basic Flash Parameter DWORD-6 | FFh                          | Reserved                                                                                                                                                                                                                                                                                                                                                                      |
| 115h              |                                     | FFh                          |                                                                                                                                                                                                                                                                                                                                                                               |
| 116h              |                                     | 00h                          | Not Supported                                                                                                                                                                                                                                                                                                                                                                 |
| 117h              |                                     | 00h                          |                                                                                                                                                                                                                                                                                                                                                                               |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                         | Data                         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------|-----------------------------------------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 118h              | JEDEC Basic Flash Parameter<br>DWORD-7  | FFh                          | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 119h              |                                         | FFh                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 11Ah              |                                         | 00h                          | Not Supported                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 11Bh              |                                         | 00h                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 11Ch              | JEDEC Basic Flash Parameter<br>DWORD-8  | 0Ch                          | Erase Type 1 Size, 4KB erase instruction = Erase type size = $2^N$ (where N = 12) = 0Ch                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 11Dh              |                                         | 21h                          | Erase Type 1 Instruction                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 11Eh              |                                         | 00h                          | Erase Type 2 Not Supported                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 11Fh              |                                         | FFh                          | Erase Type 2 Not Supported                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 120h              | JEDEC Basic Flash Parameter<br>DWORD-9  | 00h                          | Erase Type 3 Not Supported                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 121h              |                                         | FFh                          | Erase Type 3 Not Supported                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 122h              |                                         | 12h                          | Erase Type 4 Size, 256KB erase instruction = Erase type size = $2^N$ (where N = 18) = 12h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 123h              |                                         | DCh                          | Erase Type 4 Instruction                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 124h              | JEDEC Basic Flash Parameter<br>DWORD-10 | 23h                          | Bits 31:30 = Erase type 4 Erase, Typical time units<br>(00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 128 ms = 10b<br>Bits 29:25 = Erase type 4 Erase, Typical time count = 00101b<br>Bits 24:23 = Erase type 3 Erase, Typical time units<br>(00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU)<br>Bits 22:18 = Erase type 3 Erase, Typical time count = 11111b (RFU)<br>Bits 17:16 = Erase type 2 Erase, Typical time units<br>(00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU)<br>Bits 15:11 = Erase type 2 Erase, Typical time count = 11111b (RFU)<br>Bits 10:9 = Erase type 1 Erase, Typical time units<br>(00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16ms = 01b<br>Bits 8:4 = Erase type 1 Erase, Typical time count = 00010b<br>(typ erase time = count + 1 * units = 3 * 16 ms = 48 ms)<br>Bits 3:0 = Count = (Max Erase time / (2 * Typical Erase time)) - 1 = 0011b |
| 125h              |                                         | FAh                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 126h              |                                         | FFh                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 127h              |                                         | 8Bh                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 128h              |                                         | 82h                          | Bits 31 = Reserved = 1b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 129h              |                                         | E7                           | Bits 30:29 = Chip Erase Typical time units<br>(00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 11b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 12Ah              |                                         | FFh                          | Bits 28:24 = Chip Erase Typical time count = 00011b (512M), and 00110b (1G)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 12Bh              | JEDEC Basic Flash Parameter<br>DWORD-11 | E3h for 512Mb<br>E6h for 1Gb | Bits 23:19 = Byte Program Typical Time, additional byte = 11111b<br>Bits 18:14 = Byte Program Typical Time, first byte = 11111b<br>Bits 13 = Page Program Typical Time unit (0: 8 $\mu$ s, 1: 64 $\mu$ s) = 64 $\mu$ s = 1b<br>Bits 12:8 = Page Program Typical Time Count = 00111<br>Bits 7:4 = Page Size (256B) = $2^N$ bytes = 1000h<br>Bits 3:0 = Count = [Max page program time / (2 * Typical page program time)] - 1 = 0010b                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                         | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------------------|-----------------------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12Ch              | JEDEC Basic Flash Parameter<br>DWORD-12 | ECh  | Bit 31 = Suspend and Resume supported = 0b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 12Dh              |                                         | 23h  | Bits 30:29 = Suspend in-progress erase max latency units (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 8 µs = 10b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 12Eh              |                                         | 19h  | Bits 28:24 = Suspend in-progress erase max latency count = 01001b = 10 * 8 µs = 80 µs                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 12Fh              |                                         | 49h  | Bits 23:20 = Erase resume to suspend interval count = 0001b<br>Bits 19:18 = Suspend in-progress program max latency units (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 8 µs = 10b<br>Bits 17:13 = Suspend in-progress program max latency count = 01001b = 10 * 8 µs = 80 µs<br>Bits 12:9 = Program resume to suspend interval count = 0001b<br>Bit 8 = Reserved = 1b<br>Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted)<br>+ xx1xb: May not initiate a page program in the erase suspended sector size<br>+ x1xxb: May not initiate a read in the erase suspended sector size<br>+ 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1110b<br>Bits 3:0 = Prohibited Operations During Program Suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted)<br>+ xx0xb: May not initiate a new page program anywhere (program nesting not permitted)<br>+ x1xxb: May not initiate a read in the program suspended page size<br>+ 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1100b |
| 130h              | JEDEC Basic Flash Parameter<br>DWORD-13 | 7Ah  | Bits 7:0 = Program Resume Instruction = 7Ah (1S-1S-1S)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 131h              |                                         | B0h  | Bits 15:8 = Program Suspend Instruction = B0h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 132h              |                                         | 7Ah  | Bits 23:16 = Erase Resume Instruction = 7Ah (1S-1S-1S)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 133h              |                                         | B0h  | Bits 31:24 = Erase Suspend Instruction = B0h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 134h              | JEDEC Basic Flash Parameter<br>DWORD-14 | F7h  | Bits 7:4 = RFU = Fh<br>Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0 = ready; 1 = busy).<br>Bits 1:0 = RFU = 11b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 135h              |                                         | 66h  | Bit 31 = DPD Supported = supported = 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 136h              |                                         | 80h  | Bits 30:23 = Enter DPD Instruction = B9h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 137h              |                                         | 5Ch  | Bits 22:15 = Exit DPD Instruction not supported = 00h<br>Bits 14:13 = Exit DPD to next operation delay units = (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 64 µs = 11b<br>Bits 12:8 = Exit DPD to next operation delay count = 00110, Exit DPD to next operation delay = (count + 1) * units = (6 + 1) * 64 µs = 448 µs                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                         | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------------|-----------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 138h              | JEDEC Basic Flash Parameter<br>DWORD-15 | 00h  | Bits 31:24 = Reserved = FFh<br>Bit 23 = Hold or RESET Disable = Not Supported = 0b<br>Bits 22:0 = Not supported = 000000h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 139h              |                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 13Ah              |                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 13Bh              |                                         | FFh  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 13Ch              | JEDEC Basic Flash Parameter<br>DWORD-16 | F9h  | Bit 7 = Reserved = 1<br>Bits 6:0 = Volatile or Non-volatile Register and Write Enable Instruction for Status Register 1<br>xxx_1b: Non-volatile Status Register 1, powers-up to last written value, use instruction 06h to enable write.<br>+ xxx_1xxx: Non-volatile/Volatile Status Register 1 powers-up to last written value in the non-volatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register.<br>+ xx1_1xxx: Status Register 1 contains a mix of volatile and non-volatile bits. The 06h instruction is used to enable writing of the register.<br>+ x1x_1xxx: Reserved<br>+ 1xx_1xxx: Reserved<br>= 1111001b |
| 13Dh              | JEDEC Basic Flash Parameter<br>DWORD-16 | 10h  | Bits 23:14 = Exit 4-Byte Addressing<br>= xx_xx1x_1xxx: Hardware reset<br>+ xx_x1xx_1xxx: Software reset (see bits 13:8 in this DWORD)<br>+ xx_1xxx_1xxx: Power cycle<br>+ x1_1xxx_1xxx: Reserved<br>+ 1x_1xxx_1xxx: Reserved<br>= 11_1110_0000b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 13Eh              | JEDEC Basic Flash Parameter<br>DWORD-16 | F8h  | Bits 13:8 = Soft Reset and Rescue Sequence Support<br>+ x1_1xxx: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode.<br>= 010000b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 13Fh              | JEDEC Basic Flash Parameter<br>DWORD-16 | A1h  | Bits 31:24 = Enter 4-byte Addressing<br>+ xxxx_1b: Issue instruction B7h (Preceding write enable not required)<br>+ xx1x_1xxx: Supports dedicated 4-Byte address instruction set. Refer the vendor datasheet for the instruction set definition<br>+ 1xxx_1xxx: Reserved = 1010_0001b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 140h              | JEDEC Basic Flash Parameter<br>DWORD-17 | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 141h              |                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 142h              |                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 143h              |                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                      | Data                         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------------|--------------------------------------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 144h              | JEDEC Basic Flash Parameter DWORD-18 | 00h                          | Bit 31 = High byte and low byte of 16-bit words are in the same order when read in 1-1-1 mode and 8-8-8 mode = 0b<br>Bit 30:29 = The Command Extension is the same as the Command = 00b<br>Bit 28 = Reserved = 0b<br>Bit 27:26 = Not supported = 00b<br>Bits 25:24 = First rising edge of DS in the middle of the first data bit, start of first data bit aligned with the first falling edge of DS = 10b<br>Bit 23 = JEDEC SPI Protocol Reset Supported = 1b<br>Bit 22:18 = 01111b<br>Bits 17:0 = Reserved = 00000h |
| 145h              |                                      | 00h                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 146h              |                                      | BC h                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 147h              |                                      | 02h                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 148h              | JEDEC Basic Flash Parameter DWORD-19 | 00h                          | Not Supported                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 149h              |                                      | 00h                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 14Ah              |                                      | 00h                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 14Bh              |                                      | 00h                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 14Ch              | JEDEC Basic Flash Parameter DWORD-20 | FFh                          | Bits 31:28 = Maximum operation speed of device in 8D-8D-8D mode when utilizing Data Strobe = 1000b (200 MHz) / 0111b (166 MHz)<br>Bits 27:24 = 8D-8D-8D mode without using Data Strobe is not characterized = 1110b<br>Bits 23:20 = Maximum operation speed of device in 8S-8S-8S mode when utilizing Data Strobe = 1000b (200 MHz) / 0111b (166 MHz)<br>Bits 19:16 = 8S-8S-8S mode without using Data Strobe is not characterized = 1110b<br>Bit 15:0 = Not supported = FFFFh                                       |
| 14Dh              |                                      | FFh                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 14Eh              |                                      | 8Eh for HS-T<br>7Eh for HL-T |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 14Fh              |                                      | 8Eh for HS-T<br>7Eh for HL-T |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                                     | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------|-----------------------------------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 150h              | JEDEC 4-Byte Address Instructions Parameter DWORD-1 | 41h  | Supported = 1, Not Supported = 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 151h              |                                                     | 12h  | Bits 31:25 = Reserved = 1111_111b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 152h              |                                                     | 0F   | Bit 24 = Support for (1-8-8) Page Program Command, Instruction = 8Eh = 0b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 153h              |                                                     | FE   | Bit 23 = Support for (1-1-8) Page Program Command, Instruction = 84h = 0b<br>Bit 22 = Support for (1-8-8) DTR READ Command, Instruction = FDh = 0b<br>Bit 21 = Support for (1-8-8) FAST_READ Command, Instruction = CCh = 0b<br>Insert<br>Bit 20 = Support for (1-1-8) FAST_READ Command, Instruction = 7Ch = 0b<br>Bit 19 = Support for non-volatile individual sector lock write command, Instruction = E3h = 1b<br>Bit 18 = Support for non-volatile individual sector lock read command, Instruction = E2h = 1b<br>Bit 17 = Support for volatile individual sector lock Write command, Instruction = E1h = 1b<br>Bit 16 = Support for volatile individual sector lock Read command, Instruction = E0h = 1b<br>Bit 15 = Support for (1-4-4) DTR_Read Command, Instruction = EEh = 0b<br>Bit 14 = Support for (1-2-2) DTR_Read Command, Instruction = BEh = 0b<br>Bit 13 = Support for (1-1-1) DTR_Read Command, Instruction = 0Eh = 0b<br>Bit 12 = Support for Erase Command – Type 4 = 1b<br>Bit 11 = Support for Erase Command – Type 3 = 0b<br>Bit 10 = Support for Erase Command – Type 2 = 0b<br>Bit 9 = Support for Erase Command – Type 1 = 1b<br>Bit 8 = Support for (1-4-4) Page Program Command, Instruction = 3Eh = 0b<br>Bit 7 = Support for (1-1-4) Page Program Command, Instruction = 34h = 0b<br>Bit 6 = Support for (1-1-1) Page Program Command, Instruction = 12h = 1b<br>Bit 5 = Support for (1-4-4) FAST_READ Command, Instruction = ECh = 0b<br>Bit 4 = Support for (1-1-4) FAST_READ Command, Instruction = 6Ch = 0b<br>Bit 3 = Support for (1-2-2) FAST_READ Command, Instruction = BCh = 0b<br>Bit 2 = Support for (1-1-2) FAST_READ Command, Instruction = 3Ch = 0b<br>Bit 1 = Support for (1-1-1) FAST_READ Command, Instruction = 0Ch = 0b<br>Bit 0 = Support for (1-1-1) READ Command, Instruction = 13h = 1b |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                                     | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------------------|-----------------------------------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 154h              | JEDEC 4-Byte Address Instructions Parameter DWORD-2 | 21h  | Bits 31:24 = DCh = Instruction for Erase Type 4<br>Bits 23:16 = Instruction for Erase Type 3: RFU<br>Bits 15:8 = Instruction for Erase Type 2: RFU<br>Bits 7:0 = 21h = Instruction for Erase Type 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 155h              |                                                     | FFh  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 156h              |                                                     | FFh  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 157h              |                                                     | DCh  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 158h              | JEDEC xSPI Profile 1.0 DWORD-1                      | 00h  | Bits 7:0 = Read Fast Wrapped command not supported = 00h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 159h              |                                                     | EEh  | Bits 15:8 = Read Fast command = EEh (DDR Read)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 15Ah              |                                                     | 80h  | Bit 23 = Number of Additional Modifier Bytes Used for Write any Register command = 4 bytes = 1b<br>Bit 22 = Number of Data Bytes Used for Write Register command = 1 byte = 0b<br>Bits 21:16 = Reserved = 000000b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 15Bh              |                                                     | 0Bh  | Bit 31 = xSPI Support, Device implements the SFDP command in 8D-8D-8D protocol mode as defined in the Jedec xSPI spec = 0b<br>Bit 30 = SFDP Command in 8D-8D-8D mode – Dummy Cycles = 8 bytes = 0b<br>Bit 29 = Number of Additional Modifier Bytes Used for Read Status Register command = 0 bytes = 0b<br>Bit 28 = Initial Latency (CK cycles) for Read Status Register command = 3 CK Cycle = 0b<br>Bit 27 = Number of Additional Modifier Bytes Used for Read Register command = 4 bytes = 1b<br>Bit 26 = Initial Latency (CK cycles) for Read Volatile Register command = 4CK = 0b<br>Bit 25 = Initial Latency (CK cycles) for Read Volatile Non-Register command = 8 CK cycles = 1b<br>Bit 24 = Number of Additional Modifier Bytes Used for Write Status-Cfg Register command = 4 bytes = 1b |
| 15Ch              |                                                     | 71h  | Write Non-volatile Register command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15Dh              | JEDEC xSPI Profile 1.0 DWORD-2                      | 71h  | Write Volatile Register command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 15Eh              |                                                     | 65h  | Read NV Register command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 15Fh              |                                                     | 65h  | Read Volatile Register command                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                                        | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------------|--------------------------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 160h              | JEDEC xSPI Profile 1.0 DWORD-3                         | 00h  | Bits 7:0 = Reserved = 00h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 161h              |                                                        | B0h  | Bit 31 = Read SFDP 8D-8D-8D command supported = 1b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 162h              |                                                        | FFh  | Bit 30 = Read Fast Wrapped command not supported = 0b<br>Bit 29 = Setup Read Wrap command not supported = 0b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 163h              |                                                        | 96h  | Bit 28 = Erase 4KB command supported = 1b<br>Bit 27 = Erase 32KB command not supported = 0b<br>Bit 26 = Erase Chip command supported = 1b<br>Bit 25 = Read Configuration Register command supported = 1b<br>Bit 24 = Read Flag Status Register command not supported = 0b<br>Bit 23 = Read Register command supported = 1b<br>Bit 22 = Read Volatile Register command supported = 1b<br>Bit 21 = Read NV Register command supported = 1b<br>Bit 20 = Write Status-Configuration Register command supported = 1b<br>Bit 19 = Clear Flag Status Reg command supported = 1b<br>Bit 18 = Write Register command supported = 1b<br>Bit 17 = Write volatile register command supported = 1b<br>Bit 16 = Write NV register command supported = 1b<br>Bit 15 = Enter Deep Power Down command not supported = 1b<br>Bit 14 = Exit Deep Power Down command not supported = 0b<br>Bit 13 = Soft Reset command supported = 1b<br>Bit 12 = Reset Enable command supported = 1b<br>Bit 11 = Soft Reset and Enter default protocol mode command supported = 0b<br>Bit 10 = Enter default protocol mode command not supported = 0b<br>Bits 9:8 = Reserved = 00b |
| 164h              | JEDEC xSPI Profile 1.0 DWORD-4                         | A8h  | Bits 31:12 = 00000h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 165h              |                                                        | 0Bh  | Bits 11:7 = 200MHz operation: number of dummy cycles required = 23 = 10111b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 166h              |                                                        | 00h  | Bit 6:2 = 200MHz operation: configuration bit pattern to set this number of dummy cycles = 01010b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 167h              |                                                        | 00h  | Bits 1:0 = Reserved = 00b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 168h              | JEDEC xSPI Profile 1.0 DWORD-5                         | 0Ch  | Bits 31:27 = 166 MHz operation: number of dummy cycles required = 20 = 10100b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 169h              |                                                        | 55h  | Bit 26:22 = 166 MHz operation: configuration bit pattern to set this number of dummy cycles = 01000b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 16Ah              |                                                        | 1Ch  | Bits 21:17 = 133 MHz operation: number of dummy cycles required = 14 = 01110b<br>Bit 16:12 = 133 MHz operation: configuration bit pattern to set this number of dummy cycles = 00101b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 16Bh              |                                                        | A2h  | Bits 11:7 = 100 MHz operation: number of dummy cycles required = 10 = 01010b<br>Bit 6:2 = 100 MHz operation: configuration bit pattern to set this number of dummy cycles = 00011b<br>Bits 1:0 = Reserved = 00b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 16Ch              | Status, Control and Configuration Register Map DWORD-1 | 00h  | Bits 31:0 = Address offset for volatile registers = 00800000h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 16Dh              |                                                        | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 16Eh              |                                                        | 80h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 16Fh              |                                                        | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                                           | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------------------|-----------------------------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 170h              | Status, Control and Configuration Register Map<br>DWORD-2 | 00h  | Bits 31:0 = Address offset for non-volatile registers = 00000000h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 171h              |                                                           | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 172h              |                                                           | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 173h              |                                                           | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 174h              | Status, Control and Configuration Register Map<br>DWORD-3 | C0h  | Bit 31 = Generic Addressable Read Status/Control register command for volatile registers supported for some (or all) registers = 1b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 175h              |                                                           | CCh  | Bit 30 = Generic Addressable Write Status/Control register command for volatile registers supported for some (or all) registers = 1b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 176h              |                                                           | FFh  | Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for volatile registers = 3 byte (default) = 10b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 177h              |                                                           | EBh  | Bit 27:26 = Number of dummy bytes used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 10b<br>Bit 25:14 = Not supported = FFFh<br>Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (8S-8S-8S) mode = 3 = 0011b<br>Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (8D-8D-8D) mode = 3 = 0011b<br>Bit 5:4 = Reserved = 00b<br>Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for volatile registers in (1S-1S-1S) mode = 0000b |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                                           | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------------|-----------------------------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 178h              | Status, Control and Configuration Register Map<br>DWORD-4 | 88h  | Bit 31 = Generic Addressable Read Status/Control register command for non-volatile registers supported for some (or all) registers = 1b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 179h              |                                                           | FBh  | Bit 30 = Generic Addressable Write Status/Control register command for non-volatile registers supported for some (or all) registers = 1b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 17Ah              |                                                           | FFh  | Bits 29:28 = Number of address bytes used for Generic Addressable Read/Write Status/Control register commands for non-volatile registers = 3 byte (default) = 10b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 17Bh              |                                                           | EBh  | Bit 27:26 = Number of dummy bytes used for Generic Addressable Read Status/Control register command for non-volatile registers in (1S-1S-1S) mode = 10b<br>Bit 25:14 = Not supported = FFFh<br>Bit 13:10 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (8S-8S-8S) mode = 20 = 1110b (Max available option is 14 cycles)<br>Bit 9:6 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (8D-8D-8D) mode = 20 = 1110b (Max available option is 14 cycles)<br>Bit 5:4 = Reserved = 00b<br>Bit 3:0 = Number of dummy cycles used for Generic Addressable Read Status/Control register command for non-volatile registers in (1S-1S-1S) mode = 1000b |
| 17Ch              | Status, Control and Configuration Register Map<br>DWORD-5 | 00h  | Bits 7:0 = Command used for write access = read only = 00h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 17Dh              |                                                           | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 17Eh              |                                                           | 00h  | Bits 23:16 = Address of register where WIP is located = 00h (status reg -1 volatile)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 17Fh              |                                                           | 90h  | Bit 31 = Write In Progress (WIP) bit is supported = 1b<br>Bit 30 = Write In Progress polarity, WIP = 1 indicates write is in progress = 0b<br>Bits 29 = Reserved = 0b<br>Bits 28 = Bit is set /cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of WIP bit in register = bit [0] = 000b                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 180h              | Status, Control and Configuration Register Map<br>DWORD-6 | 06h  | Bits 7:0 = Command used for write access                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 181h              |                                                           | 05h  | Bits 15:8 = Command used for read access                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 182h              |                                                           | 00h  | Bits 23:16 = Address of register where WEL is located = 00h (status reg -1 volatile)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 183h              |                                                           | A1h  | Bit 31 = Write Enable (WEL) bit is supported = 1b<br>Bit 30 = Write Enable polarity, WEL = 1 means write is in progress = 0b<br>Bits 29 = Write command is a direct command to wet WEL bit = 1b<br>Bits 28 = Bit is accessed by direct commands to set WEL bit = 1b<br>Bit 27 = Local address for WEL bit is found in last byte of the address = 0b<br>Bits 26:24 = Bit location of WEL bit in register = bit [1] = 001b                                                                                                                                                                                                                                                                                                                                                                        |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                                        | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------------------|--------------------------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 184h              |                                                        | 00h  | Bits 7:0 = Command used for write access = read only = 00h = Read Only                                                                                                                                                                                                                                                                                                                                                                                |
| 185h              |                                                        | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                                                        |
| 186h              |                                                        | 00h  | Bits 23:16 = Address of register where Program Error is located = 00h (status reg -1 volatile)                                                                                                                                                                                                                                                                                                                                                        |
| 187h              | Status, Control and Configuration Register Map DWORD-7 | 96h  | Bit 31 = Program Error bit supported = 1b<br>Bit 30 = Positive polarity (Program Error = 0 indicates no error, Program Error = 1 indicates last Program operation created an error) = 0b<br>Bit 29 = The device has separate bits for Program Error and Erase Error = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of Program Error bit in register = bit [6] = 110b |
| 188h              |                                                        | 00h  | Bits 7:0 = Command used for write access = read only = 00h = Read Only                                                                                                                                                                                                                                                                                                                                                                                |
| 189h              |                                                        | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                                                        |
| 18Ah              |                                                        | 00h  | Bits 23:16 = Address of register where Erase Error is located = 00h                                                                                                                                                                                                                                                                                                                                                                                   |
| 18Bh              | Status, Control and Configuration Register Map DWORD-8 | 95h  | Bit 31 = Erase Error bit supported = 1b<br>Bit 30 = Positive polarity Erase Error = 0 indicates no error, Erase Error = 1 indicates last erase operation created an error) = 0b<br>Bit 29 = The device has separate bits for Program Error and Erase Error = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of erase Error bit in register = bit [5] = 101b            |
| 18Ch              |                                                        | 71h  | Bits 7:0 = Command used for write access = read only = 71h                                                                                                                                                                                                                                                                                                                                                                                            |
| 18Dh              |                                                        | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                                                        |
| 18Eh              |                                                        | 03h  | Address of register where wait states bits are located = 03h (Configuration Reg - 2 Non-volatile)                                                                                                                                                                                                                                                                                                                                                     |
| 18Fh              |                                                        | D0h  | Bit 31 = Variable number of dummy cycles supported = 1b<br>Bits 30:29 = Number of physical bits used to set wait states - 4 bit = 10b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of LSB of physical bits in register = bit [0] = 000b                                                                                                                                 |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                                            | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------------------|------------------------------------------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 190h              | Status, Control and Configuration Register Map<br>DWORD-10 | 71h  | Bits 7:0 = Command used for write access = 71h                                                                                                                                                                                                                                                                                                                                                                         |
| 191h              |                                                            | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                         |
| 192h              |                                                            | 03h  | Address of register where wait states bits are located = 03h<br>(Configuration Reg - 2 non-volatile)                                                                                                                                                                                                                                                                                                                   |
| 193h              |                                                            | D0h  | Bit 31 = Variable number of dummy cycles supported = 1b<br>Bits 30:29 = Number of physical bits used to set wait states - 4 bit = 10b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of LSB of physical bits in register = bit [0] = 000b                                                                                                  |
| 194h              | Status, Control and Configuration Register Map<br>DWORD-11 | A4h  | Bit 31 = 30 dummy cycles supported = 0b                                                                                                                                                                                                                                                                                                                                                                                |
| 195h              |                                                            | 6Bh  | Bit 30:26 = Bit pattern used to set 30 dummy cycles = 00000b                                                                                                                                                                                                                                                                                                                                                           |
| 196h              |                                                            | FBh  | Bit 25 = 28 dummy cycles supported = 1b                                                                                                                                                                                                                                                                                                                                                                                |
| 197h              |                                                            | 02h  | Bit 24:20 = Bit pattern used to set 28 dummy cycles = 01111b<br>Bit 19 = 26 dummy cycles supported = 1b<br>Bit 18:14 = Bit pattern used to set 26 dummy cycles = 01101b<br>Bit 13 = 24 dummy cycles supported = 1b<br>Bit 12:8 = Bit pattern used to set 24 dummy cycles = 01011b<br>Bit 7 = 22 dummy cycles supported = 1b<br>Bit 6:2 = Bit pattern used to set 22 dummy cycles = 01001b<br>Bits 1:0 = Reserved = 00b |
| 198h              | Status, Control and Configuration Register Map<br>DWORD-12 | 90h  | Bit 31 = 20 dummy cycles supported = 1b                                                                                                                                                                                                                                                                                                                                                                                |
| 199h              |                                                            | A5h  | Bit 30:26 = Bit pattern used to set 20 dummy cycles = 01000b                                                                                                                                                                                                                                                                                                                                                           |
| 19Ah              |                                                            | 79h  | Bit 25 = 18 dummy cycles supported = 1b                                                                                                                                                                                                                                                                                                                                                                                |
| 19Bh              |                                                            | A2h  | Bit 24:20 = Bit pattern used to set 18 dummy cycles = 00111b<br>Bit 19 = 16 dummy cycles supported = 1b<br>Bit 18:14 = Bit pattern used to set 16 dummy cycles = 00110b<br>Bit 13 = 14 dummy cycles supported = 1b<br>Bit 12:8 = Bit pattern used to set 14 dummy cycles = 00101b<br>Bit 7 = 12 dummy cycles supported = 1b<br>Bit 6:2 = Bit pattern used to set 12 dummy cycles = 00100b<br>Bits 1:0 = Reserved = 00b |
| 19Ch              | Status, Control and Configuration Register Map<br>DWORD-13 | 00h  | Bit 31 = 10 dummy cycles supported = 1b                                                                                                                                                                                                                                                                                                                                                                                |
| 19Dh              |                                                            | 40h  | Bit 30:26 = Bit pattern used to set 10 dummy cycles = 00011b                                                                                                                                                                                                                                                                                                                                                           |
| 19Eh              |                                                            | 28h  | Bit 25 = 8 dummy cycles supported = 1b                                                                                                                                                                                                                                                                                                                                                                                 |
| 19Fh              |                                                            | 8Eh  | Bit 24:20 = Bit pattern used to set 8 dummy cycles = 00010b<br>Bit 19 = 6 dummy cycles supported = 1b<br>Bit 18:14 = Bit pattern used to set 6 dummy cycles = 00001b<br>Bit 13 = 4 dummy cycles supported = 0b<br>Bit 12:8 = Bit pattern used to set 4 dummy cycles = 00000b<br>Bit 7 = 2 dummy cycles supported = 0b<br>Bit 6:2 = Bit pattern used to set 2 dummy cycles = 00000b<br>Bits 1:0 = Reserved = 00b        |
| 1A0h              | Status, Control and Configuration Register Map<br>DWORD-14 | 00h  | Not Supported                                                                                                                                                                                                                                                                                                                                                                                                          |
| 1A1h              |                                                            | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 1A2h              |                                                            | FFh  |                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 1A3h              |                                                            | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                        |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                                         | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------------------|---------------------------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1A4h              | Status, Control and Configuration Register Map DWORD-15 | 00h  | Not Supported                                                                                                                                                                                                                                                                                                                                                                                               |
| 1A5h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1A6h              |                                                         | FFh  |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1A7h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1A8h              | Status, Control and Configuration Register Map DWORD-16 | 71h  | Bits 7:0 = Command used for write access = 71h                                                                                                                                                                                                                                                                                                                                                              |
| 1A9h              |                                                         | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                              |
| 1AAh              |                                                         | 06h  | Bits 23:16 = Address of register where Octal Mode Enable volatile bit is located = 800006h (Configuration Reg - 5 volatile)                                                                                                                                                                                                                                                                                 |
| 1ABh              |                                                         | 90h  | Bit 31 = Octal Mode Enable volatile bit supported = 1b<br>Bits 30 = Octal Mode Enable volatile bit polarity: Positive (Octal Mode Enable bit = 1 indicates Octal mode is enabled) = 0b<br>Bits 29 = Reserved = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of Octal Mode enable bit in register = bit [0] = 000b          |
| 1ACh              | Status, Control and Configuration Register Map DWORD-17 | 71h  | Bits 7:0 = Command used for write access = 71h                                                                                                                                                                                                                                                                                                                                                              |
| 1ADh              |                                                         | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                              |
| 1AEh              |                                                         | 06h  | Address of register where Octal Mode Enable non-volatile bit is located = 06h (Configuration Reg - 5 non-volatile)                                                                                                                                                                                                                                                                                          |
| 1AFh              |                                                         | 90h  | Bit 31 = Octal Mode Enable non-volatile bit supported = 1b<br>Bits 30 = Octal Mode Enable non-volatile bit polarity: Positive (Octal Mode Enable bit = 1 indicates Octal mode is enabled) = 0b<br>Bit 29 = No OTP Bit = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of Octal Mode enable bit in register = bit [0] = 000b |
| 1B0h              | Status, Control and Configuration Register Map DWORD-18 | 00h  | Not Supported                                                                                                                                                                                                                                                                                                                                                                                               |
| 1B1h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1B2h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1B3h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1B4h              | Status, Control and Configuration Register Map DWORD-19 | 00h  | Not Supported                                                                                                                                                                                                                                                                                                                                                                                               |
| 1B5h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1B6h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1B7h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                             |

**Table 91**      **JEDEC SFDP Rev D parameter table** (Continued)

| SFDP byte address | SFDP DWORD name                                         | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------------|---------------------------------------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1B8h              |                                                         | 71h  | Bits 7:0 = Command used for write access = 71h                                                                                                                                                                                                                                                                                                                                                                                           |
| 1B9h              |                                                         | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                                           |
| 1BAh              |                                                         | 06h  | Address of register where STR Octal Mode Enable bit is located = 800006h (Configuration Reg - 5 Volatile)                                                                                                                                                                                                                                                                                                                                |
| 1BBh              | Status, Control and Configuration Register Map DWORD-20 | D1h  | Bit 31 = STR Octal Mode Enable volatile bit supported = 1b<br>Bits 30 = STR Octal Mode Enable volatile bit polarity: Inverted (STR Octal Mode Enable = 0 indicates STR Octal Mode is enabled) = 1b<br>Bit 29 = Reserved = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of STR Octal Mode Enable bit in register = bit [1] = 001b                        |
| 1BCh              |                                                         | 71h  | Bits 7:0 = Command used for write access = 71h                                                                                                                                                                                                                                                                                                                                                                                           |
| 1BDh              |                                                         | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                                           |
| 1BEh              |                                                         | 06h  | Address of register where STR Octal Mode Enable bit is located = 06h (Configuration Reg - 5 Non-volatile)                                                                                                                                                                                                                                                                                                                                |
| 1BFh              | Status, Control and Configuration Register Map DWORD-21 | D1h  | Bit 31 = STR Octal Mode Enable non-volatile bit supported = 1b<br>Bits 30 = STR Octal Mode Enable non-volatile bit polarity: Inverted (STR Octal Mode Enable = 0 indicates STR Octal Mode is enabled) = 1b<br>Bit 29 = No OTP Bit = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of STR Octal Mode Enable non-volatile bit in register = bit [1] = 001b |
| 1C0h              |                                                         | 71h  | Bits 7:0 = Command used for write access = 71h                                                                                                                                                                                                                                                                                                                                                                                           |
| 1C1h              |                                                         | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                                           |
| 1C2h              |                                                         | 06h  | Address of register where DTR Octal Mode Enable volatile bit is located = 800006h (Configuration Reg - 5 Volatile)                                                                                                                                                                                                                                                                                                                       |
| 1C3h              | Status, Control and Configuration Register Map DWORD-22 | 91h  | Bit 31 = DTR Octal Mode Enable volatile bit supported = 1b<br>Bits 30 = DTR Octal Mode Enable volatile bit polarity positive (DSTR Octal Mode Enable = 1 indicates DTR Octal Mode is enabled) = 0b<br>Bit 29 = Reserved = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of DTR Octal Mode Enable volatile bit in register = bit [1] = 001b               |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                                         | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------------------|---------------------------------------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1C4h              | Status, Control and Configuration Register Map DWORD-23 | 71h  | Bits 7:0 = Command used for write access = 71h                                                                                                                                                                                                                                                                                                                                                                              |
| 1C5h              |                                                         | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                              |
| 1C6h              |                                                         | 06h  | Address of register where DTR Octal Mode Enable non-volatile bit is located = 06h<br>(Configuration Reg - 5 non-volatile)                                                                                                                                                                                                                                                                                                   |
| 1C7h              |                                                         | 91h  | Bit 31 = DTR Octal Mode Enable non-volatile bit supported = 1b<br>Bits 30 = DTR Octal Mode Enable non-volatile bit polarity positive (DSTR Octal Mode Enable = 1 indicates DTR Octal Mode is enabled) = 0b<br>Bit 29 = No OTP Bit = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not supported = 0b<br>Bits 26:24 = Bit location of DTR Octal Mode Enable bit in register = bit [1] = 001b |
| 1C8h              | Status, Control and Configuration Register Map DWORD-24 | 00h  | Not Supported                                                                                                                                                                                                                                                                                                                                                                                                               |
| 1C9h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1CAh              |                                                         | FFh  |                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1CBh              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1CCh              | Status, Control and Configuration Register Map DWORD-25 | 00h  | Not Supported                                                                                                                                                                                                                                                                                                                                                                                                               |
| 1CDh              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1CEh              |                                                         | FFh  |                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1CFh              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1D0h              | Status, Control and Configuration Register Map DWORD-26 | 71h  | Bits 7:0 = Command used for write access = 71h                                                                                                                                                                                                                                                                                                                                                                              |
| 1D1h              |                                                         | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                              |
| 1D2h              |                                                         | 05h  | Address of register where Output Driver Strength volatile bits are located = 800005h (Configuration Reg - 4 Volatile)                                                                                                                                                                                                                                                                                                       |
| 1D3h              |                                                         | D5h  | Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b<br>Bit 29 = Reserved = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of Least Significant Output Driver Strength bit in register = bit [5] = 101b                                                                                                   |
| 1D4h              | Status, Control and Configuration Register Map DWORD-27 | 71h  | Bits 7:0 = Command used for write access = 71h                                                                                                                                                                                                                                                                                                                                                                              |
| 1D5h              |                                                         | 65h  | Bits 15:8 = Command used for read access = 65h                                                                                                                                                                                                                                                                                                                                                                              |
| 1D6h              |                                                         | 05h  | Address of register where Output Driver Strength non-volatile bits are located = 05h<br>(Configuration Reg - 4 non-volatile)                                                                                                                                                                                                                                                                                                |
| 1D7h              |                                                         | D5h  | Bits 31: 30 = Number of physical bits used to set Output Driver Strength = 3 bits = 11b<br>Bit 29 = Reserved = 0b<br>Bits 28 = Bit is set/cleared by commands using address = 1b<br>Bit 27 = Not Supported = 0b<br>Bits 26:24 = Bit location of Least Significant Output Driver Strength bit in register = bit [5] = 101b                                                                                                   |

**Table 91 JEDEC SFDP Rev D parameter table (Continued)**

| SFDP byte address | SFDP DWORD name                                                     | Data | Description                                                                                                                                                                                                                                                                                                       |
|-------------------|---------------------------------------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1D8h              | Status, Control and Configuration Register Map<br>DWORD-28          | 00h  | Bit 7:0 = Reserved = 00h                                                                                                                                                                                                                                                                                          |
| 1D9h              |                                                                     | 00h  | Bit 15:8 = Reserved = 00h                                                                                                                                                                                                                                                                                         |
| 1DAh              |                                                                     | A0h  | Bits 31:29 = Bit pattern to support Driver type 0 = 45 Ohms = 000b                                                                                                                                                                                                                                                |
| 1DBh              |                                                                     | 15h  | Bits 28:26 = Bit pattern to support Driver type 1 = 30 Ohm = 101b<br>Bits 25:23 = Bit pattern to support Driver type 2 = 60 Ohm = 011b<br>Bits 22:20 = Bit pattern to support Driver type 3 = 90 Ohm = 010b<br>Bits 19:17 = Bit pattern to support Driver type 4 = Not supported = 000b<br>Bit 16 = Reserved = 0b |
| 1DCh              | Command Sequences to Change to Octal DDR (8D-8D-8D) mode<br>DWORD-1 | 00h  | Bits 7:0 = Byte 3 of first command sequence                                                                                                                                                                                                                                                                       |
| 1DDh              |                                                                     | 00h  | Bits 15:8 = Byte 2 of first command sequence                                                                                                                                                                                                                                                                      |
| 1DEh              |                                                                     | 06h  | Bits 23:16 = Byte 1 of first command sequence                                                                                                                                                                                                                                                                     |
| 1DFh              |                                                                     | 01h  | Bits 31:24 = Length of first command sequence = 1 byte                                                                                                                                                                                                                                                            |
| 1E0h              | Command Sequences to Change to Octal DDR (8D-8D-8D) mode<br>DWORD-2 | 00h  | Bits 7:0 = Byte 7 of first command sequence                                                                                                                                                                                                                                                                       |
| 1E1h              |                                                                     | 00h  | Bits 15:8 = Byte 6 of first command sequence                                                                                                                                                                                                                                                                      |
| 1E2h              |                                                                     | 00h  | Bits 23:16 = Byte 5 of first command sequence                                                                                                                                                                                                                                                                     |
| 1E3h              |                                                                     | 00h  | Bits 31:24 = Byte 4 of first command sequence                                                                                                                                                                                                                                                                     |
| 1E4h              | Command Sequences to Change to Octal DDR (8D-8D-8D) mode<br>DWORD-3 | 00h  | Bits 7:0 = Byte 3 of second command sequence - volatile register address                                                                                                                                                                                                                                          |
| 1E5h              |                                                                     | 80h  | Bits 15:8 = Byte 2 of second command sequence - volatile register address                                                                                                                                                                                                                                         |
| 1E6h              |                                                                     | 71h  | Bits 23:16 = Byte 1 of second command sequence                                                                                                                                                                                                                                                                    |
| 1E7h              |                                                                     | 05h  | Bits 31:24 = Length of second command sequence = 5 bytes                                                                                                                                                                                                                                                          |
| 1E8h              | Command Sequences to Change to Octal DDR (8D-8D-8D) mode<br>DWORD-4 | 00h  | Bits 7:0 = Byte 7 of second command sequence                                                                                                                                                                                                                                                                      |
| 1E9h              |                                                                     | 00h  | Bits 15:8 = Byte 6 of second command sequence                                                                                                                                                                                                                                                                     |
| 1EAh              |                                                                     | 43h  | Bits 23:16 = Byte 5 of second command sequence                                                                                                                                                                                                                                                                    |
| 1EBh              |                                                                     | 06h  | Bits 31:24 = Byte 4 of second command sequence - volatile register address                                                                                                                                                                                                                                        |

### Sector map parameter table notes

**Table 92** provides a means to identify how the device address map is configured and provides a sector map for each supported configuration. This is done by defining a sequence of commands to read out the relevant configuration register bits that affect the selection of an address map. When more than one configuration bit must be read, all the bits are concatenated into an index value that is used to select the current address map.

To identify the sector map configuration in device the following configuration bits are read in the following MSb to LSb order to form the configuration map index value:

- CFR3V[3] - 0 = Hybrid Architecture, 1 = Uniform Architecture
- CFR1V[2] - 0 = 4KB parameter sectors at bottom, 1 = 4 KB sectors at top
- CFR1V[6] - 0 = 4KB parameter grouped together, 1 = 4 KB sectors split between bottom and top
- The value of some configuration bits may make other configuration bit values not relevant (don't care), hence not all possible combinations of the index value define valid address maps. Only selected configuration bit combinations are supported by the SFDP Sector Map Parameter table (see **Table 93**). Other combinations must not be used in configuring the sector address map when using this SFDP parameter table to determine the sector map. The following index value combinations are supported.

**Table 92**      **Sector map parameter**

| CFR3V[3] | CFR1V[6] | CFR1V[2] | Index value | Description                                                             |
|----------|----------|----------|-------------|-------------------------------------------------------------------------|
| 0        | 0        | 0        | 00h         | 4 KB sectors at bottom with remainder 256 KB sectors                    |
| 0        | 0        | 1        | 01h         | 4 KB sectors at top with remainder 256 KB sectors                       |
| 0        | 1        | 0        | 02h         | 4 KB sectors split between top and bottom with remainder 256 KB sectors |
| 1        | 0        | 0        | 04h         | Uniform 256 KB sectors                                                  |

**Table 93 JEDEC SFDP Rev D, sector map parameter**

| SFDP byte address | SFDP DWORD name                                           | Data | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------------------|-----------------------------------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1ECh              | JEDEC Sector Map Parameter<br>DWORD-1 Config.<br>Detect-1 | FCh  | Config. Detect -1 Uniform 256 KB Sectors or Hybrid Sectors<br>Bits 31:24 = Read data mask = 0000_1000b: Select bit 3 of the data byte for UNHYSA value 0 = Hybrid map with 4KB parameter sectors 1 = Uniform map<br>Bits 23:22 = Configuration detection command address length = 11b: Variable length<br>Bits 21:20 = RFU = 11b<br>Bits 19:16 = Configuration detection command latency = 1111b: variable latency<br>Bits 15:8 = Configuration detection instruction = 65h: Read any register<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Command Descriptor = 0<br>Bit 0 = Not the end descriptor = 0                                                                        |
| 1EDh              |                                                           | 65h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1EEh              |                                                           | FFh  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1EFh              |                                                           | 08h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1F0h              | JEDEC Sector Map Parameter<br>DWORD-2 Config.<br>Detect-1 | 04h  | Bits 31:0 = Address Value Configuration Register 3 (bit 3) = 00800004h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 1F1h              |                                                           | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1F2h              |                                                           | 80h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1F3h              |                                                           | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1F4h              | JEDEC Sector Map Parameter<br>DWORD-3 Config.<br>Detect-2 | FCh  | Config. Detect-2 4 KB Hybrid Sectors Split between Top and Bottom<br>Bits 31:24 = Read data mask = 0100_0000b: Select bit 6 of the data byte for SP4KBS value<br>0 = 4 KB parameter sectors are grouped together<br>1 = 4 KB parameter sectors are split between High and Low Addresses<br>Bits 23:22 = Configuration detection command address length = 11b: Variable length<br>Bits 21:20 = RFU = 11b<br>Bits 19:16 = Configuration detection command latency = 1111b: variable latency<br>Bits 15:8 = Configuration detection instruction = 65h: Read any register<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Command Descriptor = 0<br>Bit 0 = Not the end descriptor = 0 |
| 1F5h              |                                                           | 65h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1F6h              |                                                           | FFh  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1F7h              |                                                           | 40h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1F8h              | JEDEC Sector Map Parameter<br>DWORD-4 Config.<br>Detect-2 | 02h  | Bits 31:0 = Address Value Configuration Register 1 (bit 6)= 00800002h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1F9h              |                                                           | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1FAh              |                                                           | 80h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1FBh              |                                                           | 00h  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Table 93 JEDEC SFDP Rev D, sector map parameter (Continued)**

| SFDP byte address | SFDP DWORD name                                         | Data | Description                                                                                                                                                                                                                                                                                                                                                                                 |
|-------------------|---------------------------------------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1FCh              | JEDEC Sector Map Parameter<br>DWORD-5 Config. Detect-3  | FDh  | Config Detect-3 4 KB Hybrid Sectors on Top or Bottom                                                                                                                                                                                                                                                                                                                                        |
| 1FDh              |                                                         | 65h  | Bits 31:24 = Read data mask = 0000_0100b: Select bit 2 of the data byte for TB4KBS value                                                                                                                                                                                                                                                                                                    |
| 1FEh              |                                                         | FFh  | 0 = 4 KB parameter sectors at bottom<br>1 = 4 KB parameter sectors at top                                                                                                                                                                                                                                                                                                                   |
| 1FFh              |                                                         | 04h  | Bits 23:22 = Configuration detection command address length = 11b: Variable length<br>Bits 21:20 = RFU = 11b<br>Bits 19:16 = Configuration detection command latency = 1111b: variable latency<br>Bits 15:8 = Configuration detection instruction = 65h: Read any register<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Command Descriptor = 0<br>Bit 0 = End of command descriptor = 1           |
| 200h              | JEDEC Sector Map Parameter<br>DWORD-6 Config. Detect-3  | 02h  | Bits 31:0 = Address Value Configuration Register 1 (bit 2)= 00800002h                                                                                                                                                                                                                                                                                                                       |
| 201h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                             |
| 202h              |                                                         | 80h  |                                                                                                                                                                                                                                                                                                                                                                                             |
| 203h              |                                                         | 00h  |                                                                                                                                                                                                                                                                                                                                                                                             |
| 204h              | JEDEC Sector Map Parameter<br>DWORD-7 Config-0 Header   | FEh  | Configuration Index 00h 4 KB sectors at bottom with remainder 256 KB                                                                                                                                                                                                                                                                                                                        |
| 205h              |                                                         | 00h  | Bits 31:24 = RFU = FFh                                                                                                                                                                                                                                                                                                                                                                      |
| 206h              |                                                         | 02h  | Bits 23:16 = Region count (DWORDs -1) = 02h: Three regions                                                                                                                                                                                                                                                                                                                                  |
| 207h              |                                                         | FFh  | Bits 15:8 = Configuration ID = 00h, 4KB sectors bottom with remainder 256 KB<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Map Descriptor = 1<br>Bit 0 = Not the end descriptor = 0                                                                                                                                                                                                                |
| 208h              | JEDEC Sector Map Parameter<br>DWORD-8 Config-0 Region-0 | F1h  | Region 0 of 4 KB sectors                                                                                                                                                                                                                                                                                                                                                                    |
| 209h              |                                                         | FFh  | Bits 31:8 = Region size (32 4 KB) = 0001FFh: Region size as count-1 of 256 Byte units = 32 x 4 KB sectors = 128 KB Count = 128KB/256 = 512, value = count -1 = 512 - 1 = 511 = 1FFh                                                                                                                                                                                                         |
| 20Ah              |                                                         | 01h  | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1                                                                                                                                                                                                                                                                                                                            |
| 20Bh              |                                                         | 00h  | Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported<br>Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region |

**Table 93 JEDEC SFDP Rev D, sector map parameter (Continued)**

| SFDP byte address | SFDP DWORD name                                             | Data                       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------------------|-------------------------------------------------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20Ch              | JEDEC Sector Map Parameter<br>DWORD-9 Config-0<br>Region-1  | F8h                        | Region 1 of 128 KB sector                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 20Dh              |                                                             | FFh                        | Bits 31:8 = Region size = 0001FFh: Region size as count - 1 of 256 Byte units = 1 x 128 KB sectors                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 20Eh              |                                                             | 01h                        | = 128 KB Count = 128 KB/256 = 512, value = count - 1 = 512 - 1 = 511 = 1FFh                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 20Fh              |                                                             | 00h                        | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 128 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4KB erase and is not supported in the 4 KB sector region                                                                                                                                                                                                                          |
| 210h              | JEDEC Sector Map Parameter<br>DWORD-10<br>Config-0 Region-2 | F8h                        | Region 2 Uniform 256 KB sectors                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 211h              |                                                             | FFh                        | Bits 31:8 = 512 Mb device Region size = 03FBFFh:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 212h              |                                                             | FBh                        | Region size as count-1 of 256 Byte units = 255 x 256 KB sectors = 65,280 KB Count = 65,280 KB/256 = 261,120 value = count - 1 = 261,120 - 1 = 261119 = 3FBFFh                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 213h              |                                                             | 03h (512 Mb)<br>07h (1 Gb) | Bits 31:8 = 1 Gb device Region size = 01FEFFh: Region size as count - 1 of 256 Byte units = 511 x 256 KB sectors = 130,816 KB Count = 130,816 KB/256 = 523,364, value = count - 1 = 523,364 - 1 = 523263 = 07FBFFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region |
| 214h              | JEDEC Sector Map Parameter<br>DWORD-11<br>Config-3 Header   | FEh                        | Configuration Index 01h 4 KB sectors at Top with remainder 256 KB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 215h              |                                                             | 01h                        | Bits 31:24 = RFU = FFh                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 216h              |                                                             | 02h                        | Bits 23:16 = Region count (DWORDs -1) = 02h: Three regions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 217h              |                                                             | FFh                        | Bits 15:8 = Configuration ID = 01h: 4KB sectors at top with remainder 256 KB sectors<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Map Descriptor = 1<br>Bit 0 = Not the end descriptor = 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 93 JEDEC SFDP Rev D, sector map parameter (Continued)**

| SFDP byte address | SFDP DWORD name                                             | Data                       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------------|-------------------------------------------------------------|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 218h              | JEDEC Sector Map Parameter<br>DWORD-12<br>Config-3 Region-0 | F8h                        | Region 0 Uniform 256KB sectors                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 219h              |                                                             | FFh                        | Bits 31:8 = 512 Mb device Region size = 03FBFFh:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 21Ah              |                                                             | FBh                        | Region size as count – 1 of 256 Byte units = 255 x 256 KB sectors = 65,280 KB Count = 65,280 KB/256 = 261,120 value = count – 1 = 261,120 – 1 = 261119 = 3FBFFh                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 21Bh              |                                                             | 03h (512 Mb)<br>07h (1 Gb) | Bits 31:8 = 1 Gb device Region size = 07FBFFh: Region size as count – 1 of 256 Byte units = 511 x 256 KB sectors = 130,816 KB Count = 130,816 KB/256 = 523,264, value = count – 1 = 523,264 – 1 = 523263 = 07FBFFh<br>Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region |
| 21Ch              | JEDEC Sector Map Parameter<br>DWORD-13<br>Config-3 Region-1 | F8h                        | Region 1 of 128 KB sector                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 21Dh              |                                                             | FFh                        | Bits 31:8 = Region size = 0001FFh: Region size as count – 1 of 256 Byte units = 1 x 128 KB sectors =                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 21Eh              |                                                             | 01h                        | 128 KB Count = 128 KB/256 = 512, value = count – 1 = 512 – 1 = 511 = 1FFh                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 21Fh              |                                                             | 00h                        | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 128 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region                                                                                                                                                                                                                         |
| 220h              | JEDEC Sector Map Parameter<br>DWORD-14<br>Config-3 Region-2 | F1h                        | Region 2 of 4 KB sectors                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 221h              |                                                             | FFh                        | Bits 31:8 = Region size (32 4 KB) = 0001FFh: Region size as count – 1 of 256 Byte units = 32 x 4 KB sectors = 128 KB Count = 128                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 222h              |                                                             | 01h                        | KB/256 = 512, value = count – 1 = 512 – 1 = 511 = 1FFh                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 223h              |                                                             | 00h                        | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported<br>Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region                                                                                                                                                                                                      |
| 224h              | JEDEC Sector Map Parameter<br>DWORD-15<br>Config-1 Header   | FEh                        | Configuration Index 02h 4 KB sectors split between Bottom and Top with remainder 256 KB                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 225h              |                                                             | 02h                        | Bits 31:24 = RFU = FFh                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 226h              |                                                             | 04h                        | Bits 23:16 = Region count (DWORDs – 1) = 04h: Five regions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 227h              |                                                             | FFh                        | Bits 15:8 = Configuration ID = 02h: 4 KB sectors split between bottom and top with remainder 256 KB sectors<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Map Descriptor = 1<br>Bit 0 = Not the end descriptor = 0                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 93 JEDEC SFDP Rev D, sector map parameter (Continued)**

| SFDP byte address | SFDP DWORD name                                             | Data                       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------------|-------------------------------------------------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 228h              | JEDEC Sector Map Parameter<br>DWORD-16<br>Config-1 Region-0 | F1h                        | Region 0 of 4 KB sectors                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 229h              |                                                             | FFh                        | Bits 31:8 = Region size (16 x 4 KB) = 0000FFh: Region size as count – 1 of 256 Byte units = 16 x 4 KB sectors = 64 KB Count = 64 KB/256 = 256, value = count – 1 = 256 – 1 = 255 = FFh                                                                                                                                                                                                                                                                          |
| 22Ah              |                                                             | 00h                        | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported<br>Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region |
| 22Bh              |                                                             | 00h                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 22Ch              | JEDEC Sector Map Parameter<br>DWORD-17<br>Config-1 Region-1 | F8h                        | Region 1 of 192 KB sector                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 22Dh              |                                                             | FFh                        | Bits 31:8 = Region size = 0002FFh: Region size as count – 1 of 256 Byte units = 1 x 192KB sectors = 192KB Count = 192KB/256 = 768, value = count -1 = 768 – 1 = 767 = 2FFh                                                                                                                                                                                                                                                                                      |
| 22Eh              |                                                             | 02h                        | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 192 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4 KB erase and is not supported in the 4 KB sector region                   |
| 22Fh              |                                                             | 00h                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 230h              | JEDEC Sector Map Parameter<br>DWORD-18<br>Config-1 Region-2 | F8h                        | Region 2 Uniform 256 KB sectors                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 231h              |                                                             | FFh                        | Bits 31:8 = 512 Mb device Region size = 03F7FF:                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 232h              |                                                             | F7h                        | Region size as count – 1 of 256 Byte units = 254 x 256 KB sectors = 65,024 KB Count = 65,024 KB/256 = 260,096 value = count – 1 = 260,096 – 1 = 260,095 = 3F7FFh                                                                                                                                                                                                                                                                                                |
| 233h              |                                                             | 03h (512 Mb)<br>07h (1 Gb) | Bits 31:8 = 1 Gb device Region size = 07F7FFh: Region size as count – 1 of 256 Byte units = 510 x 256 KB sectors = 130,560 KB Count = 130,560 KB/256 = 522,240, value = count – 1 = 522,240 – 1 = 522,239 = 7F7FFh                                                                                                                                                                                                                                              |
|                   |                                                             |                            | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region                  |
| 234h              | JEDEC Sector Map Parameter<br>DWORD-19<br>Config-1 Region-3 | F8h                        | Region 3 of 192 KB sector                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 235h              |                                                             | FFh                        | Bits 31:8 = Region size = 0002FFh: Region size as count – 1 of 256 Byte units = 1 x 192 KB sectors = 192 KB Count = 192 KB/256 = 768, value = count -1 = 768 – 1 = 767 = 2FFh                                                                                                                                                                                                                                                                                   |
| 236h              |                                                             | 02h                        | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 192 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 22 is not defined<br>Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4KB erase and is not supported in the 4 KB sector region                    |
| 237h              |                                                             | 00h                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

**Table 93 JEDEC SFDP Rev D, sector map parameter (Continued)**

| SFDP byte address | SFDP DWORD name                                             | Data                       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------|-------------------------------------------------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 238h              | JEDEC Sector Map Parameter<br>DWORD-20<br>Config-1 Region-5 | F1h                        | Region 5 of 4KB sectors                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 239h              |                                                             | FFh                        | Bits 31:8 = Region size (16 x 4 KB) = 0000FFh: Region size as count – 1 of 256 Byte units = 16 x 4 KB sectors = 64 KB Count = 64 KB/256 = 256, value = count – 1 = 256 – 1 = 255 = FFh                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 23Ah              |                                                             | 00h                        | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 0b ---Erase Type 4 is not defined<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is 256 KB erase and is not supported in the 4 KB sector region<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is 64 KB erase and is not supported<br>Bit 0 = Erase Type 1 support = 1b ---Erase Type 1 is 4 KB erase and is supported in the 4 KB sector region |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 23Bh              |                                                             | 00h                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 23Ch              | JEDEC Sector Map Parameter<br>DWORD-21<br>Config-4 Header   | FFh                        | Configuration Index 04h Uniform 256 KB sectors                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 23Dh              |                                                             | 04h                        | Bits 31:24 = RFU = FFh                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 23Eh              |                                                             | 00h                        | Bits 23:16 = Region count (DWORDs – 1) = 00h: One region                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 23Fh              |                                                             | FFh                        | Bits 15:8 = Configuration ID = 04h: Uniform 256KB sectors<br>Bits 7:2 = RFU = 111111b<br>Bit 1 = Map Descriptor = 1<br>Bit 1= End of map descriptor = 1                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 240h              | JEDEC Sector Map Parameter<br>DWORD-22<br>Config-4 Region-0 | F8h                        | Region 0 Uniform 256 KB sectors                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 241h              |                                                             | FFh                        | Bits 31:8 = 512 Mb device Region size = 03FFFFh:                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 242h              |                                                             | FFh                        | Region size as count – 1 of 256 Byte units = 256 x 256 KB sectors = 65,536 KB Count = 65,280 KB/256 = 262,144 value = count – 1 = 262,144 – 1 = 262,143 = 3FFFFh                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 243h              |                                                             | 03h (512 Mb)<br>07h (1 Gb) |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Bits 31:8 = 1 Gb device Region size = 07FFFFh: Region size as count – 1 of 256 Byte units = 512 x 256 KB sectors = 131,072 KB Count = 131,072 KB/256 = 524,288, value = count – 1 = 524,288 – 1 = 524,287 = 7FFFFh                                                                                                                                                                                                                             |
|                   |                                                             |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Bits 7:4 = RFU = Fh Erase Type not supported = 0 / supported = 1<br>Bit 3 = Erase Type 4 support = 1b ---Erase Type 4 is 256 KB erase and is supported in the 256 KB sector region<br>Bit 2 = Erase Type 3 support = 0b ---Erase Type 3 is not defined<br>Bit 1 = Erase Type 2 support = 0b ---Erase Type 2 is not defined<br>Bit 0 = Erase Type 1 support = 0b ---Erase Type 1 is 4 KB erase and is not supported in the 256 KB sector region |

## 9.2 Manufacturer and Device ID

**Table 94**      **Manufacturer and Device ID**

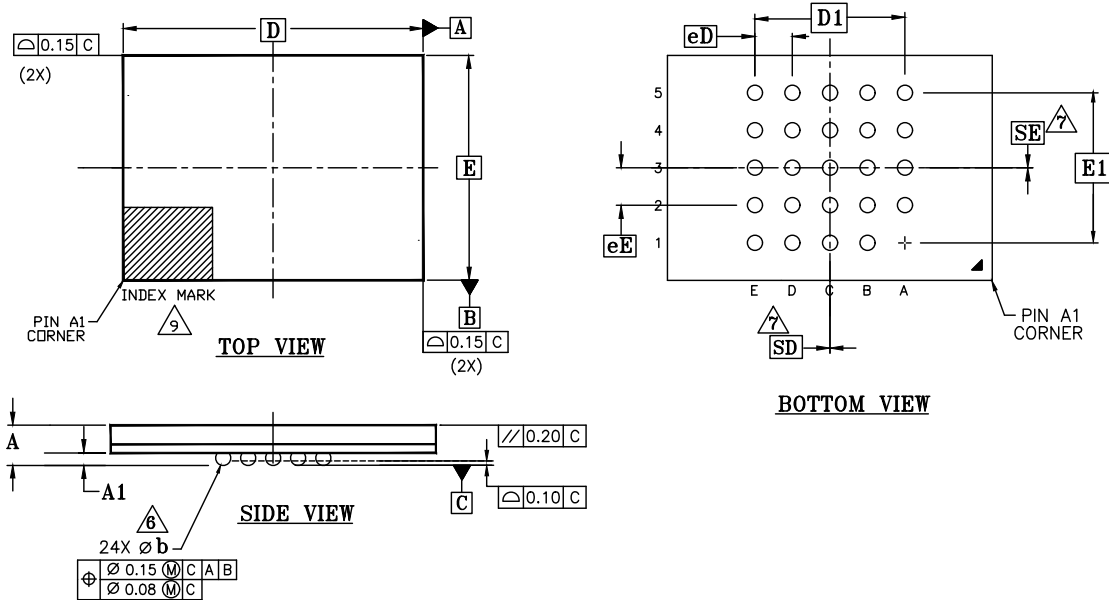
| Byte address | Data                           | Description                                                                                                                                                                                                    |
|--------------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00h          | 34h                            | Manufacturer ID for Infineon                                                                                                                                                                                   |
| 01h          | 5Ah (HL-T) /<br>5Bh (HS-T)     | Device ID MSB - Memory Interface Type                                                                                                                                                                          |
| 02h          | 1Ah (512Mb) /<br>1Bh (1Gb)     | Device ID LSB - Density                                                                                                                                                                                        |
| 03h          | 0Fh                            | ID Length - number bytes following. Adding this value to the current location of 03h gives the address of the last valid location in the ID legacy address map.                                                |
| 04h          | 03h<br>(Default Configuration) | Physical Sector Architecture<br>The HS/L-T family may be configured with or without 4 KB parameter sectors in addition to the uniform sectors.<br>03h = Uniform 256 KB with thirty-two 4 KB Parameter Sectors) |
| 05h          | 90h<br>(HL-T/HS-T Family)      | Family IDs                                                                                                                                                                                                     |

## 9.3 Unique Device ID

**Table 95**      **Unique Device ID**

| Byte address | Data                    | Description             |
|--------------|-------------------------|-------------------------|
| 00h to 07h   | 8-Byte Unique Device ID | 64-bit unique ID number |

## 10 Package diagrams



| SYMBOL | DIMENSIONS |      |      |
|--------|------------|------|------|
|        | MIN.       | NOM. | MAX. |
| A      | -          | -    | 1.00 |
| A1     | 0.20       | -    | -    |
| D      | 8.00 BSC   |      |      |
| E      | 6.00 BSC   |      |      |
| D1     | 4.00 BSC   |      |      |
| E1     | 4.00 BSC   |      |      |
| MD     | 5          |      |      |
| ME     | 5          |      |      |
| N      | 24         |      |      |
| Ø b    | 0.35       | 0.40 | 0.45 |
| eE     | 1.00 BSC   |      |      |
| eD     | 1.00 BSC   |      |      |
| SD     | 0.00 BSC   |      |      |
| SE     | 0.00 BSC   |      |      |

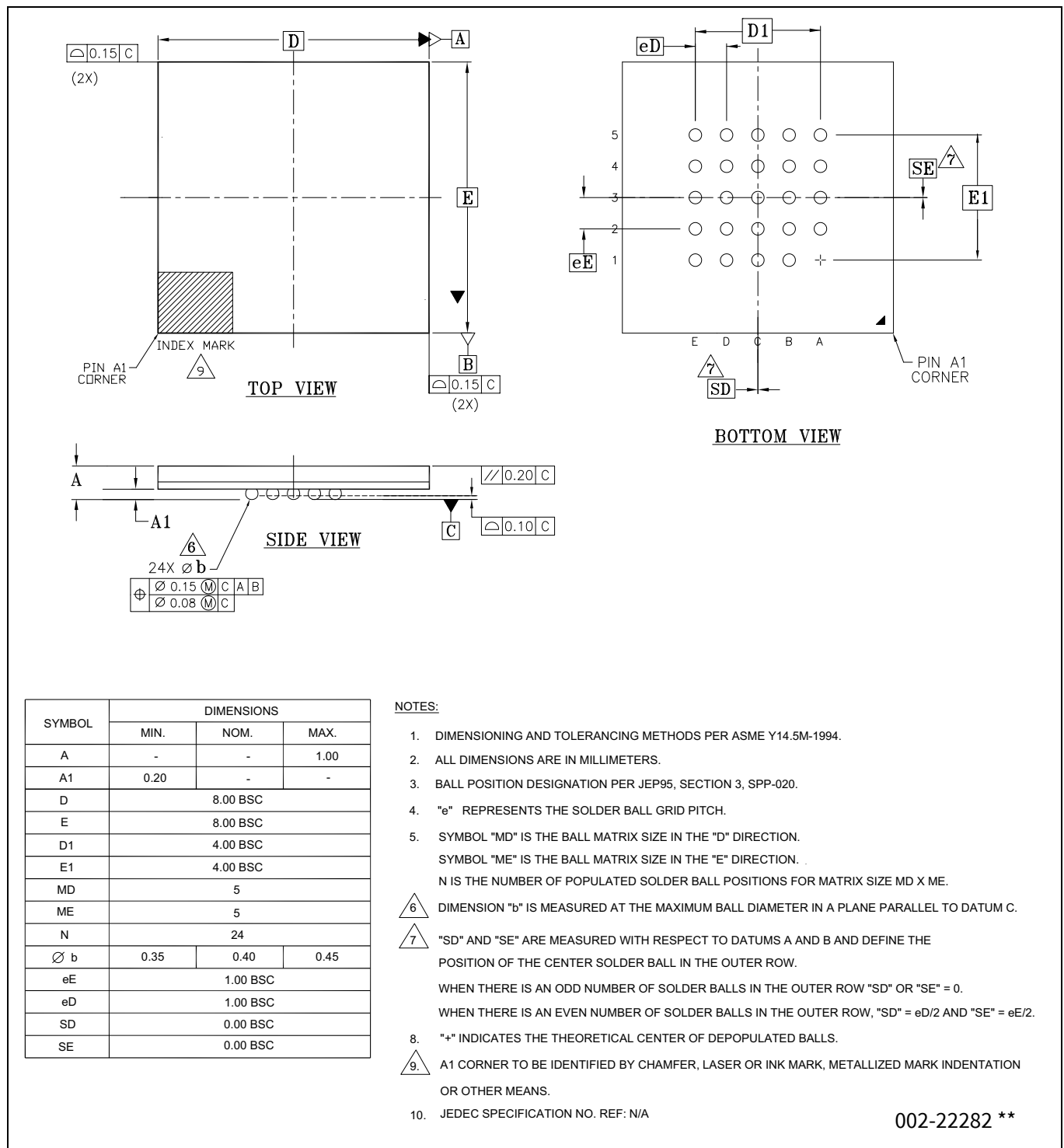
### NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
- JEDEC SPECIFICATION NO. REF: MO-234E

002-15550 \*B

Figure 79 24-ball BGA (8 × 6 × 1 mm) VAA024/ELA024/E2A024 package outline (PG-BGA-24), 002-15550

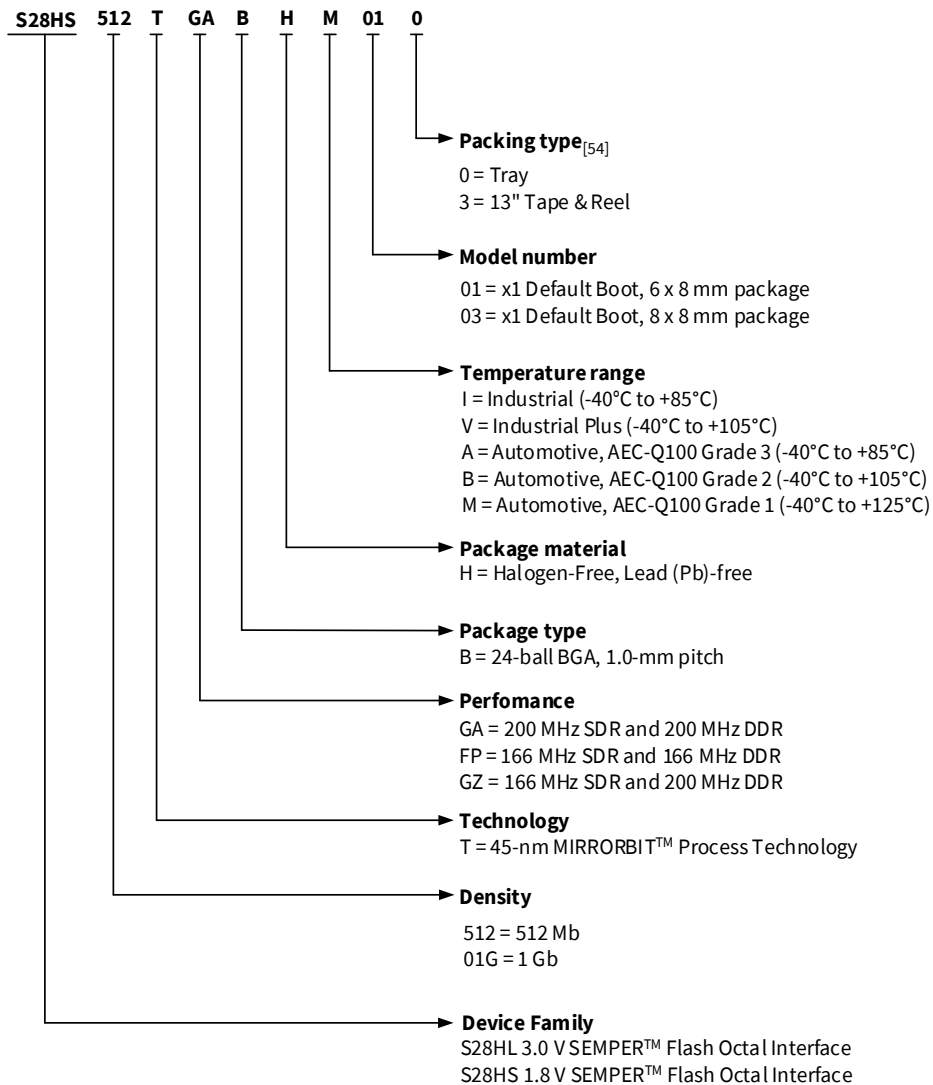
Package diagrams



**Figure 80 24-ball BGA (8 × 8 × 1 mm) VAC024 package outline (PG-BGA-24), 002-22282**

## 11 Ordering information

The ordering part number is formed by a valid combination of the following:



### Note

54. See Packing and Packaging Handbook on [www.infineon.com](http://www.infineon.com) for further information.

## 11.1 Valid combinations — standard grade

**Table 96** lists configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

**Table 96 Valid combinations — standard grade**

| Base ordering part number | Speed option | Package and materials | Temperature range | Model number | Packing type | Ordering part number (x = Packing type) | Package marking |
|---------------------------|--------------|-----------------------|-------------------|--------------|--------------|-----------------------------------------|-----------------|
| S28HL512T                 | FP           | BH                    | I, V              | 01           | 0, 3         | S28HL512TFPBHI01x                       | 28HL512TPI01    |
|                           |              |                       |                   |              |              | S28HL512TFPBHV01x                       | 28HL512TPV01    |
| S28HS512T                 | GA           |                       |                   |              |              | S28HS512TGABHI01x                       | 28HS512TAI01    |
|                           |              |                       |                   |              |              | S28HS512TGABHV01x                       | 28HS512TAV01    |
| S28HL01GT                 | FP           |                       |                   |              |              | S28HL01GTFPBHI03x                       | 28HL01GTPI03    |
|                           |              |                       |                   |              |              | S28HL01GTFPBHV03x                       | 28HL01GTPV03    |
| S28HS01GT                 | FP           |                       |                   |              |              | S28HS01GTFPBHI03x                       | 28HS01GTPI03    |
|                           |              |                       |                   |              |              | S28HS01GTFPBHV03x                       | 28HS01GTPV03    |
| S28HS01GT                 | GZ           |                       |                   |              |              | S28HS01GTGZBHI03x                       | 28HS01GTZI03    |
|                           |              |                       |                   |              |              | S28HS01GTGZBHV03x                       | 28HS01GTZV03    |

## 11.2 Valid combinations — automotive grade / AEC-Q100

**Table 97** lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non-AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements. AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

**Table 97 Valid combinations — automotive grade / AEC-Q100**

| Base ordering part number | Speed option | Package and materials | Temperature range | Model number | Packin g type | Ordering part number (x = Packing type) | Package marking |                   |              |
|---------------------------|--------------|-----------------------|-------------------|--------------|---------------|-----------------------------------------|-----------------|-------------------|--------------|
| S28HL512T                 | FP           | BH                    | A, B, M           | 01           | 0, 3          | S28HL512TFPBHA01x                       | 28HL512TPA01    |                   |              |
|                           |              |                       |                   |              |               | S28HL512TFPBHB01x                       | 28HL512TPB01    |                   |              |
|                           |              |                       |                   |              |               | S28HL512TFPBHM01x                       | 28HL512TPM01    |                   |              |
| S28HS512T                 | GA           |                       |                   |              |               | S28HS512TGABHA01x                       | 28HS512TAA01    |                   |              |
|                           |              |                       |                   |              |               | S28HS512TGABHB01x                       | 28HS512TAB01    |                   |              |
|                           |              |                       |                   |              |               | S28HS512TGABHM01x                       | 28HS512TAM01    |                   |              |
| S28HL01GT                 | FP           |                       |                   |              |               |                                         | 03              | S28HL01GTFPBHA03x | 28HL01GTPA03 |
|                           |              |                       |                   |              |               |                                         |                 | S28HL01GTFPBHB03x | 28HL01GTPB03 |
|                           |              |                       |                   |              |               |                                         |                 | S28HL01GTFPBHM03x | 28HL01GTPM03 |
| S28HS01GT                 | FP           |                       |                   |              |               |                                         |                 | S28HS01GTFPBHA03x | 28HS01GTPA03 |
|                           |              |                       |                   |              |               |                                         |                 | S28HS01GTFPBHB03x | 28HS01GTPB03 |
|                           |              |                       |                   |              |               |                                         |                 | S28HS01GTFPBHM03x | 28HS01GTPM03 |
| S28HS01GT                 | GZ           |                       |                   |              |               |                                         |                 | S28HS01GTGZBHA03x | 28HS01GTZA03 |
|                           |              |                       |                   |              |               |                                         |                 | S28HS01GTGZBHB03x | 28HS01GTZB03 |
|                           |              |                       |                   |              |               |                                         |                 | S28HS01GTGZBHM03x | 28HS01GTZM03 |

## Revision history

| Document revision | Date       | Description of changes                                                                                                                                                                                                                                                                                                           |
|-------------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| *X                | 2022-04-08 | Publish to web.                                                                                                                                                                                                                                                                                                                  |
| *Y                | 2022-11-10 | Updated <b>“Valid combinations — automotive grade / AEC-Q100”</b> on page 178 and <b>“Valid combinations — automotive grade / AEC-Q100”</b> on page 178.                                                                                                                                                                         |
| *Z                | 2023-08-09 | Updated <b>Table 91, Table 93</b> .<br>Updated <b>Figure 79</b> .                                                                                                                                                                                                                                                                |
| AA                | 2024-03-25 | Updated “Data integrity” under <b>Features</b> .<br>Updated “SPI (1S-1S-8S, 1S-8S-8S 256T only)” under <b>Features</b> .<br>Updated “Program / erase (PE) endurance - high endurance (256KB sectors)” under <b>Data integrity</b> .<br>Updated <b>Table 57, Table 81, Table 76, Table 87, Table 89, Table 91, and Table 93</b> . |
| AB                | 2024-05-13 | Removed Device S28HL256T & S28HS256T. Devices move to separate datasheet.<br>Removed the typo that present in the description of changes in Rev. AA revision history.                                                                                                                                                            |
| AC                | 2024-10-09 | Updated the parameter for $t_{DIS}$ and unit of $t_{BE}$ in <b>Table 89</b> .<br>Updated <b>Table 84</b> .                                                                                                                                                                                                                       |

#### Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2024-10-09**  
**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

**© 2024 Infineon Technologies AG.**  
**All Rights Reserved.**

**Do you have a question about this document?**  
Go to [www.infineon.com/support](https://www.infineon.com/support)

**Document reference**  
**002-18216 Rev. AC**

#### IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenhheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

#### WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.